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(54) Current copy circuit arrangement

(57) An accurate and fast copy current circuit arrangement (250) and method for high current ratio having a first branch for carrying a first current (I_{load}) ; a second branch for carrying a second current ($2I_{fb}$) ; and a twisted current mirror arrangement (282, 284, 286, 288) coupled between the first branch and the second branch, wherein the second current ($2I_{fb}$) is a copy representative of the first current (I_{load}). The twisted current mirror arrangement (282, 284, 286, 288) includes a first current mirror having a first bipolar transistor (282) and a second bipolar transistor (284) whose bases are coupled together; and a second current mirror having a first MOSFET transistor (286) connected in series with the first bipolar transistor (282) and a second MOSFET transistor (288) connected in series with the second bipolar transistor (284), the first and second MOSFET transistors having their gates coupled together. A start-up current source (299) applies a start-up current to the junction between the first bipolar transistor (282) and the first MOSFET transistor (286) and provides bias during circuit operation.

This avoids a conventional error amplifier, uses no closed voltage loop, and no capacitor to stabilize the voltage loop, and provides a faster response time.

This provides more accurate copy current for high current ratio, better linearity and zero input error voltage.

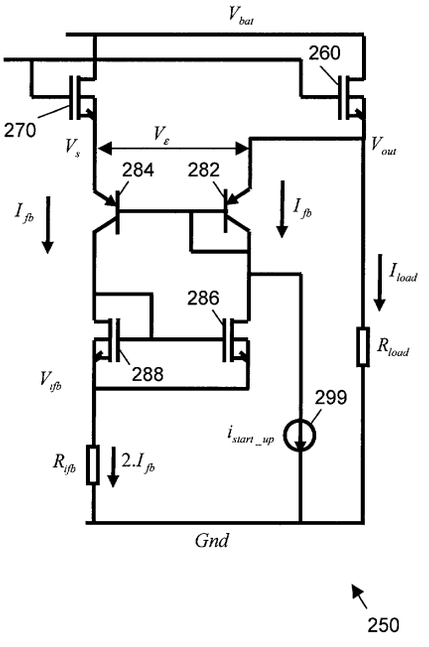


FIG. 2

EP 1 387 234 A1

Description

Field of the Invention

[0001] This invention relates to the copying (often referred to as 'mirroring') of currents in electronic circuits. Such current copying or mirroring is widely used in electronic circuits for purposes such as regulation.

Background of the Invention

[0002] In the field of this invention it is known that to copy the current of a power MOSFET (Metal-Oxide-Semiconductor Field-Effect Transistor), a well-known technique is to design another (typically small) transistor to serve as a sense FET, and to design a loop with an amplifier to force the same voltage on the drains of both the power transistor and the sense transistor. In this way, the current in the sense transistor is proportional to (typically less than) current in the power transistor.

[0003] A known example of this technique to copy or mirror current of a high- or low-side power switch uses a feedback loop with a high gain amplifier to match both drain voltages. However, if a high gain amplifier is used, capacitor compensation is required to ensure closed-loop stability, and this makes the circuit slower.

[0004] Additionally, accuracy in such an arrangement is determined by the input offset and the input error (output voltage divided by the open-loop gain), and even if the offset is close to zero, input error will still be produced. A high gain amplifier (sometimes 2 stages, e.g., with gain in the range of 1,000) is needed to decrease this error.

[0005] A problem to be solved with this example is to copy or mirror the current of the high or low side power switch, without using a high gain voltage amplifier.

[0006] A need therefore exists for accurate and fast current copying or mirroring circuit for high current ratio wherein the abovementioned disadvantage(s) may be alleviated.

Statement of Invention

[0007] The present invention provides a copy current circuit arrangement and a method for copying current in a circuit arrangement as described in the accompanying claims.

Brief Description of the Drawings

[0008] Two accurate and fast copy current circuit arrangements and methods for high current ratio incorporating the present invention will now be described, by way of example only, with reference to the accompanying drawings, in which:

FIG. 1A and FIG. 1B show prior art copy-current circuits for use in a low-side power switch and a high-side power switch respectively;

FIG. 2 shows a schematic circuit diagram of a copy-current circuit for use in a high-side power switch in accordance with an embodiment of the present invention, given by way of example;

FIG. 3 shows a schematic circuit diagram of an improved copy-current circuit, developed from the circuit of FIG. 2, for use in a high-side power switch;

FIG. 4A and FIG. 4B show a simplified schematic re-drawing of the circuit of FIG. 2 and a similar complementary-type circuit respectively;

FIG. 5 shows a simplified re-drawing of the circuit of FIG. 2 based on the schematic of FIG. 4A or FIG. 4B; and

FIG. 6A and 6B show simplified source-up and source-down variants of the circuit of FIG. 5.

Description of Preferred Embodiments

[0009] Referring firstly to FIG. 1A, a copy-current low-side switch circuit 100 includes a power FET 110 which has its drain connected to a supply voltage rail V_{bat}, via a load resistance r_{load}, and which has its source connected to ground voltage *Gnd.* A sense FET 120 has its source connected to the ground voltage *Gnd.* The drains of the FETs 110 and 120 are connected to respective inputs of a differential amplifier 130. The output of the amplifier 130 is connected to the gate of an FET 140, whose source is connected to the drain of the sense FET 120. The gates of the power FET 110 and the sense FET 120 are connected to receive a switching control voltage. In use, the load current i_{load} carried by the power FET 110 is copied or mirrored in the output current i_{out} carried by the sense FET 120 and the FET 140. The copied or mirrored current i_{out} is related to the load current i_{load} by the equation

$$i_{out} = \frac{i_{load}}{k}$$

where $k = A_{out}/A_s$, A_{out} is the area of the power FET 110 and A_s is the area of the sense FET 120.

[0010] It will be understood that the amplifier 130 has high impedance inputs; it will also be understood that in order to ensure stability of the amplifier feedback loop capacitance (shown symbolically within the amplifier 130) must be provided in the feedback loop, and that this capacitance creates a delay in the current.

[0011] Referring now also to FIG. 1B, a copy-current high-side switch circuit 150 includes a power FET 160 which has its drain connected to a supply voltage rail V_{bat}, and which has its source connected, via a load re-

sistance R_{load}, to ground voltage *Gnd.* A sense FET 170 has its drain connected to the supply voltage rail V_{bat}. The sources of the FETs 160 and 170 are connected to respective inputs of a differential amplifier 180. The output of the amplifier 180 is connected to the gate of an FET 190, whose drain is connected to the source of the sense FET 170 and whose source is connected via a feedback resistor R_{ifb} to the ground voltage *Gnd.* The gates of the power FET 160 and the sense FET 170 are connected to receive a switching control voltage. In use, a power output voltage V_{out} is developed at the source of the power FET 160 and a sense voltage V_s is developed at the source of the sense FET 190 (giving rise to an error voltage V_ε between the inputs of the amplifier 180), and a current feedback voltage V_{ifb} is developed at the drain of the sense FET 190, the error voltage V_ε being given by the equation

$$V_\varepsilon = offset + \frac{V_{ifb}}{A}$$

where *offset* is the offset voltage of the amplifier 180 and A is its open-loop gain. The load current I_{load} carried by the power FET 160 is copied or mirrored in the feedback current I_{fb} carried by the sense FET 170 and the FET 190. The copied or mirrored current I_{fb} is related to the load current I_{load} by the equation

$$I_{fb} = \frac{I_{load}}{K}$$

where $K = A_{out}/A_s$, A_{out} being the area of the power FET 160 and A_s being the area of the sense FET 170.

[0012] It will be understood that $\frac{V_{ifb}}{A}$ gives, in practice, for example, a 1mV error for $V_{out} \triangleq$ 1V and A = 1000, and that the error voltage changes with V_{ifb}.

[0013] Referring now to FIG. 2, the copy-current high-side switch circuit 250 shown, which is in accordance with an embodiment of the present invention, includes a power FET 260 which has its drain connected to a supply voltage rail V_{bat}, and which has its source connected, via a load resistance R_{load}, to ground voltage *Gnd.* A sense FET 270 has its drain connected to the supply voltage rail V_{bat}. The sources of the FETs 260 and 270 are connected to respective emitters of PNP bipolar transistors 282 and 284, whose bases are connected to each other and to the collector of PNP transistor 282. Two FET transistors 286 and 288 have their drains connected respectively to the collectors of the PNP transistors 282 and 284. The FETs 286 and 288 have their sources connected via a feedback resistor R_{fb} to the ground voltage *Gnd.* The gates of the FETs 286 and 288 are connected together and to the drain of the FET 288. A start-up current source 299 is connected between the collector of PNP transistor 282 and the ground voltage *Gnd.* The gates of the power FET 260 and the sense FET 270 are connected to receive a switching control voltage.

[0014] As can be seen by comparing the circuit of FIG. 2 with that of FIG. 1B, essentially the voltage amplifier 180 of FIG. 1B has been replaced by a twisted current mirror arrangement (284/282 - 288/286). These current mirrors have a gain of 1, forcing both branches (284 & 288 and 282 & 286) to have the same current (named I_{fb}), whatever the current value.

[0015] As the gain of the mirror (284/282 - 288/286) is 1, the differential offset between its inputs (V_{out}-V_s) has to be zero, if the offset is zero.

[0016] In use it will be appreciated that the twisted current mirror arrangement (282, 284, 286, 288) is used to create a current source by generating a *"*$\Delta V_{be}/R$*"*, ΔV_{be} being generated by a different area between transistors 282 and 284 (ΔV_{be} = *offset*). This twisted current mirror arrangement in this particular application produces an image of the current. So to compare with the current source generation, an *offset* of zero is used, assuming the V_{out} voltage is a source voltage (very low impedance) and this source voltage is applied across the sense resistor (sense FET resistance), to generate

$$I_{fb} = \frac{(V_{bat} - V_{out})}{R_{sense}}.$$

It will be understood that basically this circuit allows copying of a voltage (without gain offset), from a low impedance voltage source across a resistor.

[0017] It will therefore be appreciated that the circuit of FIG. 3 produces the same result (V_{out}-V_s=0) as that of FIG. 1B, but without using a voltage loop and a voltage amplifier. In the circuit of FIG. 2 the voltage V_{bat} - V_{out} is given by the load current through the power MOS 282. This voltage is copied on the sense FET 284, because the differential voltage (V_{out} - V_s) is zero.

[0018] The two currents I_{fb} in the branches of the twisted current mirror arrangement 282-288 go through the R_{ifb} resistor, creating a voltage V_{ifb}, which is the image of the current in the load.

[0019] It will be appreciated that a significant difference between this new topology shown in FIG. 2 and the standard architecture shown in FIG. 1B is that the twisted current mirror arrangement (282-288) provides a high impedance input and so doesn't create any current error on the branches.

[0020] It can be shown that, comparing the performance of the circuit of FIG. 2 with that of FIG. 1B, with typical values of K = 1000 , A = 1000, *offset* = 1mV, I_{load} = 1A, R_{load} = 20mΩ, V_{bat}-V_{out} = 20mV , although an error current of 0.1% may be produced in the FIG. 2 circuit compared with an error current of 0% in the FIG. 1B circuit, an error voltage of 20% may be produced in the FIG. 1B circuit compared with an error voltage of only 5% in the FIG. 2 circuit. It will be appreciated that this improvement in error voltage, in spite of a worsening of

error current, is advantageous because the circuit is much less sensitive to current error than to voltage error.

[0021] Referring now also to FIG. 3, in an improved version 300 of the circuit of FIG. 2, like components are denoted by the same reference numbers. As can be seen from comparing the circuit of FIG. 3 with of FIG. 2, added components in the circuit of FIG. 3 include NPN bipolar transistors 283 and 285 having their bases connected to the collectors of the PNP transistors 282 and 284 respectively; the collectors of the NPN transistors 283 and 285 are connected to the emitters of the PNP transistors 282 and 284 respectively; and the emitters of the NPN transistors 283 and 285 are connected to their bases via resistors 283' and 285' respectively. A MOS transistor 292 has its gate and source connected to the source of the MOS transistor 296. A MOS transistor 294 has its drain connected to the drains of the MOS transistors 286 and 288, and has its source connected via the current feedback resistance R_{ifb} to the ground voltage *Gnd.* A MOS transistor 296 has its gate and source connected to the gate of the MOS transistor 294; the drain of the MOS transistor 296 is connected to the drain of the MOS transistor 292; and the source of the MOS transistor is connected via the start-up current source 299 to the ground voltage *Gnd.* A MOS transistor 298 has its drain connected to the bases of the PNP transistors 282 and 284, has its source connected to the drains of the MOS transistors2865 and 288, and has its gate connected to the source of the MOS transistor 286.

[0022] It will be appreciated that the NPN bipolar transistors 283 and 285 allows the circuit 300 to drive more current. It will also be appreciated that the MOS transistors 294 and 296 allow the circuit 300 to sustain higher V_{bat} voltage. It will also be appreciated that the MOS transistor 298 improves operation of the bipolar current mirror 282 and 284 by bringing the current ratio closer to unity, due to base current compensation as follows. Considering the circuit of FIG. 2, the base currents of bipolar transistors 284 and 282 are injected in the MOS transistor 286 in addition to the collector current of the bipolar transistor 282. This results in the ratio current in the MOS transistors 286 and 288 being not exactly equal to unity, but instead $(i_c + 2.i_b)/ic$, the $2.i_b$ factor clearly giving rise to current ratio error. In the circuit of FIG 3, the MOS transistor 298 injects those two base currents ($2.i_b$) into the feedback resistance R_{ifb} through the MOS transistor 294. Since the gate of the MOS transistor 298 has no current, the MOS transistors 286 and 288 will see the ratio current close to unity.

[0023] It will also be understood that the MOS transistor 292 compensates for the V_{gs} of the MOS transistor 288 and allows the voltages at the sources of the MOS transistors 286 and 288 to be substantially equalised (MOS transistors 286 and 288 having the same V_{ds} for good matching). Finally, it will be appreciated that the start-up current source 299 can stay on (for example at a low current of 10μA), providing bias for the MOSFET transistors 296 and 292. Thus, in conclusion, it will be understood that the modifications of FIG. 3 provide improved matching to obtain a current mirror gain as close as possible to 1, to minimize the offset by design.

[0024] In summary, it will be understood that the new copy current circuit for high current ratio described above in relation to FIG. 2 and FIG. 3 provides the following advantages:

More accurate copy current for high current ratio (for example, greater than 1000)

- Better linearity because V_{ifb} variation doesn't introduce input error
- Faster response time due to no feed back loop capacitor
- 0mV input error voltage (I_{fb} not created by an amplifier)
- Simpler circuit design

[0025] Finally, it will be understood that although the new copy current circuits for high current ratio described above in relation to FIG. 2 and FIG. 3 have presented the invention in the context of High-side switches, the invention could equally be applied to low-side switch circuits.

[0026] Referring now to FIG. 4A, it will be appreciated that the circuit 250 of FIG. 2 can be considered as made up of P-type current mirror 410 (comprising bipolar PNP transistors 282 and 284) and NMOS current mirror 420 (comprising NMOS transistors 286 and 288), each of these current mirrors having inputs ***in*** and ***sd_in*** and having outputs ***out*** and ***sd_out***. Similarly, referring now to FIG. 4B, it will be appreciated that an complementary-type version of the circuit can be considered as made up of N-type current mirror 430 (comprising bipolar NPN transistors) and PMOS current mirror 440 (comprising PMOS transistors), each of these current mirrors having inputs ***in*** and ***sd_in*** and having outputs ***out*** and ***sd_out.***

[0027] It will be appreciated that, based on the current mirrors 410 and 420, the circuit of FIG. 2 can be redrawn as shown in FIG. 5. As shown, the bipolar transistor current mirror 410 is supplied from supply voltage V_{bat} via a resistor R and low impedance voltage source V respectively, the low impedance source V being generated by the power FET 260 and the load, and the resistor R representing the on-state drain-to-source resistance (r_{dson}) of the FET sense transistor 270 of FIG. 2. It will be understood that $V = V_{bat}$-V_{out}, which will be copied across the resistor R and so the voltage error V_ε will be 0mV due to no loop gain. The only voltage between ***sd_out*** and ***sd_in*** can be the offset of the structure (components unmatched).

[0028] FIG. 6A shows a version of the circuit of FIG. 5, working when the source voltage is connected to V_{bat} (source up), in which the current feedback resistor R_{ifb} is not shown for simplicity. Similarly, FIG. 6B shows a complementary version of the circuit of FIG. 5, working when the source voltage is connected to the *Gnd*

(source down). It will be understood that the current mirror 410 of FIG. 6A could be replaced by the current mirror 440 (since any P-type current mirror could be used at this position), and the current mirror 420 of FIG. 6A could be replaced by the current mirror 430 (since any N-type current mirror could be used at this position); similarly, it will be understood that the current mirror 440 of FIG. 6B could be replaced by the current mirror 410 (since any P-type current mirror could be used at this position), and the current mirror 430 of FIG. 6B could be replaced by the current mirror 420 (since any N-type current mirror could be used at this position). It will be appreciated that in both the circuit of FIG. 6A and 6B (and also in the circuit of FIG. 5), the output current I is generally given by $I = \frac{2.V}{R}$

[0029] Thus it will be appreciated that the output current I is generated by applying a voltage V across R without using an amplifier having a closed loop of unity gain.

[0030] It will therefore be appreciated that the circuit 250 of FIG. 2 is a particular case of the general circuit of FIG. 5 (and 6A), the voltage generator V_{out} being the voltage across the drain-to-source of the power MOS transistor 260, the resistor R being the resistance of the sense MOS transistor 270, and the current output going directly through the current feedback resistor R_{ifb} to create the voltage V_{ifb}.

[0031] Thus it will be understood that the general circuits of FIG. 6A and 6B can be used in other circuits other than a copy current in a power switch, for example where it is desired to transform a voltage to a current without error voltage and without using a closed loop amplifier, where the source impedance is small compare to the output impedance R. If the internal impedance of the source is not negligible (but known, as in the case where it is desired to copy a voltage across a resistor R_{in} biased by a current source), the internal impedance of the source can be compensated by adding the same impedance R_{in} in series with the output resistor R to compensate error due to internal impedance.

[0032] Another possible application involves an EEPROM cell, where for example an NMOS transistor in block 420 (FIG. 4A) is replaced by a EEPROM cell (effectively an NMOS transistor with adjustable threshold voltage). If in this block the MOS transistor 288 has a threshold of 1V over the transistor MOS transistor 286, this is equivalent to the FIG. 6B arrangement with a voltage V of 1V and standard NMOS transistors.

Claims

1. A copy current circuit arrangement (250), comprising:

a first branch for carrying a first current (I_{load});
a second branch for carrying a second current ($2I_{fb}$); and
current mirror means (282, 284, 286, 288) coupled between the first branch and the second branch, wherein the second current ($2I_{fb}$) is a copy representative of the first current (I_{load}).

2. The copy current circuit arrangement as claimed in claim 1, wherein the current mirror means (282, 284, 286, 288) comprises:

first current mirror means (282, 284) comprising a first bipolar transistor (282) and a second bipolar transistor (284), the first and second bipolar transistors having their bases coupled together;
second current mirror means (286, 288) comprising a first MOSFET transistor (286) connected in series with the first bipolar transistor (282) and a second MOSFET transistor (288) connected in series with the second bipolar transistor (284), the first and second MOSFET transistors having their gates coupled together; and
start-up current means (299) arranged to apply a start-up current to the junction between the first bipolar transistor (282) and the first MOSFET transistor (286).

3. The copy current circuit arrangement as claimed in claim 2, wherein the first (282) and second (284) bipolar transistors are PNP transistors.

4. The copy current circuit arrangement as claimed in claim 2 or 3, wherein

the first current mirror means further comprises:

a third bipolar transistor (283) of opposite conductivity type to the first bipolar transistor (282), the base of the third bipolar transistor (283) being coupled to the collector of the first bipolar transistor (282), the collector of the third bipolar transistor (283) being coupled to the emitter of the first bipolar transistor (282), and the emitter of the third bipolar transistor (283) being coupled to the collector of the first bipolar transistor (282) and to the first MOSFET transistor (286); and a fourth bipolar transistor (285) of opposite conductivity type to the second bipolar transistor (284), the base of the fourth bipolar transistor (285) being coupled to the collector of the second bipolar transistor (284), the collector of the fourth bipolar transistor (285) being coupled to the emitter of the second bipolar transistor (284), and the emitter of the fourth bipolar transistor (285) being coupled to the collector of the second bipolar transistor (284) and to the second MOSFET transistor (288).

5. The copy current circuit arrangement as claimed in

claim 2, 3 or 4, wherein the second current mirror means comprises:

a third MOSFET transistor (294) coupled in series with the second MOSFET transistor (288), and a fourth MOSFET transistor (296) coupled in series with the start-up current means, the third MOSFET transistor (294) and the fourth MOSFET transistor (296) having their gates coupled together.

6. The copy current circuit arrangement as claimed in claim 5, further comprising a sixth MOSFET transistor (292) coupled in series with the fourth MOSFET transistor (296), the gate and source of the sixth MOSFET transistor (292) being coupled together and to the junction between the first bipolar transistor (282) and the first MOSFET transistor (286).

7. The copy current circuit arrangement as claimed in any one of claims 2-6, further comprising a seventh MOSFET transistor (298) coupled in series between the bases of the first (282) and second (284) bipolar transistors and the drain electrodes of the third (294) and fourth MOSFET transistors (296), the gate of the seventh MOSFET transistor (298) being coupled to the junction between the first bipolar transistor (282) and the first MOSFET transistor (286).

8. The copy current circuit arrangement as claimed in any preceding claim, wherein the first (I_{load}) and second currents ($2I_{fb}$) are in a ratio of the order of 1000.

9. The copy current circuit arrangement as claimed in any preceding claim, wherein the first branch comprises power switch means (260).

10. The copy current circuit arrangement as claimed in any one of claims 2-9, wherein the start-up current means is arranged also to provide bias during circuit operation.

11. The copy current circuit arrangement as claimed in any preceding claim wherein the copy current circuit arrangement comprises a source-up circuit.

12. The copy current circuit arrangement as claimed in any one of claims 1-11 wherein the copy current circuit arrangement comprises a source-down circuit.

13. A method for copying current in a circuit arrangement (250), the method comprising:

providing a first branch for carrying a first current (I_{load});

providing a second branch for carrying a second current (2_{Ifb}); and

providing current mirror means (282, 284, 286, 288) coupled between the first branch and the second branch, wherein the second current ($2I_{fb}$) is a copy representative of the first current (I_{load}).

14. The method as claimed in claim 13, wherein the current mirror means (282, 284, 286, 288) comprises:

first current mirror means (282, 284) comprising a first bipolar transistor (282) and a second bipolar transistor (284), the first and second bipolar transistors having their bases coupled together;

second current mirror means (286, 288) comprising a first MOSFET transistor (286) connected in series with the first bipolar transistor (282) and a second MOSFET transistor (288) connected in series with the second bipolar transistor (284), the first and second MOSFET transistors having their gates coupled together; and

start-up current means (299) arranged to apply a start-up current to the junction between the first bipolar transistor (282) and the first MOSFET transistor (286).

15. The method as claimed in claim 14, wherein the first (282) and second (284) bipolar transistors are PNP transistors.

16. The method as claimed in claim 14 or 15, wherein the first current mirror means further comprises:

a third bipolar transistor (283) of opposite conductivity type to the first bipolar transistor (282), the base of the third bipolar transistor (283) being coupled to the collector of the first bipolar transistor (282), the collector of the third bipolar transistor (283) being coupled to the emitter of the first bipolar transistor (282), and the emitter of the third bipolar transistor (283) being coupled to the collector of the first bipolar transistor (282) and to the first MOSFET transistor (286); and

a fourth bipolar transistor (285) of opposite conductivity type to the second bipolar transistor (284), the base of the fourth bipolar transistor (285) being coupled to the collector of the second bipolar transistor (284), the collector of the fourth bipolar transistor (285) being coupled to the emitter of the second bipolar transistor (284), and the emitter of the fourth bipolar transistor (285) being coupled to the collector of the second bipolar transistor (284) and to the second MOSFET transistor (288).

17. The method as claimed in claim 14, 15 or 16, wherein the second current mirror means comprises:

a third MOSFET transistor (294) coupled in series with the second MOSFET transistor (288), and a fourth MOSFET transistor (296) coupled in series with the start-up current means, the third MOSFET transistor (294) and the fourth MOSFET transistor (296) having their gates coupled together.

18. The method as claimed in claim 17, further comprising a sixth MOSFET transistor (292) coupled in series with the fourth MOSFET transistor (296), the gate and source of the sixth MOSFET transistor (292) being coupled together and to the junction between the first bipolar transistor (282) and the first MOSFET transistor (286).

19. The method as claimed in any one of claims 14-18, further comprising a seventh MOSFET transistor (298) coupled in series between the bases of the first (282) and second (284) bipolar transistors and the drain electrodes of the third (294) and fourth MOSFET transistors (296), the gate of the seventh MOSFET transistor (298) being coupled to the junction between the first bipolar transistor (282) and the first MOSFET transistor (286).

20. The method as claimed in any one of claims 13-19, wherein the first (I_{load}) and second current ($2I_{fb}$) are in a ratio of the order of 1000.

21. The method as claimed in any one of claims 13-20, wherein the first branch comprises power switch means (260).

22. The method as claimed in any one of claims 14-21, wherein the start-up current means also provides bias during circuit operation.

23. The method as claimed in any one of claims 13-22 wherein the circuit arrangement comprises a source-up circuit.

24. The method as claimed in any one of claims 13-22 wherein the circuit arrangement comprises a source-down circuit.

FIG. 1B - Prior Art

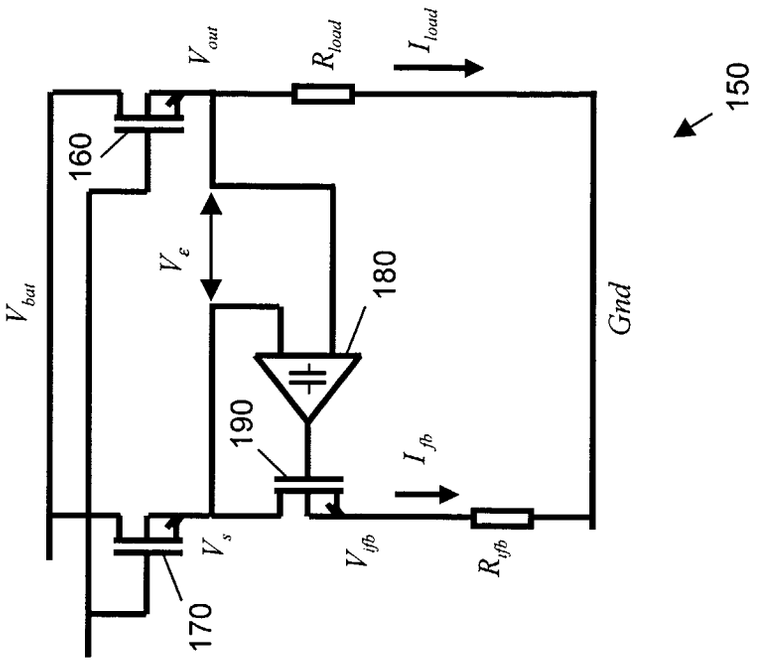


FIG. 1A - Prior Art

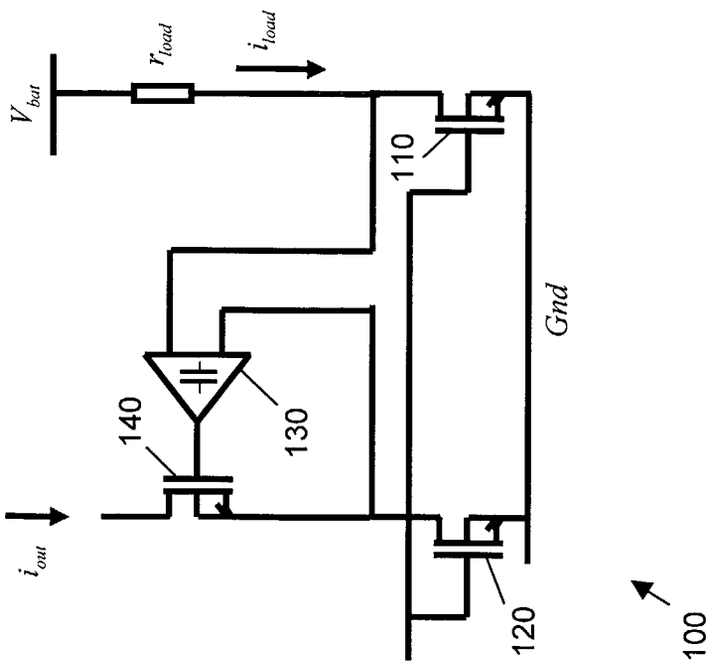
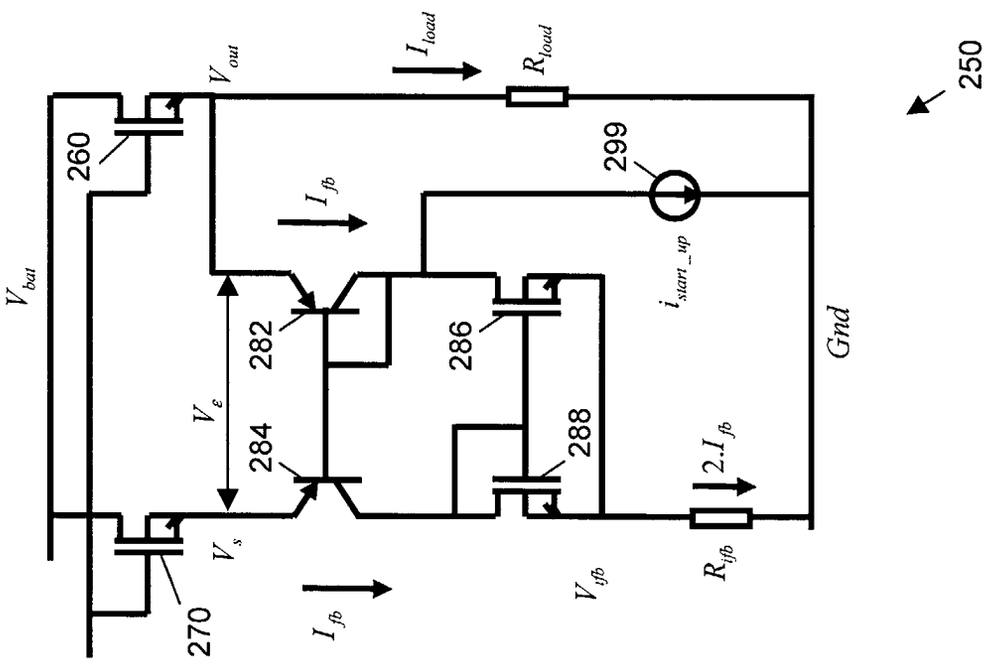


FIG. 2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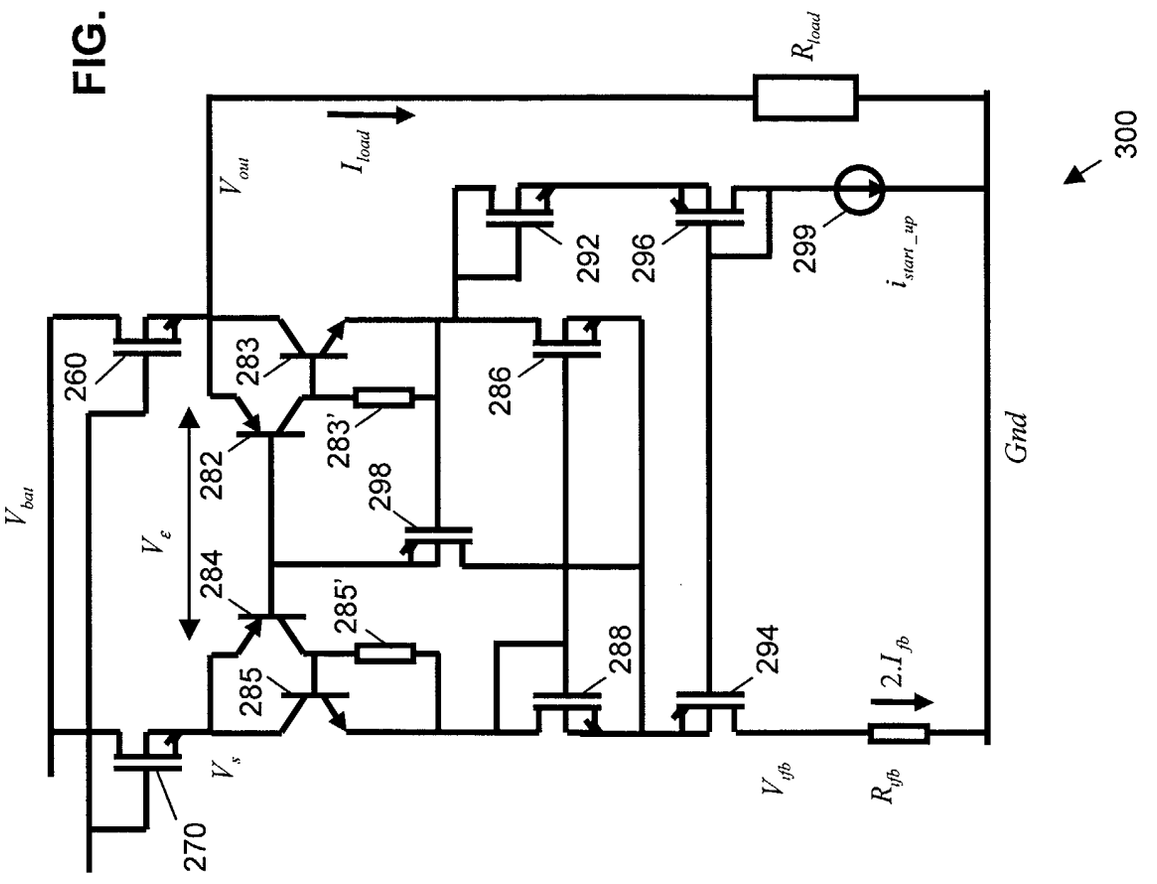
V_{out}
I_{load}
R_{load}
260
299
I_{fb}
V_{bat}
i_{start_up}
282
286
V_ε
284
288
$2.I_{fb}$
Gnd
V_s
V_{ifb}
R_{ifb}
270
I_{fb}

FIG. 3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V_s
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Gnd
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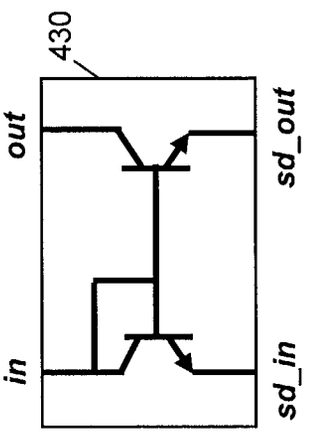
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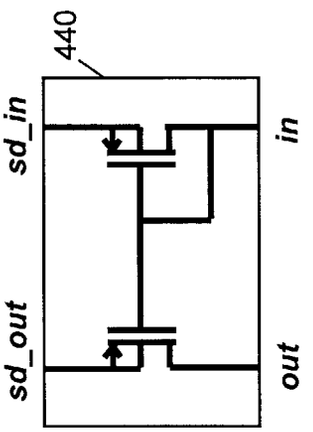
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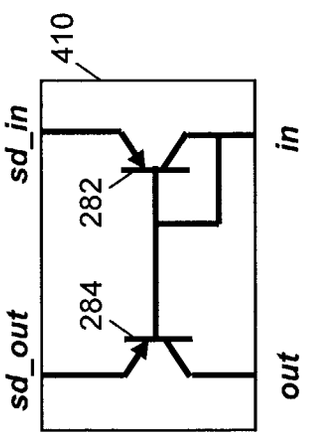
sd_out
out

FIG. 4B


410
sd_in
282
in
284
sd_out
out

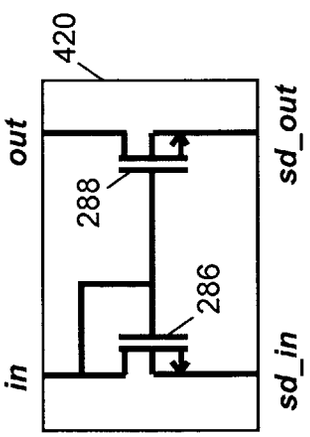

420
out
288
sd_out
286
in
sd_in

FIG. 4A

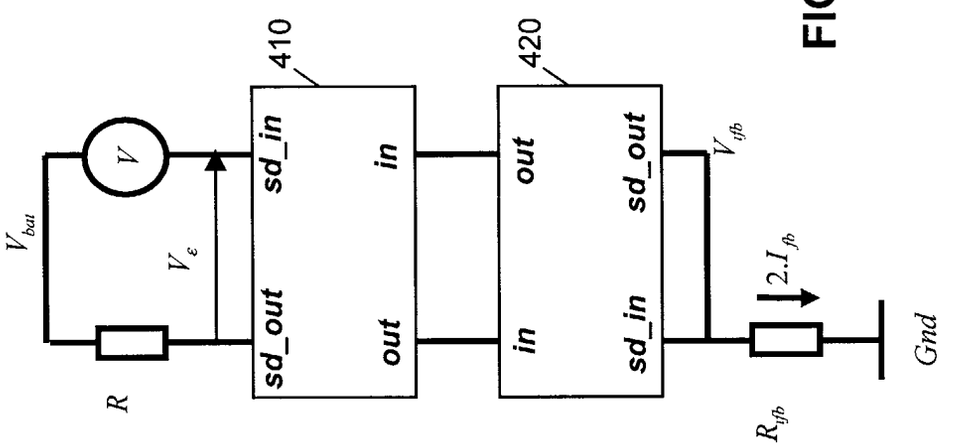

410
420
V
V_{bat}
V_ε
R
sd_in
in
sd_out
out
out
sd_out
in
sd_in
V_{ifb}
$2.I_{fb}$
R_{ifb}
Gnd

FIG. 5

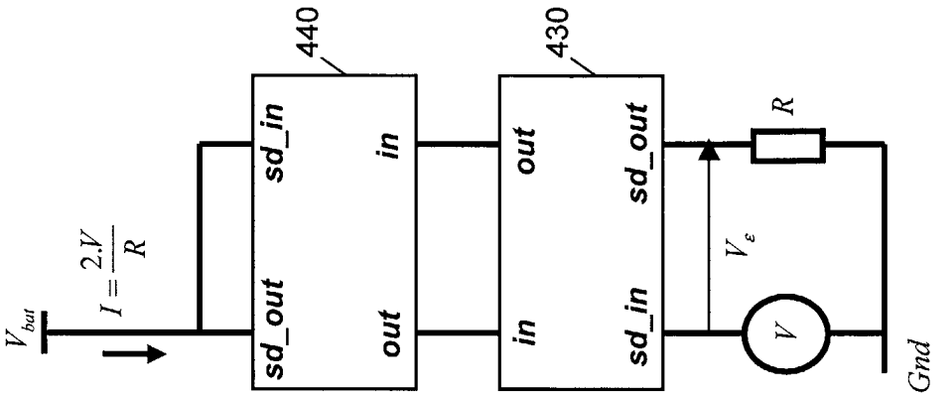

440
430
V_{bat}
$I = \frac{2.V}{R}$
sd_out
sd_in
out
in
in
out
sd_in
sd_out
V_ε
R
V
Gnd

FIG. 6B

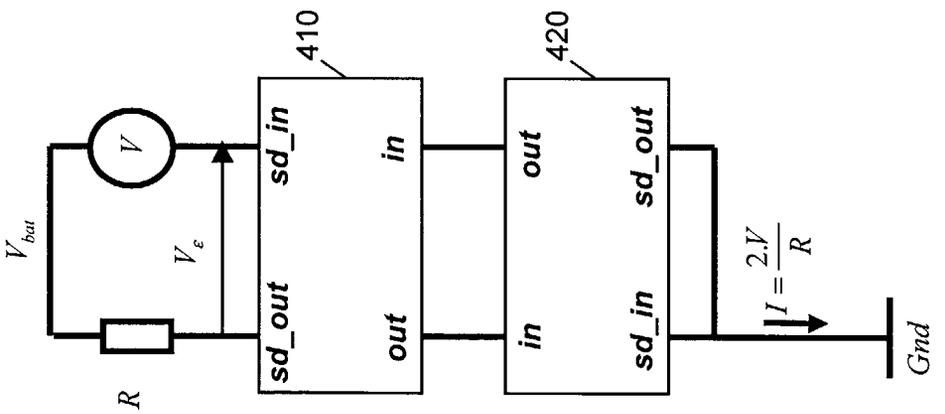

410
420
V_{bat}
V
V_ε
R
sd_out
sd_in
out
in
in
out
sd_in
sd_out
$I = \frac{2.V}{R}$
Gnd

FIG. 6A

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 02 29 1922

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
X A	US 6 351 111 B1 (LARAIA J MARCOS) 26 February 2002 (2002-02-26) * the whole document *	1-3, 13-15 4-12, 16-24	G05F3/26
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TECHNICAL FIELDS SEARCHED (Int.Cl.7)

G05F

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	12 March 2003	Schobert, D

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12-03-2003

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