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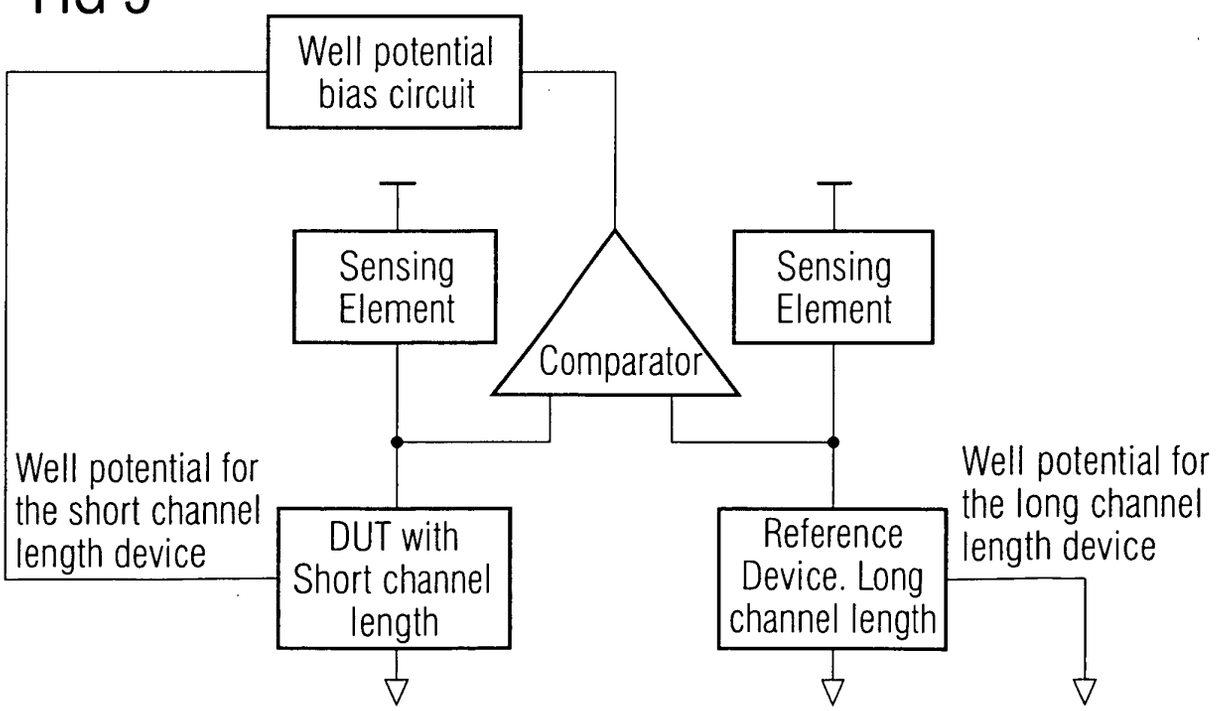
(54) Semiconductor device for adjusting threshold value shift due to short channel effect

(57) The present invention generally relates to a semiconductor device and more specific to a semiconductor device for detecting and adjusting leakage current dependent on threshold voltage of an integrated semiconductor device implemented in sub-micron technology, i.e. transistors, and a method related thereto. To adjust the threshold voltage variation due to uncertainties in the channel length induced by the fabrication process (short channel effect) in the semiconductor a comparison between small and long channel devices is proposed. According to the comparison result, a bias potential is provided to the semiconductor device to adjust the threshold voltage.

FIG 5



EP 1 396 777 A1

Description

[0001] The present invention generally relates to a semiconductor device and more specific to a semiconductor device for detecting and adjusting leakage current dependent on threshold voltage of an integrated semiconductor device implemented in sub-micron technology, i.e. transistors, and a method related thereto.

[0002] Recent measurements taken on NMOS and PMOS transistors implemented in sub-micron technologies have shown a great dependence of the threshold voltage values of the transistors on the channel length. Transistors realised in sub-micron technology provide a channel length below 1μm. Figure 1 shows a cross-section of a state of the art NMOS transistor in sub-micron technology on a bulk or wafer (6). The distance between n-doped-source (1) and -drain (2) under gate (3) in a p-doped-well 5 is referred to as the channel length (4). A small channel length variation which may be caused by tolerances in the fabrication process, can shift the threshold voltage value around 80 mV. Figure 2 shows the qualitative evolution of the threshold voltage value versus the channel length L in logarithmic scale. When minimum length transistors with low threshold voltage values (V_t) are implemented (with V_t in the range from 0 mV to 400 mV), a small variation of the channel length has great impact on the threshold voltage value (see Fig. 2). This effect is referred to as Short Channel Effect. Therefore, the shift due to the uncertainty introduced in the channel length has a great impact in the performance of the device. Moreover, the impact on the performance of the circuits provided with these transistors is also highly affected in terms of static and dynamic terms. For digital circuits, static and dynamic power consumption increases and the performance in terms of speed is also affected. With regard to these problems, it is necessary to implement any kind of strategy capable to determine whether the length of minimum length devices (NMOS and PMOS transistors) is shifted and therefore causes a change in the threshold voltage value V_t.

[0003] Besides of the shifting in V_t due to variations in the channel length L, V_t can also change by reason of the doping dose used to implant the channel or a change in the thickness of the gate oxide. These two technology parameters, the doping dose and thickness of the oxide, will determine the status of the transistors. Three different status are allocated, "fast", "nominal" and "slow" corresponding to small, nominal and high value of V_t, respectively. Short channel effects can appear in any one of these status of the technology.

[0004] Several strategies have been reported to establish a certain well potential bias in digital circuits when this bias is necessary. Well known strategies are based on delay lines and off current detection. Delay lines are formed by several transistors in series. Therefore, a change of the V_t value of the transistors changes the introduced delay. In dependence of the introduced delay the well potential bias is applied. The strategy based on delay lines can also be realised using critical path replicas. US 6,091,283 describes a subthreshold leakage tuning circuit which aims to compensate for process, activity and temperature-induced device threshold variations in a semiconductor circuit having a transistor, a potential of the gate wherein the transistor is held to a preset subthreshold potential and a channel current of the channel region is compared with a reference current to obtain a comparison result. A bias potential of a substrate is adjusted according to the comparison result to hold the subthreshold current at the reference current. The reference current is provided by a separate reference source. The device under test (DUT) is configured in a circuit in which the current is compared with said isolated reference current. The proposed method does only provide a solution for compensation for changes in device characteristics across process and temperature.

[0005] Another well known strategy is based on detection of the off current. However, some of these strategies require the use of band gap references to allow proper operation for a large range of temperatures. Moreover, none of these strategies allow to compare the performance of a DUT with the performance of a long channel device operating as a reference without requiring any additional temperature reference circuit.

[0006] It is thus an object of the invention to provide a semiconductor device and a method capable to detect the change of V_t due to the short channel effects but not the change due to the status of the technology whereby not requiring any additional temperature reference circuit. It is further an object of the invention to provide a semiconductor device and a method to adjust the V_t value by means of well potential control.

[0007] The object of the invention is solved by a semiconductor device that comprises a test circuit containing at least one transistor as a device under test (DUT) having a drain, a source, a gate and a channel region under the gate between the drain and the source with a short channel length, a reference circuit containing at least one transistor as a reference device having a drain, a source, a gate and a channel region under the gate between the drain and the source with a long channel length, a comparator circuit comparing the output of the test circuit with the output of the reference circuit and providing a comparison result and a bias circuit providing a bias potential to the well of the test circuit when the output of the test circuit is smaller than output of the reference circuit.

[0008] The new method is based on the use of a DUT or a group of parallel DUTs, implemented with minimum length, which are compared with a reference device, or a group of reference devices, designed with long channel length. It is understood that said bias circuit can be implemented on the same bulk or substrate as the test and reference circuit but may also be an external circuit. In front of many other reported solutions, according to the inventive semiconductor device the control of the

well potential is established by means of comparison of a device under test (DUT) with adjustable well potential and a long channel devise as a reference device (Reference) with a fixed well potential. Providing an appropriate potential to the well of the DUT leads to an increase of the absolute value of the threshold voltage and a decrease of the leakage current of the DUT. The well potential can be set to a fixed value referring to a minimum of the leakage current or adjusted in steps. When a reference circuit with one or more transistors with long channels is used to provide the reference in the semiconductor device according to the invention, the output of the reference circuit is smaller than that of the test circuit whenever the DUT is not affected by the Short Channel Effect. Thus, the shift of the threshold voltage due to the Short Channel Effect is detected and adjusted but not the variations due to changes in temperature or process. This achievement is enhanced by implementation of the test and the reference circuit on the same die of the semiconductor device and so that they are subject to the same temperature and process variations. By using a set of devices, i.e. transistors, both in the reference circuit and the test circuit a shift due to statistical variations of the threshold voltage is avoided. In other words, in the proposed invention, temperature variations are affecting to the output voltage of both circuits in a similar way. Therefore, it is not necessary to provide any kind of temperature compensation for a large range of operating temperatures.

[0009] Advantageously, a proper circuit design in the proposed invention allows only detection of the variation of V_t due to short channel effects. The short channel effects due to variations during the fabrication process will be common for all the implemented transistors in a wafer. However variations in the doping profile or the thickness of the gate oxide layer are also taken into account in the proposed invention. In order to minimise the impact of the statistic variation of the V_t of the DUTs and the reference device, several devices in parallel can be implemented.

[0010] Some preferred and advantageous developments of the inventive semiconductor device are adduced in the dependent claims. Particularly, the semiconductor device of the proposed invention can be applied to sense the off-current or the current in saturation of the DUT and the reference device. The method is not limited to cut-off operation of the devices. Moreover, the proposed compensation of the threshold voltage variation (due to uncertainties in the channel length introduced during the fabrication process) can be based on voltage monitoring or current detection. The possible strategies can be summarised as follows:

[0011] In a current mode the comparator circuit is addressed to achieve a fixed ratio between the current of the DUT and the reference circuit. In this mode, said comparator circuit compares the drain current of the test circuit with the drain current of the reference circuit and provides a comparison result and said bias circuit provides a bias potential to the well of the test circuit when the drain current of the test circuit is smaller than the drain current of the reference circuit.

In a voltage mode the output voltage of the DUT and the Reference circuit are monitored. In this mode, a first sensing element is connected to the drain of the DUT providing a test circuit output voltage according to the drain current of the test circuit. A second sensing element is connected to the drain of the reference device providing a reference circuit output voltage according to the drain current of the reference circuit. Said comparator circuit compares the output voltage of the test circuit with the output voltage of the reference circuit and said bias circuit provides a bias potential to the well of the test circuit when the output voltage of the test circuit is smaller than the output voltage of the reference circuit. In both modes the DUT and the Reference device can either work in saturation region or in cut-off region.

[0012] Furthermore, the method can be easily applied to control current consumption during the dynamic or the static operation of digital circuits. The control of the well potential of the DUT taking the output of the reference circuit as reference value in the comparator allows the adjustment of the current flowing through a sensing element. Therefore the applied value in the well of the DUT can be also applied to the digital circuits implemented in the same die.

[0013] Without limiting the scope of protection a preferred embodiment of the general invention is explained with reference to the accompanying drawings, which show in

Fig. 1: a cross-section of an NMOS transistor from the state of the art,

Fig. 2: a diagram of the qualitative evolution of the threshold voltage value versus the channel length,

Fig. 3: a block diagram of the semiconductor device according to the invention,

Fig. 4: a block diagram of the proposed detection method for threshold voltage variations due to short channel effects whereby the configuration is based on NMOS DUTs and NMOS reference devices,

Fig. 5: a block diagram of the proposed leakage current control method whereby the configuration is based on NMOS DUTs and NMOS reference devices,

Fig. 6 a: a circuit configuration for the detection of V_t variations in NMOS transistors of a reference circuit,

Fig. 6 b: a circuit configuration for the detection of V_t variations in NMOS transistors of a circuit under test,

Fig. 7: a diagram of the detection of "fast" DUTs with short channel effects in front of "fast" devices without short channel effects (case "fast" PMOS),

Fig. 8: a diagram of the detection of "fast" DUTs with short channel effects in front of "fast" devices without short channel effects (case "slow" PMOS),

Fig. 9: a diagram of the detection of "nom." DUTs with short channel effects in front of "nom." devices without short channel effects

Fig. 10: a diagram of the detection of "slow" DUTs with short channel effects in front of "slow" devices without short channel effects (case "fast" PMOS),

Fig. 11: a diagram of the detection of "slow" DUTs with short channel effects in front of "slow" devices without short channel effects,

Fig. 12: a circuit configuration for the control of the leakage current based on the proposed method for detection of V_t variation,

Fig. 13: a diagram of the output voltage evolution when back bias is applied to the p-well of the NMOS DUTs of the test circuit and the reference devices are tied to ground (case T=25°C and 125°C, and "fast" transistors),

Fig. 14: a diagram of the output voltage evolution when back bias is applied to the p-well of the NMOS DUTs of the test circuit and the reference devices are tied to ground (case T=25°C and 125°C, and "nom." transistors),

Fig. 15: a diagram of the output voltage evolution when back bias is applied to the p-well of the NMOS DUTs of the test circuit and the reference devices are tied to ground (case T=25°C and 125°C, and "slow" transistors),

Fig. 16: a circuit configuration for the detection of V_t variations in NMOS transistors based on detection of current in saturation,

Fig. 17: a diagram of the detection of "nom." DUTs with short channel effects in front of "nom." devices without short channel effects when circuit configuration of Fig. 15 is implemented,

Fig. 18: a diagram of the output voltage evolution when back bias is applied to the pwell of the NMOS DUTs of the test circuit and the reference devices are tied to ground (case T=25°C and 125°C, and "nom." transistors),

Fig. 19: a block diagram of the method according to the invention based on current comparison,

Fig. 20: an implementation of the inventive semiconductor device with transistors working in cut-off regime,

Fig. 21: an implementation of the inventive semiconductor device with transistors working in saturation regime,

Fig. 22: a general implementation of the inventive semiconductor device in which a voltage source bias the gate of the DUT and the reference device

Fig. 23: a block diagram of the leakage control method according to the invention.

[0014] As shown in Fig. 3 there are three constitutive circuit blocks that are required for detecting the V_t value variations. A first circuit block 7 with a device under test (DUT), a second circuit block 8 with a reference device and a third circuit block 9 with a comparator for comparing the outputs of the test circuit and the reference circuit. In order to control the current consumption of the circuit a change in the V_t value has to be detected and adjusted by a system capable to adjust the well potential to the desired value as shown in Fig. 4 and 5. The well potential can be applied by a charge pump in a well potential bias circuit 10, for instance. The test circuit contains the DUT and the reference circuit contains the reference devices on a wafer 11.

[0015] As shown in Fig. 4 and 5 both circuit blocks comprise a sensing element. The sensing element is a device providing a voltage drop caused by the current flowing through it. The current depends on the V_t of the DUT in the test circuit or the reference devices in the reference circuit. The sensing element is connected between V_{DD} and the drain of the DUT in the case of an NMOS DUT. A similar configuration is implemented for the reference circuit. In the case of PMOS DUT, the sensing element is connected between VSS and the drain of the PMOS devices. The output voltage is taken in the drain of the DUTs and the drain of the reference devices. The sensing element can be implemented with a resistor or a long channel transistor.

[0016] Adjustment of the threshold voltage is carried out comparing the output voltage of the test circuit 7 and the reference circuit 8. When the output voltage of the test circuit 7 is higher than the output voltage of the reference circuit 8 the well potential of the DUT is not adjusted. When the output voltage of the test circuit 7 is smaller, the well potential is decreased for the NMOS DUTs and increased for the PMOS DUTs. The well potential is changed up to the point in which the output of the test circuit 7 is equal to the output of the reference circuit 8. The output of the reference circuit 8 is maintained constant because the well potential of the reference devices is not changed. It is important to notice

that only in the case of having short channel effects in the DUT, the output voltage in the test circuit 7 is smaller than the output voltage in the reference circuit 8.

[0017] When this online detection of the V_t variation is implemented in a die 11 with other digital circuits 12, the adjustment of the well potential can be carried out for all the devices in all the circuits. In such a way, current consumption in dynamic operation would be reduced without penalty on the designed performance of the circuits. The performance is not degraded because the circuits are designed to work with a value of the V_t without short channel effect, thus, when the shift due to short channel is detected the V_t is adjusted to the right value, and the performance is adjusted to the designed one.

[0018] Following, two different examples are explained; one of them in which the gate of the DUT and the reference device are tied to ground so that the devices operate in cut-off region. The second one, the gate of the devices is fixed to a certain value allowing saturation operation of the transistors.

[0019] As depicted in Fig. 6a and Fig. 6b the reference device and the device under test are a set of devices in order to avoid the shifting due to statistical variations of V_t. With this configuration the output voltage is only affected by variations due to the length of the transistors. A PMOS transistor with the gate connected to its drain is used as sensing element. In the proposed semiconductor device the detection of the V_t shift is carried out for "fast", "slow", and "nominal" transistors. That is, the method is capable to determine when the shift in the V_t value is due to short channel effects or only to a change in the status of the devices (that is "fast", "slow" or "nom."). The semiconductor device according to the present invention will compensate the case in which the shift in V_t is only due to the short channel effect.

[0020] In this scenario simulations show how the short channel effects are detected from every status of operation (that is, "fast", "nom." or "slow" conditions) and for a large range of temperatures (0, 150°C). The simulations have been carried out in order to show that the output voltage of the reference circuit will be always smaller than the output voltage of the circuit under test when the DUTs are not affected by the short channel effect ("Fast Device" line for Fig. 7, "Fast NMOS Device" line in Fig. 8 , "Nom. Device" line in Fig. 9, "Slow NMOS Device" line in Fig. 10, and "Slow Device" in Fig. 11). However as depicted in the same figures (from Fig. 7 to Fig. 11) the output of the reference circuit is always greater than that of the DUT affected by the short channel effects ("Fast DUT" line for Fig. 7, "Fast NMOS DUT" line in Fig. 8, "Nom. DUT" line in Fig. 9, "Slow NMOS DUT" line in Fig. 10, and "Slow DUT" in Fig. 11).

[0021] In the proposed semiconductor device the current consumption control would be carried out as depicted in Fig. 12. The comparator would switch on or switch off the well potential bias block. The adjustment of the well potential can be easily implemented with charge pump circuits.

[0022] Simulations of the output voltage of the circuit under test show how the voltage is increased applying the well bias. However with the fixed value for the long channel devices the output of the reference circuit will be maintained constant, as depicted in Fig. 13, Fig. 14 and Fig. 15, when "fast", "nom." and "slow" status of the transistors are considered. The same behaviour has been checked for all the other possible combination of operating status between PMOS and NMOS transistors, that is "slow-fast" and "fast-slow".

[0023] The following example illustrates the detection of Vt and leakage control method based on the saturation regime of the DUTs and the reference devices.

[0024] In this example the DUT and the reference devices are working in saturation. The saturation can be fixed by connecting the gate of the NMOS DUTs and the reference devices to VDD. If low current consumption is desired, it is also possible to fix the gates to a lower voltage value allowing also saturation operating conditions, see Fig. 16. The same implementation presented in Fig. 4 and 5 will be also used in the case in which the gate of the DUTs and the reference transistors would be connected to voltage values allowing operation in saturation regime. The same operating principle pointed out above is also observed when the saturation current is detected. In nominal operating status, only the short channel effect is detected, and the detection is carried out for the operating temperature range as depicted in Fig. 17. The same behaviour has been also checked for the other status of operation ("fast", "slow", "slow-fast", "fast-slow"). As pointed out above the well potential would be adjusted up to the point in which the output voltage of the reference circuit and the circuit under test would be the same, see Fig. 18. The circuit configuration, depicted in Fig. 5, involving the comparator and the well potential bias circuit for the control of the leakage current, would be also implemented taking the outputs in the drains of the DUTs and the drains of the reference device as the inputs of the comparator.

[0025] In the Fig. 19 to 23 an embodiment of the inventive semiconductor device is illustrated whereby the threshold voltage variation is detected by current comparison. Fig. 19 shows a block diagram for current comparison when NMOS devices are considered. The configuration in which the devices work in cut-off regime is depicted in Fig. 20 whereas Fig. 21 shows a configuration in which the transistors are working in saturation regime. As can been seen from Fig. 22, in a more general configuration the gate of the transistors are tied to a desired value so that they operate in saturation regime whereby the current consumption is adjusted. In this scenario the control of the leakage current for a digital circuit would be establish as depicted in Fig. 23. In this block diagram the connection of the gate of the DUT and the reference devices can be any of the implemented in Fig. 20, Fig. 21, and Fig. 22.

Claims

1. Semiconductor device comprising

   - a test circuit (7) containing at least one transistor as a device under test (DUT) having a drain (2), a source (1), a gate (3) and a channel region (4) under the gate (3) between the drain and the source in a well (5) with a short channel length,
   - a reference circuit (8) containing at least one transistor as a reference device having a drain (2), a source (1), a gate (3) and a channel region (4) under the gate between the drain and the source in a well (5) with a long channel length,
   - a comparator circuit (9) comparing the output of the test circuit (7) with the output of the reference circuit (8) and providing a comparison result,
   - a bias circuit (10) providing a bias potential to the well (5) of the test circuit when the output of the test circuit (7) is smaller than output of the reference circuit (8).

2. Semiconductor device according to claim 1, **characterised in that**,

   - said comparator circuit (9) compares the drain current of the test circuit (7) with the drain current of the reference circuit (8) and provides a comparison result,
   - said bias circuit (10) provides a bias potential to the well (5) of the test circuit when the drain current of the test circuit (7) is smaller than the drain current of the reference circuit (8).

3. Semiconductor device according to claim 2, **characterised in that**,
   the gate (3) of said transistor of the test circuit (DUT) and said transistor of the reference circuit are connected to ground so that the transistors work in cut-off regime.

4. Semiconductor device according to claim 2, **characterised in that**,
   the gate (3) of said transistor of the test circuit (DUT) and said transistor of the reference circuit are connected to a fixed voltage so that the transistors work in saturation regime.

5. Semiconductor device according to claim 1, **characterised in that**,

   - a first sensing element is connected to the drain of the DUT in the test circuit (7) providing a test circuit output voltage according to the drain current of the test circuit (7),
   - a second sensing element is connected to the drain of the reference device providing a reference circuit (8) output voltage according to the drain current of the reference circuit (8),
   - said comparator circuit (9) compares the output voltage of the test circuit (7) with the output voltage of the reference circuit (8),
   - said bias circuit (10) provides a bias potential to the well (5) of the test circuit when the output voltage of the test circuit (7) is smaller than the output voltage of the reference circuit (8).

6. Semiconductor device according to claim 5, **characterised in that**,
   the gate (3) of said transistor of the test circuit (DUT) and said transistor of the reference circuit are connected to ground so that the transistors work in cut-off regime.

7. Semiconductor device according to claim 5, **characterised in that**,
   the gate (3) of said transistor of the test circuit (DUT) and said transistor of the reference circuit are connected to a fixed voltage so that the transistors work in saturation regime.

8. Semiconductor device according to claim 5, **characterised in that**,
   said transistors of the test circuit and of the reference circuit are NMOS transistors.

9. Semiconductor device according to claim 8, **characterised in that**,
   said first sensing element is connected between the drain of the DUT and V_{DD} voltage of the semiconductor device and said second sensing element is connected between the drain of the reference device and V_{DD} voltage of the semiconductor device.

10. Semiconductor device according to claim 5, **characterised in that**,
    said transistors of the test circuit and of the reference circuit are PMOS transistors.

11. Semiconductor device according to claim 10, **characterised in that**,
    said first sensing element is connected between the drain of the DUT and V_{SS} voltage of the semiconductor device and said second sensing element is connected between the drain of the reference device and V_{SS} voltage of the semiconductor device.

12. Semiconductor device according to claim 1, **characterised in that**,
    said bias circuit provides a bias potential to the well of the test circuit until the output of the test circuit is equal to the output of the reference circuit.

13. Semiconductor device according to claim 1, **characterised in that**, said bias circuit comprises a voltage source for providing a fixed potential to the well of the DUT and the well of further devices of a digital circuit (12) wherein said digital circuit (12) is integrated the semiconductor device.

14. Semiconductor according to claim 1, **characterised in that**, said bias circuit comprises a charge pump as a voltage source.

15. Method for detecting and adjusting variations of the threshold voltage V_t caused by short channel effect in a semiconductor device in sub-micron technology comprising a test circuit (7) containing at least one transistor as a device under test (DUT) having a drain (2), a source (1), a gate (3) and a channel region (4) under the gate between the drain and the source with a short channel length and a reference circuit (8) containing at least one transistor as a reference device having a drain (2), a source (1), a gate (3) and a channel region (4) under the gate between the drain and the source with a long channel length,
said method comprising,
comparing the output of the test circuit (7) with the output of the reference circuit (8),
providing a comparison result,
applying a bias potential to the well (5) of the test circuit when the output of the test circuit (7) is smaller than output of the reference circuit (8) according to the comparison result.

16. Method according to claim 15,
wherein the method comprises the steps,
connecting a first sensing element to the drain of the DUT, providing a test circuit output voltage according to the drain current of the test circuit by said first sensing element,
connecting a second sensing element to the drain of the reference device,
providing a reference circuit output voltage according to the drain current of the reference circuit by said second sensing element,
comparing the output voltage of the test circuit with the output voltage of the reference circuit by said comparator circuit,
providing a bias potential to the well of the test circuit when the output voltage of the test circuit is smaller than the output voltage of the reference circuit.

FIG 1

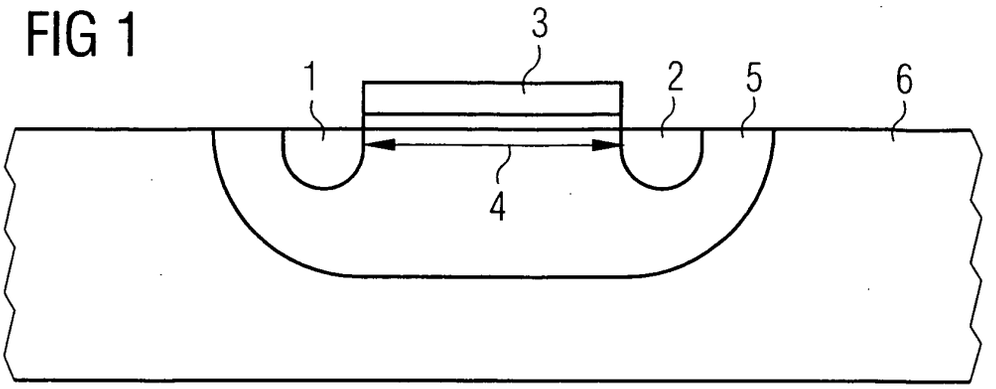


FIG 2

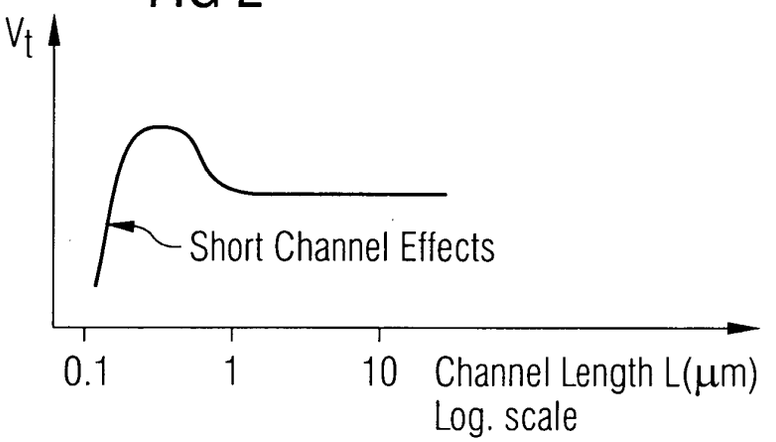


FIG 3

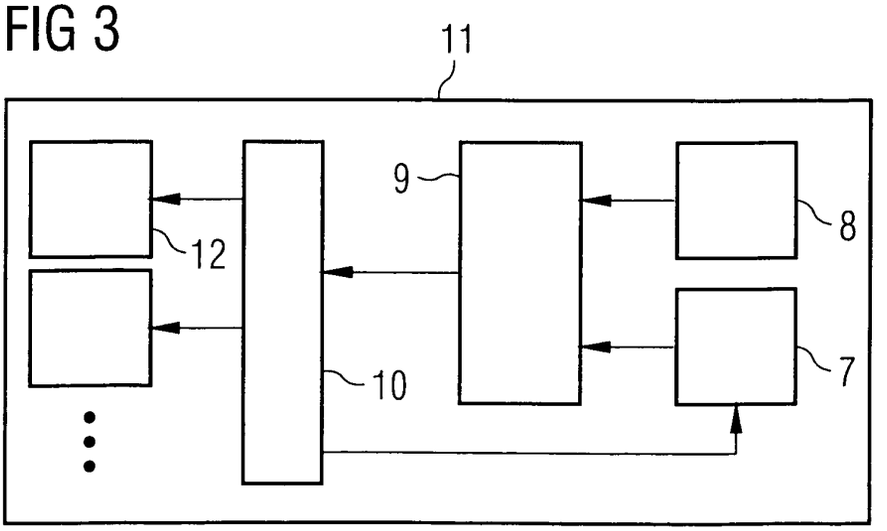


FIG 4

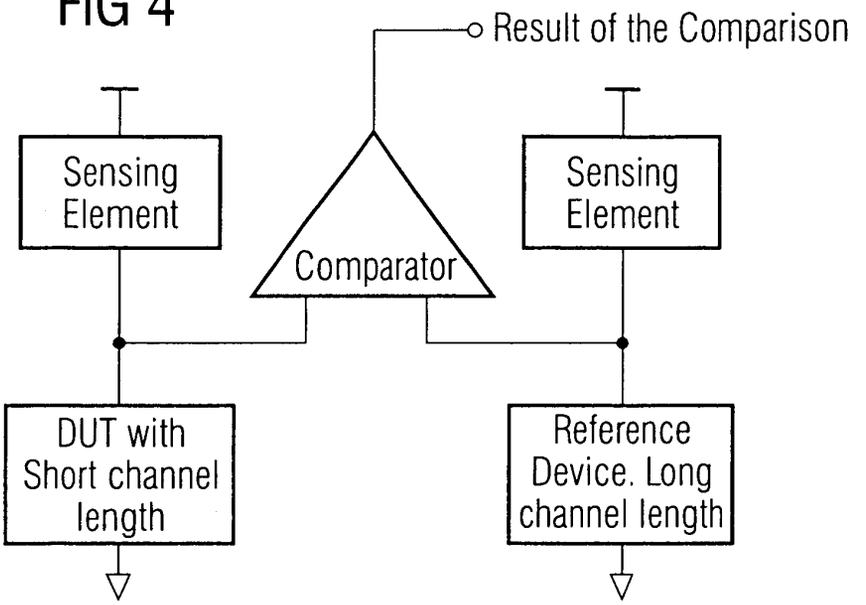

Result of the Comparison
Sensing Element
Comparator
Sensing Element
DUT with Short channel length
Reference Device. Long channel length

FIG 5

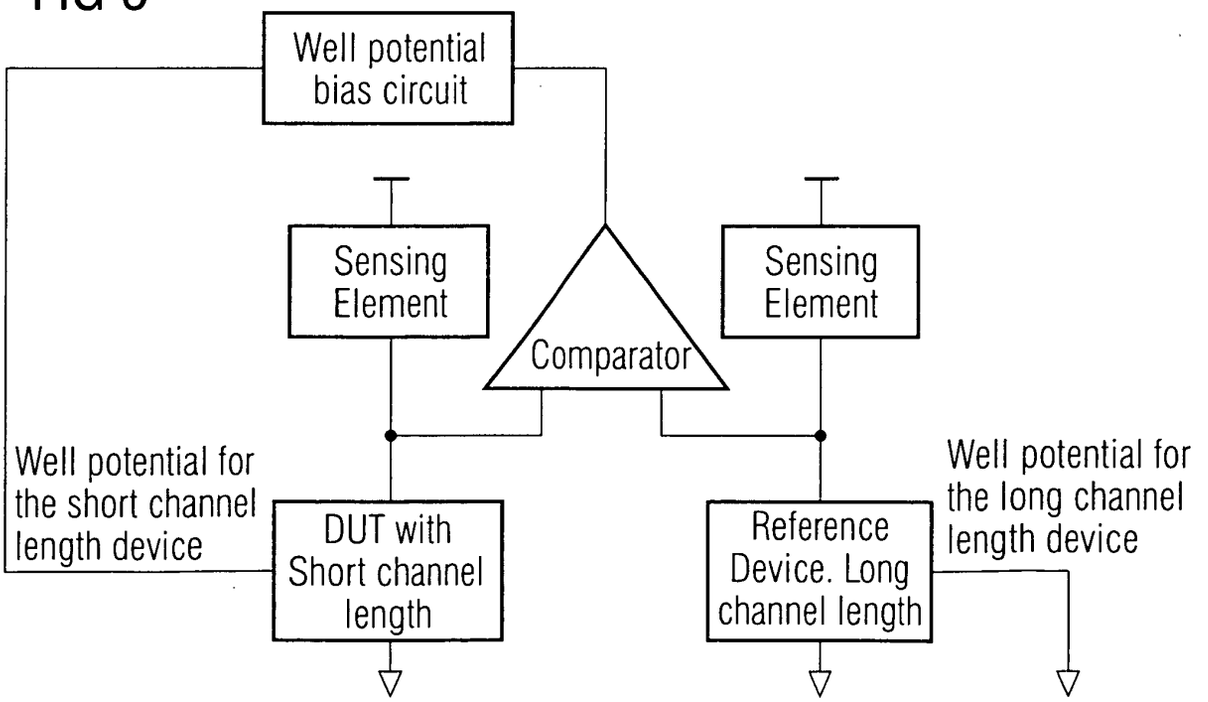

Well potential bias circuit
Sensing Element
Comparator
Sensing Element
Well potential for the short channel length device
DUT with Short channel length
Reference Device. Long channel length
Well potential for the long channel length device

FIG 6A

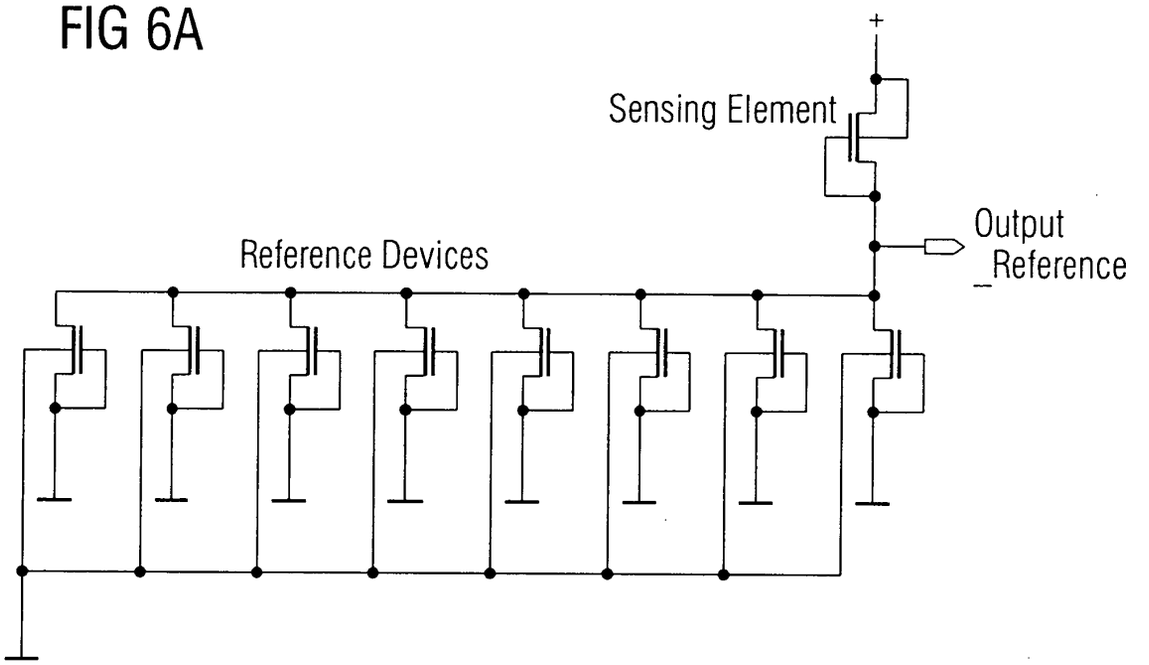

+
Sensing Element
Output
_Reference
Reference Devices

FIG 6B

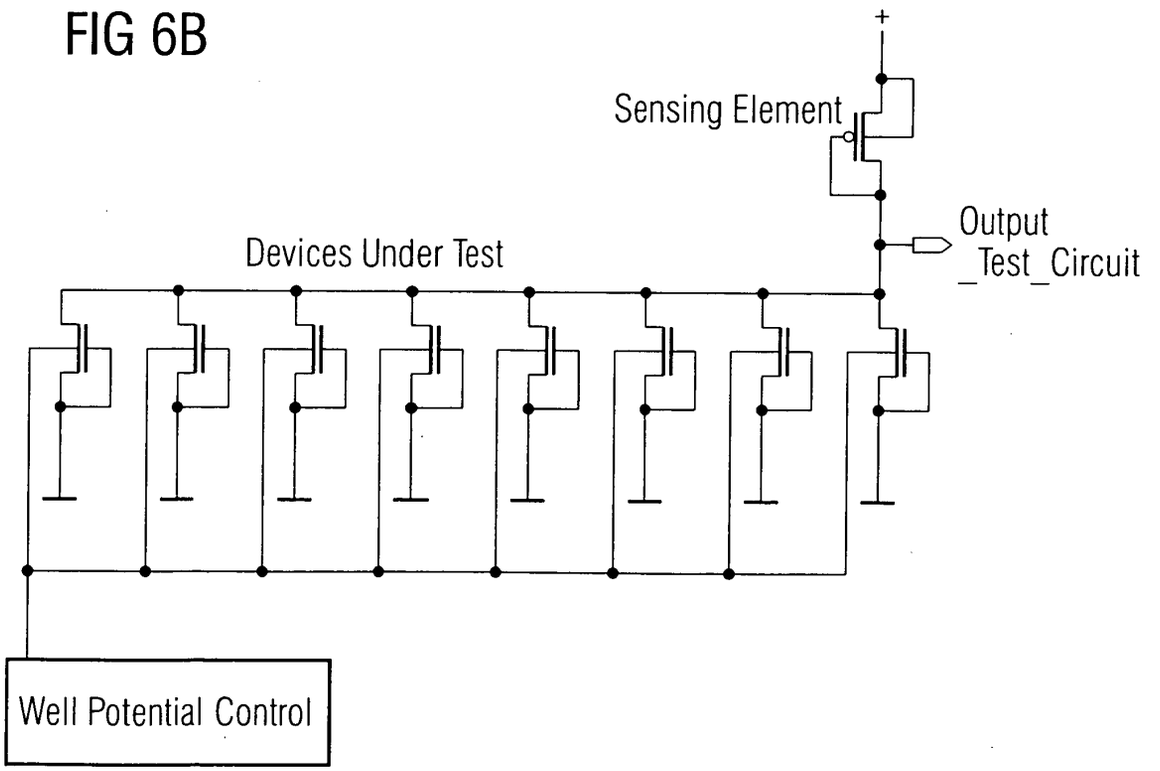

+
Sensing Element
Output
_Test_Circuit
Devices Under Test
Well Potential Control

FIG 7

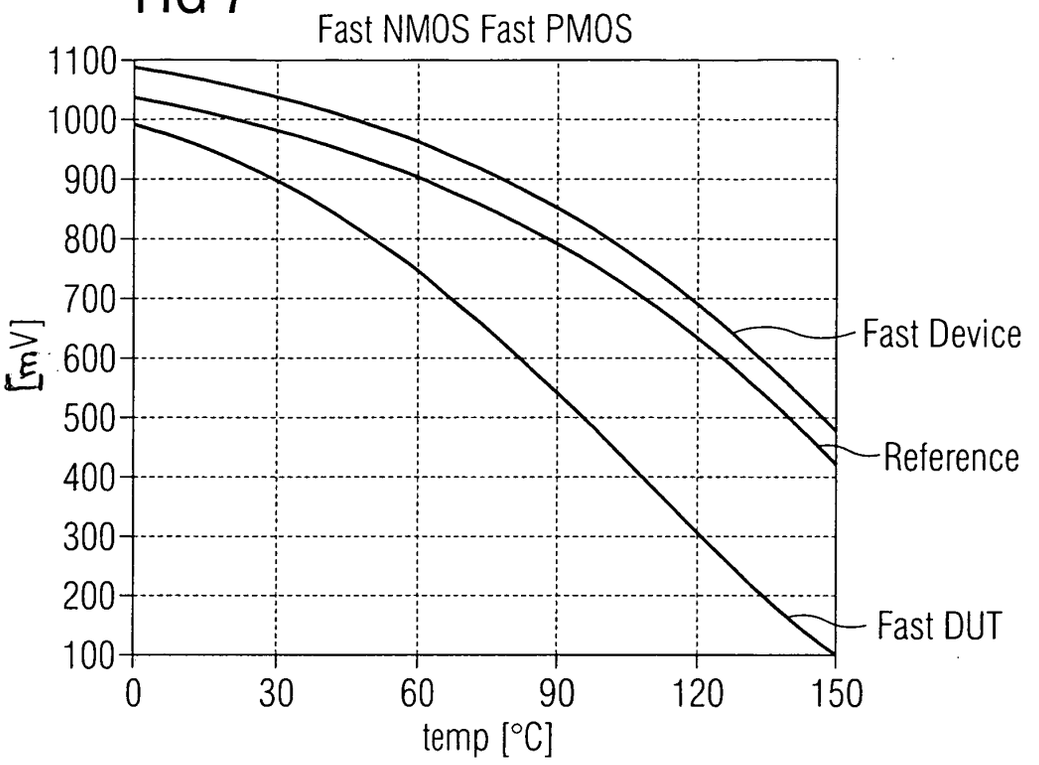

Fast NMOS Fast PMOS
1100
1000
900
800
700
600
500
400
300
200
100
[mV]
0
30
60
90
120
150
temp [°C]
Fast Device
Reference
Fast DUT

FIG 8

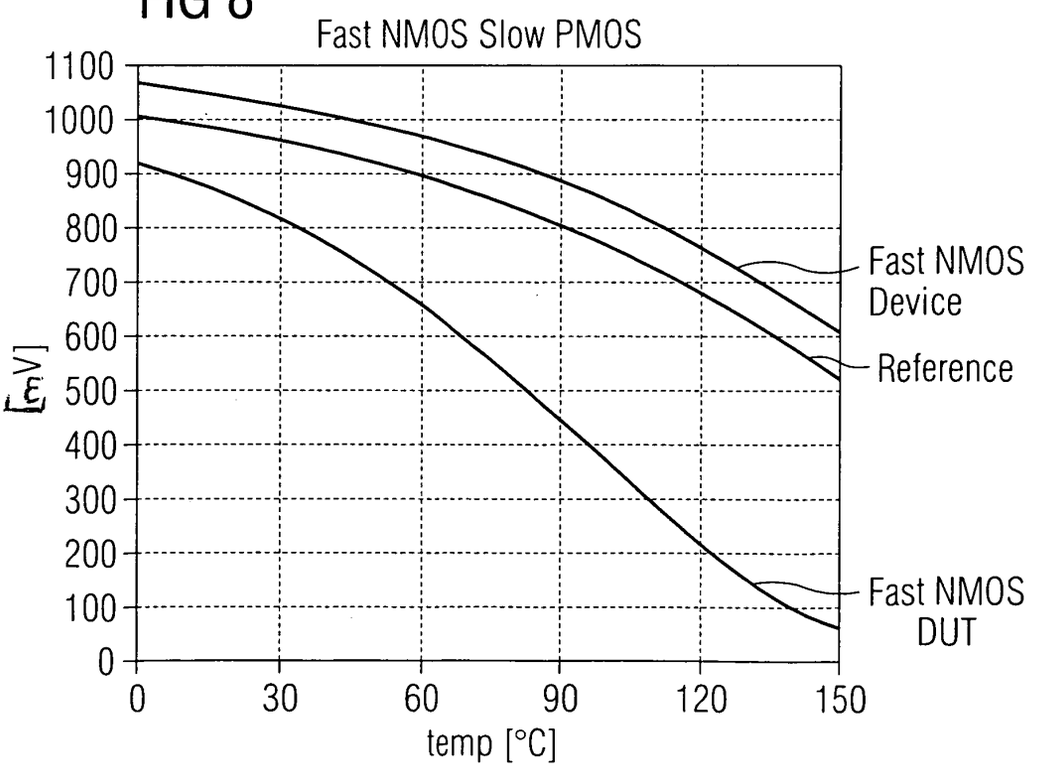

Fast NMOS Slow PMOS
1100
1000
900
800
700
600
500
400
300
200
100
0
[mV]
0
30
60
90
120
150
temp [°C]
Fast NMOS Device
Reference
Fast NMOS DUT

FIG 9

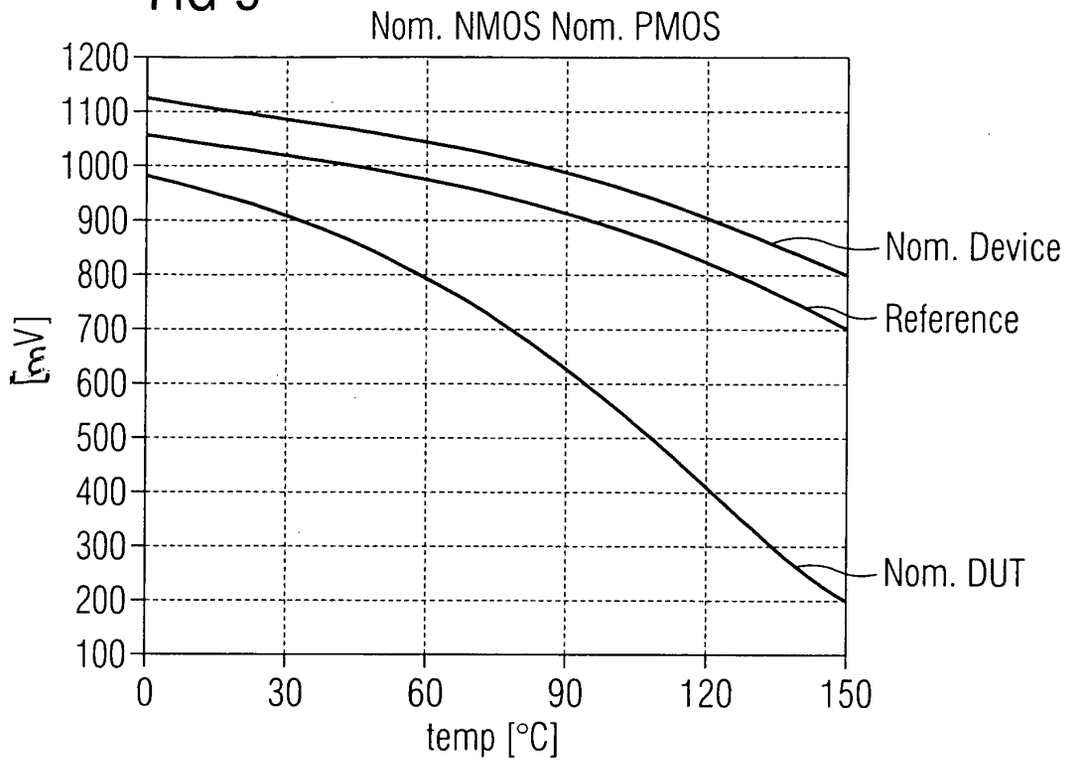

Nom. NMOS Nom. PMOS
1200
1100
1000
900
800
700
600
500
400
300
200
100
[mV]
0
30
60
90
120
150
temp [°C]
Nom. Device
Reference
Nom. DUT

FIG 10

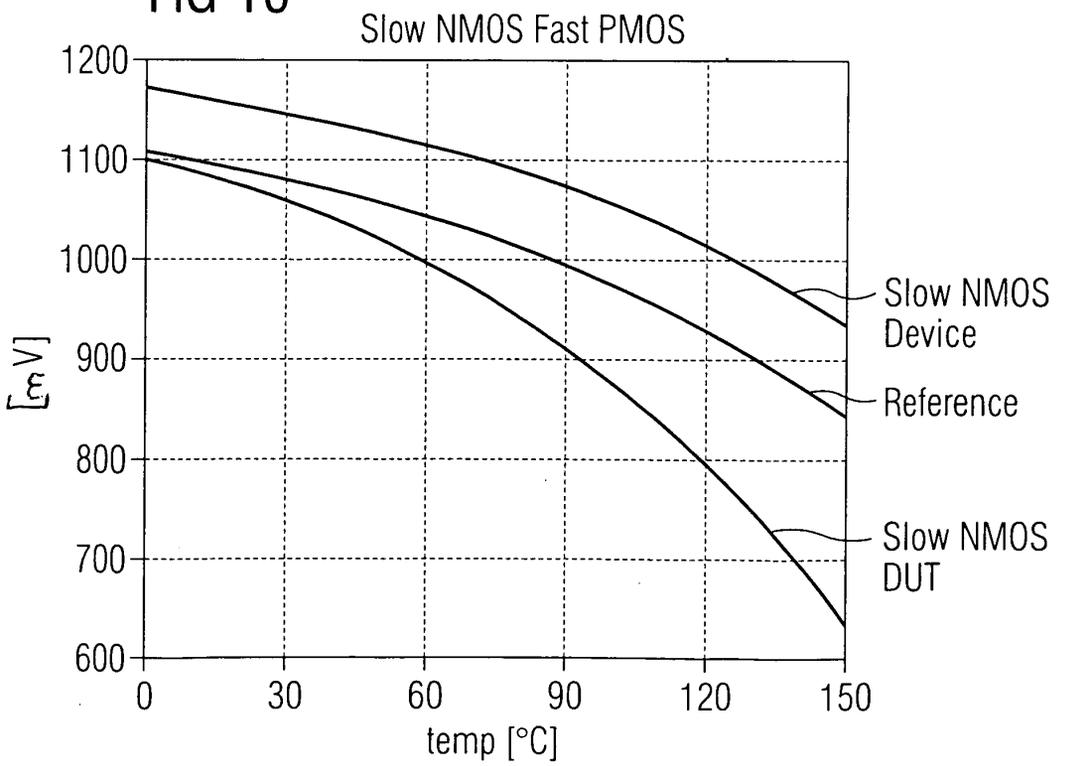

Slow NMOS Fast PMOS
1200
1100
1000
900
800
700
600
[mV]
0
30
60
90
120
150
temp [°C]
Slow NMOS Device
Reference
Slow NMOS DUT

FIG 11

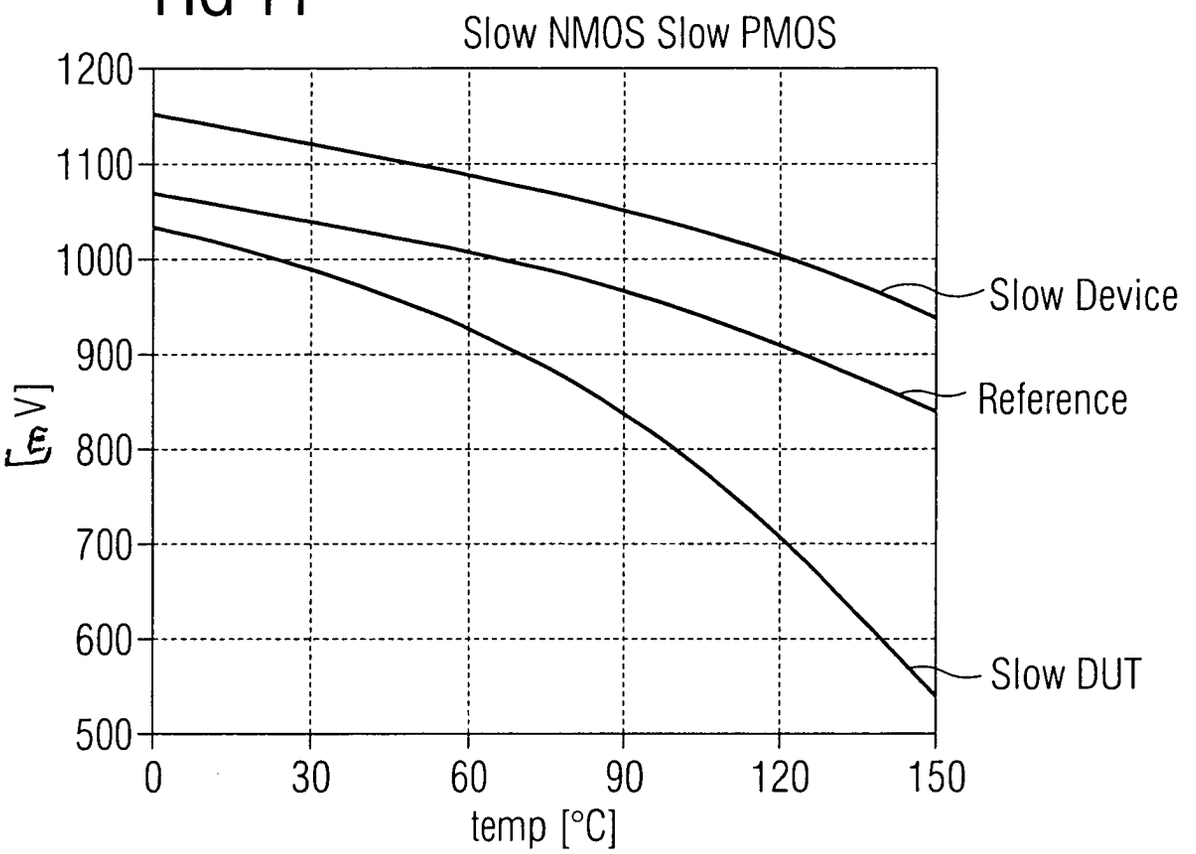

Slow NMOS Slow PMOS
1200
1100
1000
900
800
700
600
500
[mV]
0
30
60
90
120
150
temp [°C]
Slow Device
Reference
Slow DUT

FIG 12

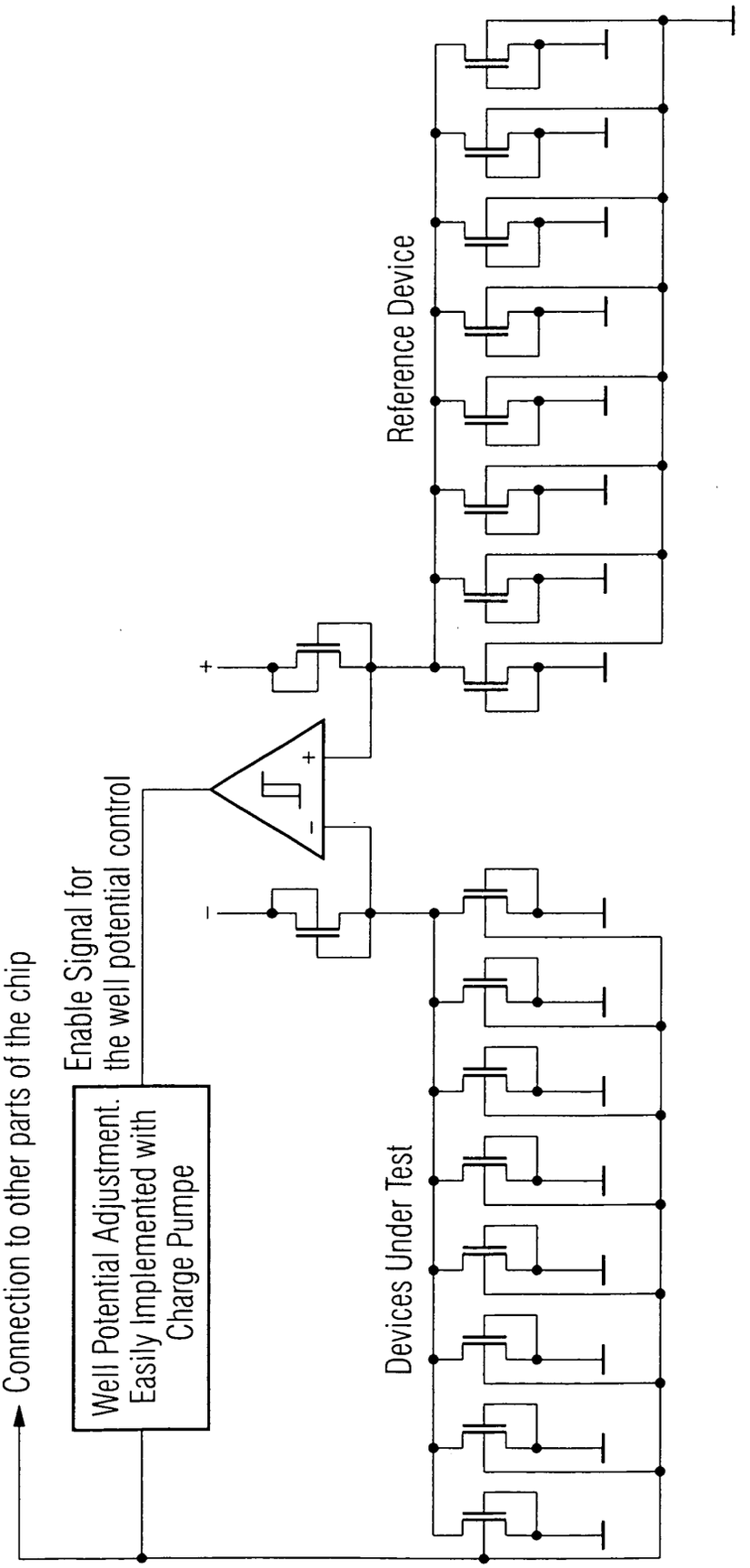

Connection to other parts of the chip
Well Potential Adjustment. Easily Implemented with Charge Pumpe
Enable Signal for the well potential control
Devices Under Test
Reference Device
+
-

FIG 13

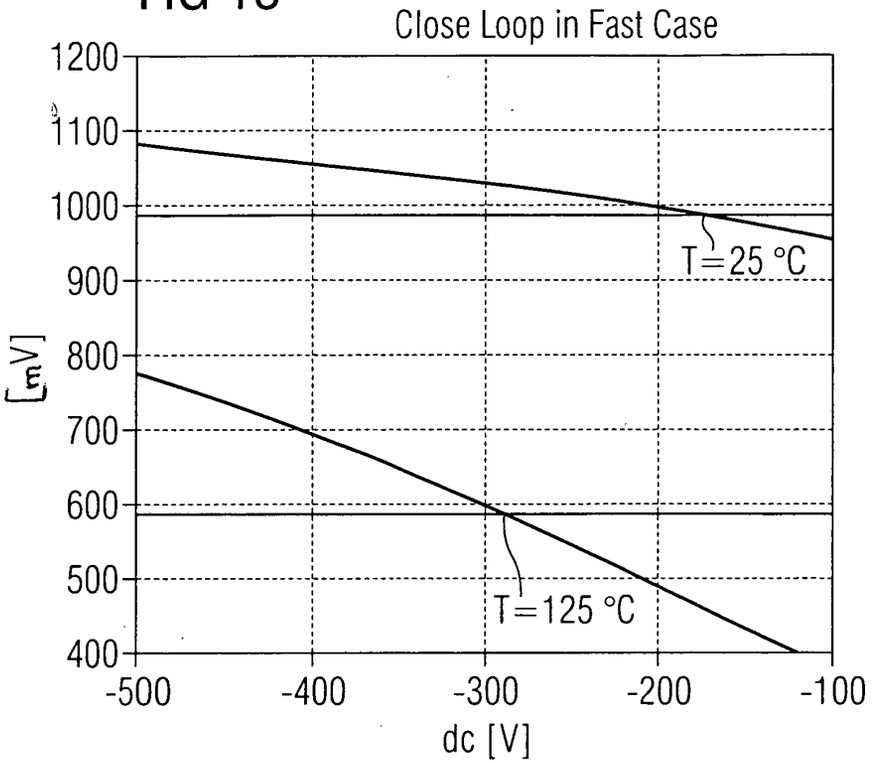

Close Loop in Fast Case
1200
1100
1000
900
800
700
600
500
400
[mV]
T=25 °C
T=125 °C
-500
-400
-300
-200
-100
dc [V]

FIG 14

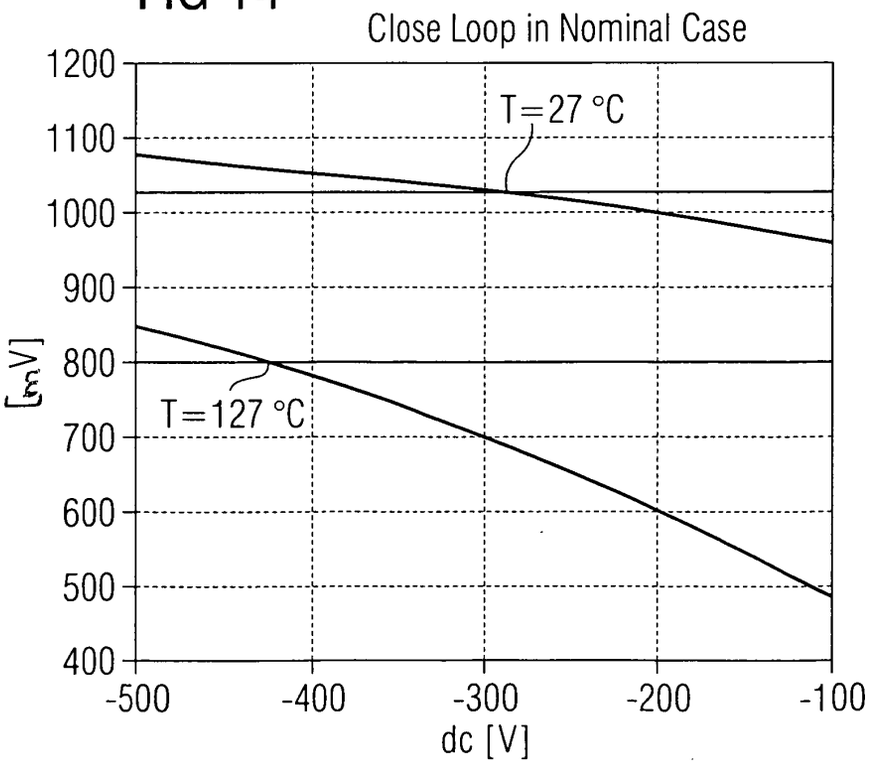

Close Loop in Nominal Case
1200
1100
1000
900
800
700
600
500
400
[mV]
T=27 °C
T=127 °C
-500
-400
-300
-200
-100
dc [V]

FIG 15

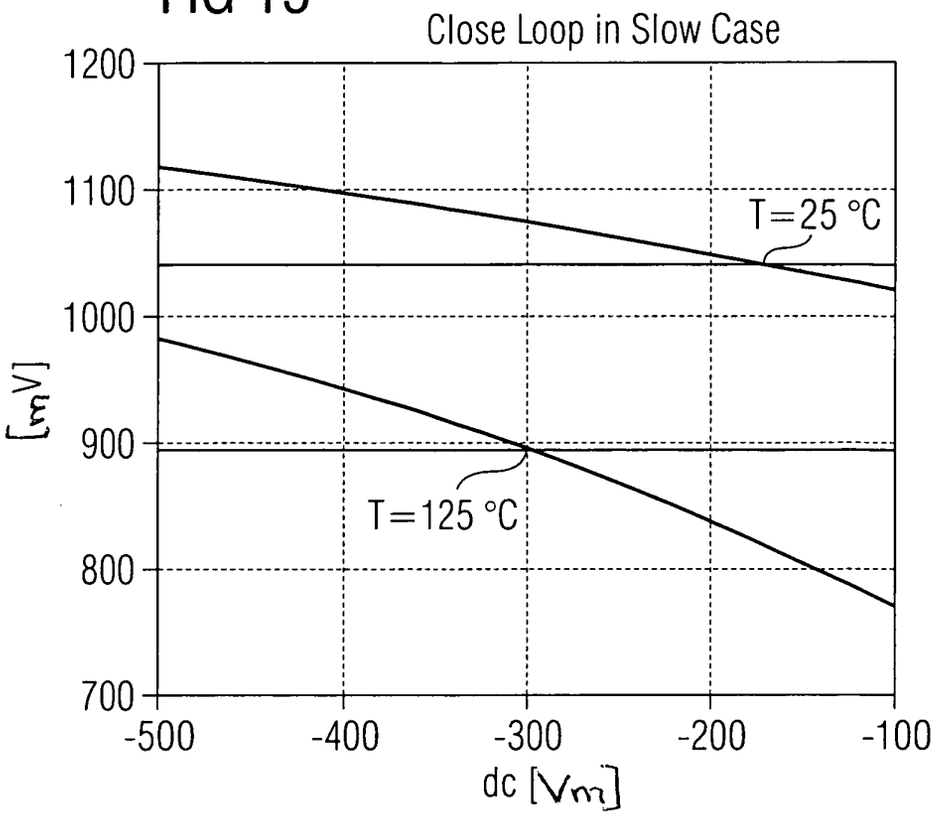

Close Loop in Slow Case
1200
1100
1000
900
800
700
[mV]
T=25 °C
T=125 °C
-500
-400
-300
-200
-100
dc [Vm]

FIG 16

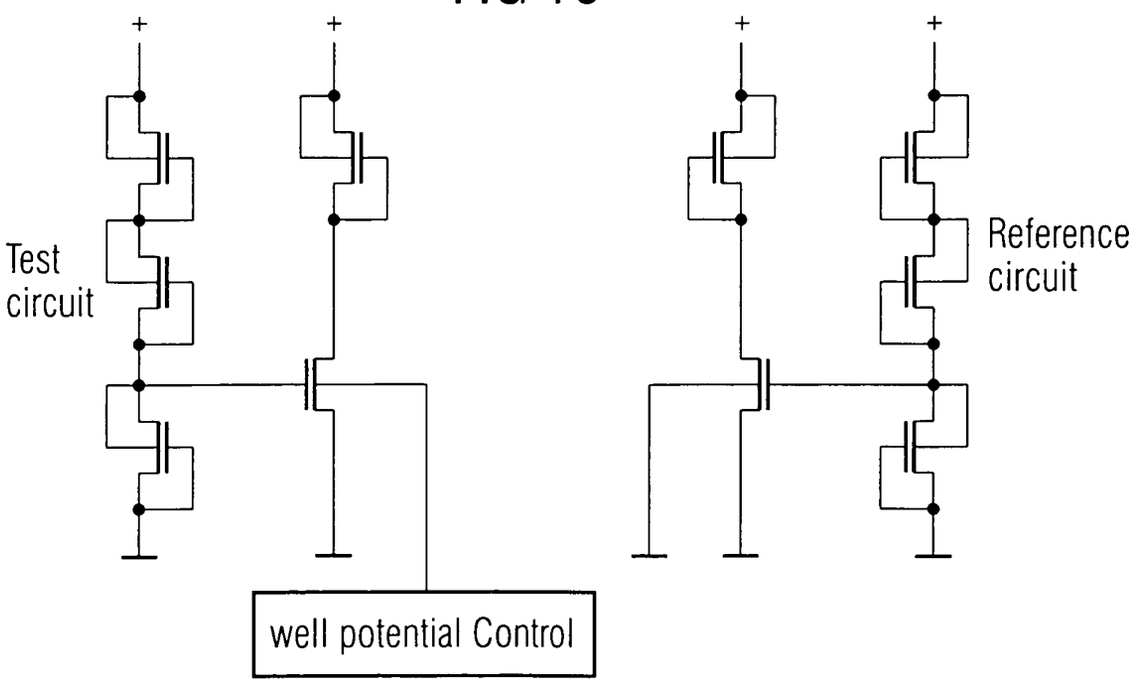

Test circuit
Reference circuit
well potential Control

FIG 17

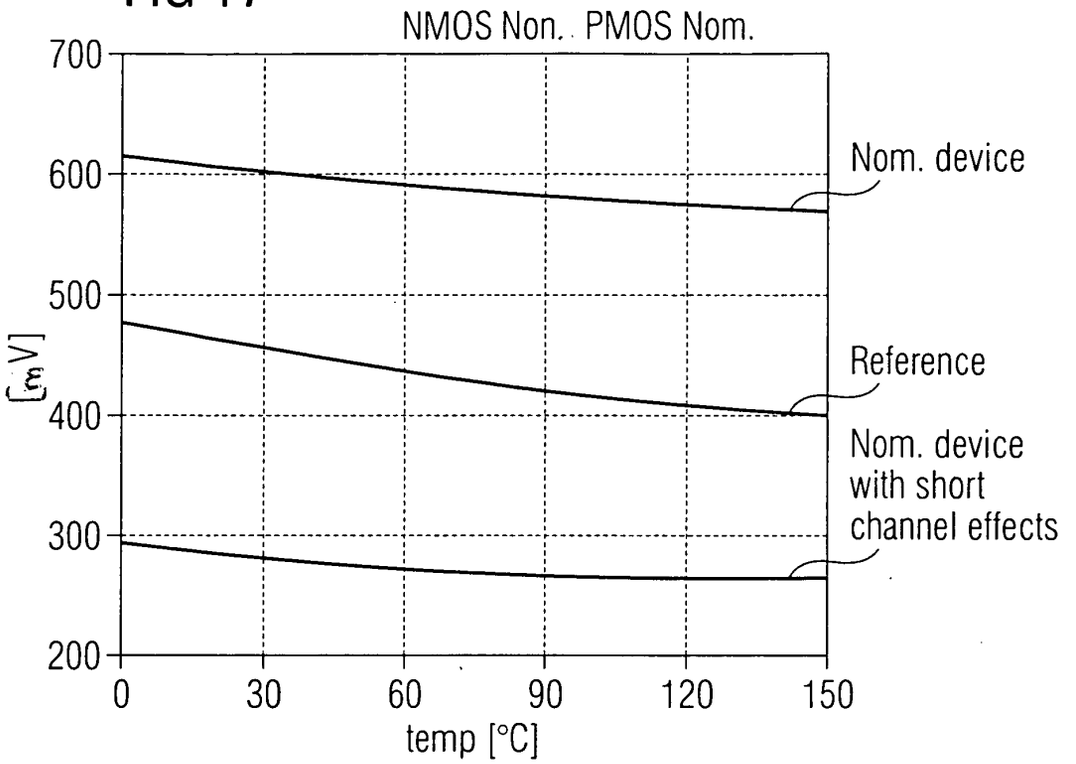

NMOS Non. PMOS Nom.
700
600
500
400
300
200
[mV]
0
30
60
90
120
150
temp [°C]
Nom. device
Reference
Nom. device with short channel effects

FIG 18

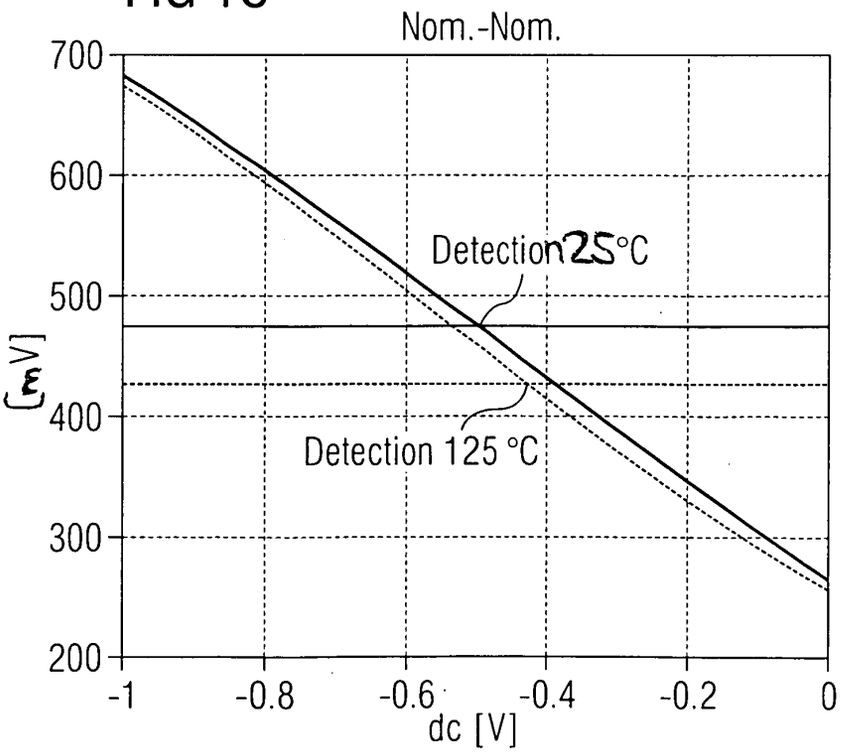

Nom.-Nom.
700
600
500
400
300
200
[mV]
-1
-0.8
-0.6
-0.4
-0.2
0
dc [V]
Detection 25°C
Detection 125 °C

FIG 19

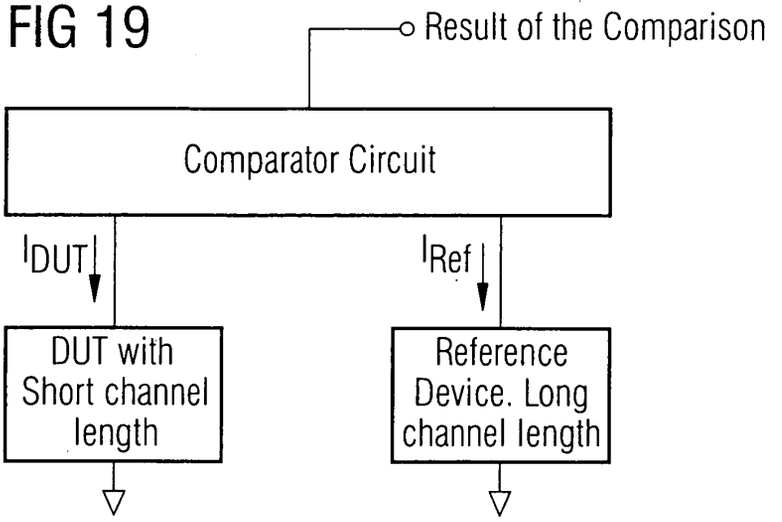


FIG 20

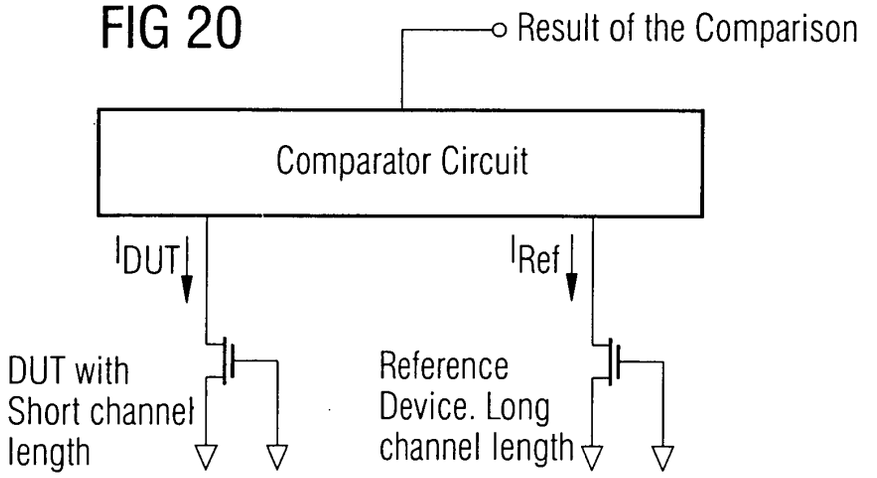


FIG 21

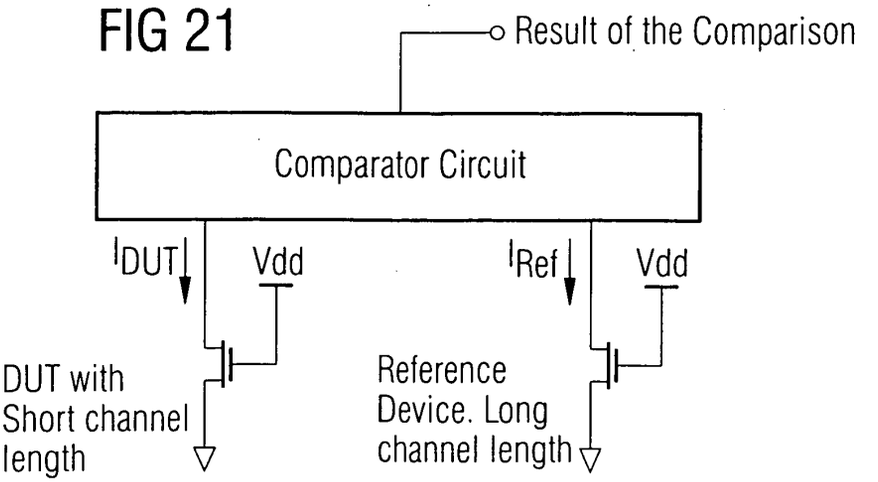


FIG 22

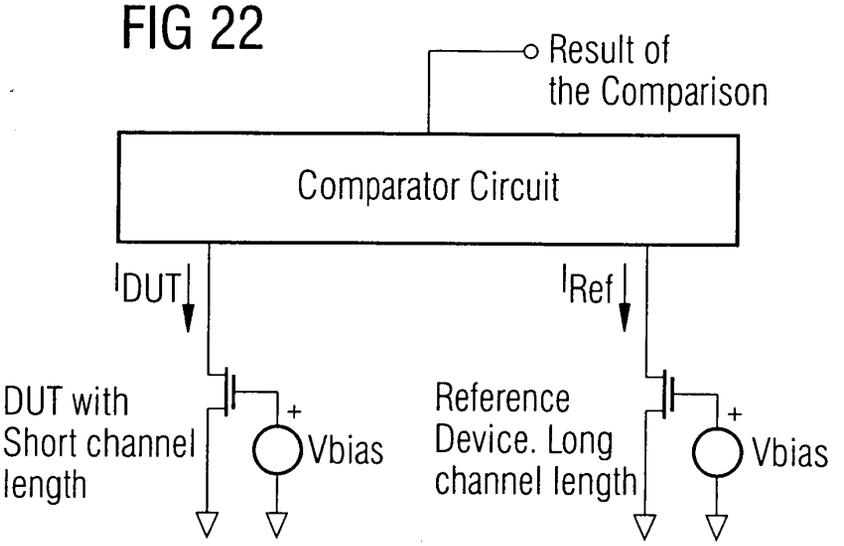
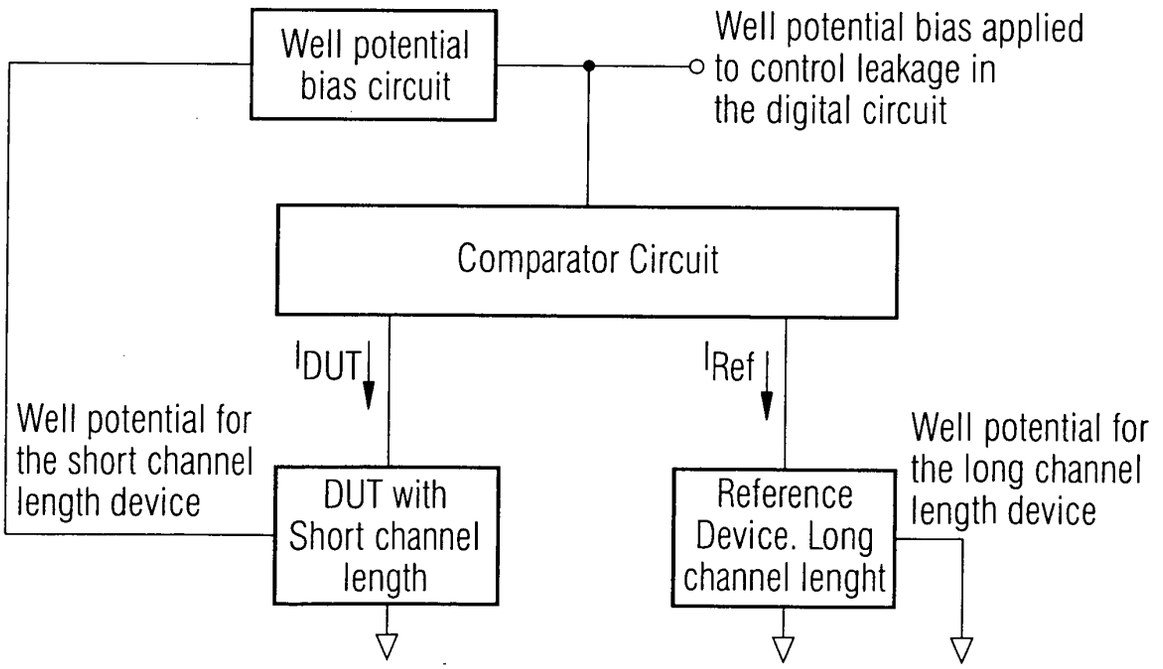

Result of
the Comparison
Comparator Circuit
IDUT
IRef
DUT with
Short channel
length
+
Vbias
Reference
Device. Long
channel length
+
Vbias

FIG 23


Well potential
bias circuit
Well potential bias applied
to control leakage in
the digital circuit
Comparator Circuit
IDUT
IRef
Well potential for
the short channel
length device
DUT with
Short channel
length
Reference
Device. Long
channel lenght
Well potential for
the long channel
length device

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 02 02 8136

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
X	US 4 346 344 A (BLAUSCHILD ROBERT A) 24 August 1982 (1982-08-24) * abstract * * column 1, line 45 - line 67 * * column 2, line 15 - column 4, line 10 * * figures 1-3 * * claims 1-4 * ---	1-16	G05F3/24 G05F3/20
X	US 4 789 825 A (CARELLI JOHN A ET AL) 6 December 1988 (1988-12-06) * abstract * * column 1, line 28 - line 48 * * column 1, line 67 - column 2, line 10 * * column 2, line 27 - line 63 * * column 3, line 1 - line 35 * * column 3, line 45 - line 51 * * column 5, line 6 - line 11 * * claims 1-7 * * figures 1,2 * ---	1-16	
X	US 4 305 011 A (AUDAIRE LUC ET AL) 8 December 1981 (1981-12-08) * abstract * * column 1, line 65 - column 2, line 26 * * column 3, line 39 - line 54 * * column 4, line 56 - column 6, line 59 * * column 8, line 6 - line 10 * * claims 1-9 * * figures 1-5 * ---	1-16	TECHNICAL FIELDS SEARCHED (Int.Cl.7) G05B G05F
A	US 4 716 307 A (AOYAMA KEIZO) 29 December 1987 (1987-12-29) * abstract * * column 3, line 13 - line 46 * * column 4, line 12 - column 5, line 2 * * figures 1-4 * --- -/--	1-16	

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
MUNICH	15 December 2003	Pöllmann, H.M.

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EUROPEAN SEARCH REPORT

Application Number
EP 02 02 8136

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
A	US 6 091 283 A (BURR JAMES B ET AL) 18 July 2000 (2000-07-18) * abstract * * the whole document * -----	1-16	
			TECHNICAL FIELDS SEARCHED (Int.Cl.7)

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
MUNICH	15 December 2003	Pöllmann, H.M.

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A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

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US 6091283 A	18-07-2000	NONE	

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