(54) **Ring oscillator with a digitally programmable frequency**

(57)   One embodiment of the present invention provides a ring oscillator with a digitally programmable frequency. This ring oscillator includes an odd number of inverting stages coupled input to output to form a ring, and a programming mechanism configured to digitally program the drive strength for each inverting stage in the ring oscillator, thereby changing the propagation delay between inverting stages and thereby allowing the frequency of the ring oscillator to be adjusted. The given inverting stage may include a plurality of tri-state inverters coupled in parallel, so that inputs of the tri-state inverters are coupled to a common input for the given inverting stage, and outputs of the tri-state inverters are coupled to a common output for the given inverting stage. Each of the tri-state inverters can be selectively enabled, thereby allowing the drive strength of the given inverting stage to be adjusted.
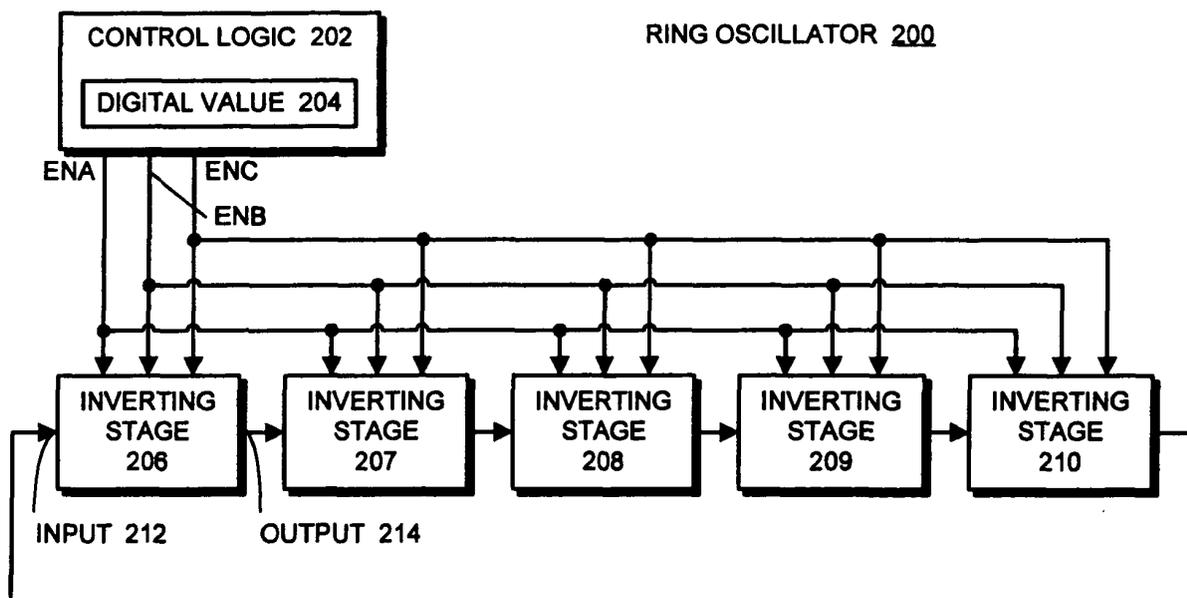
FIG. 2

EP 1 408 610 A1

Description

Field of the Invention

[0001] The present invention relates to digital circuits. More specifically, the present invention relates to a method and an apparatus for digitally programming a frequency for a ring oscillator.

Background of the Invention

[0002] Digital circuits typically operate under control of a system clock signal that is used to synchronize interactions between circuit elements. Because of the simplicity of its design, a ring oscillator is often used to generate such a clock signal.

[0003] A ring oscillator comprises an odd number of inverting stages connected into a ring. For example, referring to FIG. 1, ring oscillator 103 on semiconductor chip 102 includes five inverters 104-108 connected input-to-output to form a ring in which the output of the last inverter 108 feeds back into the input of the first inverter 104.

[0004] Assuming that each inverting stage is identical, this circuit produces a clock signal that oscillates with a period equal to twice the gate delay of each inverting stage multiplied by the number of inverting stages. For example, if each of the five inverters 104-108 in FIG. 1 has a one-nanosecond delay, ring oscillator 103 will oscillate with a period of 10 nanoseconds.

[0005] It is often useful to be able to dynamically change the clock frequency of a digital system. For example, the clock frequency can be decreased during latent periods of operation in order to decrease the power consumption of the digital circuit. Furthermore, it is often desirable to fine tune circuitry after fabrication to achieve a desired clock speed. Note that variations in the processes used to manufacture semiconductor chips often cause substantial variations in propagation delay through circuit elements. It is therefore not possible to determine how fast a digital circuit will operate before it is manufactured. Hence, it is typically necessary to fine tune a digital circuit after it is manufactured to achieve a desired frequency.

[0006] A number of ring oscillator designs allow the number of inverting stages in the ring oscillator to be adjusted through fuses or semiconductor switches. For example, see U.S. Patent No. 5,689,213, entitled "Post-Fabrication Programmable Integrated Circuit Ring Oscillator," by inventor Joseph C. Sher, filed on August 23, 1995 and issued on November 18, 1997. However, in these designs, inverting stages must be added or removed from the ring oscillator in pairs. This means that only coarse frequency adjustments are possible using this technique.

Summary of the Invention

[0007] Accordingly, one embodiment of the present invention provides a ring oscillator with a digitally programmable frequency. This ring oscillator includes an odd number of inverting stages coupled input to output to form a ring, and a programming mechanism configured to digitally program the drive strength for each inverting stage in the ring oscillator, thereby changing the propagation delay between inverting stages and thereby allowing the frequency of the ring oscillator to be adjusted.

[0008] In one embodiment, a given inverting stage includes a plurality of tri-state inverters coupled in parallel, so that the inputs of the tri-state inverters are coupled to a common input for the given inverting stage, and the outputs of the tri-state inverters are coupled to a common output for the given inverting stage. Moreover, each of the tri-state inverters can be selectively enabled, thereby allowing the drive strength of the given inverting stage to be adjusted.

[0009] In one particular embodiment, the tri-state inverters for the given inverting stage have equal drive strength, so that enabling additional tri-state inverters increases the drive strength of the given inverting stage linearly. Alternatively, the tri-state inverters for the given inverting stage may have different gate lengths and hence different drive strengths. For example, the tri-state inverters for the given inverting stage may have drive strengths that vary by powers of two, so that the drive strength of the given inverting stage can be digitally programmed with a binary number.

[0010] In one particular embodiment, a tri-state inverter in the given inverting stage includes: a first P-type transistor with a source coupled to V_{DD}, and a gate coupled to the input of the tri-state inverter; a second P-type transistor with a source coupled to the drain of the first P-type transistor, a gate coupled to an enable signal for the tri-state inverter and a drain coupled to the output of the tri-state inverter; a first N-type transistor with a drain coupled to the output of the tri-state inverter, and a gate coupled to the inverse of the enable signal; and a second N-type transistor with a drain coupled to the source of the first N-type transistor, a gate coupled to the input of the tri-state inverter and a source coupled to ground.

Brief Description of the Figures

[0011] Various embodiments of the invention will now be described in detail by way of example only with reference to the following drawings:

FIG. 1 illustrates a ring oscillator on a semiconductor chip.
FIG. 2 illustrates a ring oscillator with a programmable frequency in accordance with one embodiment of the present invention.
FIG. 3 illustrates an implementation of a stage in a

ring oscillator in accordance with one embodiment of the present invention.

FIG. 4 illustrates an alternative implementation of a stage in a ring oscillator in accordance with one embodiment of the present invention.

FIG. 5 illustrates yet another implementation of a stage in a ring oscillator in accordance with one embodiment of the present invention.

FIG. 6 is a flow chart of the process of configuring the frequency of a ring oscillator in accordance with one embodiment of the present invention.

Detailed Description

Programmable Ring Oscillator

[0012] FIG. 2 illustrates a ring oscillator 200 with a programmable frequency in accordance with one embodiment of the present invention. The ring oscillator 200 illustrated in FIG. 2 includes five inverting stages 206-210. However, in general any odd number of inverting stages can be used.

[0013] Ring oscillator 200 additionally includes control logic 202, which holds a digital value 204 corresponding to a frequency for ring oscillator 200. Control logic 202 uses digital value 204 to generate a set of enable signals, ENA, ENB and ENC, which feed into inverting stages 206-210. These enable signals ENA, ENB and ENC are used to selectively enable tri-state inverters that are coupled together in parallel within inverting stages 206-210. Note that FIG. 2 does not show complementary enable signals ENA_L, ENB_L and ENC_L that accompany enable signals ENA, ENB and ENC. Also note that control logic 202 can generally include any type of state machine, programmable Read-Only Memory (ROM), or other type of control mechanism that can be used to generate enable signals for inverting stages 206-210.

[0014] By selectively enabling tri-state drivers in inverting stages 206-210, control logic 202 is able to adjust the drive strength for each inverting stage in ring oscillator 200. This changes the propagation delay between inverting stages 206-210 and thereby allows the frequency of ring oscillator 200 to be adjusted. This adjustment process is described in more detail below with reference to FIGs. 3-6.

Inverting Stages

[0015] FIG. 3 illustrates an implementation of inverting stage 206 within ring oscillator 200 in accordance with one embodiment of the present invention. During operation, inverting stage 206 receives an input signal 212 and generates an inverted output signal 214 (see FIG. 2).

[0016] The implementation of inverting stage 206 in FIG. 3 includes three tri-state inverters connected in parallel. Note that in general inverting stage 206 can include

any number of tri-state inverters connected in parallel, and is not limited to the three parallel tri-state inverters illustrated in FIG. 3.

[0017] As is illustrated in FIG. 3, a first tri-state inverter 320 in inverting stage 206 includes P-type transistors 302 and 305 as well as N-type transistors 308 and 311, which are coupled in series between V_{DD} and ground. When enable signal ENA is asserted to a low voltage and complementary enable signal ENA_L is asserted to V_{DD}, P-type transistor 305 and N-type transistor 308 become transparent. This allows P-type transistor 302 and N-type transistor 311 to invert input signal 212 to produce output signal 214.

[0018] A second tri-state inverter 321 includes P-type transistors 303 and 306 as well as N-type transistors 309, and 312, which are coupled in series between V_{DD} and ground. Tri-state inverter 321 can similarly be enabled by asserting enable signal ENB to a low voltage and asserting complementary enable signal ENB_L to V_{DD}.

[0019] Finally, a third tri-state inverter 322 includes P-type transistors 304 and 307 as well as N-type transistors 310 and 313, which are coupled in series between V_{DD} and ground. Tri-state inverter 322 can also be enabled by asserting enable signal ENC to a low voltage and asserting complementary enable signal ENC_L to V_{DD}.

[0020] By selectively enabling different combinations of tri-state inverters 320, 321 and 322, different drive strengths can be generated by inverting stage 206. In one embodiment of the present invention, the drive strengths of inverters 320, 321 and 322 are all the same. In this case, enabling additional inverters increases the drive strength of inverting stage 206 linearly. Note the drive strength for a given tri-state inverter can be adjusted prior to manufacture by adjusting the gate widths of the transistors in the given tri-state inverter.

[0021] In another embodiment of the present invention, the drive strengths of inverters 320, 321 and 322 vary by successive by powers of two. For example, the drive strength of the second inverter 321 can be twice the drive strength of the first inverter 320, and the drive strength of the third inverter 322 can be twice the drive strength of the second inverter 321. In this way, a three digit binary value can be used to selectively enable different combinations of inverters 320, 321 and 322 to produce a corresponding drive strength that is proportional to the three digit binary value.

[0022] FIG. 4 illustrates an alternative implementation of inverting stage 206 in accordance with another embodiment of the present invention. This alternative implementation is the same as the implementation illustrated in FIG. 3, except that the drains of P-type transistors 302-304 have been coupled together at terminal 323, and the drains of N-type transistors 311-313 have been coupled together at terminal 324. In this embodiment, P-type transistors 302-303 and N-type transistors 311-313 always remain active.

[0023] Moreover, enable signals ENA, ENB and ENC determine the resistance between terminal 323 and output terminal 214, and enable signals ENA_L, ENB_L, and ENC_L determine the resistance between terminal 324 and output terminal 214. In this way, enable signals ENA, ENA_L, ENB, ENB_L, ENC, and ENC_L determine the drive strength of inverting stage 206.

[0024] FIG. 5 illustrates yet another implementation of inverting stage 206 in accordance with another embodiment of the present invention. This implementation is a variation on the embodiment illustrated in FIG. 4 in which the three parallel P-type transistors 302-304 are replaced be a single P-type transistor 325, and the three parallel N-type transistors 311-313 are replaced by a single N-type transistor 326. This embodiment operates in generally the same way as the embodiment illustrated in FIG. 4, wherein enable signals ENA, ENB, and ENC determine the resistance between terminal 323 and output 214, and enable signals ENA_L, ENB_L, and ENC_L determine the resistance between terminal 324 and output terminal 214. This allows enable signals ENA, ENA_L, ENB, ENB_L, ENC, and ENC_L to determine the drive strength of inverting stage 206.

[0025] Although the enable signals illustrated in FIGs. 3-5 are "active low," which means that they are asserted with a low voltage, the present invention is not limited to circuits with active low enable signals. Equivalent circuitry which makes use of "active high" enable signals can also be used.

Configuration Process

[0026] FIG. 6 is a flow chart of a process for configuring the frequency of a ring oscillator in accordance with one embodiment of the present invention. The process starts when control logic 202 produces a digital value 204 composed of a series of ones and zeros associated with a specific frequency for ring oscillator 200 (see FIG. 2) (step 602). This digital value 204 can be received from an external source, can be programmed, or can be generated internally by control logic 202.

[0027] Next, control logic 202 uses digital value 204 to program the drive strength for the inverting stages by asserting enable signals ENA, ENA_L, ENB, ENB_L, ENC and ENC_L (step 604). This can involve performing a function on digital value 204 to compute enable signals ENA, ENA_L, ENB, ENB_L, ENC and ENC_L. Ring oscillator 200 is then able to operate at the selected frequency (step 606).

[0028] Although the present invention has been described in the context of the implementations illustrated in FIGs. 2-6, the present invention is not meant to be limited to these specific implementations. For example, any suitable technique for varying the drive strength of inverting stages in a ring oscillator based on a digital input may be used.

[0029] The foregoing descriptions of embodiments of the present invention have been presented for purposes of illustration in order to enable a person skilled in the art to appreciate and implement the invention. They are provided in the context of particular applications and their requirements, but are not intended to be exhaustive or to limit the present invention to the forms disclosed. Accordingly, many modifications and variations will be apparent to practitioners skilled in the art, and the scope of the present invention is defined by the appended claims.

Claims

1. A ring oscillator with a digitally programmable frequency, comprising:

    an odd number of inverting stages coupled input to output to form a ring; and
    a programming mechanism configured to digitally program the drive strength for each inverting stage in the ring oscillator, thereby changing the propagation delay between inverting stages to allow the frequency of the ring oscillator to be adjusted.

2. The ring oscillator of claim 1, wherein a given inverting stage includes:

    a plurality of tri-state inverters coupled in parallel, so that the inputs of the tri-state inverters are coupled to a common input for the given inverting stage, and the outputs of the tri-state inverters are coupled to a common output for the given inverting stage;

    wherein each of the tri-state inverters can be selectively enabled, to allow the drive strength of the given inverting stage to be adjusted.

3. The ring oscillator of claim 2, wherein the tri-state inverters for the given inverting stage have equal drive strength, so that enabling additional tri-state inverters increases the drive strength of the given inverting stage linearly.

4. The ring oscillator of claim 2, wherein the tri-state inverters for the given inverting stage have different gate lengths and hence different drive strengths.

5. The ring oscillator of claim 4, wherein the tri-state inverters for the given inverting stage have drive strengths that vary by powers of two, so that the drive strength of the given inverting stage can be digitally programmed with a binary number.

6. The ring oscillator of any of claims 2 to 5, wherein a tri-state inverter in the given inverting stage includes:

a first P-type transistor with a source coupled to V_{DD}, and a gate coupled to the input of the tri-state inverter;

a second P-type transistor with a source coupled to the drain of the first P-type transistor, a gate coupled to an enable signal for the tri-state inverter and a drain coupled to the output of the tri-state inverter;

a first N-type transistor with a drain coupled to the output of the tri-state inverter, and a gate coupled to the inverse of the enable signal; and

a second N-type transistor with a drain coupled to the source of the first N-type transistor, a gate coupled to the input of the tri-state inverter and a source coupled to ground.

7. A method for digitally programming a frequency of a ring oscillator, wherein the ring oscillator includes an odd number of inverting stages coupled input to output to form a ring, comprising:

receiving a digital value associated with the frequency for the ring oscillator; and

using the digital value to program a drive strength for each inverting stage in the ring oscillator;

wherein programming the drive strength changes the propagation delay between inverting stages and thereby adjusts the frequency of the ring oscillator.

8. The method of claim 7, wherein a given inverting stage includes:

a plurality of tri-state inverters coupled in parallel, so that the inputs of the tri-state inverters are coupled to a common input for the given inverting stage, and the outputs of the tri-state inverters are coupled to a common output for the given inverting stage;

wherein each of the tri-state inverters can be selectively enabled, thereby allowing the drive strength of the given inverting stage to be adjusted.

9. The method of claim 8, wherein the tri-state inverters for the given inverting stage have equal drive strength, so that enabling additional tri-state inverters increases the drive strength of the given inverting stage linearly.

10. The method of claim 8, wherein the tri-state inverters for the given inverting stage have different gate lengths and hence different drive strengths.

11. The method of claim 10, wherein the tri-state inverters for the given inverting stage have drive strengths that vary by powers of two, so that the drive strength of the given inverting stage can be digitally programmed with a binary number.

12. The method of any of claims 8 to 11, wherein a tri-state inverter in the given inverting stage includes:

a first P-type transistor with a source coupled to V_{DD}, and a gate coupled to the input of the tri-state inverter;

a second P-type transistor with a source coupled to the drain of the first P-type transistor, a gate coupled to an enable signal for the tri-state inverter and a drain coupled to the output of the tri-state inverter;

a first N-type transistor with a drain coupled to the output of the tri-state inverter, and a gate coupled to the inverse of the enable signal; and

a second N-type transistor with a drain coupled to the source of the first N-type transistor, a gate coupled to the input of the tri-state inverter and a source coupled to ground.

13. A semiconductor chip comprising:

a semiconductor substrate;

a ring oscillator on the semiconductor substrate according to any of claims 1 to 6.

14. The semiconductor chip of claim 13, wherein the semiconductor chip includes a central processing unit.

15. A computer system comprising:

a processor;
a memory;
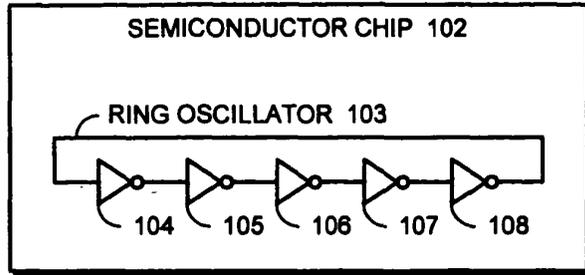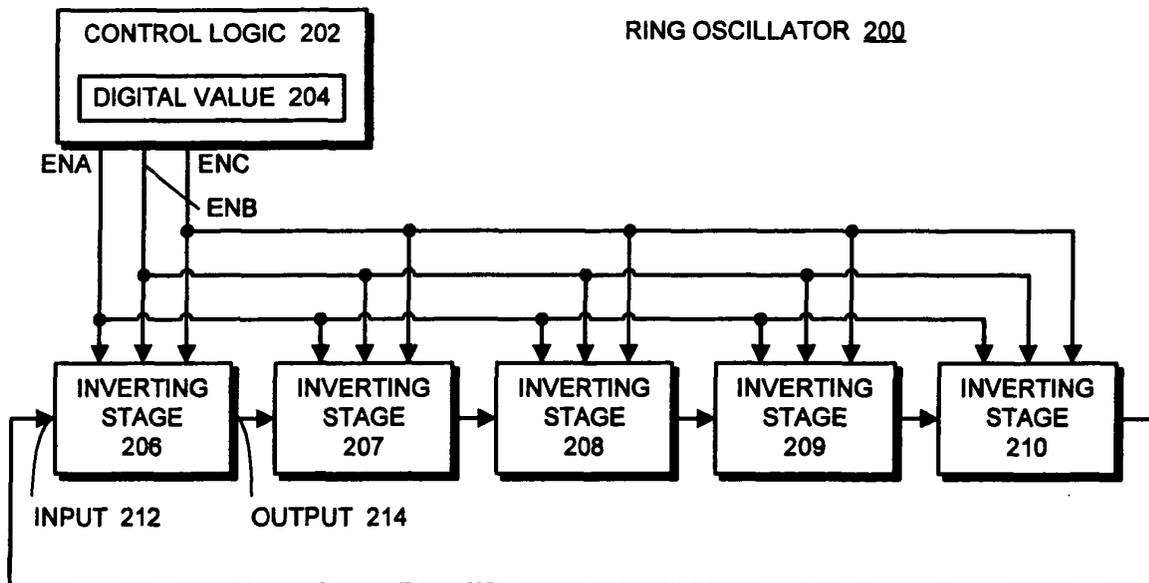a ring oscillator according to any of claims 1 to 6.

SEMICONDUCTOR CHIP 102
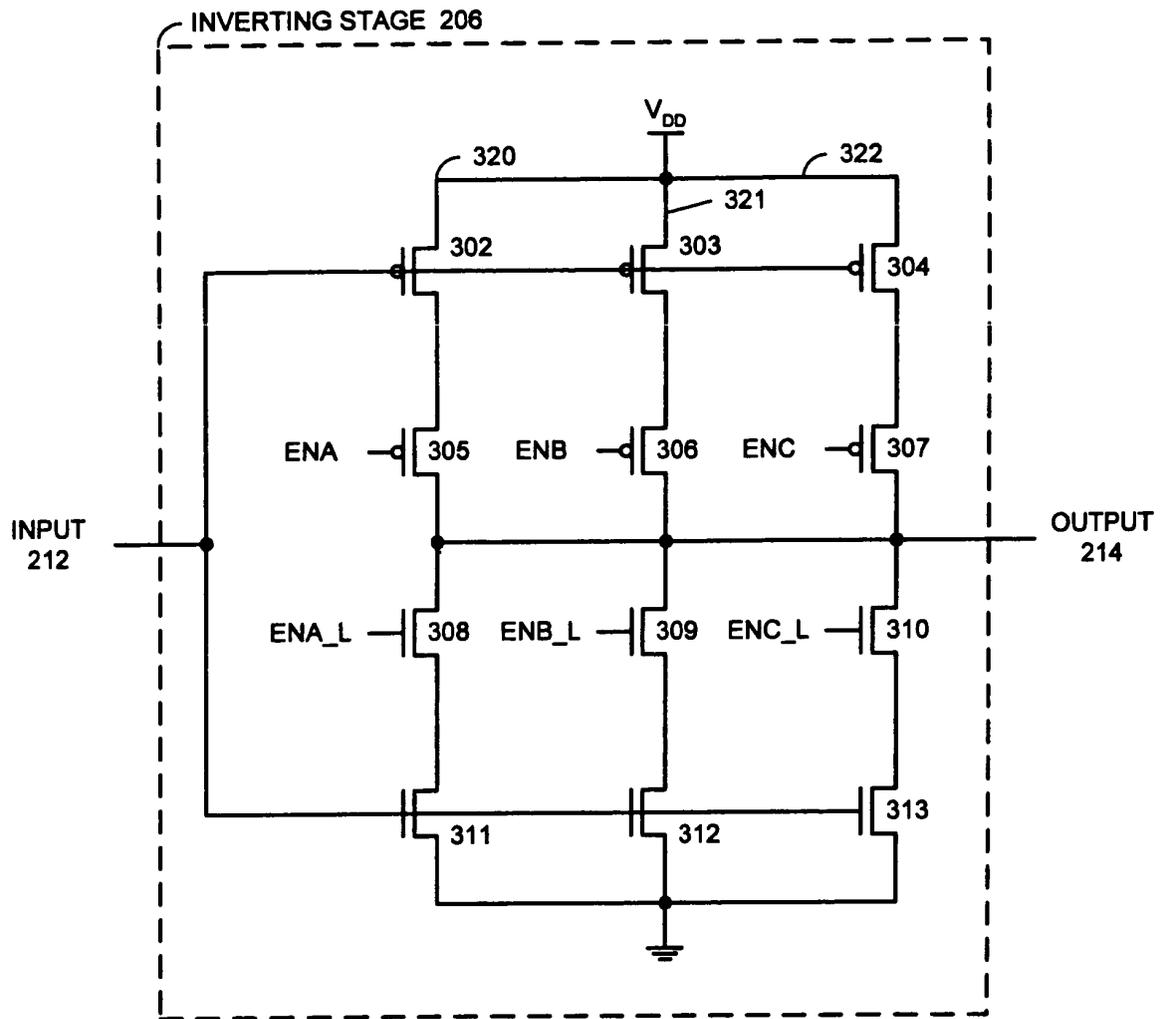
RING OSCILLATOR 103

104 105 106 107 108

FIG. 1
(PRIOR ART)

CONTROL LOGIC 202

DIGITAL VALUE 204

RING OSCILLATOR 200

ENA ENC

ENB

INVERTING STAGE 206

INVERTING STAGE 207

INVERTING STAGE 208

INVERTING STAGE 209

INVERTING STAGE 210

INPUT 212 OUTPUT 214

FIG. 2

FIG. 3

FIG. 4

FIG. 5

START

RECEIVE DIGITAL VALUE
602

USE DIGITAL VALUE TO PROGRAM
THE DRIVE STRENGTH FOR EACH
INVERTING STAGE
604

OPERATE RING OSCILLATOR
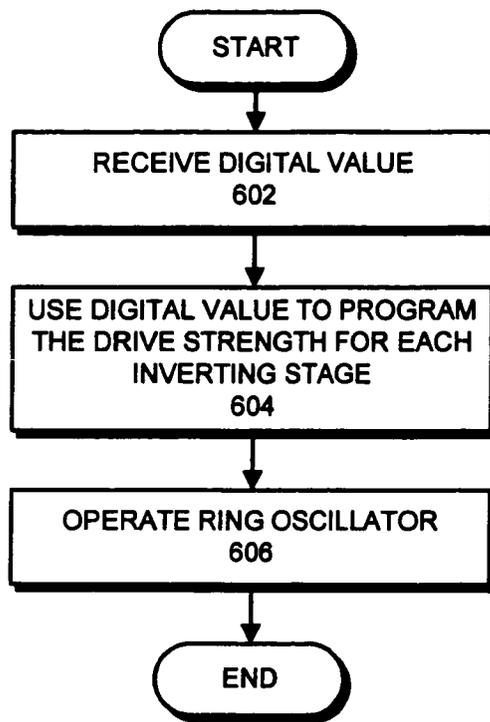606

END
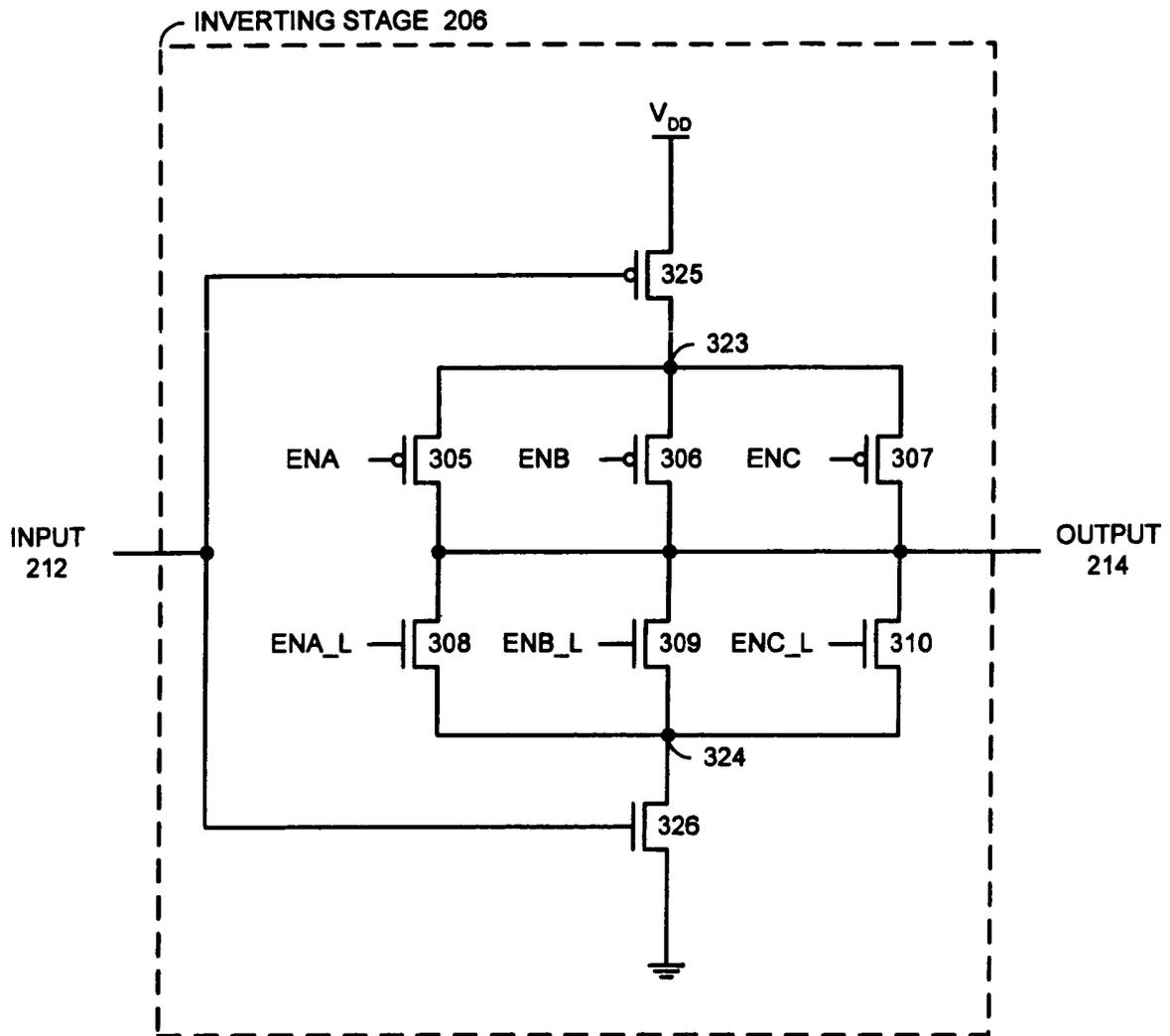
FIG. 6

European Patent Office

EUROPEAN SEARCH REPORT

Application Number

EP 03 25 5857

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
X	US 6 204 694 B1 (ROY AUBIN P J ET AL) 20 March 2001 (2001-03-20) * figure 8 *	1-15	H03K3/03 H03K23/54
X	US 6 272 439 B1 (BUER MARK L ET AL) 7 August 2001 (2001-08-07) * figure 4 *	1	

TECHNICAL FIELDS SEARCHED (Int.Cl.7)

H03K

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
MUNICH	30 December 2003	Brown, J

EPO FORM 1503 03.82 (P04C01)

ANNEX TO THE EUROPEAN SEARCH REPORT
ON EUROPEAN PATENT APPLICATION NO.

EP 03 25 5857

This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report.
The members are as contained in the European Patent Office EDP file on
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30-12-2003

Patent document cited in search report		Publication date	Patent family member(s)	Publication date
US 6204694	B1	20-03-2001	NONE	
US 6272439	B1	07-08-2001	NONE	

For more details about this annex : see Official Journal of the European Patent Office, No. 12/82