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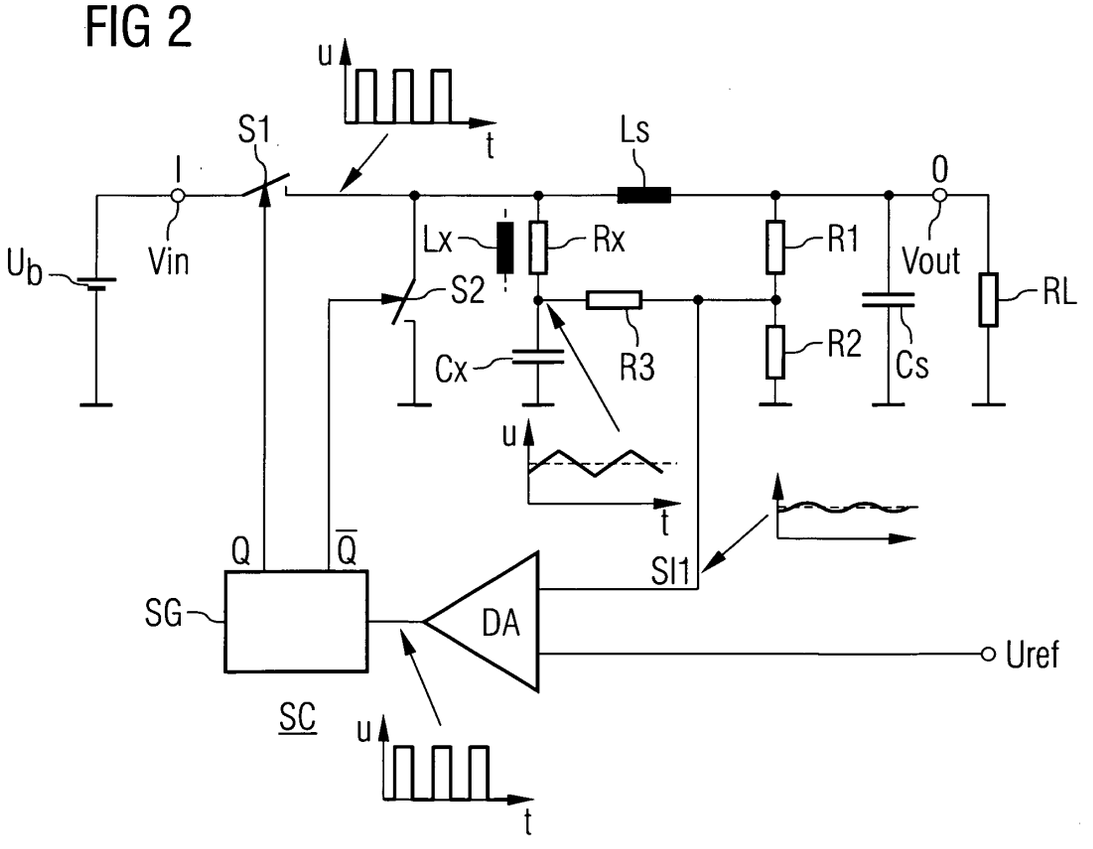
(54) Buck converter

(57) Buck converter for generating a regulated DC output voltage (Vout) from an unregulated DC input voltage (Vin) comprising:

- switch means (S1) for switching said unregulated DC input voltage (Vin) to provide a pulse train;
- output filtering means (Ls,Cs) for low pass filtering of said pulse train;
- a regenerative loop providing regenerative feed back of said pulse train through a switching control circuit (SC) to a switching control input of said switch means (S1).

To obtain ripple reduction in the output signal of the buck converter in accordance with the invention in particular when using low ESR ceramic output capacitors, said regenerative loop includes a loop filter circuit (Lx, Cx or Rx, Cx) coupled between an output of said switch means (S1) and said switching control circuit (SC) and provides a loop time constant substantially smaller than the time constant of said output filtering means (Ls, Cs).

FIG 2



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Description

[0001] The invention relates to a buck converter for generating a regulated DC output voltage from an unregulated DC input voltage comprising:

- input means for receiving said unregulated DC input voltage;
- output means for providing said regulated DC output voltage to a load;
- first switch means following said input means for switching said unregulated DC input voltage to provide a pulse train;
- output filtering means coupled between said first switch means and said output means for low pass filtering of said pulse train;
- a regenerative loop providing regenerative signal feed back at the repetition frequency of said pulse train through a switching control circuit to a switching control input of said first switch means.

[0002] Such buck converter is on itself known, e.g. from published PCT application WO 02/052707.

[0003] A simplified circuit diagram of such known converter showing its basic functions, is given in Figure 1. This conventional type of buck converter receives an unregulated DC input voltage Vin from an input voltage source Ub through input means I. The unregulated DC input voltage Vin is chopped into a pulse train in a serially connected first switch means S1 being controlled in its switching actions by a switching control signal supplied to its switching control input. The pulse train is being supplied from an output of the first switch means S1 to output filtering means. The output filtering means is to low pass filter or integrate said pulse train, i.e. to suppress the higher order harmonics thereof, in order to obtain a more or less sinusoidal varying voltage, which is supplied as regulated DC output voltage Vout through output means O to the load R1. The output filtering means therefore comprises a first serial LC circuit LsCs, an inductance Ls thereof receiving said pulse train from said first switch means S1 and being serially coupled between the output of said first switch means S1 and a mass connected capacitance Cs, the inductance Ls and the capacitance Cs at their common junction being coupled to said output means O. To obtain inductor current when S1 is in OFF state, in which the inductance Ls is disconnected from the unregulated DC input voltage Vin, the cathode of a freewheeling diode D is connected at the common junction between S1 and Ls, the anode thereof being massconnected. The buck converter is provided with a regenerative loop securing regenerative signal feed back. In the prior art example of Figure 1, the regenerative loop includes a switching control circuit SC controlling the switching actions of the first switch means S1 and deriving from the DC output voltage Vout the switching control signal such, that a stable overall oscillation condition for the pulse train is obtained, i.e. unity loop gain and 360 degrees phase shift at the pulse train repetition frequency.

[0004] However, the steady state DC output voltage Vout of this conventional type of buck converter S1 is severely affected by an unwanted ripple or AC component, which in despite of the output filtering means LsCs may be higher than desirable. In particular when using a ceramic output capacitor with very low to nearly zero ESR for the capacitance Cs, the amplitude of the AC output voltage component grossly exceeds the AC tolerance input voltage range of the load R1, making the conventional buck converter unsuitable for commercial use. The conventional buck converter will be of no practical use with ceramic capacitors, or more in general capacitors with an ESR of about 0 ohm in the output filtering means Ls, Cs, as such capacitors give rise to steep phase jumps, causing the circuit to oscillate at or near the resonance frequency of said output filtering means.

[0005] In consequence, amongst other things, it is an object of the present invention to strongly reduce the AC component or ripple in the output voltage of a buck converter while using output capacitor types with ESR about 0 Ohms, without unwanted oscillation at the output O.

[0006] Now therefore, according to one of its aspects the invention is characterised by said regenerative loop including a loop filter circuit coupled between an output of said first switch means and said switching control circuit and providing a loop time constant substantially smaller than the time constant of said output filtering means.

[0007] The invention is based on the recognition that the suppression of the AC component which remains after lowpass filtering of the pulse train in the output filtering means Ls, Cs increases with the frequency difference between the pulse train repetition frequency on the one hand and the resonance frequency of the output filtering means LsCs on the other hand.

[0008] The measure according to the invention allows to separate the pulse train repetition frequency from the resonance frequency of the output filtering means. According to the invention, the regenerative loop is set to oscillate at a higher frequency than the resonance frequency of the output filtering means LsCs. This causes the on-time of S1, i.e. the state, in which the inductance Ls is connected to the unregulated DC input voltage Vin, to be smaller with respect to the integration time constant of the output filtering means LsCs than with the above conventional buck converter. Consequently, the time intervals within each pulse signal period during which the capacitor Cs of the output filtering means LsCs defining the output voltage Vout, is being charged or discharged are smaller, therewith causing the ripple to be smaller as well.

[0009] A preferred embodiment of the invention allowing easy and cost-effective implementation is characterised by said output filtering means comprising a first serial LC circuit receiving said pulse train from said switch means, an inductance thereof being serially coupled be-

tween the output of said first switch means and a mass connected capacitance, the inductance and the capacitance at their common junction being coupled to said output means, said loop filter circuit comprising a frequency dependent phase shifting network coupled on the one hand at the output of said first switch means and on the other hand at an input of said switching control circuit.

[0010] To adjust DC output voltage independent from the reference voltage Vref, said frequency dependent phase shifting network is provided with an output being coupled through a resistor to a tap of a resistive voltage divider being connected in shunt across the capacitance of the first serial LC circuit.

[0011] According to another aspect of the invention, said frequency dependent phase shifting includes a serial RC circuit comprising subsequently coupled between the output of said first switch means and mass a serial arrangement of a resistor and a capacitor, said resistor and said capacitor at their common junction being coupled to the output of said frequency dependent phase shifting network.

[0012] Alternatively, said frequency dependent phase shifting network may include a serial LC circuit comprising subsequently coupled between the output of said first switch means and mass a serial arrangement of an inductor and a capacitor, said inductor and said capacitor being coupled at their common junction to the output of said frequency dependent phase shifting network.

[0013] A preferred embodiment of a buck converter according to invention providing accurate DC level adjustment and/or control of the DC output voltage through pulse width modulation is characterised by the switching control circuit comprising a differential amplifier having a differential input with first and second input terminals being respectively coupled to an output of said loop filter circuit and a DC level control input of the buck converter, an output of said differential amplifier being coupled to the switching control input of said first switch means.

[0014] A preferred embodiment of a buck converter according to invention minimising energy loss in particular by decreasing therewith enabling to further improve converter efficiency is characterized by a synchronous rectifier comprising second switch means for a synchronous rectification of said pulse train and being controlled to switch in a phase mode, which is substantially inversed to the switching phase mode of the first switch means.

[0015] A preferred embodiment of a buck converter according to invention minimising energy loss therewith enabling to further improve converter efficiency is characterised by a synchronous rectifier comprising second switch means for a synchronous rectification of said pulse train and being controlled to switch in a phase mode, which is substantially inversed to the switching phase mode of the first switch means.

[0016] To guarantee mutually coinciding conduction of the first and second switch means, a preferred embodiment of a buck converter according to the invention is characterised by said first and second switch means being controlled to switch alternately in mutually phase opposition from a conducting state into a non-conducting state via dead zone periods in which both said first and second switch means are in a non-conducting state.

[0017] To simplify the control of both first and second switch means said differential amplifier is being followed by a differential output stage providing a pair of phase opposite first and second output signals, said first and second output signals being respectively supplied to the switching control input of said first switch means and a switching control input of said second switch means.

[0018] To speed up the switching action a buck converter according to the invention is preferably characterised by a driver circuit coupled to a gate electrode of said MOSFET having an output resistance at most in the order of magnitude of ten Ohm.

[0019] To introduce a softstart to the regulation loop the invention is preferably characterised by an integrating RC circuit included between the level control input of the buck converter on the one hand and the second input terminal of the differential amplifier on the other hand.

[0020] These and further aspects and advantages of the invention will be discussed more in detail hereinafter with reference to the disclosure of preferred embodiments, and in particular with reference to the appended Figures in which like reference numerals designate the same elements, that show:

- Figure 1, a basic configuration of a prior art buck converter;
- Figure 2, a basic configuration of a first embodiment of a buck converter according to the invention comprising a synchronous rectifier;
- Figure 3, a circuit diagram of a second embodiment of a buck converter according to the invention, using a freewheeling diode.
- Figure 4, a circuit diagram of said first embodiment of a buck converter according to the invention, using an additional synchronous rectifier.

[0021] Figure 2 shows a basic configuration of a first embodiment of a buck converter according to the invention using a synchronous rectifier and comprising a resistive voltage divider (R1, R2) being connected in shunt across the capacitance Cs of the first serial LC circuit (Ls, Cs) and including a serial arrangement of resistors R1 and R2 being coupled through a tap at their common junction to the first input SC1 of the switching control circuit SC. The regenerative loop of the buck converter is provided with a loop filter circuit, the propagation delay thereof defining together with the propagation delay of all other circuitry and/or elements in the loop, such as the switching control circuit SC following upon the loop filter circuit, the loop oscillation conditions i.e. the fre-

quency of the signal within the loop at unity gain and 360 degrees phase shift or loop oscillation frequency.

[0022] The loop filter circuit comprises a frequency dependent phase shifting network (Rx, Cx or Lx, Cx) coupled on the one hand at the output of said first switch means S1 and on the other hand via a resistor R3 to the first input SI1 of the switching control circuit SC. This results in a mutual addition of the output signals of the frequency dependent phase shifting network (Rx, Cx or Lx, Cx) and the resistive voltage divider (R1, R2) at said first input SC1 of the switching control circuit SC. The switching control circuit SC comprises a differential amplifier DA having a differential input with first and second input terminals, the output of said differential amplifier DA being followed by a logic circuit SG functioning as switching signal generator SG and deriving a pair of phase opposite first and second output signals Q and Q' from the output signal of the differential amplifier DA, being supplied as switching control signals to respectively, the switching control input of said first switch means S1 and a switching control input of a second switch means S2.

[0023] The first input terminal of the differential amplifier DA constitutes the abovementioned first input SI1 of the switching control circuit SC, the second input terminal thereof constitutes a DC level control input of the buck converter for applying thereto a variable voltage reference level Vref. The differential amplifier DA provides an output signal varying with the mutual difference of the signals at its first and second input terminals. The differential amplifier DA therewith functions as a comparator for comparing the summation of the output signals of the frequency dependent phase shifting network (Rx, Cx or Lx, Cx) and the resistive voltage divider (R1, R2) at said first input SC1 of the switching control circuit SC, which varies with the more or less sinusoidally varying output voltage Vout, with said variable voltage reference level Vref. This allows to vary the open (ON) versus closed (OFF) state periods of the first switch means S1 and therewith to vary or modulate the pulse width or duty cycle of the pulse train at the output of the first switch means S1. The greater pulse width, the longer duty cycle and the higher the DC level of the output voltage Vout at the output means O. The steady state DC output voltage Vout is therefore directly dependent upon the input voltage Vin at the input means I and the duty cycle of the pulse train. By varying the signal at the DC level control input, the switching phase of the first switching means S1 is controlled by the regenerative loop and along therewith the pulse width or duty cycle of the pulse train at the output of the first switch means S1, allowing to control the DC level of the output voltage Vout at the output means O.

[0024] The voltage dividing factor of the voltage divider (R1, R2) versus the gain and phase performance of the circuitry in the loop at the output of the loop filter, is dimensioned such that the AC amplitude of the signal supplied to said first input SI1 of the switching control circuit SC from the frequency dependent phase shifting network (Rx, Cx or Lx, Cx) through the resistor R3 is substantially larger than the AC amplitude of the buck converters output divided by the resistive voltage divider (R1, R2). The AC voltage at the node between Rx and Cx has to be very much higher than at the node between R1 and R2. In a practical embodiment of a buck converter according to the invention, typical values at SI1 are respectively between 200mV and 50mV. The frequency dependent phase shifting network (Rx, Cx or Lx, Cx) therewith dominates the loop oscillation conditions.

[0025] The frequency dependent phase shifting network (Rx, Cx or Lx, Cx) is formed by a serial arrangement of either a resistor Rx and a capacitor Cx or alternatively an inductor Lx and a capacitor Cx subsequently coupled between an output of the first switch means S1 and mass. The output of the frequency dependent phase shifting network (Rx, Cx or Lx, Cx) is being constituted by the common junction of said resistor Rx and said capacitor Cx or alternatively said inductor Lx and said capacitor Cx. The alternative modes has been illustrated in this Figure 2 by the representation of the inductor Lx next to the capacitor Cx to indicate the possibility to use either a single pole (Rx, Cx) or a dual pole (Lx, Cx) network as loop filter.

[0026] According to the invention the single pole (Rx, Cx), respectively dual pole (Lx, Cx) network, provides a time constant $\tau l1 = Rx*Cx$, respectively $\tau l2 = \sqrt{(Lx*Cx)}$, which is dominantly effective in the regenerative loop and which is chosen substantially smaller than the time constant $\tau o = \sqrt{(Ls*Cs)}$ of the first serial LC circuit (Ls, Rs) of the output filtering means. As a result thereof, the loop oscillates at a much higher frequency than the resonance frequency of the first serial LC circuit (Ls, Rs) of the output filtering means, giving rise to a likewise much higher repetition frequency of the pulse train at the output of the first switch means S1. Along therewith the charge up and charge down intervals within each period of this pulse train during which the voltage across the capacitor Cs of the first serial LC circuit (Ls, Rs) increases, respectively decreases, are much shorter than in the conventional buck converter of Figure 1, whereas the integration time constant of the first serial LC circuit (Ls, Rs) of the output filtering means, which defines the slope of voltage variation across said capacitor Cs, may be the same as in the conventional buck converter. Consequently the ripple or AC component of the DC output voltage Vout is much smaller than in the conventional buck converter when using a low or zero ESR output capacitor for the output capacitance Cs. In a practical embodiment of a buck converter according to the invention, the ripple can be reduced to better than +/- 5%. This allows to use widely available low tolerance loads for the load resistor Rl.

[0027] The influence of line and load changes on the DC output voltage Vout is minimised by chosing the impedance of the voltage divider (R1, R2) very low with respect to the impedance of the frequency dependent

phase shifting network (Rx, Cx or Lx, Cx) and the resistor R3. The voltage at the output of the frequency dependent phase shifting network (Rx, Cx or Lx, Cx) has been chosen relatively high. To obtain a high filter quality factor Q for the frequency dependent phase shifting network (Lx, Cx) and loop oscillation conditions exactly at the resonance frequency thereof, the inductors Ls internal serial resistor of the first serial LC circuit (Ls, Rs) has been chosen as small as possible. The loop oscillation frequency, which defines the switching frequency of the first and second switch means S1 and S2, depends on the gain and phase shift of the frequency dependent phase shifting network (Rx, Cx or Lx, Cx) and those occurring in all other circuitry included in the regenerative loop, such as the switching control circuit SC as will be described in more detail hereinafter. In general, the oscillation frequency increases at a reduction of such delay and vice versa.

[0028] The synchronously rectifying type buck converter of Figure 2 provides a relatively high efficiency compared with the above conventional buck converter with freewheeling diode of Figure 1.

[0029] The buck converter comprises a synchronous rectifier formed by second switch means S2 coupled between the output of the first switch means S1 providing synchronous rectification of the output signal of said first switch means S1 by a periodically intermittent mass connection thereof. For this purpose, said second switch means S2 is being controlled to switch in a phase mode, which is substantially inverted to the switching phase mode of the first switch means S1 thereof. The use of such synchronous rectifier strongly prevents the oscillation frequency of the regenerative loop and therewith the pulse repetition frequency at the output of the first switch means from being affected by line and load variations, in particular when the buck converter is to provide only relatively small current values to the load Rl. The use of a synchronous rectifier avoids the occurrence of a burst mode, even at small load values, because inductor current of the inductance Ls is always continuous, i.e. not interrupted.

[0030] The use of a differential output stage in the logic circuit of the switching control circuit SC secures accurate switching control of both first and second switch means S1 and S2, in that a pair of phase opposite first and second output signals are being provided, said first and second output signals being respectively supplied to the switching control input of said first switch means S1 and a switching control input of said second switch means S2. Said first and second switch means S1 and S2 are therewith being controlled to switch alternately in mutually phase opposition from a conducting state into a non-conducting state. This results in a decreasing power dissipation of the 'freewheeling' diode D1 to nearly zero. The freewheeling diode can be an additional external diode or the synchronous rectifier MosFet internal body diode.

[0031] According to an aspect of the invention the conversion efficiency of the buck converter is increased in that the first and second switch means S1 and S2 are being controlled to switch alternately in mutually phase opposition via dead zone periods in which both said first and second switch means are in a non-conducting state.

[0032] Figure 3 shows a circuit diagram of a second embodiment of a buck converter according to the invention deviating from the buck converter of Figure 2 in that it uses a freewheeling diode. The buck converter receives through its input means I a DC input voltage Vin from a DC voltage source, which is supplied to the first switch means S1, which in the embodiment shown is constituted by a P-Channel enhancement type MOSFET M1, having its drain-source signal path serially included within a signal path of the buck converter. The gate electrode of the P-Channel enhancement type MOSFET M1, hereinafter also being referred to as MOSFET M1 switch, constitutes the switching control input of the first switch means S1 and receives a gate-source input control voltage or current to switch over from a non-conducting or open state, in which the source and drain of the MOSFET M1 are mutually disconnected, into a conducting or closed state in which the source and drain of the MOSFET M1 are mutually more or less short-circuited, or vice versa. The source being coupled at the input means I, the drain forming the output of the first switch means S1 supplying the pulse train. The MOSFET M1 switch is open, if the gain source voltage Ugs =0 V and it is closed when Ugs>4,5V (< 10V), i.e. when the switching control signal voltage at its gate is low. The drain is connected to a so-called freewheeling diode D1 permitting current conduction through the inductor Ls when the MOSFET M1 switch is turned-off so that the diode D1 receives the current generated by the collapse of the magnetic field of the inductor Ls.

[0033] The serial LC circuit LsCs constitutes the output filtering means of the buck converter, having its common junction coupled through the output means O to the load resistor Rl. The frequency dependent phase shifting network (Rx, Cx) of the regenerative loop is formed by a serial arrangement of resistor Rx and capacitor Cx having its common junction coupled through resistor R3 to the first input terminal of a differential input of the switching control circuit SC. A part of the output voltage Vout defined by the voltage divider (R1, R2) is supplied to said first input terminal of the differential input of the switching control circuit SC as well. The signal at said first input terminal is predominantly defined by the frequency dependent phase shifting network (Rx, Cx) and therewith also the oscillation frequency of the regenerative loop. According to the invention, also here the time constant of the frequency dependent phase shifting network (Rx, Cx) is chosen much smaller than the time constant of the output filtering means LsCs, resulting in the pulse repetition frequency being much higher than the resonance frequency of said output filtering means LsCs and therewith obtaining a much smaller ripple in the

DC output voltage than occurring in the above conventional buck converter.

[0034] Furthermore the regenerative loop automatically adapts the pulse duty cycle to the output current value supplied to the load impedance R1. In particular for low output currents (< ca. 0.1A), a very high efficiency is obtained in that for such low current values, the loop oscillation automatically changes from a normal to a burst mode, in which very short multiple switching pulses and very large pauses are generated, greater than 1:100. The burst mode automatically occurs depending on the input voltage Vin and output load current, without the need for additional circuitry to detect and to switch between said normal and burst mode. Due to this automatic change to said burst mode at light load charges, the dynamic output voltage tolerance can be typically better than 0,1Vpp, and mainly depends on the feedback resistor R3 of Figure 3.

[0035] The switching control circuit SC is being provided by an amplifier device type TS391. The DC level control input Cli of the buck converter is coupled through a serial RC member R5C4 to the second input terminal of the differential input of the switching control circuit SC. This serial RC member R5C4 comprises a serial arrangement of a resistor R5 coupled between the level control input Cli on the one hand and the second input terminal of the differential input of the switching control circuit SC on the other hand, the end of this resistor R5 directed to the second input terminal of the differential input of the switching control circuit SC being couple to a mass connected capacitor C5. The serial RC member R5C4 gives rise to an exponential 'soft start' ramp up of the reference voltage at the second input terminal of the differential input of the switching control circuit SC. This results in an equal exponential rising of the output voltage. The reference voltage Vref at the level control input Cli is adjustable to control the DC level of the DC output signal Vout at the output means O. This method of soft start ramp up can also be used in the synchronous rectifying type embodiment of a buck converter according to the invention of Figure 2.

[0036] The output of the switching control circuit SC is coupled through a complementary double transistor output driver stage T1, T2 to the gate of the MOSFET M1 switch. This output driver stage T1, T2 includes a cascade of a npn and a pnp type transistor T1, respectively T2, having their base electrodes commonly connected at the output of the switching control circuit SC, their collector electrodes respectively to the input means I and mass, and their emitter electrodes in common at the switching control input of the first switch means, i.e. gate electrode of the MOSFET M1 switch. The complementary double transistor output driver stage T1, T2 decreases the dynamic output resistance of the switching control circuit SC amplifier, i.e. the amplifier device type TS391, down to a few ten ohms. The lower the output resistance of the driver stage T1, T2, the faster the MOSFET M1 switch switches and the higher the efficiency. The gain of the complementary double transistor output driver stage T1, T2 is unity. This simple concept of a buck converter according to the invention is suitable for DC conversion of DC input voltages up to the order of magnitude of 5 Volt.

[0037] Figure 4 shows a circuit implementation of a buck converter type according to the invention differing from the buck converter of Figure 3 in that it comprises a second switch means S2 constituting a synchronous rectifier. This second switch means S2 is being implemented by a MOSFET type corresponding with the MOSFET 1 type of the first switch means S1, hereinafter also being referred to as MOSFET M2 switch. The switching control circuit SC now comprises a first control circuit SC1 for generating the pulse train and separated therefrom a second control circuit SC2, which handles the timing of second switch means S2 (i.e. MOSFET M2 switch)such, that the second switch means S2 is open when the first switch means S1 is closed and vice versa, adding some dead time between to avoid cross conduction between both switch means. The common junction of the resistor R3 and the tap of the voltage divider (R1, R2) is coupled to the first input terminal of the first control circuit SC1 and through a resistor R6 to an input terminal of the second control circuit SC2. The resistor R6 is to introduce a certain hysteresis effect in the positive signal feed back within the regenerative loop, to allow the circuit to enter into the burst mode at light load values, in the event the synchronous rectifier switch is placed external to the PCB bearing the remainder of the buck converter circuit.

[0038] The second control circuit SC2 respectively provides a switching control signal to the switching control input of the second switch means S2, i.e. the gate electrodes of the MOSFET M2 switch and the MOSFET M2 switch through mutually corresponding complementary double transistor output driver stages T1, T2, respectively T3, T4. These two double transistor complementary drivers T1, T2, and T3, T4 decrease the dynamic output resistance resulting in an acceleration in the switching operation of the MOSFET M2 switch and the MOSFET M1 switch, respectively.

[0039] The switching control signal of the second control circuit SC2 controls the second switch means S2, i. e. the MOSFET M2 switch, in a switching phase opposite to the switching phase of the first switching means S1, i.e. the MOSFET M1 switch, such that at the alternate switching from a conducting state into a non-conducting state, dead zone periods occur, in which both said first and second switch means are in a non-conducting state. During the dead zones MOSFET M1 switch and MOSFET M2 switch are open, allowing the freewheeling diode D1 to receive the current generated by the collapse of the magnetic field of the inductor Ls.

[0040] A level shifter is arranged between the output of the first control circuit SC1 and the double transistor complementary driver T1, T2. The level shifter comprises a cascade connection of a PNP transistor T5 and a

MOSFET M3 switch, in which the emitter-collector path of the transistor T5 is serially connected to the source-drain path of the MOSFET M3, the emitter of the transistor T5 being coupled to the input means I of the buck converter through an emitter resistor R7 and the drain of the MOSFET M3 switch being mass connected. The collector of the transistor T5 is coupled to the source of the MOSFET M3 switch as well as through a resistor R8 to the base of this transistor T5. The base of the transistor T5 is coupled through a zenerdiode Z1 to the input means I of the buck converter. The level shifter is to adapt the DC level of the DC input signal before applying the latter to the first switch means S1, i.e. the p-channel MOSFET M1 switch, in order to prevent the gate-source voltage Ugs of the MOSFET M1 switch from exceeding its maximum value of 10V. When applying an input voltage Vin of e.g. 40 V, the level shifter is to set the gate voltage of the MOSFET M1 switch at a minimum value of 30 V. This allows to operate the buck converter at substantially higher input voltages Vin.than possible with the buck converter of Figure 3.

[0041] In a practical embodiment, the level shifter is a discrete linear regulator which is switched on and off by the MOSFET M3 switch, which is an enhancement type MOSFET.

The signal input of the second switching control circuit SC2 is coupled through a resistor R9 to a bias voltage when using an amplifier without push pull output stage such as type LM 2901 or like amplifiers. the resistor R9 can be left out when using an amplifier with a push pull output stage, such as a type TS861 amplifier.

The advantages achieved with the buck converter are a.o. a simple and cost-effective realization of the buck converter as a whole and more in particular, the frequency dependent phase shifting network (Rx, Cx or Lx, Cx), using low cost differential amplifier devices and comparators and elements, such as the MOSFET type switches, freewheeling diodes, inductors and capacitors, and an appropriate dynamic regulation behavior. In addition thereto, the embodiment of the buck converter according to the invention of Figure 3, comprising a freewheeling diode shows an excellent low power burst mode efficiency. Using the described level shifter, this self oscillating buck converter is applicable within a wide range of input voltage values.

[0042] Furthermore the use of an RC phase shifting network in a buck converter according to the invention allows synchronization of the pulse repetition frequency to an external frequency, which in practice is possible in a typical range +-30% around the loop oscillation frequency without noticeably limitation of the buck converters dynamic performance.

[0043] In practice the input voltage Vin has a small influence on the output DC voltage Vout. In a practical embodiment, a variation of the input voltage from 5V to 12V caused the output DC voltage Vout to change typically approximately 50mV. The exact value depends on the difference between the impedance of the feedback divider R1/R2 and the impedance of the oscillation network Rx/Cx/R3. The lower the feedback impedance in the regenerative loop, the lower said influence of input voltage variation. From a practical point of view, the impedance relation cannot be ideal, because too low output divider impedance significantly decreases light load efficiency and too high oscillation network impedance is too sensitive to noise. Elimination of said influence while avoiding these conflicting impedance requirements, is obtained by inserting a capacitor (not shown) in series with resistor R3. To prevent this capacitor from affecting the phase, its value is chosen in the order of magnitude of 100 nF.

[0044] The present invention has been disclosed with reference to preferred embodiments that should be considered as exemplary, instead of restrictive, inasmuch as persons skilled in the art would recognize numerous alternative embodiments of amendments thereof within the scope of the appended Claims.

[0045] For example, other phase shifting networks (RX/Cx/Lx) may be used, which only have to meet the requirement to provide a negative phase shifting at higher frequency.

[0046] Furthermore, the transistor type of the first and second switch means S1 and S2 only has a minimal influence to the circuits behaviour. Instead of P-channel enhancement type MOSFETs for these switch means S1 and S2, N-channel enhancement type MOSFETs can be used to increase the conversion efficiency. In principle, however, any transistor type, be it N- or P-Channel Field Effect Transistors or bipolar transistors, or others, may be applied.

Claims

1. Buck converter for generating a regulated DC output voltage (Vout) from an unregulated DC input voltage (Vin) comprising:

   - input means (I) for receiving said unregulated DC input voltage (Vin);
   - output means (O) for providing said regulated DC output voltage (Vout) to a load (R1);
   - first switch means (S1) following said input means (I) for switching said unregulated DC input voltage (Vin) to provide a pulse train;
   - output filtering means (Ls, Cs) coupled between said first switch means (S1) and said output means (O) for low pass filtering of said pulse train;
   - a regenerative loop providing regenerative feed back of said pulse train through a switching control circuit (SC) to a switching control input of said first switch means (S1),

   characterized by said regenerative loop including a loop filter circuit (Lx, Cx or Rx, Cx) coupled be-

tween an output of said first switch means (S1) and said switching control circuit (SC) and providing a loop time constant substantially smaller than the time constant of said output filtering means (Ls, Cs).

2. Buck converter according to claim 1, **characterized by** said output filtering means (Ls, Cs) comprising a first serial LC circuit receiving said pulse train from said switch means (S1), an inductance (Ls) thereof being serially coupled between the output of said first switch means (S1) and a mass connected capacitance (Cs), the inductance (Ls) and the capacitance (Cs) at their common junction being coupled to said output means (O), said loop filter circuit (Lx, Cx or Rx, Cx) comprising a frequency dependent phase shifting network coupled on the one hand at the output of said first switch means (S1) and on the other hand at an input of said switching control circuit (SC).

3. Buck converter according to claim 2, **characterized by** said frequency dependent phase shifting network(Lx, Cx or Rx, Cx) having an output being coupled through a resistor (R3) to a tap of a resistive voltage divider (R1, R2) being connected in shunt across the capacitance (Cs) of the first serial LC circuit (Ls, Cs).

4. Buck converter according to claim 3, **characterized by** said frequency dependent phase shifting network (Rx, Cx) including a serial RC circuit comprising subsequently coupled between the output of said first switch means (S1) and mass a serial arrangement of a resistor (Rx) and a capacitor (Cx), said resistor (Rx) and said capacitor (Cx) at their common junction being coupled to the output of said frequency dependent phase shifting network (Rx, Cx).

5. Buck converter according to claim 3, **characterized by** said frequency dependent phase shifting network (Lx, Cx) comprising a second serial LC circuit (Lx, Cx) comprising subsequently coupled between the output of said first switch means (S1) and mass a serial arrangement of an inductance (Lx) and a capacitance (Cx), said inductance (lx) and said capacitance (Cx) at their common junction being coupled to the output of said frequency dependent phase shifting network (Lx, Cx).

6. Buck converter according to one of claims 1 to 5, **characterized by** the switching control circuit (SC) comprising a differential amplifier (D1) having a differential input with first and second input terminals being respectively coupled to an output of said loop filter circuit (Lx, Cx or Rx, Cx) and a DC level control input (Cli) of the buck converter, an output of said differential amplifier (D1) being coupled to the switching control input of said first switch means (S1).

7. Buck converter according to one of claims 1 to 6, **characterized by** a synchronous rectifier comprising second switch means S2) for a synchronous rectification of the output of said first switch means (S1) and being controlled to switch in a phase mode, which is substantially inverted to the switching phase mode of the first switch means (S1).

8. Buck converter according to claims 6 and 7, **characterized by** the output of said differential amplifier (D1) being followed by a differential output stage providing a pair of phase opposite first and second output signals, said first and second output signals being respectively supplied to the switching control input of said first switch means (S1) and a switching control input of said second switch means (S2).

9. Buck converter according to claim 7, **characterized by** said first and second switch means (S1 and S2, respectively) being controlled to switch alternately in mutually phase opposition from a conducting state into a non-conducting state via dead zone periods in which both said first and second switch means (S1 and S2, respectively) are in a non-conducting state.

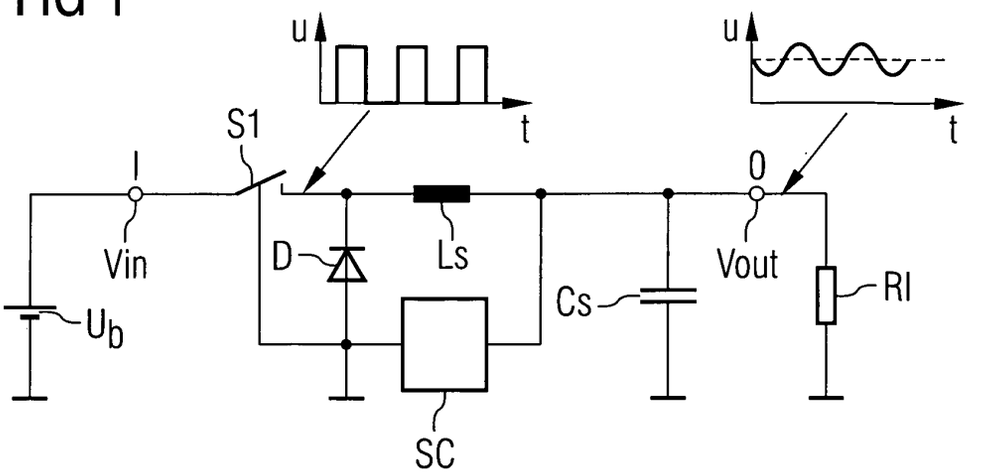
10. Buck converter according to one of claims 1 to 9, **characterized by** a level shifter being arranged between the input means (I) and the first switch means (S1) for DC level adaptation of the DC input signal (Vinj).

11. Buck converter according to one of claims 1 to 10, **characterized by** the first switch means (S1) comprising an P-Channel enhancement type MOSFET.

12. Buck converter according to claim 11, **characterized by** a driver circuit (T1, T2 and T3, T4) coupled to a gate electrode of said MOSFET (S1) and having an output resistance at most in the order of magnitude of ten ohm.

13. Buck converter according to claim 6, **characterized by** an integrating RC circuit (R5, C4) included between the level control input (Cli) of the buck converter on the one hand and the second input terminal of the differential amplifier (D1) on the other hand.

FIG 1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S1
I
Vin
D
Ls
Cs
Ub
SC
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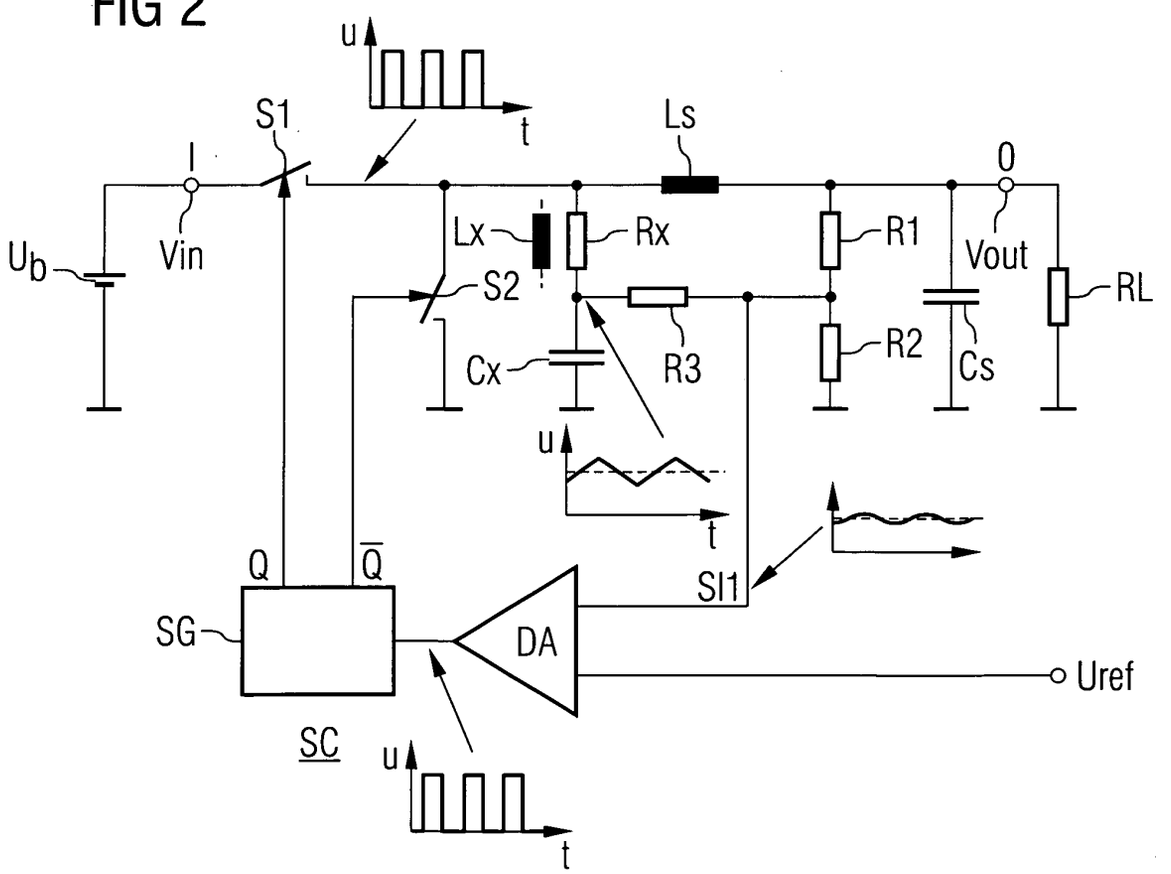
0
Vout
Rl

FIG 2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S1
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Vin
Lx
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Vout
RL
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SI1
SG
DA
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SC
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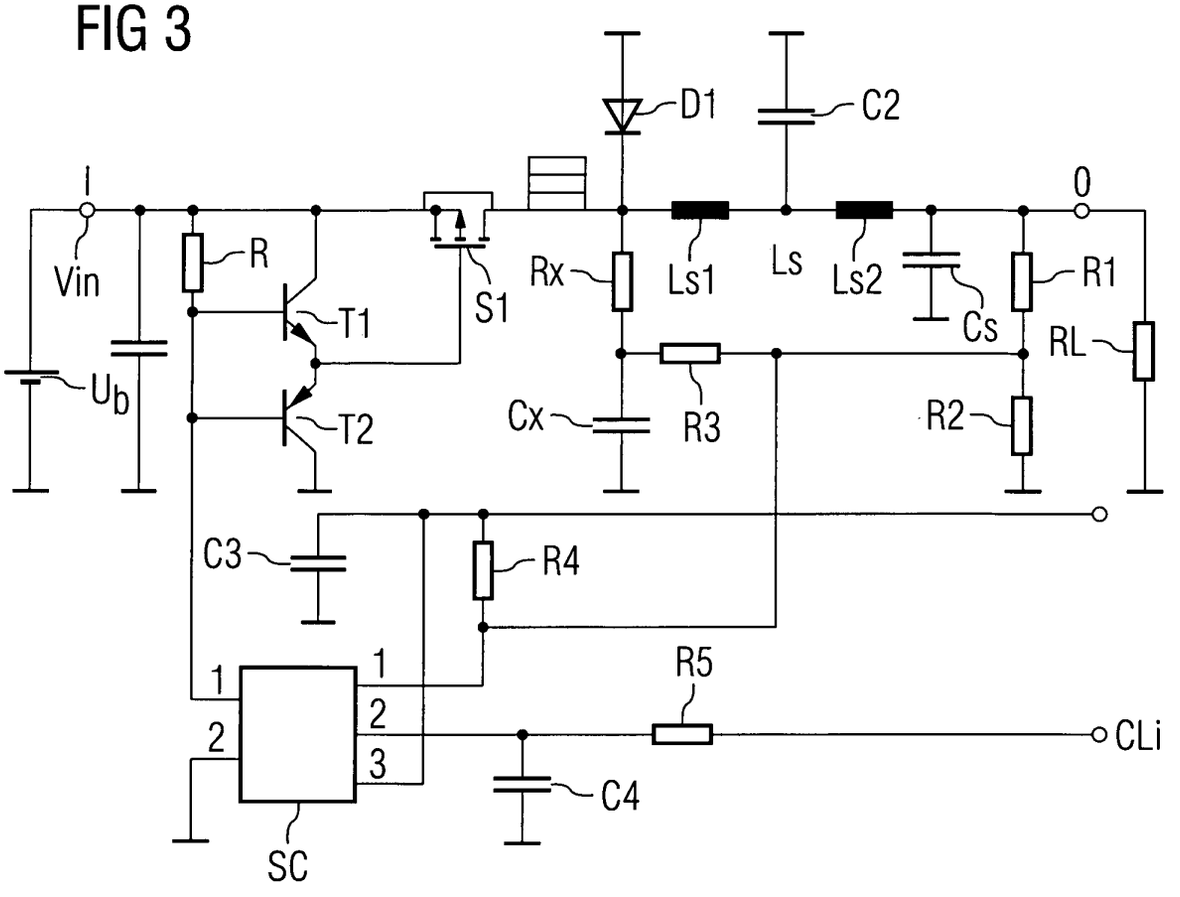
FIG 3


D1
C2
I
O
Vin
R
T1
T2
S1
Rx
Ls1
Ls
Ls2
Cs
R1
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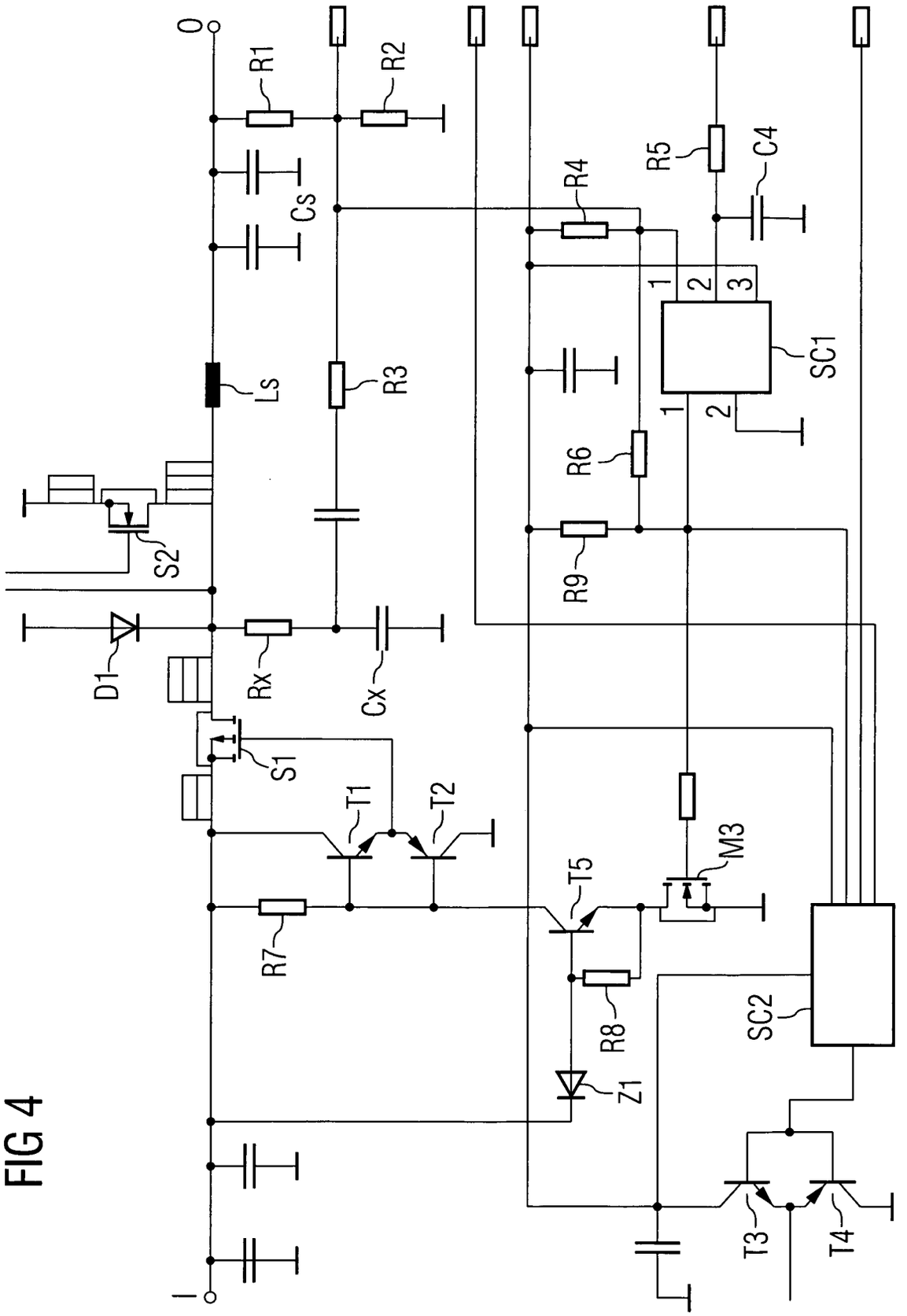
R3
R2
C3
R4
R5
1
2
3
CLi
C4
SC

FIG 4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R1
R2
Cs
R4
R5
C4
1
2
3
SC1
Ls
R3
R6
S2
R9
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Rx
Cx
S1
T1
T2
M3
T5
R7
R8
SC2
Z1
T3
T4
I

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EUROPEAN SEARCH REPORT

Application Number
EP 02 02 7400

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G05F

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
MUNICH	7 May 2003	Villafuerte Abrego

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07-05-2003

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