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(54) **Acquisition circuit for low chip rate option for mobile telecommunication system**

Erfassungsschaltung für eine Niedrig-Chipraten-Option für ein Mobilkommunikationssystem

Circuit d'acquisition pour option faible debit d'éléments d'un système de télécommunications mobile

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Description

[0001] FIELD OF INVENTION

[0002] The present invention relates to the field of wireless communication. Specifically, the present invention relates to enabling the synchronization step between the User Equipment and the base station in the low chip rate option (1.28 Mcps) of Universal Mobile Telecommunication System (UMTS) Time Division Duplex (TDD) and TD-SCDMA.

[0003] BACKGROUND

[0004] In order to establish communications in a wireless system a User Equipment (UE) must first synchronize with a base station. Once synchronization is established, the substantive communication and/or data transfer may occur such that a wireless telephone call may be conducted.

[0005] The 3rd Generation Partnership Project (3GPP) in, for example, 3GPP TS 25.221 v5.2.0, 3GPP TS 25.223v5.1.0 and 3GPP TS 25.224 v5.2.0, specifies communication systems that employ a relatively high chip rate of 3.84 Mcps or, optionally, a relatively low chip rate of 1.28 Mcps. In the specified high rate option, a User Equipment (UE) searches for a known Primary Synchronization Code (PSC) and then identifies one of a number of different groups of secondary synchronization codes. However, there is no single PSC in the low chip rate option. A UE must search for a downlink synchronization code SYNC-DL which may be one of 32 different 64 element sequences.

[0006] Figure 1 illustrates the time frame structure for the 1.28 Mcps low chip rate option of a wireless system as currently specified by 3GPP. Ten (10) ms frames are divided into two sub-frames of five (5) ms each. Each sub-frame includes seven (7) timeslots and a separate area for uplink and downlink synchronization (SYNC) signals. Each Timeslot 0-6 is configured to receive communication data symbols and an identifying midamble code. Timeslot 0 is always a downlink (DL) slot. Timeslot 1 is always an uplink (UL) slot. Timeslots 2-7 are configurable for either UL or DL usage.

[0007] Between Timeslot 0 and Timeslot 1, there exists a ninety-six (96) chip long Downlink Pilot Timeslot (DwPTS), a ninety-six (96) chip long guard period (GP) and a one-hundred sixty (160) chip long uplink pilot timeslot (UpPTS). Within the DwPTS there is a thirty-two (32) chip long guard period and a 64 chip Synchronous (SYNC-DL) code section. In addition, every two (2) frames (four sub-frames) defines a 20 ms superframe.

[0008] In the current 3GPP system specification, there are thirty-two (32) SYNC-DL codes, each having sixty four (64) elements. Each SYNC-DL code points to four basic midamble codes (of length 128) so that there are total of 128 basic midamble codes. In addition, each timeslot's midamble code (of length 144) is generated from a basic midamble code (of length 128). From each basic midamble code, up to 16 timeslot midamble codes of length 144 can be generated.

[0009] Quadrature Phase Shift Keying (QPSK) modulation is used on the SYNC-DL codes. In each sub-frame, the midamble code in the DL Timeslot 0 provides a QPSK phase reference of the SYNC-DL code in the DwPTS. Accordingly, once the midamble code of Timeslot 0 is determined the QPSK modulation of a SYNC-DL code in the DwPTS of the sub-frame can be ascertained. The timing of the superframe (SFT) is indicated by a specified sequence of the Quadrature Phase Shift Keying (QPSK) modulation on the SYNC-DL code over a specified number of sequential sub-frames.

[0010] An objective of synchronization is to be able to receive data of a broadcast channel (BCH) which is carried by a Primary Common Control Physical Channel (P-CCPCH) in Timeslots 0 of a superframe. Presently, two different sequences of SYNC-DL code modulation are specified for four sequential DwPTS in a superframe, 3GPP TS 25.223 v5.1.0 Sec. 9.1.1. A first sequence, S1, indicates that there is a P-CCPCH carrying a BCH in the next superframe; a second sequence, S2, indicates that there is no such P-CCPCH in the next superframe. Where sequence S1 of the modulation of the SYNC-DL codes of a superframe is found, the data from the BCH can be read from the P-CCPCH of the next super frame.

[0011] Annex D of 3GPP TS 25.224 V5.2. 0 suggests a four step procedure for UE determination of synchronization which is graphically depicted in Figure 2. The first step requires the system to search through the 32 codes to determine which SYNC-DL code is being received and to determine the code timing, i. e. where in the stream of received data the DwPLTSs carrying the SYNC-DL code are located as a reference with respect to the system time frame structure. Step two of the process determines which one of the four basic midamble codes, as indicated by the SYNC-DL, is used. This is completed by processing the midamble section of Timeslot 0 (P-CCPCH). Since the midamble and the scrambling code are tied together on a one-to-one correlation, once midamble is known, the scrambling code is also known. If this step fails, the first step is repeated.

[0012] During step three, the process determines the phases of the QPSK modulation that is on the SYNC code over multiple sub-frames and from this the super frame timing (SFT) is determined. At step four, the complete broadcast channel (BCH) information is read by the UE.

[0013] In view of the provision for the 1.28 Mcps option, there is a need for a UE which has a receiver capable of conducting synchronization in an efficient manner without undo hardware cost. An example of a known CDMA demodulator is described in EP 0 994 573 A2. A solution for efficient cell search is provided in EP 0 924 868.

[0014] SUMMARY

[0015] The present invention discloses a circuit for a User Equipment (UE) that performs the acquisition for the low chip rate option of the UMTS TDD standard of a 3GPP system as currently specified. The present invention implements the basic acquisition steps in a reliable

efficient manner. The first step is detection of the base synchronization (SYNC-DL) code, step two is the detection of the midamble used, step three is the detection of the super frame timing. Completion of these steps enables reading of the full BCH message.

[0016] The User Equipment (UE) is configured for use in a wireless telecommunications system which utilizes a time frame format where base stations transmit in a down link pilot timeslot a synchronization code selected from a predetermined number X of downlink synchronization codes of Y sequential elements, where X and Y are integers greater than 15. In the low chip rate option of 3GPP, X and Y are currently specified as 32 and 64, respectively. The signals are transmitted at a predetermined chip rate and the UE receives communications signals and samples them at a sampling rate which is at least as fast as the chip rate.

[0017] The UE has a synchronization circuit for processing the received communication signal samples. The synchronization circuit has a synchronization code determination circuit which receives samples at an input rate which is at least as fast as the chip rate and processes sets of sequential samples at a processing rate faster than the sample input rate. The synchronization code determination circuit includes a plurality M of Y element correlators, where $M \leq X/2$, which each have an input for receiving in parallel at the sample input rate received communication signal samples. The correlators correlate each set of samples with at least two synchronization codes of the set of X downlink synchronization codes. A detection circuit is operatively associated with the correlators to detect and track positive correlations of downlink synchronization codes with sequential sample sets. Each correlator has an output for outputting code correlations for each set of samples at at least twice the sample input rate such that collectively the correlators output to the detection circuit correlation data for all X synchronization codes before processing further communication signal samples.

[0018] Where the predetermined number of downlink synchronization codes is 32, each having 64 sequential elements, there are no more than 16 correlators in the synchronization code determination circuit. Preferably, there are no more than 8 correlators in the synchronization code determination circuit for the currently specified 3GPP type system. Each correlator receives in parallel, at the sample input rate, received communication signal samples and correlates each set of samples with at least four synchronization codes of the set of 32 downlink synchronization codes during one input rate period. Preferably, each correlator in the synchronization code determination circuit includes N match filters which each correlate 64/N element segments of received communication signal sample sets with corresponding 64/N element segments of at least four synchronization codes of the set of 32 downlink synchronization codes during one input rate period. In one embodiment, each correlator in the synchronization code determination circuit includes 8 match filters which correlate 4-element segments.

[0019] The UE receives data of a specified channel (BCH) which is carried on a primary common control physical channel (P-CCPCH) in selected timeslots of a predefined system time frame structure to enable the UE to proceed with bi-directional communication with a base station which transmitted the BCH data. Each transmitted downlink synchronization code has a modulation which is indicated by a midamble transmitted in a specified timeslot and a specified modulation sequence of consecutive downlink synchronization codes identifies the location of the BCH data. Accordingly, the UE also preferably has a midamble determination circuit and a phase modulation sequence detection circuit. The midamble determination circuit is operatively associated with the synchronization code determination circuit to determine the respective transmitted midamble based on the relative location and the identity of a detected downlink synchronization code. The phase modulation sequence detection circuit is operatively associated with the midamble determination circuit and the synchronization code determination circuit to determine sequences of phase modulation of consecutive detected downlink synchronization codes based on downlink synchronization codes detected by the synchronization code determination circuit and the midamble determined by the midamble determination circuit.

[0020] Preferably, the synchronization code determination circuit includes a noise estimation circuit and an Automatic Frequency Control circuit (AFC) associated with synchronization code determination circuit's detection circuit. The noise estimation circuit provides the detection circuit with a noise estimate upon which synchronization code detection is based. The detection circuit controls the AFC to produce a frequency correction signal which is mixed with received communication samples input to the midamble generating circuit.

[0021] In the low chip rate 3GPP specified system, each synchronization code points to a predefined set of midambles from which one is transmitted with each transmitted downlink synchronization code to indicate the modulation of that transmitted code. Accordingly, the midamble determination circuit preferably includes a buffer, at least one midamble correlator, a midamble generator and a midamble decision circuit. The buffer has an input for receiving AFC corrected communication samples from the synchronization code determination circuit. The midamble generator has an input for receiving the determined synchronization code from the synchronization code determination circuit and sequentially generates midambles based on the predefined set of midambles to which the determined synchronization code points. The midamble correlator has an input for receiving sets of signal samples from the buffer corresponding to a midamble portion of the specified timeslot, an input for receiving generated midambles from the midamble generator and an output for outputting correlation data to the midamble decision circuit. The midamble decision circuit

determines which of the midambles of the predefined set of midambles to which the determined synchronization code points was transmitted with the determined synchronization code based on correlation data between sets of signal samples from the buffer corresponding to a midamble portion of the specified timeslot and generated midambles from the midamble generator. The midamble decision circuit has an output for outputting a selection signal to the midamble generator which in turn has an output which outputs a midamble based on the selection signal to the phase modulation sequence detection circuit. Preferably, there are a plurality of midamble correlators and the correlators in the synchronization code determination circuit are used as the midamble correlators.

[0022] The phase modulation sequence detection circuit preferably includes a buffer, a phase correlator means, and a phase sequence decision circuit. The phase modulation sequence detection circuit's buffer has an input for receiving communication samples from the synchronization code determination circuit. The phase correlator means receives sets of signal samples from the phase modulation sequence detection circuit's buffer corresponding to synchronization code portions of the received signal samples, receives the selected midamble from the midamble generator and outputs phase correlation data to the sequence decision circuit. The sequence decision circuit identifies phase sequences of consecutive sets of signal samples corresponding to the determined synchronization code. The sequence decision circuit has an input for receiving phase correlation data from the phase correlator means and an output for outputting a signal identifying the location of the BCH data when a specified phase sequence is detected. Optionally, the buffer in said midamble determination circuit is used as the phase modulation sequence detection circuit's buffer.

[0023] Other objects and advantages of the present invention will be apparent to those skilled in the art from the following detailed description.

[0024] BRIEF DESCRIPTION OF THE DRAWINGS

[0025] Figure 1 is a burst diagram illustrating the frame structure for the 1.28 Mcps option of a 3GPP system.

[0026] Figure 2 is a flow chart of a process for establishing synchronous communication by a UE in the context of the 1.28 Mcps option of a 3GPP system.

[0027] Figure 3 is a block diagram illustrating components of a UE receiver made in accordance with the teachings of the present invention.

[0028] . Figure 4 is an expanded block diagram of a Matched Filter/Correlator component of the UE receiver of Figure 3.

[0029] DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT(S)

[0030] Referring to Figure 3, there is shown a block diagram of a portion of a receiver for a user equipment (UE) for use in conjunction with a wireless telecommunication system in accordance with current 3GPP specification utilizing a 1.28 Mcps chip rate. The UE receives wireless signals via an antenna (not shown) and samples of them using at least the chip rate of 1.28 Mcps. Preferably, sampling is done at twice the chip rate or at some other multiple of the chip rate. A sampling rate higher than the chip rate improves performance, but too high of a sampling rate can require the expense of additional processing equipment in order to maintain sufficient processing speed. Where sampling is done at twice the chip rate, various processing options are available as known in the art. For example, alternate samples may be processed independently as two different data streams or, alternatively, the samples may be selectively combined in accordance with conventional methods.

[0031] The synchronization processing circuit shown in Figure 3 is designed to generate information regarding the timing of the communication signals sent by a base station in accordance with the 3GPP specified 1.28 Mcps option frame formatting to enable the UE to communicate with that base station. When an appropriate modulation sequence of SYNC-DL codes is detected, such as sequence S1 above, the UE can then read data sent by the base station in a broadcast channel (BCH) which is carried on a P-CCPCH in the Timeslots 0 of a superframe which then enables the UE to proceed with bi-directional communication with the base station which sent the BCH data. The synchronization processing circuit has three main components: a SYNC-DL determination circuit 10, a midamble determination circuit 20 and a phase modulation sequence detection circuit 30.

[0032] The SYNC-DL determination circuit 10 includes a plurality of M parallel match filter/correlators 12_1 through 12_M which output correlation data to a detection circuit 13. The received communication signal samples are input to each of the correlators 12_1-12_M. Each correlator 12_1-12_M also has an input from a synchronization code generator 11 to enable it to correlate a set of samples being processed against one of the 32 different SYNC-DL codes.

[0033] In the currently specified 1.28 Mcps option, each SYNC-DL code has 64 elements so that the correlators 12_1-12_M are configured to process sets of 64 received signal samples at one time. As shown in Figure 4, each correlator of correlators12_1-12_M is preferably configured as a bank of N matched filters, each with an associated squaring or similar device, and a summer. Each matched filter processes a different segment which is 64/N in length of a set of 64 received signal samples. Corresponding segments of a SYNC-DL code are directed to a code input of each of the match filters. Each matched filter has an output which outputs a signal to a respective squaring or similar device which in turn collectively output signals to a summer which sums the collective segment outputs to provide an output of the correlator.

[0034] The correlators 12_1-12_M receive the signal samples at a first input rate, but operate much faster so that each correlator can output correlation data for at least

two different SYNC-DL codes before processing subsequent signal samples. For example, with reference to Figure 4, for a given sample input rate (ir), the code input rate from the SYNC-DL code generator 11 is at least eight (8) code elements per ir period to each of the N matched filters. After each corresponding set of four elements of a SYNC-DL code is received by each of the N matched filters, correlation data output is squared, collectively summed and then output. Since each correlator 12_1-12_M processes at least two SYNC-DL codes per sample input rate period, the number M of correlators which are required without incurring any significant processing delay is no more than half the number of possible codes.

[0035] In the preferred construction, each correlator 12_1-12_M preferably operates at a speed which processes four SYNC-DL codes per sample input rate period so that eight (M=8) correlators are used, i.e. the number of possible codes (32) divided by the rate factor (4). In a preferred embodiment each correlator is comprised of eight (N=8) matched filters of length eight, i.e. code length (64) divided by number of segments (8). In the case where the matched filters are of length four, from an element processing perspective, for each element of signal sample which is processed 16 elements of SYNC-DL codes are processed by each matched filter.

[0036] The detection circuit 13 receives the output from the correlators 12_1-12_M and tracks positive correlations over a selected number of frames. A noise estimation circuit 15 is provided which also receives the communication signal samples and outputs a noise estimate. The detection circuit 13 uses the noise estimate from the noise estimation circuit 15 to determine whether or not the output from one of the correlators 12_1-12_M is positive. Preferably, a positive correlation is detected when a correlator output for a SYNC-DL code correlation exceeds the noise estimate multiplied by a selected noise coefficient constant.

[0037] If the same SYNC-DL code generates a positive correlation at the same relative location over a plurality of sub-frames, preferably eight, the detection circuit determines that it has identified both the specific SYNC-DL code being received and the relative position of the DwPTS within the communication signal which in turn provides the location of Timeslot 0 of each of the subframes and the associated midamble.

[0038] Preferably, an Automatic Frequency Control (AFC) circuit 16 is provided which is controlled by the detection circuit 13 to adjust the frequency of the input signal which is fed to a buffer 21 of the midamble detection circuit 20. An output of the AFC is mixed with the signal sample input via a mixer 17 to provide a frequency adjusted sample input to the midamble detection circuit. AFC, carrier recovery, can be completed in conjunction with SYNC-DL code determination so that subsequent steps are able to perform coherent processing. With each positive detection of the SYNC-DL code, the detection circuit sends a control signal to the AFC 16. The AFC process is completed when the determination of the SYNC-DL by the detection circuit 13 is completed. As an alternative, the mixer 17 may be placed at the input of the SYNC-DL determination circuit 10 so that AFC corrections are made to the input signal which the circuit 10 is receiving while continuing its determination function. This alternate location for mixer 17 is also in advance of the input to the sequence determination circuit 30.

[0039] Once the SYNC-DL determination circuit 10 has determined which of the 32 SYNC-DL codes is being received from a base station, the midamble selection circuit is able to operate to determine which of the four basic midambles are being utilized in the P-CCPCH transmitted by the base station which transmitted the received SYNC-DL code. In the currently specified 3GPP system, the P-CCPCH is comprised of two channels P-CCPCH1 and P-CCPCH2 which are mapped onto the first two code channels of sub-frame Timeslots 0.

[0040] The midamble selection circuit 20 includes a midamble generator which receives the SYNC-DL code identification and relative timing information from the detection circuit 13 of the SYNC-DL determination circuit 10. The midamble generator 23 then generates 144 bit midambles from each of the four 128 bit midambles associated with the SYNC-DL code which was previously identified by detection circuit 13. Having determined the relative position of the DwPTS, the samples corresponding to the location of sequential Timeslots 0 midamble are input from a buffer 21 to a match filter/correlator 24a with respect to the first code channel representing P-CCPCH1 and to a matched filter/correlator 24b representing the second code channel P-CCPCH2. These inputs are correlated with an input from the midamble generator 23 derived from each of the four basic midambles corresponding to the identified SYNC-DL code. The decision circuit 26 receives the correlation of each iteration comparison of midambles from matched filter/correlators 24a and 24b in order to identify which of the four midambles was transmitted by the base station. Preferably, this determination is made in comparison to a noise estimate received from noise estimator15 multiplied by a second selected correlation factor constant.

[0041] The matched filter/correlators 12_1-12_M do not need to be used by the SYNC-DL determination circuit 10 when the midamble detection circuit 20 is determining the midamble. Accordingly, the midamble detection circuit 20 can be configured to use the matched filter/correlators 12_1-12_M as matched filter/correlators 24a and 24b. Reuse of the hardware provides efficient implementation.

[0042] Also, the use of two matched filter/correlators 24a and 24b can accommodate spaced time transmit diversity that may be used on the P-CCPCH. In this case, two midambles are used with one-half the power of one midamble in normal operation. Detection of both midambles occurs and the decision device combines them non-coherently.

[0043] When a positive midamble determination is

made, the decision circuit 26 outputs a midamble select signal to the midamble generator 23 which in turn outputs the identified midamble to the sequence detection circuit 30.

[0044] The sequence detection circuit 30 includes a buffer 31 which receives the signal samples, modulation correlators 32 and a decision circuit 34. The buffer 21 of midamble determination circuit may be reused for buffer 31 in which case the sequence detection circuit takes advantage of the AFC without relocation of the mixer 17 as discussed above.

[0045] The sequence detection circuit 30 receives the identified SYNC-DL code and DwPTS location information from the detection circuit 13 of the SYNC-DL determination circuit 10 and the midamble data from the midamble detection circuit 20. The modulation correlators 32 receive input from the buffer 31 into which the received communication samples have been stored and output data to the decision circuit 34. The correlators 32 correlate the QPSK modulation of the SYNC-DL code in the DwPTS with the identified midamble for series of subframes. This information is output to the decision circuit 34. Separate correlators are provided to detect phases of SYNC-DL and midamble codes, respectively. Alternatively, a single correlator can be shared to detect phases of both SYNC-DL and midamble codes.

[0046] The decision circuit 34 calculates the phase effect between the determined midamble and four or more consecutive SYNC-DL codes. The decision circuit 34 determines whether or not a selected sequence has been detected, such as the S1 sequence referenced above. When the selected modulation sequence is detected, the decision circuit 34 outputs superframe timing (SFT) to identify the start of a superframe in which BCH data carried on the P-CCPCH in Timeslots 0. This is currently specified in 3GPP as the next superframe following an S1 sequence of modulations of the DwPTS.

Claims

1. A User Equipment, UE, adapted to receive wireless telecommunication signals in a down link pilot timeslot of a time frame format and to sample the received communication signals to produce communication signal samples, where the communication signals were transmitted by a basle station at a predetermined chip rate and include a synchronization code selected from a predetermined number X of downlink synchronization codes each having Y sequential elements, where X and Y are integers greater than 15, the UE comprising:

   a synchronization circuit (10, 20, 30) for processing the communication signal samples;
   said synchronization circuit having a synchronization code determination circuit (10) adapted for receiving the communication signal samples at a sample input rate which is at least as fast as the chip rate and processing the communication signal sample in sets each having Y samples:

      said synchronization code determination circuit including:

         a plurality of correlators (12_1,...12_m) having an input for receiving Y samples in parallel at the sample input rate; and a detection circuit (13) operatively associated with said correlators to detect and track positive correlations of downlink synchronization codes with said sets;

   wherein
   the number of said correlators (12_1,...12_m) is no more than half the number X of said downlink synchronization codes;
   each of said correlators (12_1,...12_m) includes a plurality of parallel matched filters associated with the correlators input, and each of said parallel matched filters is adapted to process a separate segment of a set of Y samples for correlation with respective segments of the downlink synchronization codes having Y sequential elements; and
   each of said correlators (12_1,...12_m) has an output for outputting code correlations for each set of Y samples at a processing rate such that at least two synchronization codes of said X downlink synchronization codes are correlated with a set of Y samples per sample input rate period whereby collectively said correlators are configured to output to said detection circuit said code correlations for all X synchronization codes before processing further communication signal samples.

2. The UE according to claim 1 wherein the predetermined number X of downlink synchronization codes is 32, each having 64 sequential elements and there are no more than 16 correlators, each configured to correlate sets of 64 samples, in said synchronization code determination circuit.

3. The UE according to claim 2 wherein there are no more than 8 correlators in said synchronization code determination circuit and each correlator is configured to correlate each set of 64 samples with at least four synchronization codes of the set of 32 downlink synchronization codes during one sample input rate period.

4. The UE according to claim 3 wherein each correlator in said synchronization code determination circuit includes N matched filters which are each configured to correlate segments having 64/N elements of each

set of 64 samples with corresponding segments having 64/N elements of each of at least four synchronization codes of the set of 32 downlink synchronization codes during one sample input rate period.

5. The UE according to claim 4 wherein each correlator in said synchronization code determination circuit includes sixteen matched filters which are each configured to correlate four element segments.

6. The UE according to claim 2 configured to receive data of a specified broadcast channel, BCH, which is carried on a primary common control physical channel, P-CCPCH in selected timeslots of the time frame format to enable the UE to proceed with bidirectional communication with a base station which transmitted the BCH data wherein each transmitted downlink synchronization code has a modulation which is indicated by a midamble transmitted in a specified timeslot and wherein a specified modulation sequence of consecutive downlink synchronization codes identifies a location of the BCH data, the UE further comprising:

a midamble determination circuit (20) operatively associated with the synchronization code determination circuit (10) to determine the respective transmitted midamble based on a relative location and identity of a detected downlink synchronization code; and
a phase modulation sequence detection circuit (30) operatively associated with the midamble determination circuit (20) and the synchronization code determination circuit (10) to determine sequences of phase modulation of consecutive detected downlink synchronization codes based on downlink synchronization codes detected by the synchronization code determination circuit and the midamble determined by the midamble determination circuit.

7. The UE according to claim 6 wherein:

said synchronization code determination circuit includes a noise estimation circuit and an Automatic Frequency Control circuit, AFC, associated with the synchronization code determination circuit's detection circuit (13);
the noise estimation circuit is configured to provide the synchronization code determination circuit's detection circuit (13) with a noise estimate upon which synchronization code detection is based; and
the synchronization code determination circuit's detection circuit (13) is configured to control said AFC to produce a frequency correction signal which is mixed with received communication samples input to said midamble determination circuit.

8. The UE according to claim 7 where each synchronization code points to a predefined set of midambles from which one is transmitted with each transmitted downlink synchronization code to indicate the modulation of that transmitted code wherein:

the midamble determination circuit includes a buffer, at least one midamble correlator, a midamble generator and a midamble decision circuit;
the buffer has an input for receiving AFC corrected communication signal samples from said synchronization code determination circuit;
the midamble generator has an input for receiving the determined synchronization code from said synchronization code determination circuit and is configured to sequentially generate midambles based on the predefined set of midambles to which the determined synchronization code points;
the midamble correlator has an input for receiving sets of communication signal samples from said buffer corresponding to a midamble portion of a specified timeslot, an input for receiving generated midambles from the midamble generator and an output for outputting correlation data to the midamble decision circuit; and
the midamble decision circuit is configured to determine which of the midambles of the predefined set of midambles to which the determined synchronization code points was transmitted with the determined synchronization code based on correlation data between sets of communication signal samples from said buffer corresponding to a midamble portion of the specified timeslot and generated midambles from the midamble generator and has an output for outputting a selection signal to said midamble generator which in turn has an output configured to output a midamble based on the selection signal to the phase modulation sequence detection circuit.

9. The UE according to claim 8 wherein there are a plurality of midamble correlators and the correlators in said synchronization code determination circuit configured for use as the midamble correlators.

10. The UE according to claim 8 wherein:

the phase modulation sequence detection circuit includes a buffer, a phase correlator means, and a phase sequence decision circuit;
the phase modulation sequence detection circuit's buffer has an input for receiving communication signal samples from said synchroniza-

tion code determination circuit;
the phase correlator means is configured to receive sets of communication signal samples from said phase modulation sequence detection circuit's buffer corresponding to synchronization code portions of the received communication signal samples and selected midamble from the midamble generator and to output phase correlation data to the sequence decision circuit; and
the sequence decision circuit has an input for receiving phase correlation data from the phase correlator means and has an output for outputting a signal identifying the location of the BCH data when a specified phase sequence is detected.

11. The UE according to claim 10 wherein the buffer in said midamble determination circuit is used as the phase modulation sequence detection circuit's buffer.

12. A method for processing received communication signal samples of wireless telecommunication signals received in a down link pilot_timeslot of a time frame format, where the received communication signals were transmitted by a base station at a predetermined chip rate and include a synchronization code selected from a predetermined number X of downlink synchronization codes each having Y sequential elements, where X and Y are integers greater than 15, where the communication signal samples are input to a synchronization code determination circuit (10) at a sample input rate which is at least as fast as the chip rate and processed in sets each having Y samples, said synchronization code determination circuit including a plurality of correlators (12_1,...12_m) having an input for receiving Y samples in parallel at the sample input rate, and a detection circuit (12) operatively associated with said correlators to detect and track positive correlations of downlink synchronization codes with said sets,
wherein the method further comprises:

processing the communication signal samples in sets of Y samples by each of said plurality of correlators (12_1,...12_m) where the number of correlators is no more than half the number X of said downlink synchronization codes;
processing the "communication signal samples sets in each of said plurality of correlators (12_1,... 12_m) with a plurality of parallel matched filters associated with the correlator's input each of said parallel matched filters processes a separate segment of a set of Y samples for correlation with respective segments of the downlink synchronization codes having sequential elements; and
outputting from each of said plurality of correlators (12_1,...12_m) code correlations for each set of Y samples at a processing rate such that at least two synchronization codes of said X downlink synchronization codes are correlatedwith a set of Y samples per sample input rate period whereby collectively said correlators output to said detection circuit said code correlations for all X synchronization codes before processing further communication signal samples.

13. The method according to claim 12 where the predetermined number of downlink synchronization codes is 32, each having 64 elements, wherein no more than 16 correlators are used in said processing of sample sets which is performed with respect to sets of 64 samples.

14. The method according to claim 13 wherein no more than 8 correlators are used in said processing of sample sets and each correlator receives in parallel at the sample input rate received communication signal samples and correlates each set of samples with at least four synchronization codes of the set of 32 downlink synchronization codes during one sample input rate period.

15. The method according to claim 14 wherein each correlator includes N matched filters which each correlate segments having 64/N samples of sample sets with corresponding 64/N element segments of each of at least four synchronization codes of the set of 32 downlink synchronization codes during one sample input rate period.

16. The method according to claim 15 where each correlator includes 16 matched filters wherein each matched filter correlates 4 element segments.

17. The method according to claim 13 further comprising receiving data of a specified broadcast channel, BCH, which is carried on a primary common control physical channel, P-CCPCH, in selected timeslots to enable bi-directional communication with a base station which transmitted the BCH data where each transmitted downlink synchronization code has a modulation which is indicated by a midamble transmitted in a specified timeslot and where a specified modulation sequence of consecutive downlink synchronization codes identifies a location of the BCH data, the method further comprising:

determining a respective transmitted midamble based on a relative location and identity of a detected downlink synchronization code; and
determining sequences of phase modulation of consecutive detected downlink synchronization codes based on detected downlink synchronization codes and a determined midamble.

18. The method according to claim 17 further comprising:

using a noise estimation circuit to generate a noise estimate upon which synchronization code detection is based; and
using an Automatic Frequency Control circuit to produce a frequency correction signal which is mixed with received communication samples prior to said correlating.

Patentansprüche

1. Benutzerendgerät, UE, eingerichtet für den Empfang von drahtlosen Telekommunikationssignalen in einem Downlink-Pilotsignal-Zeitschlitz eines Time-Frame-Formats und zum Sampeln des empfangenen Kommunikationssignals zur Erzeugung von Kommunikationssignal-Samples, wobei die Kommunikationssignale durch eine Basisstation mit einer vorbestimmten Chip-Rate übertragen wurden und einen Synchronisationscode aufweisen, der aus einer vorbestimmten Anzahl X von Downlink-Synchronisationscodes ausgewählt ist, die jeweils Y sequenzielle Elemente haben, wobei X und Y Ganzzahlen größer als 15 sind und wobei das UE Folgendes aufweist:

eine Synchronisationsschaltung (10, 20, 30) zur Verarbeitung der Kommunikationssignal-Samples;
wobei die Synchronisationsschaltung eine Synchronisationscode-Bestimmungsschaltung (10) aufweist, die für den Empfang der Kommunikationssignal-Samples mit einer Sample-Eingangsrate eingerichtet ist, die mindestens so schnell ist wie die Chip-Rate, sowie für die Verarbeitung der Kommunikationssignal-Samples in Gruppen aus jeweils Y Samples;
wobei die Synchronisationscode-Bestimmungsschaltung Folgendes aufweist:

eine Vielzahl von Korrelatoren (12_1, ... 12_M) mit einem Eingang zum parallelen Empfang von Y Samples mit der Sample-Eingangsrate; und
eine Erkennungsschaltung (13), die operativ mit den Korrelatoren verbunden ist, um positive Korrelationen von Downlink-Synchronisationscodes mit den Gruppen zu erkennen und zu verfolgen;
wobei die Anzahl der Korrelatoren (12_1, ... 12_M) nicht größer ist als die Hälfte der Anzahl X der Downlink-Synchronisationscodes;
wobei jeder der Korrelatoren (12_1, ... 12_M) eine Vielzahl paralleler angepasster Filter in Zusammenhang mit dem Eingang des Korrelators aufweist und wobei jedes der parallelen angepassten Filter eingerichtet ist, um ein separates Segment einer Gruppe von Y Samples zur Korrelation mit entsprechenden Segmenten der Downlink-Synchronisationscodes mit sequenziellen Elementen zu verarbeiten; und
wobei jeder der Korrelatoren (12_1, ... 12_M) einen Ausgang für die Ausgabe von Code-Korrelationen für jede Gruppe von Y Samples mit einer Verarbeitungsrate aufweist, so dass mindestens zwei Synchronisationscodes der X Downlink-Synchronisationscodes mit einer Gruppe von Y Samples pro Zeitraum der Sample-Eingangsrate korreliert sind, wobei die Korrelatoren gemeinsam konfiguriert sind, um vor der Verarbeitung weiterer Kommunikationssignal-Samples die Code-Korrelationen für alle X Synchronisationscodes zur Erkennungsschaltung auszugeben.

2. UE nach Anspruch 1, wobei die vorbestimmte Anzahl X von Downlink-Synchronisationscodes 32 ist, wobei diese Codes jeweils 64 sequenzielle Elemente aufweisen und es nicht mehr als 16 Korrelatoren gibt, die jeweils konfiguriert sind, um in der Synchronisationscode-Bestimmungsschaltung Gruppen aus 64 Samples zu korrelieren.

3. UE nach Anspruch 2, wobei es in der Synchronisationscode-Bestimmungsschaltung nicht mehr als 8 Korrelatoren gibt und wobei jeder Korrelator konfiguriert ist, um jede Gruppe aus 64 Samples während eines Zeitraums der Sample-Eingangsrate mit mindestens vier Synchronisationscodes der Gruppe aus 32 Downlink-Synchronisationscodes zu korrelieren.

4. UE nach Anspruch 3, wobei jeder Korrelator in der Synchronisationscode-Bestimmungsschaltung N angepasste Filter aufweist, die jeweils konfiguriert sind, um während eines Zeitraums der Sample-Eingangsrate Segmente mit 64/N Elementen aus jeder Gruppe aus 64 Samples mit entsprechenden Segmenten mit 64/N Elementen aus jedem von mindestens vier Synchronisationscodes der Gruppe von 32 Downlink-Synchronisationscodes zu korrelieren.

5. UE nach Anspruch 4, wobei jeder Korrelator in der Synchronisationscode-Bestimmungsschaltung sechzehn angepasste Filter aufweist, die jeweils konfiguriert sind, um Segmente mit vier Elementen zu korrelieren.

6. UE nach Anspruch 2, konfiguriert für den Empfang von Daten eines angegebenen Broadcast-Kanals, BCH, der in ausgewählten Zeitschlitzen des Time-

Frame-Formats auf einem Primary Common Control Physical Channel, P-CCPCH, getragen wird, um es dem UE zu ermöglichen, die bidirektionale Kommunikation mit einer Basisstation auszuführen, die die BCH-Daten übertragen hat, wobei jeder übertragene Downlink-Synchronisationscode eine Modulation aufweist, die durch eine in einem vorgegebenen Zeitschlitz übertragene Mittambel angegeben wird, und wobei eine vorgegebene Modulationssequenz aufeinander folgender Downlink-Synchronisationscodes eine Position der BCH-Daten angibt, wobei die UE weiter Folgendes aufweist:

eine Mittambel-Bestimmungsschaltung (20), die operativ mit der Synchronisationscode-Bestimmungsschaltung (10) verbunden ist, um die jeweils übertragene Mittambel auf der Grundlage einer relativen Position zu bestimmen und einen erkannten Downlink-Synchronisationscode zu identifizieren; und
eine Erkennungsschaltung (30) der Phasenmodulationssequenz, die operativ mit der Mittambel-Bestimmungsschaltung (20) und der Synchronisationscode-Bestimmungsschaltung (10) verbunden ist, um auf der Grundlage von Downlink-Synchronisationscodes, die von der Synchronisationscode-Bestimmungsschaltung erkannt werden, sowie von der durch die Mittambel-Bestimmungsschaltung bestimmten Mittambel Sequenzen der Phasenmodulation von aufeinander folgenden erkannten Downlink-Synchronisationscodes zu bestimmen.

7. UE nach Anspruch 6,
wobei die Synchronisationscode-Bestimmungsschaltung eine der Erkennungsschaltung (13) der Synchronisationscode-Bestimmungsschaltung zugeordnete Rauschschätzschaltung und eine automatische Frequenzregelung, AFC, aufweist;
wobei die Rauschschätzschaltung konfiguriert ist, um für die Erkennungsschaltung (13) der Synchronisationscode-Bestimmungsschaltung eine Rauschschätzung bereitzustellen, auf der die Erkennung der Synchronisationscodes basiert; und
wobei die Erkennungsschaltung (13) der Synchronisationscode-Bestimmungsschaltung konfiguriert ist, um die AFC-Regelung zu steuern, um ein Frequenzkorrektursignal zu erzeugen, das mit empfangenen Kommunikations-Samples gemischt wird, die in die Mittambel-Bestimmungsschaltung eingegeben werden.

8. UE nach Anspruch 7, wobei jeder Synchronisationscode auf eine vordefinierte Gruppe von Mittambeln weist, von denen eine mit jedem übertragenen Downlink-Synchronisationscode übertragen wird, um die Modulation des betreffenden übertragenen Codes anzugeben,
wobei die Mittambel-Bestimmungsschaltung einen Puffer aufweist sowie mindestens einen Mittambel-Korrelator, einen Mittambel-Generator und eine Mittambel-Entscheidungsschaltung;
wobei der Puffer einen Eingang für den Empfang von AFC-korrigierten Kommunikationssignal-Samples von der Synchronisationscode-Bestimmungsschaltung hat;
wobei der Mittambel-Generator einen Eingang für den Empfang des bestimmten Synchronisationscodes von der Synchronisationscode-Bestimmungsschaltung hat und konfiguriert ist, um auf der Grundlage der vordefinierten Gruppe von Mittambeln sequenziell Mittambeln zu erzeugen, auf die der bestimmte Synchronisationscode weist;
wobei der Mittambel-Generator einen Eingang für den Empfang von Gruppen von Kommunikationssignal-Samples vom Puffer hat, die einem Mittambel-Abschnitt eines angegebenen Zeitschlitzes entsprechen, sowie einen Eingang für den Empfang erzeugter Mittambeln vom Mittambel-Generator und einen Ausgang für die Ausgabe von Korrelationsdaten zur Mittambel-Entscheidungsschaltung; und
wobei die Mittambel-Entscheidungsschaltung konfiguriert ist, um auf der Grundlage von Korrelationsdaten zwischen Gruppen von Kommunikationssignal-Samples vom Puffer, die einem Mittambel-Abschnitt des angegebenen Zeitschlitzes entsprechen, und vom Mittambel-Generator erzeugten Mittambeln zu bestimmen, welche der Mittambeln der vordefinierten Gruppe aus Mittambeln, auf die der bestimmte Synchronisationscode weist, mit dem bestimmten Synchronisationscode übertragen wurde und einen Ausgang für die Ausgabe eines Auswahlsignals an den Mittambel-Generator hat, der wiederum einen Ausgang hat, der für die Ausgabe einer Mittambel zur Erkennungsschaltung der Phasenmodulationssequenz auf der Basis des Auswahlsignals konfiguriert ist.

9. UE nach Anspruch 8, wobei es eine Vielzahl von Mittambel-Korrelatoren gibt und die Korrelatoren in der Synchronisationscode-Bestimmungsschaltung für die Verwendung als Mittambel-Korrelatoren konfiguriert sind.

10. UE nach Anspruch 8,
wobei die Erkennungsschaltung der Phasenmodulationssequenz einen Puffer aufweist sowie Phasenkorrelatormittel und eine Phasensequenz-Entscheidungsschaltung;
wobei der Puffer der Phasensequenz-Entscheidungsschaltung einen Eingang für den Empfang von Kommunikationssignal-Samples von der Synchronisationscode-Bestimmungsschaltung hat;
wobei die Phasenkorrelatormittel konfiguriert sind, um Gruppen von Kommunikationssignal-Samples vom Puffer der Erkennungsschaltung der Phasen-

modulationssequenz zu empfangen, die Synchronisationscodeabschnitten der empfangenen Kommunikationssignal-Samples und der ausgewählten Mittambel vom Mittambel-Generator entsprechen, und um Phasenkorrelationsdaten zur Sequenz-Entscheidungsschaltung auszugeben; und
wobei die Sequenz-Entscheidungsschaltung einen Eingang für den Empfang von Phasenkorrelationsdaten von den Phasenkorrelatormitteln und einen Ausgang für die Ausgabe eines Signals hat, dass die Position der BCH-Daten identifiziert, wenn eine angegebene Phasensequenz erkannt wird.

11. UE nach Anspruch 10, wobei der Puffer in der Mittambel-Bestimmungsschaltung als Puffer der Erkennungsschaltung der Phasenmodulationssequenz verwendet wird.

12. Verfahren zur Verarbeitung empfangener Kommunikationssignal-Samples von drahtlosen Telekommunikationssignalen, die in einem Downlink-Pilotsignal-Zeitschlitz eines Time-Frame-Formats empfangen werden, wobei die empfangenen Kommunikationssignale durch eine Basisstation mit einer vorbestimmten Chip-Rate übertragen wurden und einen Synchronisationscode aufweisen, der aus einer vorbestimmten Anzahl X von Downlink-Synchronisationscodes mit jeweils Y sequenziellen Elementen ausgewählt ist, wobei X und Y ganze Zahlen größer als 15 sind, wobei die Kommunikationssignal-Samples in eine Synchronisationscode-Bestimmungsschaltung (10) mit einer Eingangs-Rate eingegeben werden, die mindestens so schnell ist wie die Chip-Rate, und in Gruppen aus jeweils Y Samples verarbeitet werden, wobei die Synchronisationscode-Bestimmungsschaltung eine Vielzahl von Korrelatoren (12_1, ..., 12_M) mit einem Eingang für den parallelen Empfang von Y Samples mit der Sample-Eingangs-Rate aufweist, sowie eine Erkennungsschaltung (12), die operativ mit den Korrelatoren verbunden ist, um positive Korrelationen von Downlink-Synchronisationscodes mit diesen Gruppen zu erkennen und zu verfolgen, wobei das Verfahren weiter Folgendes aufweist:

Verarbeitung der Kommunikationssignal-Samples in Gruppen von Y Samples durch jeden Korrelator der Vielzahl von Korrelatoren (12_1, ..., 12_M), wobei die Anzahl der Korrelatoren nicht größer als die Hälfte der Anzahl X der Downlink-Synchronisationscodes ist;
Verarbeitung der Kommunikationssignal-Sample-Gruppen in jedem Korrelator der Vielzahl von Korrelatoren (12_1, ..., 12_M) mit einer Vielzahl von parallelen angepassten Filtern in Zusammenhang mit dem Eingang des Korrelators, wobei jedes parallele angepasste Filter einen separaten Abschnitt einer Gruppe aus Y Samples zur Korrelation mit entsprechenden Abschnitten der Downlink-Synchronisationscodes mit Y sequenziellen Elementen verarbeitet; und
Ausgabe von Code-Korrelationen von jedem Korrelator der Vielzahl von Korrelatoren (12_1, ..., 12_M) für jede Gruppe von Y Samples mit einer Verarbeitungsrate, sodass mindestens zwei Synchronisationscodes der X Downlink-Synchronisationscodes mit einer Gruppe von Y Samples pro Zeitraum der Sample-Eingangs-Rate korreliert sind, wobei die Korrelatoren gemeinsam alle X Synchronisationscodes vor der Verarbeitung von weiteren Kommunikationssignal-Samples ausgeben.

13. Verfahren nach Anspruch 12, wobei die vorbestimmte Anzahl von Downlink-Synchronisationscodes, die jeweils 64 Elemente haben, 32 ist, wobei nicht mehr als 16 Korrelatoren bei der Verarbeitung von Sample-Gruppen verwendet werden, die bezüglich der Gruppen aus 64 Samples durchgeführt wird.

14. Verfahren nach Anspruch 13, wobei nicht mehr als 8 Korrelatoren bei der Verarbeitung der Sample-Gruppen verwendet werden und wobei jeder Korrelator parallel mit der Sample-Eingangs-Rate der empfangenen Kommunikationssignal-Samples empfängt und jede Gruppe von Samples mit mindestens vier Synchronisationscodes der Gruppe aus 32 Downlink-Synchronisationscodes während eines Zeitraums der Sample-Eingangs-Rate korreliert.

15. Verfahren nach Anspruch 14, wobei jeder Korrelator N angepasste Filter aufweist, die jeweils Abschnitte mit 64/N Samples von Sample-Gruppen mit entsprechenden 64/N Elementsegmenten von jedem von mindestens vier Synchronisationscodes der Gruppe aus 32 Downlink-Synchronisationscodes während eines Zeitraums der Sample-Eingangs-Rate korrelieren.

16. Verfahren nach Anspruch 15, wobei jeder Korrelator 16 angepasste Filter aufweist, wobei jedes angepasste Filter 4 Elementsegmente korreliert.

17. Verfahren nach Anspruch 13, das weiter den Empfang von Daten eines spezifizierten Broadcast Channel, BCH, aufweist, der in ausgewählten Zeitschlitzen auf einem Primary Common Control Physical Channel, P-CCPCH, getragen wird, um die bidirektionale Kommunikation mit einer Basisstation zu ermöglichen, die die BCH-Daten übertragen hat, wobei jeder übertragene Downlink-Synchronisationscode eine Modulation aufweist, die durch eine in einem vorgegebenen Zeitschlitz übertragene Mittambel angegeben wird, und wobei eine vorgegebene Modulationssequenz aufeinander folgender Downlink-Synchronisationscodes eine Position der BCH-

Daten identifiziert, wobei das Verfahren weiter Folgendes aufweist:

Bestimmung einer entsprechenden übertragenen Mittambel auf der Grundlage einer relativen Position und Identität eines erkannten Downlink-Synchronisationscodes; und
Bestimmung von Sequenzen der Phasenmodulation von aufeinander folgenden erkannten Downlink-Synchronisationscodes auf der Grundlage von erkannten Downlink-Synchronisationscodes und einer bestimmten Mittambel.

18. Verfahren nach Anspruch 17, das weiter Folgendes aufweist:

Verwendung einer Rauschschätzschaltung zur Erzeugung einer Störgeräuschschätzung, auf der die Erkennung des Synchronisationscodes basiert; und
Verwendung einer automatischen Frequenzregelschaltung zur Erzeugung eines Frequenzkorrektursignals, das vor der Korrelation mit empfangenen Kommunikations-Samples gemischt wird.

Revendications

1. Un Terminal Utilisateur, TU, adapté à recevoir des signaux de télécommunication sans fil dans un créneau pilote de liaison descendante au format de trame temporelle et à échantillonner les signaux de communication reçus afin de produire des échantillons de signaux de communication, les signaux de communication ayant été transmis par une station de base à un débit d'éléments prédéterminé et comprenant un code de synchronisation sélectionné à partir d'un nombre X prédéterminé de codes de synchronisation de liaison descendante, chacun possédant Y éléments séquentiels, X et Y étant des nombres entiers supérieurs à 15, le TU consistant en :

un circuit de synchronisation (10, 20, 30) pour le traitement des échantillons de signaux de communication ;
ledit circuit de synchronisation ayant un circuit de détermination du code de synchronisation (10) adapté à recevoir les échantillons de signaux de communication à un débit d'entrée des échantillons qui soit au moins aussi rapide que le débit d'éléments, et à traiter les échantillons de signaux de communication regroupés en ensembles, chaque ensemble étant composé de Y échantillons ;
ledit circuit de détermination du code de synchronisation comprenant :

une pluralité de corrélateurs (12_1, ...12_M) ayant une entrée pour recevoir en parallèle Y échantillons au débit d'entrée des échantillons ; et
un circuit de détection (13) relié fonctionnellement auxdits corrélateurs afin de détecter et de retracer les corrélations positives des codes de synchronisation de liaison descendante avec lesdits ensembles, **caractérisé en ce que**
le nombre desdits corrélateurs (12_1, ...12_M) n'est pas supérieur à la moitié du nombre X desdits codes de synchronisation de liaison descendante ;
chacun desdits corrélateurs (12_1, ...12_M) comprend une pluralité de filtres adaptés en parallèle associés à l'entrée du corrélateur, et chacun desdits filtres adaptés en parallèle est approprié pour traiter un segment distinct d'un ensemble de Y échantillons afin d'établir une corrélation avec les segments respectifs des codes de synchronisation de liaison descendante ayant Y éléments séquentiels ; et
chacun desdits corrélateurs (12_1, ...12_M) possède une sortie permettant de transmettre des corrélations de code pour chaque ensemble de Y échantillons à une vitesse de traitement telle qu'au moins deux codes de synchronisation desdits X codes de synchronisation de liaison descendante soient mis en corrélation avec un ensemble de Y échantillons par période de débit d'entrée des échantillons, tandis que, collectivement, lesdits corrélateurs sont configurés pour transmettre au dit circuit de détection lesdites corrélations de code pour tous les X codes de synchronisation avant de traiter d'autres échantillons de signaux de communication.

2. Le TU selon la revendication 1, **caractérisé en ce que** le nombre X prédéterminé de codes de synchronisation de liaison descendante est de 32, chacun ayant 64 éléments séquentiels, et il n'existe pas plus de 16 corrélateurs, chacun configuré pour mettre en corrélation des ensembles de 64 échantillons, dans ledit circuit de détermination du code de synchronisation.

3. Le TU selon la revendication 2, **caractérisé en ce qu'**il n'existe pas plus de 8 corrélateurs dans ledit circuit de détermination du code de synchronisation et chaque corrélateur est configuré pour mettre en corrélation chaque ensemble de 64 échantillons avec au moins quatre codes de synchronisation de l'ensemble de 32 codes de synchronisation de liaison descendante durant une période de débit

d'entrée des échantillons.

4. Le TU selon la revendication 3, **caractérisé en ce que** chaque corrélateur dans ledit circuit de détermination du code de synchronisation comprend N filtres adaptés, chacun d'entre eux étant configuré pour mettre en corrélation des segments ayant 64/N éléments de chaque ensemble de 64 échantillons avec les segments correspondants ayant 64/N éléments de chacun d'au moins quatre codes de synchronisation de l'ensemble de 32 codes de synchronisation de liaison descendante durant une période de débit d'entrée des échantillons.

5. Le TU selon la revendication 4, **caractérisé en ce que** chaque corrélateur dans ledit circuit de détermination du code de synchronisation comprend seize filtres adaptés, chacun d'entre eux étant configuré pour mettre en corrélation quatre segments d'éléments.

6. Le TU selon la revendication 2, configuré pour recevoir des données d'un canal de diffusion spécifique, BCH, qui est supporté par un canal physique de contrôle commun primaire, P-CCPCH, dans des créneaux sélectionnés au format de trame temporelle afin de permettre au TU de poursuivre une communication bidirectionnelle avec une station de base qui a transmis les données du BCH, tandis que chaque code de synchronisation de liaison descendante transmis possède une modulation qui est indiquée par un midambule transmis dans un créneau temporel spécifique et qu'une séquence de modulation spécifique de codes de synchronisation de liaison descendante consécutifs identifie un emplacement des données du BCH, le TU consistant en outre en :

un circuit de détermination du midambule (20) relié fonctionnellement au circuit de détermination du code de synchronisation (10) afin de déterminer le midambule respectif transmis sur la base d'un emplacement relatif et d'identifier le code de synchronisation de liaison descendante détecté ; et
un circuit de détection de la séquence de modulation de phase (30) relié fonctionnellement au circuit de détermination du midambule (20) et au circuit de détermination du code de synchronisation (10) afin de déterminer les séquences de modulation de phase des codes de synchronisation de liaison descendante consécutifs détectés, sur la base de codes de synchronisation de liaison descendante détectés par le circuit de détermination du code de synchronisation et le midambule déterminé par le circuit de détermination du midambule.

7. Le TU selon la revendication 6, **caractérisé en ce que :**

ledit circuit de détermination du code de synchronisation comprend un circuit d'estimation de bruit et un circuit de commande automatique de fréquence, CAF, relié au circuit de détection du circuit de détermination du code de synchronisation (13) ;
le circuit d'estimation de bruit est configuré de sorte à fournir au circuit de détection du circuit de détermination du code de synchronisation (13) une estimation de bruit sur laquelle se base la détection du code de synchronisation ; et
le circuit de détection du circuit de détermination du code de synchronisation (13) est configuré de sorte à commander ladite CAF à produire un signal de correction de fréquence qui est mêlé aux échantillons de communication reçus entrés dans ledit circuit de détermination du midambule.

8. Le TU selon la revendication 7, **caractérisé en ce que** chaque code de synchronisation relève d'un ensemble prédéfini de midambules à partir desquels l'un est transmis avec chaque code de synchronisation de liaison descendante transmis, pour indiquer la modulation de ce code transmis, tandis que :

le circuit de détermination du midambule comprend une mémoire tampon, au moins un corrélateur de midambule, un générateur de midambule et un circuit de décision de midambule ;
la mémoire tampon possède une entrée pour recevoir dudit circuit de détermination du code de synchronisation des échantillons de signaux de communication corrigés par la CAF ;
le générateur de midambule possède une entrée pour recevoir dudit circuit de détermination du code de synchronisation le code de synchronisation déterminé et est configuré pour générer séquentiellement des midambules sur la base de l'ensemble prédéfini de midambules dont relève le code de synchronisation déterminé ;
le corrélateur de midambule possède une entrée pour recevoir de ladite mémoire tampon des ensembles d'échantillons de signaux de communication, correspondant à une fraction de midambule d'un créneau temporel spécifique, une entrée pour recevoir du générateur de midambule les midambules générés et une sortie pour transmettre les données de corrélation au circuit de décision de midambule ; et
le circuit de décision de midambule est configuré de sorte à déterminer lequel des midambules de l'ensemble prédéfini de midambules dont relève le code de synchronisation déterminé a été transmis avec le code de synchronisation déter-

miné sur la base des données de corrélation entre des ensembles d'échantillons de signaux de communication de ladite mémoire tampon correspondant à une fraction de midambule du créneau temporel spécifique et les midambules générés par le générateur de midambule, et possède une sortie pour transmettre un signal de sélection au dit générateur de midambule qui, à son tour, possède une sortie configurée pour transmettre un midambule basé sur le signal de sélection au circuit de détection de la séquence de modulation de phase.

9. Le TU selon la revendication 8, **caractérisé en ce qu'**il existe une pluralité de corrélateurs de midambule et les corrélateurs dans ledit circuit de détermination du code de synchronisation sont configurés pour fonctionner comme corrélateurs de midambule.

10. Le TU selon la revendication 8, **caractérisé en ce que :**

le circuit de détection de la séquence de modulation de phase comprend une mémoire tampon, un dispositif de corrélation de phase et un circuit de décision de séquence de phase ;
la mémoire tampon du circuit de détection de la séquence de modulation de phase possède une entrée pour recevoir dudit circuit de détermination du code de synchronisation des échantillons de signaux de communication ;
le dispositif de corrélation de phase est configuré pour recevoir de ladite mémoire tampon du circuit de détection de la séquence de modulation de phase des ensembles d'échantillons de signaux de communication, correspondant à des fractions de code de synchronisation des échantillons de signaux de communication reçus et du midambule sélectionné venant du générateur de midambule, et pour transmettre des données de corrélation de phase au circuit de décision de séquence ; et
le circuit de décision de séquence possède une entrée pour recevoir du dispositif de corrélation de phase des données de corrélation de phase et possède une sortie pour transmettre un signal identifiant l'emplacement des données du BCH lorsqu'une séquence de phase spécifique est détectée.

11. Le TU selon la revendication 10, **caractérisé en ce que** la mémoire tampon dans ledit circuit de détermination du midambule fonctionne comme la mémoire tampon du circuit de détection de la séquence de modulation de phase.

12. Un procédé de traitement d'échantillons de signaux de communication reçus de signaux de télécommunication sans fil reçus dans un créneau pilote de liaison descendante au format de trame temporelle, les signaux de communication reçus ayant été transmis par une station de base à un débit d'éléments prédéterminé et comprenant un code de synchronisation sélectionné à partir d'un nombre X prédéterminé de codes de synchronisation de liaison descendante, chacun possédant Y éléments séquentiels, X et Y étant des nombres entiers supérieurs à 15, **caractérisé en ce que** les échantillons de signaux de communication sont envoyés dans un circuit de détermination du code de synchronisation (10) à un débit d'entrée des échantillons qui soit au moins aussi rapide que le débit d'éléments, et sont regroupés en ensembles, chaque ensemble étant composé de Y échantillons, ledit circuit de détermination du code de synchronisation comprenant une pluralité de corrélateurs (12_1, ...12_M) ayant une entrée pour recevoir en parallèle Y échantillons au débit d'entrée des échantillons, et un circuit de détection (12) relié fonctionnellement auxdits corrélateurs afin de détecter et de retracer les corrélations positives des codes de synchronisation de liaison descendante avec lesdits ensembles, le procédé consistant en outre en :

le traitement des échantillons de signaux de communication, regroupés en ensembles de Y échantillons, par chacun de ladite pluralité de corrélateurs (12_1, ...12_M), le nombre de corrélateurs n'étant pas supérieur à la moitié du nombre X desdits codes de synchronisation de liaison descendante ;
le traitement des ensembles d'échantillons de signaux de communication dans chacun de ladite pluralité de corrélateurs (12_1, ...12_M) avec une pluralité de filtres adaptés en parallèle associés à l'entrée du corrélateur, chacun desdits filtres adaptés en parallèle traitant un segment distinct d'un ensemble de Y échantillons afin d'établir une corrélation avec les segments respectifs des codes de synchronisation de liaison descendante possédant Y éléments séquentiels ; et
la transmission depuis chacun de ladite pluralité de corrélateurs (12_1, ...12_M) de corrélations de code pour chaque ensemble de Y échantillons à une vitesse de traitement telle qu'au moins deux codes de synchronisation desdits X codes de synchronisation de liaison descendante soient mis en corrélation avec un ensemble de Y échantillons par période de débit d'entrée des échantillons, tandis que, collectivement, lesdits corrélateurs transmettent au dit circuit de détection lesdites corrélations de code pour tous les X codes de synchronisation avant de traiter d'autres échantillons de signaux de communication.

13. Le procédé selon la revendication 12, **caractérisé en ce que** le nombre prédéterminé de codes de synchronisation de liaison descendante est de 32, chacun ayant 64 éléments, tandis que pas plus de 16 corrélateurs sont utilisés dans ledit traitement d'ensembles d'échantillons effectué par rapport aux ensembles de 64 échantillons.

14. Le procédé selon la revendication 13, **caractérisé en ce que** pas plus de 8 corrélateurs sont utilisés dans ledit traitement d'ensembles d'échantillons et chaque corrélateur reçoit en parallèle, au débit d'entrée des échantillons, les échantillons de signaux de communication reçus et met en corrélation chaque ensemble d'échantillons avec au moins quatre codes de synchronisation de l'ensemble de 32 codes de synchronisation de liaison descendante durant une période de débit d'entrée des échantillons.

15. Le procédé selon la revendication 14, **caractérisé en ce que** chaque corrélateur comprend N filtres adaptés, chacun d'entre eux mettant en corrélation des segments ayant 64/N échantillons d'ensembles d'échantillons avec les segments correspondants ayant 64/N éléments de chacun d'au moins quatre codes de synchronisation de l'ensemble de 32 codes de synchronisation de liaison descendante durant une période de débit d'entrée des échantillons.

16. Le procédé selon la revendication 15, **caractérisé en ce que** chaque corrélateur comprend seize filtres adaptés, chacun d'entre eux mettant en corrélation quatre segments d'éléments.

17. Le procédé selon la revendication 13, consistant en outre en la réception de données d'un canal de diffusion spécifique, BCH, qui est supporté par un canal physique de contrôle commun primaire, P-CCPCH, dans des créneaux temporels sélectionnés afin de permettre une communication bidirectionnelle avec une station de base qui a transmis les données du BCH, tandis que chaque code de synchronisation de liaison descendante transmis possède une modulation qui est indiquée par un midambule transmis dans un créneau temporel spécifique et qu'une séquence de modulation spécifique de codes de synchronisation de liaison descendante consécutifs identifie un emplacement des données du BCH, le procédé consistant en outre en :

la détermination d'un midambule respectif transmis sur la base d'un emplacement relatif et l'identification d'un code de synchronisation de liaison descendante détecté ; et

la détermination de séquences de modulation de phase de codes de synchronisation de liaison descendante consécutifs détectés, sur la base de codes de synchronisation de liaison descendante détectés et un midambule déterminé.

18. Le procédé selon la revendication 17, consistant en outre en :

l'utilisation d'un circuit d'estimation de bruit afin de générer une estimation de bruit sur laquelle se base la détection du code de synchronisation ; et

l'utilisation d'un circuit de commande automatique de fréquence, CAF, afin de produire un signal de correction de fréquence qui est mêlé aux échantillons de communication reçus préalablement à ladite corrélation.

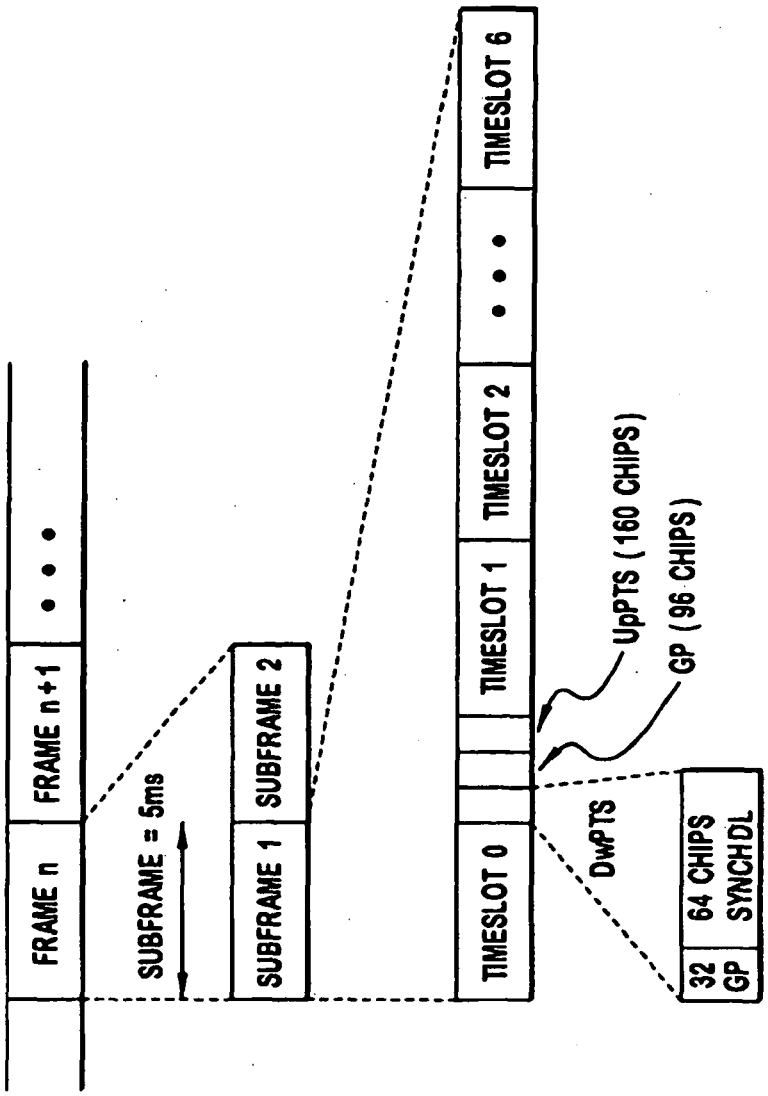

FIG. 1
PRIOR ART

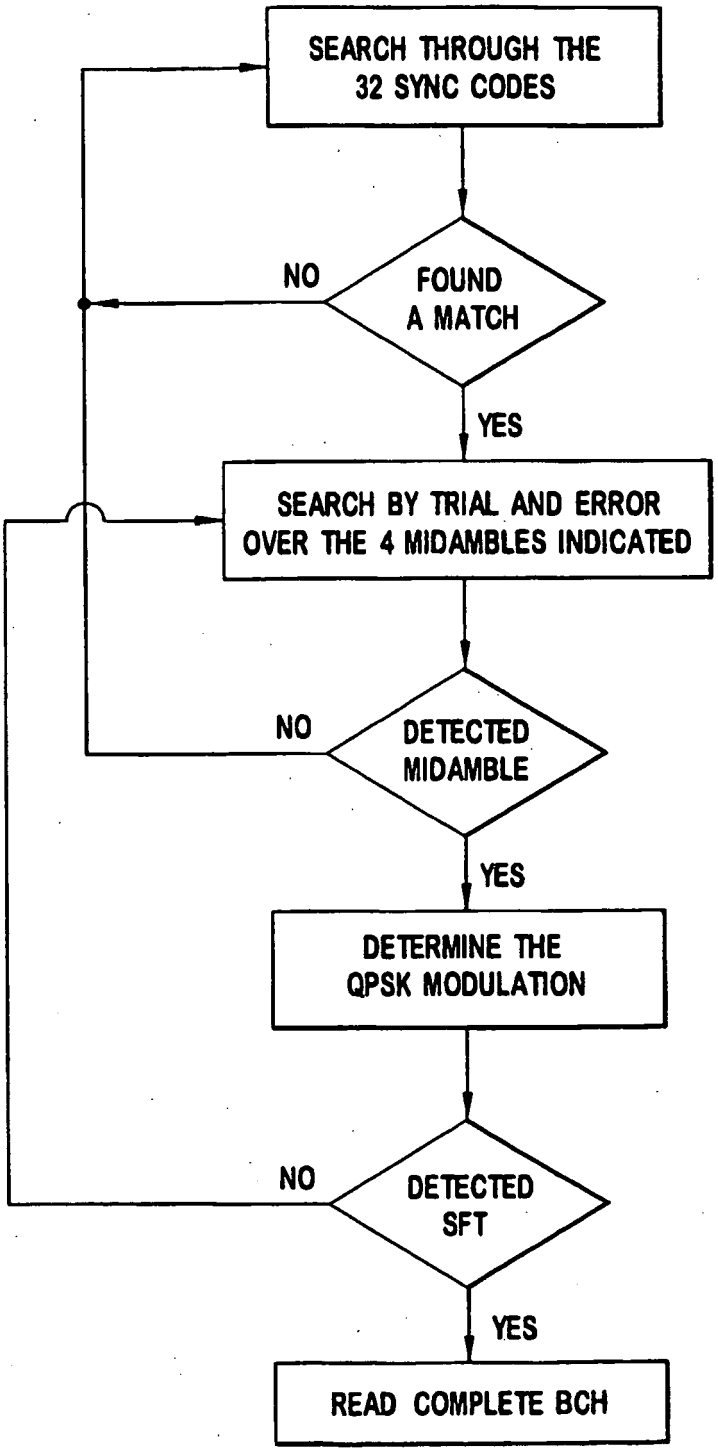

FIG. 2
PRIOR ART

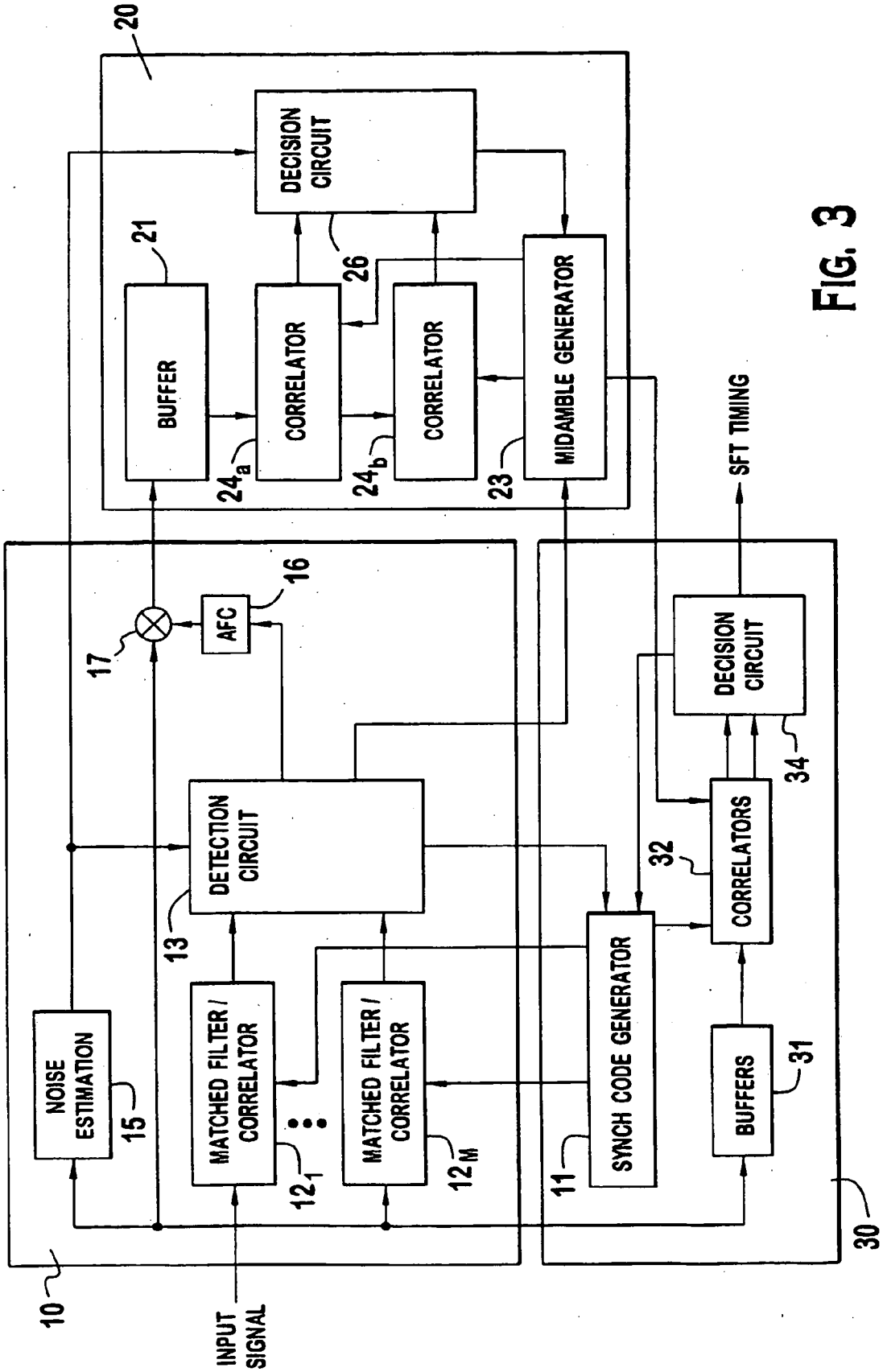
20
DECISION CIRCUIT
21
BUFFER
CORRELATOR
CORRELATOR
MIDAMBLE GENERATOR
26
24a
24b
23
SFT TIMING
16
AFC
17
DECISION CIRCUIT
34
DETECTION CIRCUIT
13
32
CORRELATORS
NOISE ESTIMATION
15
MATCHED FILTER / CORRELATOR
MATCHED FILTER / CORRELATOR
121
12M
SYNCH CODE GENERATOR
11
BUFFERS
31
30
10
INPUT SIGNAL

FIG. 3

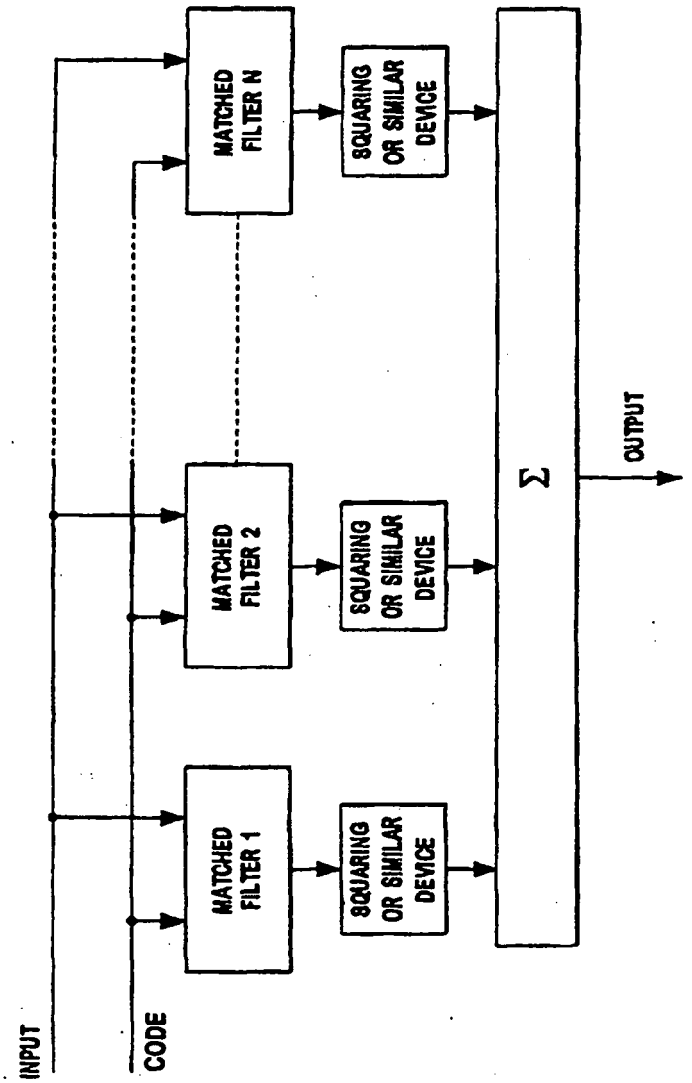
INPUT
CODE
MATCHED FILTER 1
MATCHED FILTER 2
MATCHED FILTER N
SQUARING OR SIMILAR DEVICE
SQUARING OR SIMILAR DEVICE
SQUARING OR SIMILAR DEVICE
Σ
OUTPUT

FIG. 4

REFERENCES CITED IN THE DESCRIPTION

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- EP 0924868 A **[0013]**