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(54) **Electrically erasable programmable logic device**

(57) An electrically erasable programmable logic device (EEPLD) (100) includes a P type semiconductor substrate. An N type well (110) is formed on the P type semiconductor substrate. A first PMOS transistor (101) is formed on the N well (110). The first PMOS transistor (101) comprises a floating gate (122), a first P<sup>+</sup> doped region (132) serving as a drain of the first PMOS transistor (101), and a P<sup>-</sup> doped region (140) encompassing

an N<sup>+</sup> doped region (134) for erasing the first PMOS transistor (101). A second PMOS transistor (102) is also formed on the N well (110) and serially connected to the first PMOS transistor (101). The first P<sup>+</sup> doped region (132) functions as a source of the second PMOS transistor (102), and the second PMOS transistor (102) further comprises a select gate (124) and a second P<sup>+</sup> doped region (136) serving as a drain of the second PMOS transistor (102).

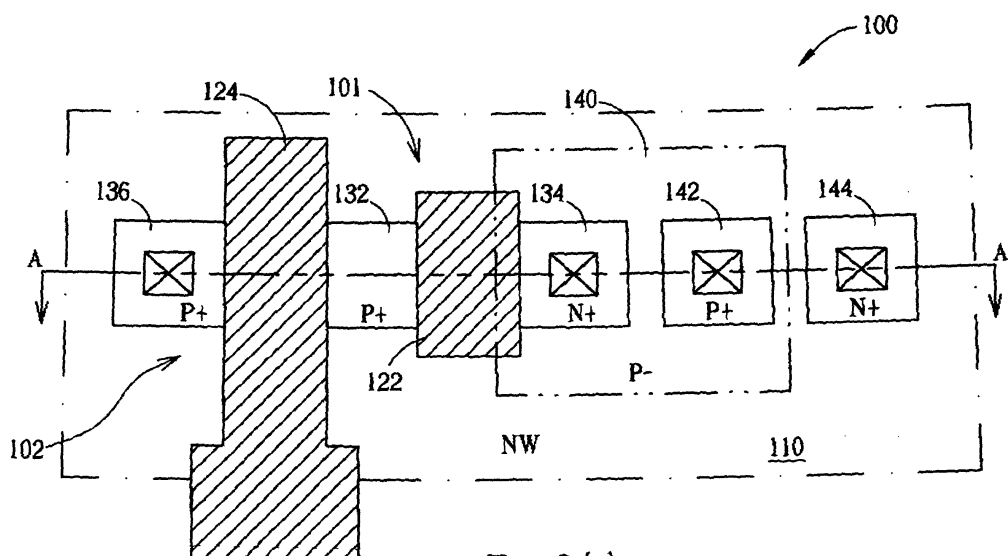


Fig. 2 (a)

## Description

**[0001]** The present invention relates to a single-poly electrically erasable programmable logic device (EEPLD) according to the pre-characterizing clause of claim 1.

**[0002]** Electronic memory comes in a variety of forms to serve a variety of purposes. Flash electrically erasable programmable read only memory (flash EEPROM) is used for easy and fast information storage in such devices as personal digital assistants (PDA), digital cameras and home video game consoles. Generally, an EEPROM chip has a grid of columns and rows with a cell that has two transistors at each intersection. One of the transistors is known as a floating gate, and the other one is the control gate. The floating gate's only link to the row, or word line, is through the control gate. As long as this link is in place, the cell has a value of 1. Changing the value to a 0 requires a well-known process called Fowler-Nordheim tunneling. It is often desirable to combine many functions on a single device, also referred to as system-on-a-chip (SOC), to reduce the number and cost of chips. Embedding flash memory in a CMOS device allows a single chip produced by a manufacturer to be configured for a variety of applications, and/or allows a single device to be configured by a user for different applications. To combine with standard CMOS process flow, single-poly flash memory devices have been developed.

**[0003]** However, the conventional flash memory architecture has a drawback in that it consumes a lot of chip area since it is typically composed of a PMOS and a NMOS, thus more costly. In addition, an extra field oxide layer is needed for isolating the PMOS from the NMOS. Furthermore, the prior art flash memory needs an extra channel stop region and formation of conductor for connecting two gates. This, in turns, means extra process steps and thus raised cost.

**[0004]** This in mind, the present invention aims at providing a corresponding high-density single-poly memory device that consumes small per unit chip area. The single-poly memory device of this invention, which is capable of implementing low-voltage data writing through a channel hot electron injection (CHEI) mechanism, can be operated under a relatively low voltage. Another object of the claimed invention is to provide a high-density single-poly EEPROM device which is power saving and can be fabricated with a conventional CMOS process. The single-poly EEPROM according to this invention, which is compatible with standard CMOS fabrication processes and is thus suited for system-on-a-chip (SOC) field, has the advantages of low power consumption, high write/erase efficiency, and high packing density.

**[0005]** These objectives are achieved by an electrically erasable programmable logic device (EEPLD) according to claim 1. The dependent claims pertain to corresponding further developments and improvements.

**[0006]** As will be seen more clearly from the detailed description following below, the electrically erasable programmable logic device (EEPLD) is disposed in a P type semiconductor substrate. An N type well is formed on the P type semiconductor substrate. A first PMOS transistor is formed on the N well. The first PMOS transistor comprises a floating gate, a first P<sup>+</sup> doped region serving as a drain of the first PMOS transistor, and a P<sup>+</sup> doped region, which serves as a source of the first PMOS transistor, encompassing an N<sup>+</sup> doped region for erasing the first PMOS transistor. A second PMOS transistor is also formed on the N well and serially connected to the first PMOS transistor. The first P<sup>+</sup> doped region functions as a source of the second PMOS transistor, and the second PMOS transistor further comprises a select gate and a second P<sup>+</sup> doped region serving as a drain of the second PMOS transistor. The EEPLD according to this invention utilizes channel hot electron injection to carry out a data write operation, while using a Band-to-Band tunneling hot hole injection to carry out a data erase operation.

**[0007]** In the following, the invention is further illustrated by way of example, taking reference to the accompanying drawings. Thereof

Fig.1 is a simplified cross section of an EEPLD cell according to the prior art.

Fig.2(a) is a plane view schematically illustrating a partial layout of the EEPLD according to one preferred embodiment of this invention.

Fig.2(b) is a schematic cross-sectional view of the EEPLD of Fig.2(a) along line AA'.

Fig.3 is a cross-sectional diagram schematically illustrating the writing operation on a selected EERLD unit according to one preferred embodiment of this invention.

Fig.4 plots the gate currents versus gate voltages of the floating gate regarding a PMOS transistor at different drain to N-well biases ( $V_d = V_1 - V_5$ ).

Fig.5 is a cross-sectional diagram schematically illustrating an erase operation on a selected EERLD unit according to one preferred embodiment of this invention.

Fig.6 is a cross-sectional diagram schematically illustrating a read operation on a selected EERLD unit according to one preferred embodiment of this invention.

**[0008]** Fig.1 is a schematic, cross-sectional view of a prior art single-poly EEPLD cell 10. The EEPLD cell 10 comprises an NMOS structure 28 and a PMOS structure 30. A field oxide layer 24 isolates the PMOS structure 30 from the NMOS structure 28. The NMOS structure 28 is formed on a P-type substrate 12 and comprises an NMOS gate 32, an N<sup>+</sup> source region 14, and an N<sup>+</sup> drain region 16. The PMOS structure 30 is formed on an N-well 18 and comprises a PMOS floating gate 34, a P<sup>+</sup> source region 20, and a P<sup>+</sup> drain region 22. A chan-

nel stop region 38 is obliquely implanted underneath the PMOS floating gate 34 for facilitating band-to-band hot electron injection into the PMOS floating gate. A conductor 36 directly electrically couples the NMOS gate 32 to the PMOS floating gate 34. That is, there is a conductive current path from one gate to the other, as opposed to indirectly coupling, such as capacitively coupling. Both gates 32 and 34 are floating, that is, they are not directly electrically coupled to a voltage or current source or sink on the IC, and are at the same electrical potential. The conductor may be a polysilicon trace formed at the same time as the gates, or may be a metal or silicide conductor formed later in the fabrication sequence.

**[0009]** As mentioned, the above described prior art EEPLD cell 10 suffers from several drawbacks. First, the prior art EEPLD cell 10 consumes a lot of chip area since it is composed of a PMOS structure 30 and a NMOS structure 28, and the extra field oxide layer 24 is needed for isolating the PMOS 30 from the NMOS 28. Second, the prior art EEPLD cell 10 needs an extra channel stop region 38 and formation of conductor 36 for connecting two gates. This, in turns, means extra process steps and thus raised cost.

**[0010]** Fig.2(a) is a plane view schematically illustrating a partial layout of the EEPLD 100 according to one preferred embodiment of this invention. Fig.2(b) is a schematic cross-sectional view of the EEPLD 100 of Fig.2(a) along line AA'. As shown in Fig.2 (a), a single-poly EEPLD unit 100 comprises a PMOS transistor 101 and a PMOS transistor 102 serially connected to the PMOS transistor 101. The PMOS transistor 101 and the PMOS transistor 102 are formed on an N-well 110. The PMOS transistor 101, which is a floating gate transistor, comprises a floating gate 122, a P<sup>+</sup> doped drain region 132 at one side of the floating gate 122, and an N<sup>+</sup> doped region 134 at the opposite side of the floating gate 122. The floating gate 122 is formed only on the N-well region and not formed over any field oxide layer region that has P-type and a dopant concentration greater than a dopant concentration of the well region. The N<sup>+</sup> doped region 134, which is formed within a P<sup>-</sup> doped region 140, is primarily used to erase data stored in the floating gate 122. As specifically indicated in Fig.2(a), the P<sup>-</sup> doped region 140 partially overlaps with the overlying floating gate 122, which may be done by using oblique ion implantation or thermal drive-in technique known in the art. It is understood that the floating gate 122 consists of a single layer polysilicon according to the present invention, that is, there is no word line or control electrode stacked thereon. A P<sup>+</sup> doped region 142, through which a source line voltage is applied to the subjacent P<sup>-</sup> doped region 140, is formed within the P<sup>-</sup> doped region 140 and is isolated from the adjacent N<sup>+</sup> doped region 134 with an field oxide layer 150 or the like. By commonly using the P<sup>+</sup> doped region 132, the PMOS transistors 101 and 102 are serially connected to each other. The PMOS transistor 102 comprises a select gate 124, the

P<sup>+</sup> doped region 132, and a P<sup>+</sup> doped region 136. The select gate 124 is electrically connected to a word line (not explicitly shown). The P<sup>+</sup> doped region 132 functions as a drain of the PMOS transistor 101 and also a source of the PMOS transistor 102. In one case, a salicide layer may be optionally formed on the P<sup>+</sup> doped region 142, the N<sup>+</sup> doped region 134, and the P<sup>+</sup> doped region 136.

**[0011]** In Fig.2(b), the PMOS transistor 101 further comprises a floating gate oxide layer 122a interposed between the floating gate 122 and the substrate. The PMOS transistor 102 further comprises a gate oxide layer 124a underneath the select gate thereof. The P<sup>+</sup> doped region 136 of the PMOS transistor 102 is electrically connected with a bit line through a contact plug formed in an inter layer dielectric (ILD) film 162 for providing the EEPLD unit 100 with a bit line voltage ( $V_1$ ). The bit line is typically defined over the dielectric film 162. In the preferred embodiment of the present invention, since the EEPLD unit 100 is operated at low operation voltages, the thickness of the floating oxide layer 122a, the thickness of the gate oxide layer 124a, and the thickness of gate oxide layer fabricated in a logic circuit area are the same. However, extra thermal processes may be carried out to increase the thickness of the floating gate oxide layer 122a or the thickness of the gate oxide layer 124a. In either case, the simplified EEP-ROM device of this invention can be combined with standard CMOS semiconductor processes.

**[0012]** Fig.3 is a cross-sectional diagram schematically demonstrating the writing operation on a selected EEPRLD unit according to one preferred embodiment of this invention. As shown in Fig. 3, by way of example, in a data write operation, a bit line voltage  $V_1$  of 0V is applied to the P<sup>+</sup> doped drain region of the PMOS transistor 102. A word line voltage  $V_2$ , which is preferably a voltage value lower than the bit line voltage  $V_1$  by at least one threshold voltage ( $V_{TH}$ ) in magnitude, for example,  $V_2 = -2V$ , is applied to the select gate 124 of the PMOS transistor 102, thereby conducting a P channel thereof. Once the P channel under the select gate 124 is conducted, the P<sup>+</sup> doped drain region 136 and the P<sup>+</sup> doped region 132 are in a condition of the same voltage level, that is, 0V, according to the preferred embodiment. A well voltage  $V_5$  of 5V is applied to the N well 110. The floating gate 122 of the PMOS transistor 101 is kept in a floating status. To keep the P<sup>-</sup> doped region 140 at a voltage level same as the N well 110, an erase voltage  $V_3$  of 5V and a source line voltage  $V_4$  of 5V are applied to the N<sup>+</sup> doped region 134 and the P<sup>+</sup> doped region 142, respectively, within the P<sup>-</sup> doped region 140. Under the above described conditions, a coupling voltage of about 3~4V will be induced at the floating gate 122 due to capacitive coupling effect, thereby turning on a P channel under the floating gate 122. Hot carriers such as electrons created by collisions are accelerated by electric field of a depletion region and surmount the energy barrier of the floating gate oxide layer 122a and are

finally trapped inside the floating gate 122.

**[0013]** Please refer to Fig.4 with reference to Fig.3, where Fig.4 plots the gate currents versus gate voltages of the PMOS at different drain to N-well 110 biases ( $V_d = V_1 - V_5$ ). As shown in Fig.4, at a drain voltage bias  $V_d = -5V$ , for example, the PMOS gate 122 acquires a relatively low-level coupling voltage of about  $-1 \sim -2V$ . At the same time, the P channel is just turned on and reaches a gate current approaching a maximum value of about  $5 \times 10^{-11} \text{ A}/\mu\text{m}$ . In other words, it is clear that a better performance during the writing operation can be achieved according to the present invention, since the gate current to drain current ratio ( $I_g/I_d$ ) is improved.

**[0014]** Fig.5 is a cross-sectional diagram schematically demonstrating the data erase operation on an EE-RLD unit according to one preferred embodiment of this invention. As shown in Fig. 5, by way of example, in a data erase operation, a bit line voltage  $V_1$  of  $0V$  is applied to the  $P^+$  doped drain region 136 of the PMOS transistor 102. A word line voltage  $V_2$  of  $0V$  is applied to the select gate 124 of the PMOS transistor 102 to turn off the P channel thereof. A well voltage  $V_5$  of  $0V$  is applied to the N well 110. The floating gate 122 of the PMOS transistor 101 is kept in a floating status. An erase voltage  $V_3$  of  $5V$  and a source line voltage  $V_4$  of  $-3V$  are applied to the  $N^+$  doped region 134 and the  $P^+$  doped region 142, respectively. Under the above-described voltage conditions, a depletion region is generated due to the bias between the  $N^+$  doped region 134 and the  $P^+$  doped region 142. Holes of the electron-hole pairs created in the depletion region may gain sufficient energy to overcome the energy barrier of the floating gate oxide 122a and thus tunnel into the floating gate 122 by a so-called Band-to-Band tunneling (BTBT) mechanism, and thereby neutralizing the electrons trapped in the floating gate 122.

**[0015]** Fig.6 is a cross-sectional diagram schematically demonstrating the data read operation on an EE-RLD unit according to one preferred embodiment of this invention. In a data read operation, a bit line voltage  $V_1 = V_{DD} - V_x$  (where  $V_x$  is a bit line to source line cross voltage of a value that is greater than  $0V$ ) is applied to the  $P^+$  doped drain region 136 of the PMOS transistor 102. A word line voltage  $V_2$  of  $0V$  is applied to the select gate 124 of the PMOS transistor 102 to turn on the P channel thereof. A well voltage  $V_5 = V_{DD}$  is applied to the N well 110. The floating gate 122 of the PMOS transistor 101 is kept in a floating status. An erase voltage  $V_3 = V_{DD}$  and a source line voltage  $V_4 = V_{DD}$  are applied to the  $N^+$  doped region 134 and the  $P^+$  doped region 142, respectively.

**[0016]** To sum up, the EEPLD of the present invention can be operated at low voltages and can thus achieve the goal of saving energy. The unique design allows a greater gate current to drain current ratio ( $I_g/I_d$ ), which means improved performance, higher data writing efficiency, and lower power dissipation. A gate current ( $I_g$ ) approaching a maximum current is achieved right on the

opening or turning on of the PMOS transistor. The  $N^+$  doped region 134, which allows the EEPLD unit to carry out efficient BTBT data erase operations, is also unique. Further, the serially connected PMOS transistors save a great deal of valuable chip area. Moreover, the single-poly EEPROM structure according to the present invention is capable of being combined with standard CMOS fabrication processes and is particularly suited for SOC fields.

**[0017]** Those skilled in the art will readily observe that numerous modification and alterations of the device may be made while retaining the teachings of the invention. For example, the electrically erasable programmable logic device may be configured as a Multiple-Time Programming (MTP) memory device, an element of a capacitor trimming circuit, an element of a resistor trimming circuit, an element of a memory redundancy circuit, or an element of an electrical fuse circuit. Accordingly, the above disclosure should be construed as limited only by the metes and bounds of the appended claims.

## Claims

1. An electrically erasable programmable logic device (EEPLD) (100) formed in a semiconductor substrate, the EEPLD (100) having an individual word line, a bit line, a source line, an erase line and a well contact, the EEPLD comprising:

a second conductivity type well (110) disposed in the semiconductor substrate, the well being electrically connected to the well contact;  
 a first source region of a first conductivity type (140) formed in the well region (110), the first source region (140) being electrically connected to the source line;  
 an erase region of the second conductivity type (134) formed in the first source region (140), the erase region (134) being electrically connected to the erase line;  
 a first drain region of the first conductivity type (132) formed in the well region (110);  
 a first channel region defined between the first drain region (132) and the erase region (134);  
 a floating gate (122) formed over the first channel region;  
 a second source region of the first conductivity type (132) formed in the well region (110);  
 a second drain region of the first conductivity type (136) formed in the well region (110), the second drain region (136) being electrically connected to the bit line;  
 a second channel region defined between the second source region (132) and the second drain region (136); and  
 a gate (124) formed over the second channel

region, the gate (124) being electrically connected to the word line.

2. The electrically erasable programmable logic device (100) of claim 1 wherein the floating gate (122) and the gate (124) are substantially in the same plane. 5
3. The electrically erasable programmable logic device (100) of claim 1 wherein the first drain region (132) and the second source region (132) are merged into a contiguous region. 10
4. The electrically erasable programmable logic device (100) of claim 1 acts as an element of a memory array. 15
5. The electrically erasable programmable logic device (100) of claim 1 wherein the second conductivity type is N-type. 20
6. The electrically erasable programmable logic device (100) of claim 1 wherein, in operation, a bit line voltage  $V_1$ , a word line voltage  $V_2$ , a source line voltage  $V_3$ , well voltage  $V_4$  and an erase line voltage  $V_5$  are applied on the electrically erasable programmable logic device (100), the floating gate (122) is induced a voltage due to capacitive coupling effect, thereby causing channel carriers injected into the floating gate (122) due to channel electric field. 25 30
7. The electrically erasable programmable logic device (100) of claim 6 wherein  $V_1$  is 0V or a negative voltage. 35
8. The electrically erasable programmable logic device (100) of claim 6 wherein  $V_2$  is a negative voltage, the negative voltage being larger than  $V_1$  in magnitude. 40
9. The electrically erasable programmable logic device (100) of claim 6 wherein  $V_3$  ranges from 5V to 10V. 45
10. The electrically erasable programmable logic device (100) of claim 6 wherein  $V_4$  ranges from 5V to 10V. 50
11. The electrically erasable programmable logic device (100) of claim 6 wherein  $V_5$  ranges from 5V to 10V. 55
12. The electrically erasable programmable logic device (100) of claim 6 wherein the operation is a programming operation.
13. The electrically erasable programmable logic device (100) of claim 1 wherein when applying a bit

line voltage  $V_1'$ , a word line voltage  $V_2'$ , a source line voltage  $V_3'$ , well voltage  $V_4'$  and an erase line voltage  $V_5'$  on the electrically erasable programmable logic device (100), a junction of the erase region (134) and the first source line region under the floating gate (122) is induced a reverse voltage and thereby induces hole injection into the floating gate (122).

14. The electrically erasable programmable logic device (100) of claim 13 wherein  $V_1'$  is 0V.
15. The electrically erasable programmable logic device (100) of claim 13 wherein  $V_2'$  is 0V.
16. The electrically erasable programmable logic device (100) of claim 13 wherein  $V_3'$  is -2V~8V.
17. The electrically erasable programmable logic device (100) of claim 13 wherein  $V_4'$  is 0V.
18. The electrically erasable programmable logic device (100) of claim 13 wherein  $V_5'$  is 3V~8V.
19. The electrically erasable programmable logic device (100) of claim 13 wherein the operation is an erase operation.
20. An electrically erasable programmable logic device (EEPLD) (100) formed in a semiconductor substrate, the EEPLD (100) comprising:
  - a second conductivity type well (110) disposed in the semiconductor substrate;
  - a first source region of a first conductivity type (140) formed in the well region (110);
  - an erase region of the second conductivity type (134) formed in the first source region (140);
  - a first drain region of the first conductivity type (132) formed in the well region;
  - a first channel region defined between the first drain region (132) and erase region (134);
  - a floating gate (122) formed over the first channel region;
  - a second source region of the first conductivity type (132) formed in the well region, the second source region (132) being electrically connected with the first drain region (132);
  - a second drain region of the first conductivity type (136) formed in the well region (110);
  - a second channel region defined between the second source region (132) and the second drain region (136); and
  - a gate (124) formed over the second channel region.
21. The electrically erasable programmable logic device (100) of claim 20 wherein the floating gate

(122) is electrically isolated.

- 22.** The electrically erasable programmable logic device (100) of claim 20 wherein the second conductivity type is N-type.

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- 23.** The electrically erasable programmable logic device (100) of claim 20 acts as an element of a memory array.

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- 24.** The memory array of claim 23 comprising:

a plurality of the electrically erasable programmable logic devices (100) arranged in rows and columns, each of the electrically erasable programmable logic devices (100) being formed in the semiconductor substrate;

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a plurality of word lines, each of the word lines being connected to each gate (124) in a row of the electrically erasable programmable logic devices (100);

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a plurality of bit lines, each of the bit lines being electrically connected to each of the second drain regions (136) in a column of the electrically erasable programmable logic devices (100);

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a plurality of source lines, each of the source lines being electrically connected to each of the first source regions (140) in a row of the electrically erasable programmable logic devices (100); and

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a plurality of erase lines, each of the erase lines being electrically connected to each of the erase regions (134).

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- 25.** The memory array of claim 24 wherein the source lines are electrically connected to each other.

- 26.** A memory array comprising:

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a plurality of electrically erasable programmable logic devices (100) arranged in rows and columns, each of the electrically erasable programmable logic devices (100) being formed in a semiconductor substrate, and comprising:

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a second conductivity type well (110) disposed in the semiconductor substrate, the well (110) being electrically connected to a well contact;

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a first source region of a first conductivity type (140) formed in the well region (110), the first source region (140) being electrically connected to a source line;

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an erase region of the second conductivity type (134) formed in the first source region (140), the erase region (134) being electrically connected to an erase line;

a first drain region of the first conductivity (132) type formed in the well region (110); a first channel region defined between the first drain region (132) and the erase region (134);

a floating gate (122) formed over the first channel region;

a second source region of the first conductivity type (132) formed in the well region (110);

a second drain region of the first conductivity type (136) formed in the well region (110), the second drain region (136) being electrically connected to a bit line;

a second channel region defined between the second source region (132) and the second drain region (136); and

a gate (124) formed over the second channel region, the gate (124) being electrically connected to a word line;

a plurality of the word lines, each of the word lines being connected to each gate (124) in a row of the electrically erasable programmable logic devices (100);

a plurality of the bit lines, each of the bit lines being electrically connected to each second drain region (136) in a column of the electrically erasable programmable logic devices (100).

a plurality of the source lines, each of the source lines being electrically connected to each first source region (140) in a row of the electrically erasable programmable logic devices (100); and

a plurality of the erase lines, each of the erase lines being electrically connected to each erase region (134).

- 27.** The memory array of claim 26 wherein the first drain region (132) and the second source region (132) are merged into a contiguous region.

- 28.** The memory array of claim 26 wherein the floating gate (122) is electrically isolated.

- 29.** The memory array of claim 26 wherein the electrically erasable programmable logic device (100) is configured as a Multiple-Time Programming (MTP) memory device.

- 30.** The memory array of claim 26 wherein the electrically erasable programmable logic device (100) is configured as an element of a capacitor trimming circuit.

- 31.** The memory array of claim 26 wherein the electrically erasable programmable logic device (100) is configured as an element of a resistor trimming circuit.

cuit.

- 32.** The memory array of claim 26 wherein the electrically erasable programmable logic device (100) is configured as an element of a memory redundancy circuit. 5
- 33.** The memory array of claim 26 wherein the electrically erasable programmable logic device (100) is configured as an element of an electrical fuse circuit. 10

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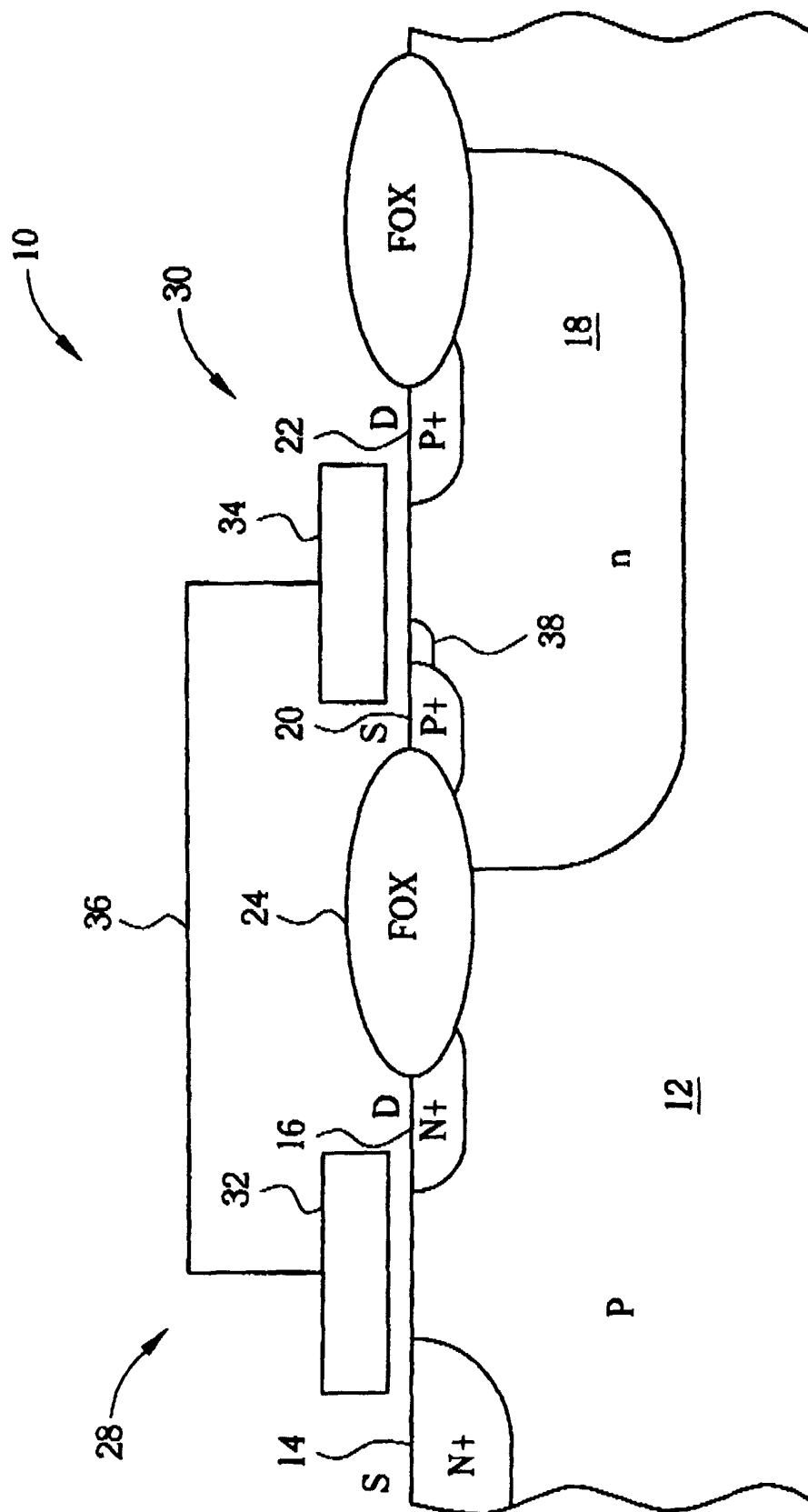


Fig. 1 Prior Art



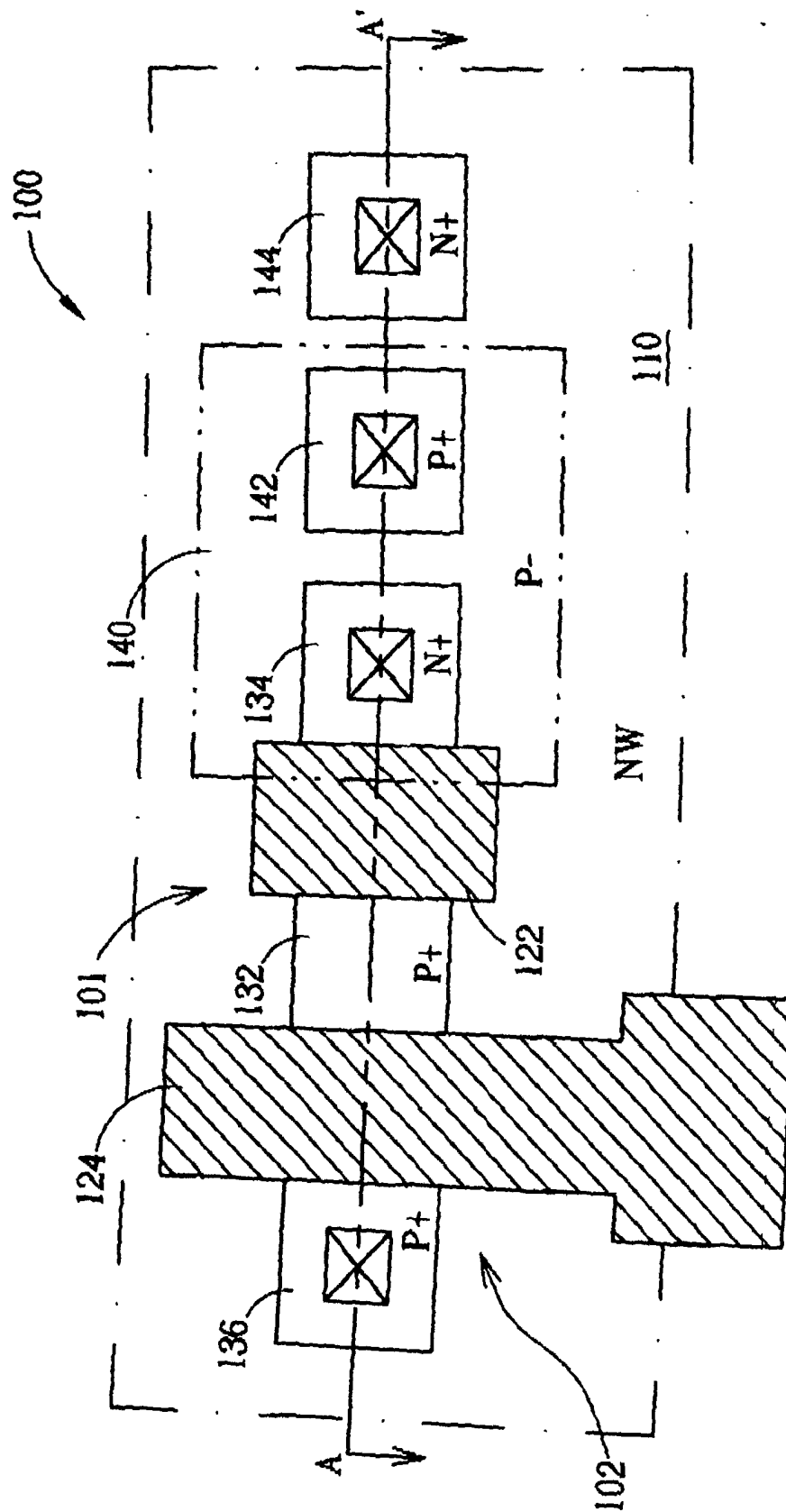


Fig. 2 (a)

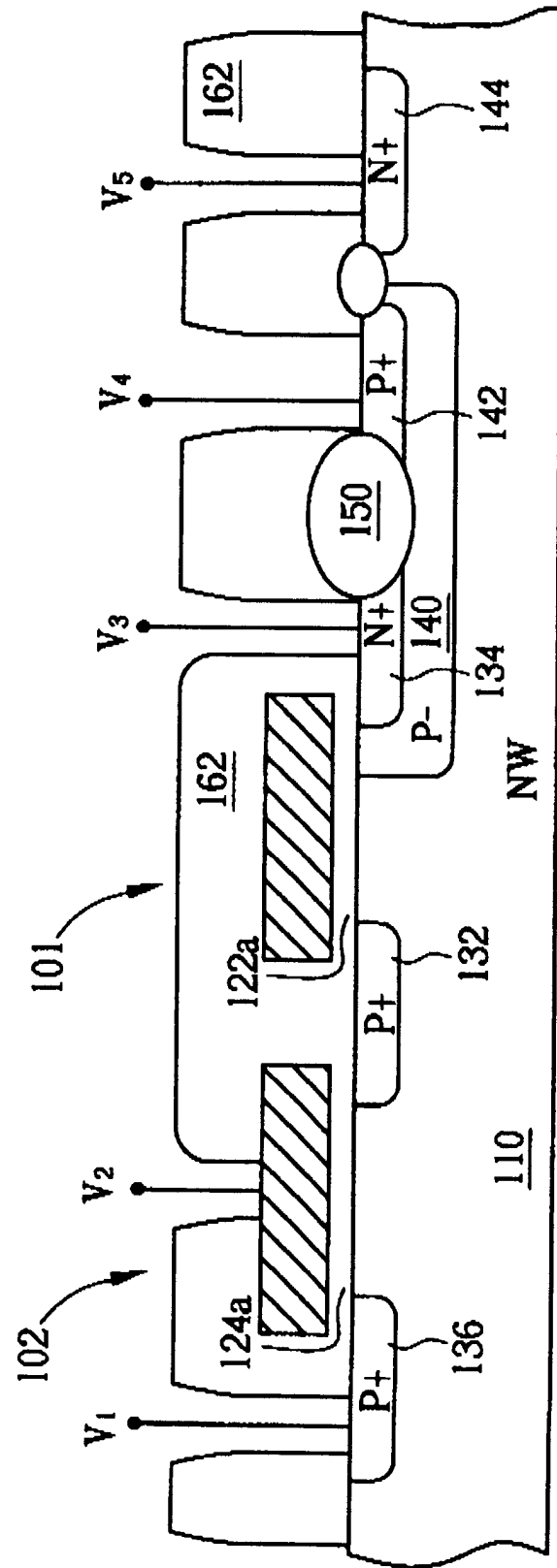


Fig. 2 (b)

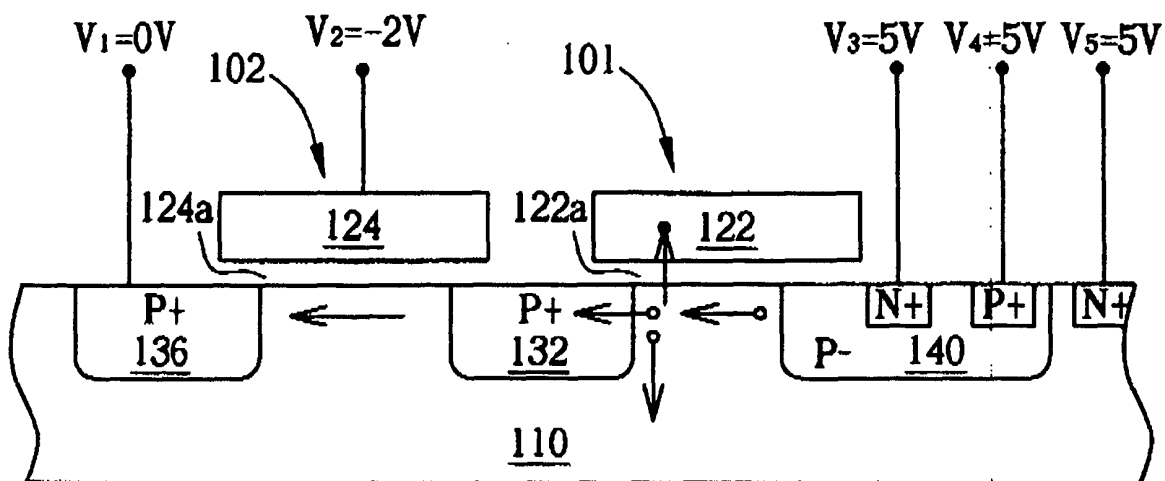


Fig. 3

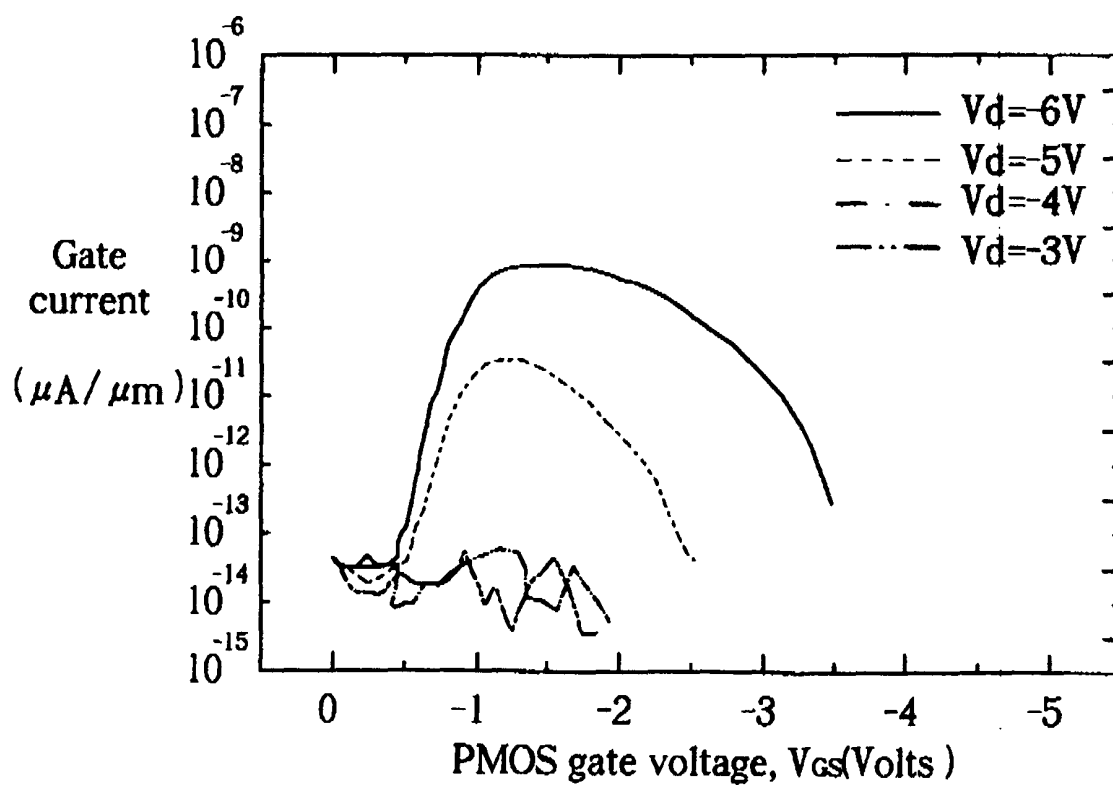


Fig. 4

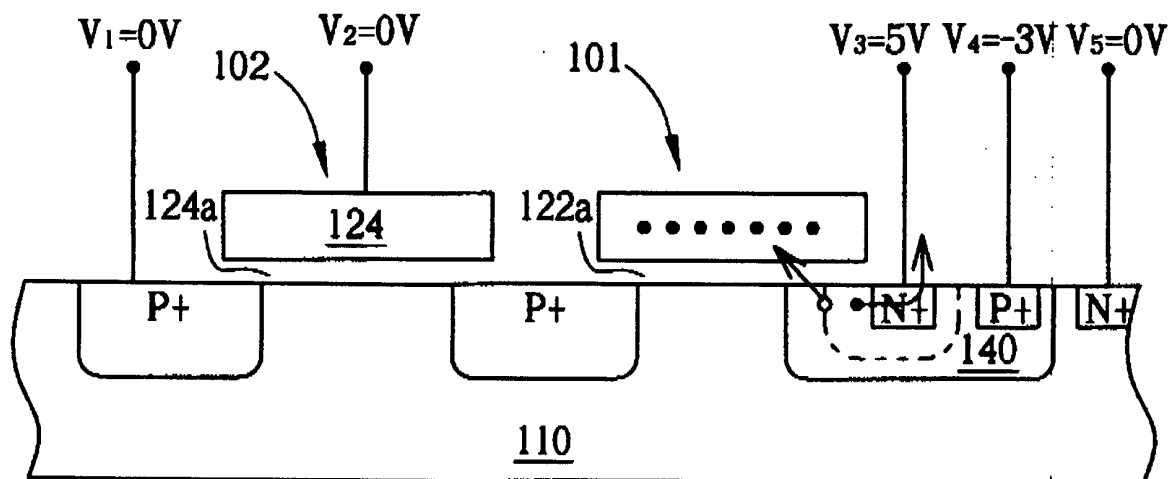


Fig. 5

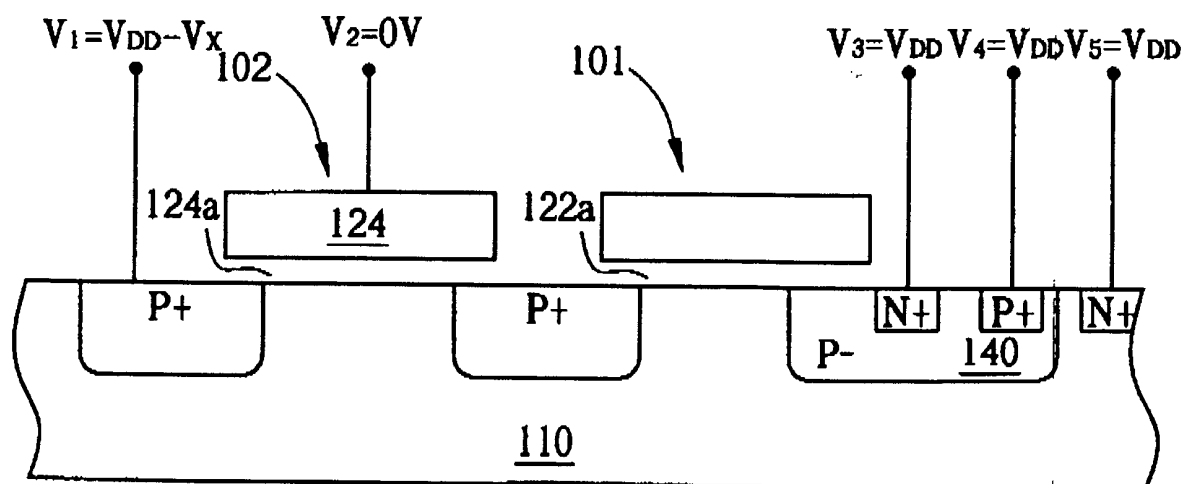


Fig. 6



European Patent  
Office

# EUROPEAN SEARCH REPORT

Application Number  
EP 03 00 0342

| DOCUMENTS CONSIDERED TO BE RELEVANT                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |                                                                                                                                |                                  |                                              |
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| Category                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | Citation of document with indication, where appropriate, of relevant passages                                                  | Relevant to claim                | CLASSIFICATION OF THE APPLICATION (Int.CI.7) |
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