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(54) **Temperature compensated bandgap voltage reference**

Bandgap-Spannungsreferenz mit Temperaturkompensation

Tension de référence à bande interdite avec compensation de température

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A (OLYMPUS OPTICAL CO LTD), 10 April 2002
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Description

BACKGROUND OF THE INVENTION

[0001] The present invention is directed to a temperature compensated bandgap voltage reference.

[0002] Figure 1 shows how a reference voltage based upon V_{be} of a bipolar transistor can be obtained. The current source I is provided in the emitter path of a bipolar transistor. A plurality of current sources can be provided each coupled to an FET of varying size to provide current sources of different magnitude, e.g., I , $10I$, etc. as shown.

[0003] V_{be} of a bipolar transistor decreases with increasing temperature in a well-known fashion. See Fig. 3. It is also known that a current mirror can be used to obtain a voltage proportional to ΔV_{be} i.e., the difference between the V_{be} of two bipolar transistors. Figure 2 shows such a current mirror circuit. ΔV_{be} is equal to V_{be2} minus V_{be1} and ΔV_{be} is equal to $kt/q \ln NI/I$. ΔV_{be} depends upon the ratio of the currents of the current sources as well as the temperature. In particular, ΔV_{be} increases with temperature. See Fig. 3. By combining the two circuits, it is possible to compensate V_{be} of a first transistor with ΔV_{be} obtained via two other transistors Q1 and Q2, to obtain a substantially constant reference voltage V_{ref} as shown in Fig. 3. In particular, V_{ref} is equal to a constant A times V_{be} plus a constant B times ΔV_{be} .

[0004] US-A-5 686 823 discloses a bandgap voltage reference circuit including a feedback controlled current mirror, a bandgap voltage generator and a voltage comparator. The current mirror generates in response to a feedback control signal from the voltage comparator a controllable reference current. The bandgap voltage generator further generates two reference voltages based upon conduction of the reference current from the current mirror through two PN diodes having different emitter areas. The voltage comparator compares the two reference voltages and generates a feedback control signal for the current mirror.

SUMMARY OF THE INVENTION

[0005] The object of the invention is to provide a new implementation of a V_{be} bandgap voltage reference that sums V_{be} and ΔV_{be} to obtain a substantially constant temperature independent voltage reference. The circuit uses a current mirror for ΔV_{be} and a bipolar transistor to provide V_{be} . A comparator is implemented as a differential amplifier and receives inputs proportional to V_{be} and ΔV_{be} . The output of the comparator is coupled back to the input of the bipolar transistor that provides V_{be} .

[0006] The bandgap voltage reference circuit comprises a first circuit providing a first voltage substantially proportional to V_{be} of a first bipolar transistor, a second circuit providing a second voltage ΔV_{be} substantially proportional of the difference of two V_{be} voltages of two bipolar transistors; and a comparator having respective inputs which receive voltages coupled to V_{be} and ΔV_{be} and an

output coupled to the base of the first bipolar transistor whereby a voltage substantially proportional to the sum of constant voltage equal to V_{be} plus a constant times ΔV_{be} is provided at the output of the comparator.

[0007] Preferably, the first circuit comprises a first bipolar transistor providing substantially a reference voltage V_{be} , whereas the second circuit comprises a current mirror circuit having two bipolar transistors coupled in a current mirror arrangement for providing a voltage difference ΔV_{be} comprising substantially a difference signal between the respective V_{be} voltages of the two bipolar transistors.

[0008] The bandgap voltage reference circuit provides a substantially temperature independent voltage reference at the output of the comparator which further may be a multiple of the bandgap voltage. This is important in applications where a 1.25V reference voltage is too low.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009]

Fig. 1 shows a prior art circuit for generating a reference voltage based on V_{be} of a bipolar transistor; Fig. 2 shows a prior art circuit mirror circuit for generating a voltage proportional to V_{be} ;

Fig. 3 is a graph showing the relationship of V_{be} and ΔV_{be} and a reference voltage comprising weighted sums of V_{be} and ΔV_{be} ;

Fig. 4 shows the reference voltage generating circuit according to the invention;

Fig. 5A and 5B shows waveforms of the circuit of Fig. 4; and

Fig. 6 shows a schematic diagram of an implementation of the circuit of the invention.

DETAILED DESCRIPTION OF THE INVENTION

[0010] According to the invention, a new implementation for deriving the voltage bandgap reference V_{ref} is provided. As shown in Fig. 4, a bipolar transistor Q1 provides V_{be} . The emitter of the bipolar transistor Q1 is coupled to a resistor divider comprising resistors R1 and R2. The output of the divider is provided to a comparator U1 inverting input. The non-inverting input of the comparator U1 is provided by the voltage source comprising ΔV_{be} which may be generated by the circuit of Fig. 2. The output of the comparator is provided back to the input IN' . This results in the following equations:

$$IN - = (IN' - V_{be}) \times \frac{R_2}{R_1 + R_2}$$

$$\Delta V_{be} = (IN'_{\Delta V_{be}} - V_{be}) \times \frac{R_2}{R_1 + R_2}$$

$$IN' = OUT$$

$$OUT = IN'_{\Delta V_{be}} \text{ (from Fig. 5B)}$$

$$IN'_{\Delta V_{be}} = V_{be} + \frac{R_1 + R_2}{R_2} \Delta V_{be}$$

$$IN'_{\Delta V_{be}} = OUT = V_{be} + \frac{R_1 + R_2}{R_2} \Delta V_{be}$$

The output of the comparator is shown in Figs. 5A and 5B versus IN^- and IN' , respectively. Figure 5A shows the output versus IN^- i.e., versus the input at the inverting input of the comparator. Figure 5B shows the output versus IN' , i.e., versus the input to the transistor Q1 providing the V_{be} reference voltage. Since the output of the comparator is coupled to the input IN' , the output equals

$$V_{be} + (R_1 + R_2)/R_2 \Delta V_{be}.$$

Accordingly, the output voltage is a constant voltage equal to V_{be} plus a constant times ΔV_{be} . With the appropriate selection of resistors R_1 and R_2 , the output can remain constant.

[0011] Figure 6 shows a complete circuit implementation where a current mirror circuit has been substituted for ΔV_{be} in Fig. 4. In addition, the comparator has been implemented by FETs Q2, Q3 and Q4 serving as a differential amplifier. The inputs IN^- and IN^+ are provided respectively at the sources of transistors Q2 and Q3 and the output $OUT = V_{REF}$ is provided at the source of transistor Q4. ΔV_{be} is provided by the current mirror across the gates of the transistors Q2 and Q3. In Fig. 6, a voltage divider comprising resistors R_3 and R_4 is provided.

$$V_{out'} = V_{out} \left(\frac{R_3 + R_4}{R_3} \right)$$

In this way, the circuit can generate a reference voltage $V_{out'}$ that is a multiple of V_{out} . This is important in applications where a 1.25V reference voltage is too low.

Claims

1. A bandgap voltage reference circuit comprising:

- a first circuit providing a first voltage (IN^-) substantially proportional to the V_{be} -voltage V_{be} of a first bipolar transistor (Q1);
- a second circuit providing a second voltage ΔV_{be} substantially proportional to the difference ΔV_{be} of the V_{be} -voltages of a second and a third bipolar transistors; and
- a comparator (UI, Q2, Q3, Q4) having respective inputs receiving said first and second voltages (IN^- , IN^+), and an output,

characterized in that the output (Out) of the comparator (UI, Q2, Q3, Q4) is coupled to the base of said first bipolar transistor (Q1) whereby a voltage substantially proportional to the sum of V_{be} plus a constant times ΔV_{be} is provided at the output of the comparator (UI, Q2, Q3, Q4).

2. A bandgap voltage reference circuit according to claim 1, **characterized in that** said first circuit comprises said first bipolar transistor (Q1) having its emitter coupled to a resistor divider (R_1 , R_2), the output of said resistor divider (R_1 , R_2) providing said first voltage (IN^-).

3. A bandgap voltage reference circuit according to claim 1 or 2, **characterized in that** said second circuit comprises a current mirror circuit comprising two bipolar transistors coupled in a current mirror arrangement for providing a voltage difference ΔV_{be} comprising substantially a difference between the respective V_{be} voltages of the two bipolar transistors.

4. A bandgap voltage reference circuit according to claim 3, **characterized in that** said comparator comprises first, second and third FET's (Q2, Q3, Q4) arranged as a differential amplifier, said voltage difference ΔV_{be} provided by said current mirror being provided across the gates of said first and second FETs (Q2, Q3).

5. A bandgap voltage reference circuit according to any of the preceding claims, **characterized in that** a substantially temperature independent voltage reference ($V_{out'}$) is provided at the output of the comparator.

Patentansprüche

1. Bandgap-Spannungs-Referenzschaltung mit:
 einer ersten Schaltung, die eine erste Spannung (IN-) liefert, die im Wesentlichen proportional zu der V_{be} -Spannung V_{be} eines ersten bipolaren Transistors (Q1) ist;
 einer zweiten Schaltung, die eine zweite Spannung (IN+) liefert, die im Wesentlichen proportional zu der Differenz ΔV_{be} der V_{be} -Spannungen eines zweiten und eines dritten bipolaren Transistors ist; und
 einem Vergleichs (UI, Q2, Q3, Q4) der jeweiligen Eingänge, die die ersten und zweiten Spannungen (IN-, IN+) empfangen, und einen Ausgang aufweist,
dadurch gekennzeichnet, dass der Ausgang (OUT) des Vergleichers (UI, Q2, Q3, Q4) mit der Basis des ersten bipolaren Transistors (Q1) gekoppelt ist, wodurch eine Spannung im Wesentlichen proportional zur Summe von V_{be} plus einer Konstante multipliziert mit ΔV_{be} an dem Ausgang des Vergleichers (UI, Q2, Q3, Q4) geliefert wird.
2. Bandgap-Spannungs-Referenzschaltung nach Anspruch 1, **dadurch gekennzeichnet, dass** die erste Schaltung den ersten bipolaren Transistor (Q1) umfasst, dessen Emitter mit einem Widerstandsteiler (R1, R2) gekoppelt ist, wobei der Ausgang des ersten Widerstandsteilers (R1, R2) die erste Spannung (IN-) liefert.
3. Bandgap-Spannungs-Referenzschaltung nach Anspruch 1 oder 2, **dadurch gekennzeichnet, dass** die zweite Schaltung eine Stromspiegelschaltung umfasst, die zwei bipolare Transistoren umfasst, die in einer Stromspiegelanordnung gekoppelt sind, um eine Spannungsdifferenz ΔV_{be} zu liefern, die im Wesentlichen eine Differenz zwischen den jeweiligen V_{be} -Spannungen der zwei bipolaren Transistoren umfasst.
4. Bandgap-Spannungs-Referenzschaltung nach Anspruch 3, **dadurch gekennzeichnet, dass** der Vergleichs erste, zweite und dritte FETs (Q2, Q3, Q4) umfasst, die als ein Differenzverstärker angeordnet sind, wobei die Spannungsdifferenz ΔV_{be} , die von dem Stromspiegel geliefert wird, längs der Gate-Elektroden der ersten und zweiten FETs (Q2, Q3) geliefert wird.
5. Bandgap-Spannungs-Referenzschaltung nach einem der vorhergehenden Ansprüche, **dadurch gekennzeichnet, dass** eine im Wesentlichen temperaturunabhängige Spannungsreferenz (Vout') an dem Ausgang des Vergleichers geliefert wird.

Revendications

1. Circuit de tension de référence à bande interdite comprenant :
 un premier circuit délivrant une première tension (IN-) sensiblement proportionnelle à la tension V_{be} d'un premier transistor bipolaire (Q1) ;
 un deuxième circuit délivrant une deuxième tension (IN+) sensiblement proportionnelle à la différence ΔV_{be} des tensions V_{be} d'un deuxième et d'un troisième transistor bipolaire ; et
 un comparateur (UI, Q2, Q3, Q4) ayant des entrées respectives recevant lesdites première et deuxième tensions (IN-, IN+) et une sortie,
caractérisé en ce que la sortie (Out) du comparateur (UI, Q2, Q3, Q4) est couplée à la base dudit premier transistor bipolaire (Q1) de telle manière qu'une tension sensiblement proportionnelle à la somme de V_{be} plus une constante que multiplie ΔV_{be} est délivrée à la sortie du comparateur (UI, Q2, Q3, Q4).
2. Circuit de tension de référence à bande interdite selon la revendication 1, **caractérisé en ce que** ledit premier circuit comprend ledit premier transistor bipolaire (Q1) ayant son émetteur couplé à un diviseur de résistance (R1, R2), la sortie dudit diviseur de résistance (R1, R2) délivrant ladite première tension (IN-).
3. Circuit de tension de référence à bande interdite selon la revendication 1 ou 2, **caractérisé en ce que** ledit deuxième circuit comprend un circuit à miroir de courant comprenant deux transistors bipolaires couplés en un agencement à miroir de courant permettant de produire une différence de tension ΔV_{be} comprenant sensiblement une différence entre les tensions respectives V_{be} des deux transistors bipolaires.
4. Circuit de tension de référence à bande interdite selon la revendication 3, **caractérisé en ce que** ledit comparateur comprend des premier, deuxième et troisième TEC (Q2, Q3, Q4) agencés en un amplificateur différentiel, ladite différence de tension V_{be} délivrée par ledit miroir de courant étant délivrée entre les grilles desdits premier et deuxième TEC (Q2, Q3).
5. Circuit de tension de référence à bande interdite selon l'une quelconque des précédentes revendications, **caractérisé en ce qu'**une tension de référence sensiblement indépendante de la température (Vout') est délivrée à la sortie du comparateur.

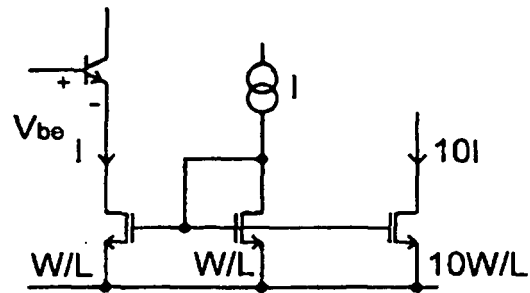


Figure 1
Prior Art

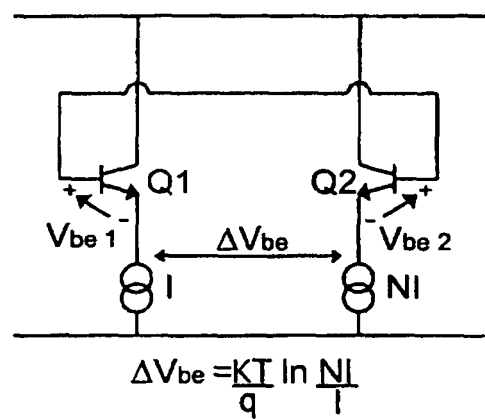


Figure 2
Prior Art

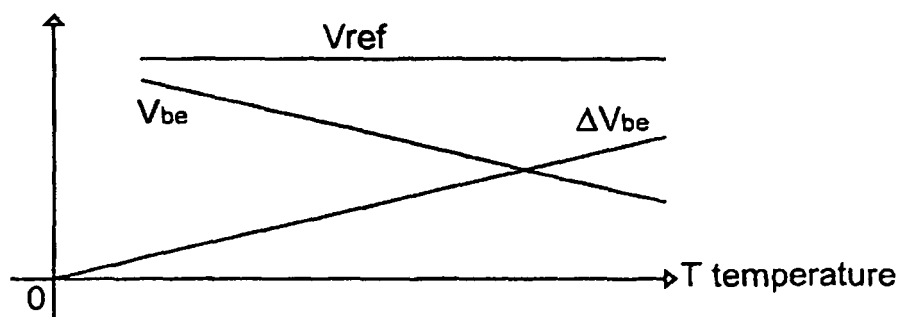


Figure 3

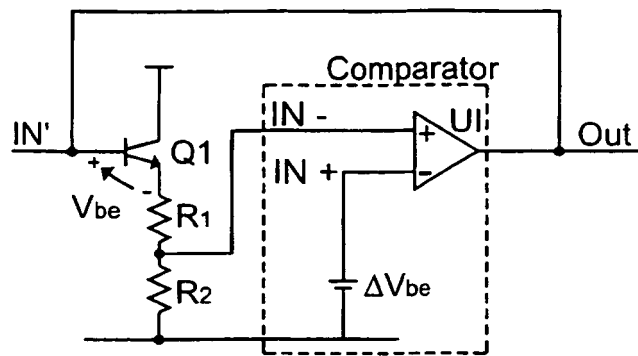


Figure 4

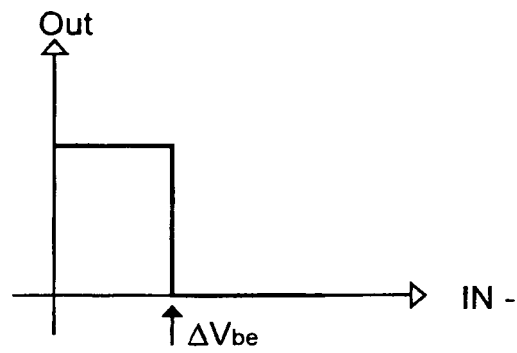


Figure 5A

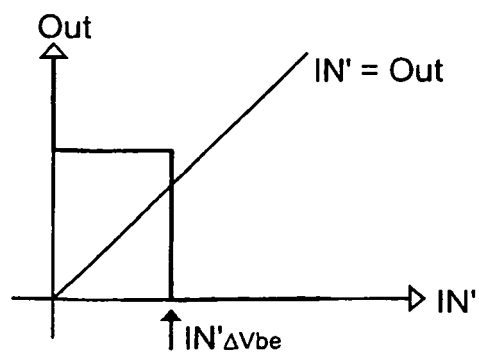


Figure 5B

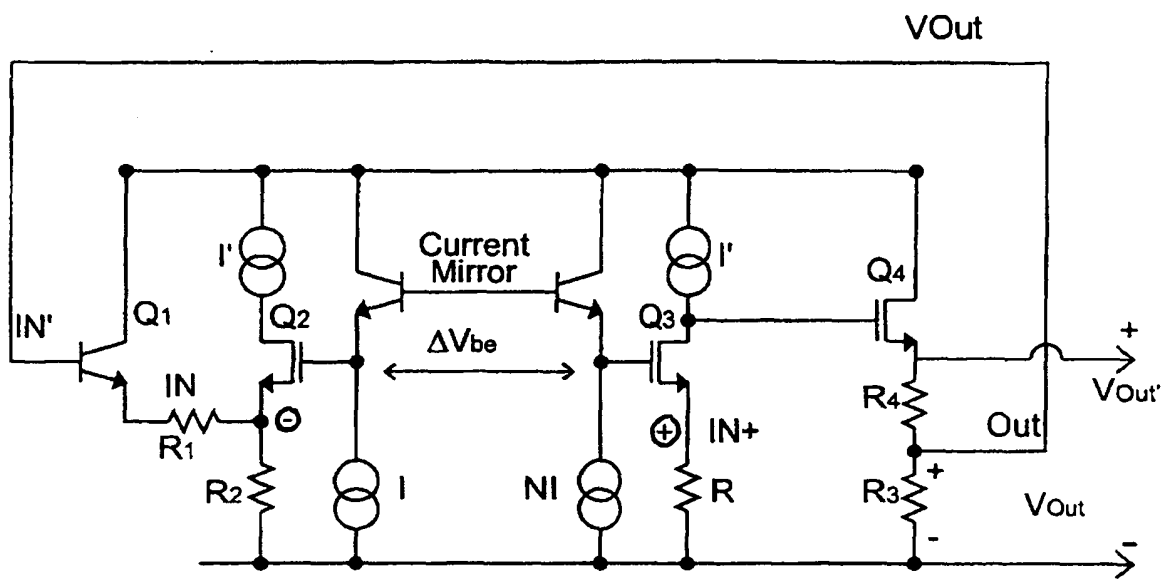


Figure 6