(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 1 446 883 B1

(12) **EUROPEAN PATENT SPECIFICATION**

(45) Date of publication and mention of the grant of the patent:
04.04.2012 Bulletin 2012/14

(21) Application number: **02802339.8**

(22) Date of filing: **17.10.2002**

(51) Int Cl.:
H03K 19/094 *(2006.01)* ***H03K 19/173*** *(2006.01)*
H03K 19/177 *(2006.01)* ***H04L 25/02*** *(2006.01)*
H03K 19/0185 *(2006.01)*

(86) International application number:
PCT/IB2002/004287

(87) International publication number:
WO 2003/039000 (08.05.2003 Gazette 2003/19)

(54) **MULTIMODE I/O CIRCUITRY SUPPORTING LOW INTERFERENCE SIGNALING SCHEMES FOR HIGH SPEED DIGITAL INTERFACES**

MEHRMODEN-E/A-SCHALTKREISE, DIE STÖRUNGSARME SIGNALISIERUNGSSCHEMATA FÜR SCHNELLE DIGITALE SCHNITTSTELLEN UNTERSTÜTZEN

CIRCUIT D'ENTREE/SORTIE A MODES MULTIPLES PRENANT EN CHARGE DES SCHEMAS DE SIGNALISATION A FAIBLE INTERFERENCE, DESTINE AUX INTERFACES NUMERIQUES HAUT DEBIT

(84) Designated Contracting States:
DE FI FR GB NL

(30) Priority: **02.11.2001 US 5766**

(43) Date of publication of application:
18.08.2004 Bulletin 2004/34

(73) Proprietor: **Nokia Corporation**
02150 Espoo (FI)

(72) Inventors:
- **RUHA, Antti**
  FIN-90550 Oulu (FI)
- **RUOTSALAINEN, Tarmo**
  FIN-90570 Oulu (FI)
- **TERVALUOTO, Jussi-Pekka**
  FIN-90570 Oulu (FI)

(74) Representative: **Higgin, Paul**
Swindell & Pearson Limited
48 Friar Gate
Derby DE1 1GY (GB)

(56) References cited:
EP-A1- 0 482 336
US-A1- 2002 003 436
US-B1- 6 243 776
US-B1- 6 424 177
US-B2- 6 472 904
US-B2- 6 480 026

Note: Within nine months of the publication of the mention of the grant of the European patent in the European Patent Bulletin, any person may give notice to the European Patent Office of opposition to that patent, in accordance with the Implementing Regulations. Notice of opposition shall not be deemed to have been filed until the opposition fee has been paid. (Art. 99(1) European Patent Convention).

EP 1 446 883 B1

Printed by Jouve, 75001 PARIS (FR)

Description

TECHNICAL FIELD:

[0001] These teachings relate generally to circuitry used in input/output (I/O) operations and, more specifically, relates to I/O circuitry for supporting high speed digital data paths between integrated circuits (ICs).

BACKGROUND:

[0002] Modem telecommunications systems transmit, receive, store and retrieve ever increasing amounts of data. The transmission of information between ICs in complex systems requires that the signaling scheme and input-output (I/O) circuitry be capable of high speed operation, generate minimal disturbances (noise), be tolerant to interference, consume little power and occupy a minimum area on the IC. Furthermore, it would be highly desirable from a usability point of view that the I/O circuitry support different supply voltages in the transmitter and receiver and be capable of multi-mode operation so as to enhance both backward and forward compatibility with ICs of different generations that may use different signaling schemes.

[0003] Conventional I/O circuit cells typically support only one type of signal, for example single-ended CMOS signals, and the supply voltage of the transmitting cell must be the same as the supply voltage of the receiving cell, and vice versa. Some conventional I/O cells can be used as transmitters or receivers to support bi-directional signaling.

[0004] The most commonly used CMOS digital signaling techniques use single-ended voltage mode signals with rail-to-rail levels and fast edges. However, this approach is known to generate a significant amount of signal disturbance and interference with other circuitry, and tends to limit the maximum usable data rates and/or seriously affects the performance of the system. The generated disturbances are especially detrimental in radio-based communications systems, where received analog signals can be extremely weak.

[0005] One technique to reduce the generation of disturbance signals is to use analog signaling between ICs. This approach implies that both the transmitter and receiver ICs must contain analog circuitry, e.g., analog-to-digital converters (ADCs) and digital-to-analog converters (DACs). However, the incorporation of any analog circuitry into an otherwise digital IC is problematic as digital ICs are typically implemented using highly optimized digital processes. In these processes the analog properties of devices are often compromised. In addition, the maximum tolerable supply voltage of these deep submicron processes is decreasing, which makes the implementation of analog functions increasingly difficult. In addition, the variety of available analog devices is limited. For example, passive devices, such as resistors, are made available only through the use of expensive additional process steps. Furthermore, analog signaling and the associated analog circuitry (e.g., ADCs and DACs) in digital ICs may lead to a prohibitively large circuit area requirement, as well as to an unacceptable power consumption. Also, implementing analog or mixed signal circuitry on large digital ICs makes design and testing more difficult, time consuming and expensive, and therefore increases both risk and delay.

[0006] Moreover, the price per silicon area in deep submicron CMOS processes is increasing. As the area of analog circuitry does not scale down at the same rate as digital circuitry, the placement of analog circuitry on digital ICs becomes increasingly expensive.

[0007] From the above it can be appreciated that it is advantageous that large digital ICs contain only digital circuitry, and that RF, analog and mixed signal circuitry is preferably placed in a separate chip that is implemented using a more appropriate process technology. This being the case, it can further be appreciated that the signaling between ICs should be optimized instead, without relying on the use of analog-based I/O circuitry.

[0008] It is thus important to develop efficient inter-IC signaling circuitry that enables an optimum system partitioning to be achieved. Prior to this invention, this need has not been adequately addressed.

[0009] EP 0 482 336 A1 discloses a transceiver interface device which includes features which allow the transceiver to be switched for operation in either a differential or a single-ended mode. First, the output levels of the transceiver's differential line driver are switchable between TTL levels and non-TTL levels with small differential swings. Second, the transceiver's differential receiver is switchable between a differential threshold and a single-ended TTL threshold. Third, while in differential mode, both outputs of the driver may be placed in the high impedance state or active at the same time, but it is also possible to switch to a single-ended mode in which one driver output is in the high impedance state while the other can be switched between being active or being in the high impedance state. Fourth, the transceiver uses the SCSI standard DIFFSENS pin or driver enable signal for switching between differential mode and single-ended mode operation.

[0010] US 6,243,776 B1 discloses a bus configurable as either a single-ended mode bus or as a differential mode bus, depending on the system environment. The bus is configured in such a way that additional lines are not required, and so that substantially the same circuitry may be used for either single-ended mode or differential mode. Further, a selectable-mode driver may be connected to a non-selectable mode receiver, and vice versa. The invention may be implemented as a selectable driver/receiver pair. The bus may apply to both uni-directional and bi-directional bus implementations. The same bus lines (i.e. wires) and substantially the same circuitry are used for both single-ended and differential modes of operation. When operating in single-ended mode, the data width of the bus is twice the data width as when oper-

ating in differential mode.

SUMMARY:

[0011] The present invention is as set out in the independent claims.

[0012] The foregoing and other problems are overcome by methods and apparatus in accordance with embodiments of these teachings.

[0013] These teachings are directed to multi-mode I/O circuitry for supporting low interference signaling schemes and protocols for high speed digital interfaces between ICs. A presently preferred, but by no means limiting, application for the multi-mode I/O circuitry is in a mobile radio communications system. The disclosed multi-mode I/O circuitry supports single-ended and differential current mode, low swing voltage mode and CMOS signaling, and the operational mode of the disclosed receiver and transmitter circuits can be selected using just a few control bits. The I/O circuitry need only use standard MOS transistors and can therefore be implemented using any conventional CMOS or BiCMOS technology.

[0014] From an interference mitigation point of view the most preferred signaling technique employs differential current mode signaling. The disclosed I/O circuitry supports this preferred mode of operation, but both the receiver and transmitter circuitry may also be used with, for example, conventional CMOS level I/O circuitry. This is an important feature for achieving compatibility with existing and emerging systems. For example, an IC equipped with the disclosed receiver I/O circuitry may communicate with transmitting I/O circuitry of an other IC from a same or a different circuit generation using different signaling schemes and I/O circuitry. Similarly, an IC equipped with the disclosed transmitter I/O circuitry may communicate with the receiving I/O circuitry of another IC from the same or different circuit generation using different signaling schemes and I/O circuitry.

[0015] While the presently preferred differential signaling scheme, by definition, employs two wires per signal link, the requirement to provide the additional wiring is at least partially offset by the fact that such differential links can support higher data rates than non-differential, single conductor types of links.

[0016] These teachings provide a solution to the general problem of how to most effectively transmit increasing amounts of data between ICs, without compromising or deteriorating the performance of the system with the interference and noise associated with the operation of high speed digital data links, and without requiring that analog circuitry be integrated into the ICs.

[0017] These teachings overcome the following specific technical problems, as well as others. First, the differential current mode signaling enabled by the I/O circuitry exhibits less noise and interference than commonly used CMOS digital signaling using single-ended voltage mode signals with rail-to-rail levels and fast edges. Second, the low interference signaling technique in accordance with these teachings enables high speed digital signaling between ICs, and can be used to advantage in radio communications systems containing extremely weak analog signals. Relatedly, the use of these teachings facilitates the system design task by allowing a more optimum partitioning of the system functions between various ICs.

[0018] In accordance with an aspect of these teachings there is provided multi-mode I/O circuitry or cells for transmitting and receiving data between ICs, wherein each data link contains at least one of the disclosed I/O circuits. Each data link between ICs includes transmitter circuitry and receiver circuitry. The transmitter circuitry sends data to the receiver circuitry in another IC, and the receiver circuitry receives data from the transmitter circuitry in another IC. The disclosed I/O circuitry is constructed with CMOS-based transistors (e.g., CMOS or BiCMOS) that are selectively interconnected together by a plurality of switches to operate as two single-ended, current or voltage mode links, or as a single differential current or voltage mode link. In the preferred embodiment the transmitter circuitry sends data to the receiver circuitry in another IC over a first pair of adjacently disposed conductors, and the receiver circuitry receives data from the transmitter circuitry in another IC over a second pair of adjacently disposed conductors.

[0019] Preferably, the transmitter circuitry and the receiver circuitry are selectively configured by at least some of the plurality of switches for operating under a condition where the power supply voltage of the transmitter circuitry is equal to the power supply voltage of the receiver circuitry in another IC, or for operating under a condition where the power supply voltage of the transmitter circuitry is less than the power supply voltage of the receiver circuitry in another IC, or for operating under a condition where the power supply voltage of the transmitter circuitry is greater than the power supply voltage of the receiver circuitry in another IC. These may be considered as various ones of double single-ended, CMOS voltage level link modes.

[0020] It is noted that a single-ended current mode link, as well as differential voltage and current mode links, all support different supply voltages in the transmitter and receiver ICs. However, as the single-ended voltage mode link presents the most difficult case, it is described in the greatest detail below.

[0021] More specifically, the transmitter circuitry and the receiver circuitry are selectively configured by the plurality of switches for operating in a double single-ended voltage mode link mode, a double single-ended current mode link mode, a mode defined by a single differential voltage mode link with a single-ended input drive, a mode defined by a single differential voltage mode link with a differential input drive, a mode defined by a single differential current mode link with a single-ended input drive mode, and a mode defined by a single differential current mode link with a differential input drive.

[0022] It is also within the scope of these teachings to provide additional switches in the disclosed I/O circuitry to convert between transmitter and receiver I/O circuitry.

[0023] Further in this regard, also disclosed is circuitry and a method for sending data between ICs. The method includes providing at least two ICs to each contain at least one instance of an I/O circuit constructed with CMOS-based transistors; programming the I/O circuit in a first IC to function as data transmitter circuitry and programming the I/O circuit in a second IC to function as data receiver circuitry that are interconnected through a plurality of electrical conductors disposed between the first and second ICs. The programming step includes programming the I/O circuits in both the first and second ICs to support two single-ended, current or voltage mode links, or to support a single differential current or voltage mode link. A next step sends data from the first IC to the second IC using the I/O circuits and the electrical conductors. During the operation of the first and second ICs the method may further include a step of reprogramming the I/O circuit in the first IC to function as the data receiver circuitry and reprogramming the I/O circuit in the second IC to function as the data transmitter circuitry. A half-duplex mode of operation is thus made possible, as well as other modes, such as providing bidirectional data signal paths between ICs.

[0024] The methods and circuitry can be used with advantage in a number of different types of equipment, including wireless communication devices and accessory devices for wireless communication devices, as well as for interfacing wireless communication devices to accessory devices.

BRIEF DESCRIPTION OF THE DRAWINGS:

[0025] The above set forth and other features of these teachings are made more apparent in the ensuing Detailed Description of the Preferred Embodiments when read in conjunction with the attached Drawings, wherein:

Fig. 1 shows a plurality of ICs of differing types and signaling requirements interconnected together by digital links made between I/O cells in accordance with these teachings;

Fig. 2 illustrates how the use of these teachings provides compatibility between new and previous generations of ICs using different signaling schemes;

Fig. 3 is a schematic circuit diagram showing a presently preferred embodiment of the multi-mode I/O transmitter and receiver circuitry;

Fig. 4 is a block diagram of the multi-mode I/O transmitter and receiver circuitry of Fig. 3, and is useful in understanding the operation of the disclosed circuitry when implementing the preferred differential signalling technique;

Fig. 5A shows the use of the multi-mode I/O circuitry in providing two single-ended (current or voltage mode) links, and is useful in understanding the Modes 1, 2, 3 and 4 depicted in Figs. 6, 7, 8 and 9, respectively;

Fig. 5B shows the use of the multi-mode I/O circuitry in providing a single differential (current or voltage mode) links, and is useful in understanding the Modes 5, 6, 7 and 8 depicted in Figs. 10, 11, 12 and 13;

Fig. 6 includes a chart showing programmable switch settings for the switches shown in Fig. 3 for achieving two single-ended CMOS level links (where VDD1=VDD2), and a diagram of the resulting Mode 1 effective circuit;

Fig. 7 includes a chart showing programmable switch settings for the switches shown in Fig. 3 for achieving two single-ended CMOS level links (where VDD1<VDD2), and a diagram of the resulting Mode 2 effective circuit;

Fig. 8 includes a chart showing programmable switch settings for the switches shown in Fig. 3 for achieving two single-ended CMOS level links (where VDD1>VDD2), and a diagram of the resulting Mode 3 effective circuit;

Fig. 9 includes a chart showing programmable switch settings for the switches shown in Fig. 3 for achieving two single-ended current mode links, and a diagram of the resulting Mode 4 effective circuit;

Fig. 10 includes a chart showing programmable switch settings for the switches shown in Fig. 3 for achieving a single differential low swing voltage mode link, with a single-ended input drive, and a diagram of the resulting Mode 5 effective circuit;

Fig. 11 includes a chart showing programmable switch settings for the switches shown in Fig. 3 for achieving a single differential low swing voltage mode link, with a differential input drive, and a diagram of the resulting Mode 6 effective circuit;

Fig. 12 includes a chart showing programmable switch settings for the switches shown in Fig. 3 for achieving a single differential current mode link, with a single-ended input drive, and a diagram of the resulting Mode 7 effective circuit;

Fig. 13 includes a chart showing programmable switch settings for the switches shown in Fig. 3 for achieving a single differential current mode link, with a differential input drive, and a diagram of the resulting Mode 8 effective circuit; and

Fig. 14 includes a chart showing programmable switch settings for converting the I/O circuitry between a receiver I/O cell and a transmitter I/O cell.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0026] Fig. 1 illustrates an example of a system containing several integrated circuits (ICs) 1, 2 and 3 with various signal types in a mobile communication terminal such as a cellular telephone or a personal communicator. Of most concern to these teachings is the signaling between the ICs 1, 2 and 3, and the associated parts of the I/O-cells 10 contained within each IC.

[0027] It is first noted that the I/O circuitry is referred to herein as well as the I/O cells 10. In general, data is transferred between the ICs through data links. In the transmitting end of a data link is disposed an I/O cell 10 containing the transmitter circuitry/cell, and in the receiving end is disposed an I/O cell 10 containing the receiver circuitry/cell. An I/O cell 10 may then be either a transmitter I/O cell or a receiver I/O cell. In a given system one IC could use either the transmitter I/O cells or the receiver I/O cells described herein, or it may contain both types of I/O cells, and other ICs could use different kinds of cells.

[0028] In the illustrated example, IC 1 is an RF IC containing high speed analog circuitry with low level signals, IC 2 is baseband (BB) IC characterized by high speed digital signals, and IC 3 is an energy management (EM) device employing mixed low speed analog and digital circuitry. The digital data communication links between the ICs 1, 2 and 3 originate and terminate at the I/O circuits or cells 10.

[0029] Fig. 2 is a diagram that visualizes the backward (and forward) compatibility requirement, which is a necessary precondition for new signaling schemes. In this Figure a "new" transmitter signaling technique is required to be compatible with a "new" receiver signalling technique, as well as with several versions of older receiver signaling techniques. In the same manner the "new" receiver signaling technique is required to be compatible with the "new" transmitter signalling technique, as well as with several versions or generations of older transmitter signaling techniques.

[0030] Fig. 3 illustrates the multi-mode I/O circuitry 10 in accordance with a presently preferred embodiment of these teachings. The embodiment of Fig. 3 provides an ability to realize the backwards and forwards compatibility shown in Fig. 2.

[0031] It is noted that typical supply voltages that may be used with the illustrated I/O circuits 10 could be, for example, 3.3 V, 2.5 V or 1.5 V. In low swing voltage mode signaling the voltage swing could be, for example, 0.5 V. VDD1 in Fig. 3 is the positive supply of the transmitter, VDD2 is the positive supply of the receiver, and ground is the negative supply of both the receiver and transmitter.

[0032] More particularly, Fig. 3 shows the disclosed I/O circuitry, one transmitter 12 and one receiver 14, which can form two single-ended links or one differential link. The various modes supported by the I/O circuitry are generally shown in Figs. 5-13, while the differential current mode signaling technique is shown conceptually in Fig. 4.

[0033] With regard to the differential current mode signalling of Fig. 4, the transmitter 12 may be considered to be composed of two constant current sources (both referred to as ibias1) and a plurality of switches SW_A, SW_B, SW_C and SW_D. The signal link between ICs is implemented with two adjacently disposed wires w1 and w2. The receiver 14 includes a differential transimpedance amplifier (DTA) 16 biased with two constant current sources (both referred to as ibias2). Both of the transmitter and receiver circuits 12 and 14 may be constructed with standard MOS transistors, as shown in Fig. 3, and do not require the use of analog circuitry, or device types that are not generally compatible with standard CMOS processes, such as resistors.

[0034] In the conceptual view of Fig. 4 the input signal (in) and its inverse control the direction of the current flow in the signal wires w1 and w2 by controlling the four transistors that implement the switches SW_A through SW_D. The current from the constant current source ibias1 is steered from one branch to another using the switches SW_A through SW_D. In the signal wires w1 and w2 the currents have equal magnitudes but opposite directions, resulting in the magnetic fields around the wires cancelling one another within a short distance. Current spikes in the transmitter 12 are eliminated because of the constant current biasing, and "floating" output nodes can be provided by the action of the switches SW_A through SW_D. The receiving end determines the common mode, and the transmitter 12 and the receiver 14 can have the same or different power supply voltages. As will be described below with regard to Figs. 6, 7 and 8, VDD1 can be equal to VDD2, or VDD1 can be less than VDD2 (within certain limits), or VDD1 can be greater than VDD2 (within certain limits).

[0035] The receiver 14 includes the differential transimpedance amplifier 16 that is constructed from an amplifier 16A and MOS feedback resistors R_A and R_B in a shunt-shunt configuration. The differential input current is converted to a differential output voltage by the DTA 16. The input impedance of the DTA 16 is low, so the signal swing in the input, and therefore also in the wiring w1 and w2 between the ICs, is small.

[0036] The illustrated I/O circuit 10 embodiment has a number of advantages, including the following. First, the current drawn from the power supplies in the transmitter 12 is constant, i.e., ibias1. The constant current is simply steered from one branch to another. In this manner the operation of transmitter 12 causes minimal disturbances in the power supply lines and substrate. A second advantage is that the current drawn from the power supplies in the receiver 14 is also constant, i.e., ibias2, and the receiver 14 also causes minimal disturbances in the pow-

er supply lines and substrate. A third advantage is that the differential signaling in the two adjacent wires w1 and w2 radiates little electromagnetic disturbance, and thus significantly reduces the possibility of causing interference into other circuitry, such as sensitive RF circuitry. As the signal swing in the wires w1 and w2 is small, the capacitive coupling to other wires or circuits is low, and as the electromagnetic fields around the differential wires w1 and w2 cancel one another within a short distance from the wires the inductive coupling from w1 and w2 to other wires or circuits is low as well. Another advantage is that externally generated disturbances mainly generate a common mode signal, as differential signals are only caused by mismatches. Another advantage is that the differential wiring w1 and w2 has a lower inductance (if properly routed) than the combination of one signal wire and a common return wire (often ground) owing to the mutual inductance. This reduces ringing in the signal lines and thereby improves the noise margin and reduces timing errors.

[0037] The I/O cells 10 may be implemented using relatively low quality MOS transistors, and other active or passive devices are not required. As such, the I/O cells 10 may be implemented in all analog, all digital or in mixed signal integrated circuits using well-characterized digital or analog CMOS or BiCMOS technologies.

[0038] The remaining Figures illustrate how various operational modes of the I/O circuitry 10 can be configured with switches to support a variety of signaling schemes.

[0039] Figs. 5A and 5B, collectively referred to herein as Fig. 5, illustrate how the proposed circuitry can be used as two single-ended links or a single differential link, both in either current mode, low swing voltage mode or CMOS mode. More specifically, Fig. 5A shows the use of the multi-mode I/O circuitry 10 in providing two single-ended (current or voltage mode) links, and is useful in understanding the Modes 1, 2, 3 and 4 depicted in Figs. 6, 7, 8 and 9, respectively, while Fig. 5B shows the use of the multi-mode I/O circuitry 10 in providing a single differential (current or voltage mode) link, and is useful in understanding the Modes 5, 6, 7 and 8 depicted in Figs. 10, 11, 12 and 13.

[0040] Fig. 3 makes it evident that a plurality of switches are provided for setting the various modes of operation. The state of these switches is set by programming bits input over a plurality of transmitter Mode signal lines 12A and a plurality of receiver Mode signal lines 14A applied via corresponding transmitter electronics 12B and receiver electronics 14B (shown in Fig. 5). A description of these various switches is now provided with reference to Fig. 3.

S1: Transmitter switch S1 is used to connect the gate of the PMOS transistor Q1A in the tail of the transmitter differential pair formed by Q2 and Q3 to ground. Similarly, the second switch S1 is used to connect the gate of the NMOS transistor Q1B in the tail of the transmitter differential pair formed by Q4 and Q5 to VDD1. In this case Q1A and Q1B change from a current source to a small resistance, and the double differential pair is effectively transformed into two separate inverters, as shown in Fig. 6.

[0041] S2: Transmitter switch S2 is used to connect the input node i2 to a DC voltage having a magnitude approximately mid-way between the positive and negative power supplies. This voltage is set by Q6 and Q7 functioning as a voltage divider. In this case a single-ended input signal is enabled to drive the double differential pair Q2, Q3, Q4 and Q5, as shown for example in Fig. 10.

[0042] S3: Receiver switches S3 are used to connect a feedback resistance comprised of CMOS transmission gates Q8, Q9 and Q10, Q11, as shown in Fig. 9, between the inputs and outputs of the receiver 14. In this manner the receiver 14 is converted from a voltage amplifier to a transimpedance amplifier having a low input impedance and a low input signal swing.

[0043] S6: Receiver switches S6 are used to connect a resistor (the transmission gates formed by Q8, Q9 and Q10, Q11) to a DC voltage having a magnitude approximately mid-way between the positive and negative power supplies. This voltage is set by Q12 and Q13 functioning as a voltage divider. This reduces the input impedance and the signal swing at the input of the receiver 14.

[0044] S7: Receiver switch S7 is used to connect the gate of the PMOS transistor Q14A in the tail of the receiver differential pair formed by Q15 and Q16 to ground. Similarly, the second switch S7 is used to connect the gate of the NMOS transistor Q14B in the tail of the receiver differential pair formed by Q17 and Q18 to VDD2. In this case Q14A and Q14B change from a current source to a small resistance, and the double differential pair is effectively transformed into two separate inverters, as shown in Fig. 6.

[0045] S8: Receiver switches S8 are used to connect the gates of the PMOS transistors Q19 and Q20, that are connected between inputs of the receiver 14 and the positive power supply VDD2, to the outputs (O1 and O2) of the receiver 14 as shown by example in Fig. 7. In this case the PMOS transistors Q19 and Q20 function as regenerative loads and pull up the inputs of the receiver 14 to the positive supply VDD2.

[0046] S9: Receiver switches S9 are used to connect the gates of the PMOS transistors Q19 and Q20 to VDD2, as shown by example in Fig. 9. In this case the PMOS transistors Q19 and Q20 are shut off, and do not function as regenerative loads.

[0047] S 11: Transmitter switches S11 are used to bypass the NMOS transistors Q21 and Q22 that are in series with the outputs of the transmitter 12. The series NMOS transistors Q21 and Q22, when not bypassed, are used to protect the transistors of the transmitter 12 when the supply voltage of the receiver 14 is higher than the supply voltage of the transmitter 12, as shown in Fig. 7. If the supply voltages of the transmitter and receiver are the same, then the series NMOS transistors S11 can

be bypassed by closing switches S11, as shown in Fig. 6.

[0048] S12: Receiver switches S 12 are used to bypass the NMOS transistors Q23 and Q24 that are in series with the inputs of the receiver 14. The series NMOS transistors Q23 and Q24, when not bypassed, are used to protect the transistors of the receiver 14 when the supply voltage of the transmitter 12 is higher than the supply voltage of the receiver 14, as shown in Fig. 8. If the supply voltages of the transmitter 12 and receiver 14 are the same, then the series NMOS transistors S12 can be bypassed by closing switches S12, as shown in Fig. 6.

[0049] Transistors Q25, Q26, Q27 and Q28 are part of the current mirrors forming the constant current sources ibias1 and ibias2.

[0050] By selectively setting the various switches shown in Fig. 3, as described in further detail below, the transmitter 12 may be used as a single differential transmitter, as shown for example in Fig. 10, or as two single-ended transmitters, as shown by example in Fig. 6. In the former case the transmitter input i2 is connected to a DC voltage with S2, and the input signal is connected to i1. In the latter case both i1 and i2are used, and each is connected to a different input signal. While Fig. 4 is more conceptual in nature, Figs. 12 and 13 show this mode of operation in more detail. In Fig. 12 the input is driven in the single-ended mode, while in Fig. 13 the input is driven differentially (symmetrically).

[0051] In the discussion of the following Figs. 6-13 Sx=1 indicates that the switch is closed (conducting), while Sx=0 indicates that the switch is open (nonconducting). In a practical implementation the switches can be NMOS or PMOS transistors (or both in parallel), and are driven with appropriate control signals as is well known to those having skill in the art.

[0052] Fig. 6 includes a chart showing programmable switch settings for the switches shown in Fig. 3 for achieving two single-ended CMOS level (rail-to-rail swing) links (where VDD1=VDD2), and also shows a diagram of the resulting Mode 1 effective circuit. In this mode both the transmitter 12 and the receiver 14 can operate with conventional CMOS I/O cells.

[0053] Note that in Figs. 6-9 W/L = Width/Length, i.e., the aspect ratio of a transistor: W/L(M1) = W/L(Q1A), W/L(M2) = W/L(Q1B), W/L(M3) = W/L(Q14A), W/L(M4) = W/L(Q14B). These relationships are shown by way of examples, and should not be viewed in a limiting sense upon the practice of these teachings.

[0054] Fig. 7 shows how the I/O circuitry 10 can be used to implement two single-ended CMOS level (rail-to-rail swing) signal links, when the supply of the transmitter is lower than that of the receiver. In this case the NMOS transistors Q21 and Q22 in series with the outputs of the transmitter 12 stop conducting before the output voltages reach the positive supply of the transmitter 12, and thus protect the output transistors of the transmitter. The voltages across the terminals of the protection NMOS transistors Q21 and Q22 are sufficiently low so that they are not damaged. The NMOS transistors Q21 and Q22 also prevent direct current flow between the positive supplies of the transmitter 12 and receiver 14 through the regenerative pull-up transistors Q19 and Q20. The regenerative pull-up using the weak transistors Q19 and Q20 is used in the receiver 14 to ensure sufficient signal level.

[0055] Another technique to deal with the difference in the supply voltages is to bring the lower supply voltage of the transmitter 12 to the receiver 14 using an additional wire, and to use this lower voltage in the I/O cells 10 of the receiver 14.

[0056] Fig. 8 shows the I/O circuitry 10 when the switches are set to implement two single-ended CMOS level (rail-to-rail swing) signal links, when the supply of the transmitter 12 is higher than that of the receiver 14. In this case the NMOS transistors Q23 and Q24 in series with the inputs to the receiver 14 stop conducting before the input voltages reach the positive supply of the receiver 14, and thus protect the input transistors of the receiver 14. The voltages across the terminals of the protection NMOS transistors Q23 and Q24 are sufficiently low so that no damage occurs. The NMOS transistors Q23 and Q24 also prevent direct current flow between the positive supplies of the transmitter 12 and the receiver 14 through the regenerative pull-up transistors Q19 and Q20.

[0057] As with the embodiment of Fig. 7, another technique to deal with the difference in the supply voltages would is to bring the lower supply voltage of the receiver 14 to the transmitter 12 using an additional conductor, and to use the lower voltage in the I/O cells 10 of the transmitter 12.

[0058] It should be noted that the single-ended current mode, as well as the differential voltage and current mode links, support different supply voltages in the transmitter and receiver ICs (within certain limits). These modes do not necessarily require any extra switches or transistors to perform this function. As the single-ended voltage mode link is the most difficult one to implement with different supply voltages at each end of the link, it is preferred to use the additional protection transistors Q21 to Q24, as well as the additional switches S11 and S12.

[0059] Fig. 9 illustrates the I/O circuitry 10 when the switches are set to implement two single-ended current mode signal links. The receiver 14 is configured as two transimpedance amplifiers, and the CMOS transmission gates Q8, Q9 and Q10, Q11 are used to implement the two feedback resistors.

[0060] Fig. 10 illustrates the I/O circuitry 10 when the switches are set to implement a single differential low swing voltage mode signal link. In this mode (Mode 5) the input drive is single-ended, and the resistive loads (Q8, Q9 and Q10, Q11) are used in the receiver 14 to limit the signal swing. These resistive loads also set the input common mode voltage due to the connection through S6 to the DC voltage between Q12 and Q13.

[0061] Fig. 11 illustrates the I/O circuitry 10 when the switches are set to implement a single differential low swing voltage mode signal link. The input drive is differ-

ential, and the resistive loads (Q8, Q9 and Q10, Q11) are used in the receiver 14 to limit the signal swing. As in the Mode 5 embodiment of Fig. 10, the resistive loads (Q8, Q9 and Q10, Q11) also set the input common mode voltage by the connection through S6 to the DC voltage between Q12 and Q13.

[0062] Fig. 12 illustrates the I/O circuitry 10 when the switches are set to implement a single differential current mode signal link. The input drive is single-ended, and the transistors Q15, Q16, Q17 and Q18 are configured as one transimpedance amplifier 16A (see Fig. 4). CMOS transmission gates Q8, Q9 and Q10, Q11 are used to implement the feedback resistors R_A and R_B, also as shown in Fig. 4.

[0063] Fig. 13 illustrates the I/O circuitry 10 when the switches are set to implement a single differential current mode signal link. In this mode (Mode 8) the input drive is differential. As in the embodiment of Fig. 12, the receiver 14 is configured as one transimpedance amplifier 16A, and the CMOS transmission gates Q8, Q9 and Q10, Q11 are used to implement the feedback resistors R A and R_B.

[0064] This invention has thus described a technique for implementing a multi-mode I/O circuit that supports a number of different digital data transfer protocols. Known technologies (differential current mode and low swing voltage mode signaling) are combined into one group of devices that are selectively interconnected through the use of programmable switches. A desired operational mode may be selected through the use of mode bits. In this regard a few bits (e.g., two coded bits) could be input to a lookup table stored in a memory device, and a resulting decoded 3-bit output used to control the states of the three switches S1, S2, S11 contained in the transmitter 12 and similarly a few bits (e.g., three coded bits) could be input to a lookup table stored in a memory device, and a resulting decoded 6-bit output used to control the states of the six switches S3, S6, S7, S8, S9, S12 in the receiver 14 end of a given data link. In other embodiments these mode bits could be hardwired to predetermined logic levels to provide the desired mode of operation. In either case the use of the generic CMOS circuitry depicted in Fig. 3 provides a number of advantages over conventional approaches, such as the use of analog circuitry, as described above.

[0065] The resulting multi-mode operation is important in order to support compatibility between IC generations, and provides a backward and a forward compatible signal interface. The use of these teachings makes it more economical (smaller total silicon area) to implement multi-mode I/O structures, as compared to a combination of several different single mode I/O structures. These teachings also provide a universal CMOS-based I/O cell solution that requires no external components or integrated resistors.

[0066] While a number of switches and resulting modes have been described above, it should be realized that more or less than this number of switches or modes can be provided. For example, if one knows *a priori* that the power supply voltages of all system ICs will be the same, then one may choose to eliminate S11, S12 and Q21, Q22, Q23 and Q24, and provide a direct connection from the transmitter 12 to the receiver 14 via wires or conductors w1 and w2.

[0067] It should also be noted that both the transmitter I/O cell 12 and the receiver I/O cell 14 contain similar functional blocks, such as a double differential pair, biasing circuitry based on current mirrors, a reference voltage generator composed of a voltage divider and protection transistors in series with the I/O lines. Therefore, by adding a few additional switches the receiver circuitry could be transformed to the transmitter circuitry, and the transmitter circuitry transformed to the receiver circuitry, thus supporting bidirectional (half-duplex) links as well.

[0068] Further in this regard, the chart shown in Fig. 14 specifies the settings for switches S4, S5, S10 and S13-S16 for an embodiment wherein the I/O circuitry 10 can be configured as a receiver I/O cell 14 or as a transmiller IO cell 12. This embodiment is particularly attractive, as it generalizes and simplifies the IC circuit layout by using a common I/O circuit core. The disclosed switches could be hardwired, or they may be programmable (at power-up or initial configuration, and/or during operation).

[0069] The methods and circuitry disclosed herein can be used with advantage in a number of different types of equipment such as, but certainly not limited to, wireless communication devices such as cellular telephones and personal communicators, and in accessory devices for wireless communication devices.

[0070] These circuits and methods can also be used for interfacing wireless communication devices to accessory devices.

[0071] Thus, while these teachings have been particularly shown and described with respect to preferred embodiments thereof, it will be understood by those skilled in the art that changes in form and details may be made therein, without departing from the scope of the claims.

Claims

1. An apparatus comprising transmitter circuitry (12) configured to send data to an integrated circuit (2), said transmitter circuitry comprising a plurality of Complementary Metal-Oxide Semiconductor based transistors (Q1A, Q1B, Q2-Q5) that are selectively interconnected together by a plurality of switches (S1) so as to be operable as each of:

two single-ended current or voltage mode links; and
a single differential current or voltage mode link;

wherein the transmitter circuitry (12) comprises:

a first set of switches (S1) configured to:

selectively change a first Complementary Metal-Oxide Semiconductor based transistor (Q1A), located in a tail of a first differential pair (Q2, Q3), from being able to provide a current source to being able to provide a resistance to the tail of the first differential pair (Q2, Q3), and
selectively change a second Complementary Metal-Oxide Semiconductor based transistor (Q1B), located in a tail of a second differential pair (Q4, Q5), from being able to provide a current source to being able to provide a resistance to the tail of the second differential pair (Q4, Q5).

2. An apparatus as claimed in claim 1 further comprising;
a first input node (i1) and a second input node (i2) coupled respectively to a first input and a second input of a double differential pair (Q2-Q5) formed by the first and second differential pairs;
a first switch (S2) configured to selectively couple the second input node (i2) to a voltage divider (Q6, Q7); and
a second set of switches (S11) configured to selectively bypass a third and a fourth Complementary Metal-Oxide Semiconductor based transistor (Q21, Q22), wherein the third and the fourth Complementary Metal-Oxide Semiconductor based transistors are in series respectively with a first output and a second output of the double differential pair (Q2-Q5).

3. An apparatus comprising receiver circuitry (14) configured to receive data from an integrated circuit (1), said receiver circuitry comprising a plurality of Complementary Metal-Oxide Semiconductor based transistors (Q8-Q18) that are selectively interconnected together by a plurality of switches (S3, S6, S7) so as to be operable as each of:

two single-ended current or voltage mode links; and
a single differential current or voltage mode link;

wherein the receiver circuitry (14) comprises:

a first set of switches (S3) configured to selectively couple a feedback resistance (Q8, Q9; Q11,12) between the inputs and outputs (o1, o2) of the receiver circuitry;
a second set of switches (S6) configured to selectively couple a resistor (Q8, Q9; Q11,12) to a voltage divider (Q10, Q13); and
a third set of switches (S7) configured to:

selectively change a first Complementary Metal-Oxide Semiconductor based transistor (Q14A), located in a tail of a first differential pair (Q15, Q16), from being able to provide a current source to being able to provide a resistance to the tail of the first differential pair (Q15, Q16), and
selectively change a second Complementary Metal-Oxide Semiconductor based transistor (Q14B), located in a tail of a second differential pair (Q17, Q18), from being able to provide a current source to being able to provide a resistance to the tail of the second differential pair (Q17, Q18).

4. An apparatus as claimed in claim 3 further comprising,
a fourth set of switches (S8) configured to selectively couple a gate of a third Complementary Metal-Oxide Semiconductor based transistor (Q19) to a first output (o1) of the receiver circuitry and to selectively couple a gate of a fourth Complementary Metal-Oxide Semiconductor based transistor (Q20) to a second output (o2) of the receiver circuitry, wherein the third transistor (Q19) is coupled between a first input of the receiver and a power supply (VDD2), and the fourth Complementary Metal-Oxide Semiconductor based transistor (Q20) is coupled between a second input of the receiver and the power supply (VDD2);
a fifth set of switches (S9) configured to couple the gates of the third and fourth Complementary Metal-Oxide Semiconductor based transistors (Q19, Q20) to the power supply (VDD2); and
a sixth set of switches (S12) configured to selectively bypass a fifth and a sixth Complementary Metal-Oxide Semiconductor based transistor (Q23, Q24), wherein the fifth and the sixth Complementary Metal-Oxide Semiconductor based transistors are in series respectively with the first and second inputs of the receiver.

5. A multi-mode Input/Output circuit (10) comprising:

the apparatus of any of claims 1 or 2, and
the apparatus of any of claims 3 or 4.

6. A multi-mode Input/Output circuit (10) as in claim 5, wherein said transmitter circuitry (12) is configured to send data to said integrated circuit (2) over a first pair of adjacently disposed conductors (W1, W2), and where said receiver circuitry (14) is configured to receive data from said integrated circuit (2) over a second pair of adjacently disposed conductors.

7. A multi-mode Input/Output circuit (10) as in claim 5, wherein said transmitter circuitry (12) and said receiver circuitry (14) are selectively configured by switches (S1:S3, S6:S9) for operating under a condition where a power supply voltage (VDD1) of said

transmitter circuitry is equal to a power supply voltage (VDD2) of said receiver circuitry in said integrated circuit (2), for operating under a condition where the power supply voltage of said transmitter circuitry is less than the power supply voltage of said receiver circuitry in said integrated circuit, and for operating under a condition where the power supply voltage of said transmitter circuitry is greater than the power supply voltage of said receiver circuitry in said integrated circuit.

8. A multi-mode Input/Output circuit (10) as in claim 5, wherein said transmitter circuitry (12) and said receiver circuitry (14) are selectively configured by switches (S1:S3, S6:S9) for operating in one of a plurality of double single-ended, Complementary Metal-Oxide Semiconductor voltage level link modes, wherein in a first mode a power supply voltage (VDD1) of said transmitter circuitry is equal to a power supply voltage (VDD2) of said receiver circuitry in said integrated circuit (2), wherein in a second mode the power supply voltage of said transmitter circuitry is less than the power supply voltage of said receiver circuitry in said integrated circuit, and wherein in a third mode the power supply voltage of said transmitter circuitry is greater than the power supply voltage of said receiver circuitry in said integrated circuit.

9. A multi-mode Input/Output circuit (10) as in claim 5, wherein said transmitter circuitry (12) and said receiver circuitry (14) are selectively configured by switches (S1:S3, S6:S9) for operating in one of said plurality of double single-ended, Complementary Metal-Oxide Semiconductor voltage level link modes, or in said differential voltage or current mode links, and wherein the integrated circuits (1, 2) at each end of the link may operate with different supply voltages.

10. A multi-mode Input/Output circuit as in claim 5, wherein said transmitter circuitry (12) and said receiver circuitry (14) are selectively configured by switches (S1:S3, S6:S9) for operating in a double single-ended voltage mode link.

11. A multi-mode Input/Output circuit (10) as in claim 5, wherein said transmitter circuitry (12) and said receiver circuitry (14) are selectively configured by switches (S1:S3, S6:S9) for operating in a double single-ended current mode link.

12. A multi-mode Input/Output circuit (10) as in claim 5, wherein said transmitter circuitry (12) and said receiver circuitry (14) are selectively configured by switches (S1:S3, S6:S9) for operating in a mode defined by a single differential voltage mode link with a single-ended input drive.

13. A multi-mode Input/Output circuit (10) as in claim 5, wherein said transmitter circuitry (12) and said receiver circuitry (14) are selectively configured by switches (S1-S3, S6:S9) for operating in a mode defined by a single differential voltage mode link with a differential input drive.

14. A multi-mode Input/Output circuit (10) as in claim 5, wherein said transmitter circuitry (12) and said receiver circuitry (14) are selectively configured by switches (S1:S3, S6:S9) for operating in a mode defined by a single differential current mode link with a single-ended input drive.

15. A multi-mode Input/Output circuit (10) as in claim 5, wherein said transmitter circuitry (12) and said receiver circuitry (14) are selectively configured by switches (S1:S3, S6:S9) for operating in a mode defined by single differential current mode link with a differential input drive.

16. A multi-mode Input/Output circuit (10) as in claim 5, wherein certain switches are provided to convert said Input/Output circuitry into either said transmitter circuitry (12) configuration or into said receiver circuitry (14) configuration.

17. A multi-mode Input/Output circuit (10) as in claim 5, wherein the integrated circuits (1, 2) are located in a wireless communication device.

18. A multi-mode Input/Output circuit (10) as in claim 5, wherein the integrated circuits (1, 2) are located in an accessory device for a wireless communication device.

19. A multi-mode Input/Output circuit (10) as in claim 5, wherein the integrated circuits (1, 2) are located in an interface between a wireless communication device and an accessory device for the wireless communication device.

20. A method comprising:

providing at least two integrated circuits (1, 2) to each contain at least one Input/Output circuit (10), said Input/Output circuit comprising at least one of transmitter circuitry (12) or receiver circuitry (14), the transmitter circuitry configured to send data to one of the at least two integrated circuits (2), and the receiver circuitry configured to receive data from the other of the at least two integrated circuits (1), the Input/Output circuit being constructed with Complementary Metal-Oxide Semiconductor based transistors (Q1A: Q24); and selectively interconnecting together the Complementary Mental-oxide Semiconductor based transistors with switches (S1:S3, S6:

S9) so as to be operable as each of:

two single-ended current or voltage mode links; and
as a single differential current or voltage mode link;

wherein the transmitter circuitry (12) comprises:
a first set of switches (S1) configured to:

selectively change a first Complementary Metal-Oxide Semiconductor based transistor (via), located in a tail of a first differential pair (Q2, Q3), from being able to provide a current source to being able to provide a resistance to the tail of the first differential pair (Q2, Q3), and
selectively change a second Complementary Metal-Oxide Semiconductor based transistor (Q1B), located in a tail of a second differential pair (Q4, Q5), from being able to provide a current source to being able to provide a resistance to the tail of the second differential pair (Q4, Q5).

wherein the receiver circuitry (14) comprises:
a first set of switches (S3) configured to selectively couple a feedback resistance (Q8, Q9; Q11,12) between the inputs and outputs (o1, o2) of the receiver circuitry;
a second set of switches (S6) configured to selectively couple a resistor (Q8, 09; Q11,12) to a voltage divider (Q10, Q13); and
a third set of switches (S7) configured to:

selectively change a first Complementary Metal-Oxide Semiconductor based transistor (Q14A), located in a tail of a first differential pair (Q15, Q16), from being able to provide a current source to being able to provide a resistance to the tail of the first differential pair (Q15, Q16), and
selectively change a second Complementary Metal-Oxide Semiconductor based transistor (Q14B), located in a tail of a second differential pair (Q17, Q18), from being able to provide a current source to being able to provide a resistance to the tail of the second differential pair (Q17, Q18).

21. A method as in claim 20, wherein said transmitter circuitry (12) sends data to said receiver circuitry (14) in said one of the at least two integrated circuits (2) over a first pair of adjacently disposed conductors (W1, W2), and where said receiver circuitry receives data from said transmitter circuitry in said other of the at least two integrated circuits (1) over a second pair of adjacently disposed conductors.

22. A method as in claim 20, wherein said transmitter circuitry (12) and said receiver circuitry (14) are selectively configured by the switches (S1:S3, S6:S9) to operate under a condition where a power supply voltage (VDD1) of said transmitter circuitry is equal to a power supply voltage (VDD2) of said receiver circuitry in said one of the at least two integrated circuits (2), to operate under a condition where the power supply voltage of said transmitter circuitry is less than the power supply voltage of said receiver circuitry in said one of the at least two integrated circuits (2), and to operate under a condition where the power supply voltage of said transmitter circuitry is greater than the power supply voltage of said receiver circuitry in said one of the at least two integrated circuits (2).

23. A method as in claim 20, wherein said transmitter circuitry (12) and said receiver circuitry (14) are selectively configured by switches (S1:S3, S6:S9) to operate in one of a plurality of double single-ended, Complementary Metal-Oxide Semiconductor voltage level link modes, wherein in a first mode a power supply voltage (VDD1) of said transmitter circuitry is equal to a power supply voltage (VDD2) of said receiver circuitry in said one of the at least two integrated circuits (2), wherein in a second mode the power supply voltage of said transmitter circuitry is less than the power supply voltage of said receiver circuitry in said one of the at least two integrated circuits (2), and wherein in a third mode the power supply voltage of said transmitter circuitry is greater than the power supply voltage of said receiver circuitry in said one of the at least two integrated circuits (2).

24. A method as in claim 20, wherein said transmitter circuitry (12) and said receiver circuitry (14) are selectively configured by the switches (S1:S3, S6:S9) to operate in either a double single-ended voltage mode link or a double single-ended current mode link.

25. A method as in claim 20, wherein said transmitter circuitry (12) and said receiver circuitry (14) are selectively configured by the switches (S1;S3, S6:S9) to operate in a mode defined by a single differential voltage mode link with either a single-ended input drive or a differential input drive,

26. A method as in claim 20, wherein said transmitter circuitry (12) and said receiver circuitry (14) are selectively configured by the switches (S1:S3, S6:S9) to operate in a mode defined by a single differential current mode link with either a single-ended input drive or a differential input drive.

27. A method as in claim 20, wherein said transmitter

circuitry (12) and said receiver circuitry (14) are selectively configured by said switches (S1:S3, S6:S9) to operate in one of said plurality of double single-ended. Complementary Metal-Oxide Semiconductor voltage level link modes, or in said differential voltage or current mode links, and wherein each of the at least two integrated circuits (1, 2) at each end of the link may operate with different supply voltages.

28. A method as in claim 20, wherein certain switches are provided to convert said Input/Output circuitry (10) into either said transmitter circuitry (12) configuration or into said receiver circuitry (14) configuration.

29. A method as in claim 20, wherein the at least two integrated circuits (1, 2) are located in a wireless communication device.

30. A method as in claim 20, wherein the at least two integrated circuits (1, 2) are located in an accessory device for a wireless communication device.

31. A method as in claim 20, wherein the at least two integrated circuits (1, 2) are located in an interface between a wireless communication device and an accessory device for the wireless communication device.

Patentansprüche

1. Vorrichtung, umfassend eine Senderschaltung (12), die eingerichtet ist, um Daten an eine integrierte Schaltung (2) zu senden, wobei die Senderschaltung mehrere auf komplementären Metall-Oxid-Halbleitern basierende Transistoren (Q1A, Q1B, Q2-Q5) umfasst, die durch mehrere Schalter (S1) selektiv miteinander verbunden sind, um betriebsfähig zu sein als jedes von:

- zwei einpolige Strom- oder Spannungsmodus-Verbindungen; und
- eine einzelne differenzielle Strom- oder Spannungsmodus-Verbindung;

wobei die Senderschaltung (12) umfasst:

- einen ersten Satz von Schaltern (S1), der eingerichtet ist, um:

  - selektiv einen ersten auf komplementären Metall-Oxid-Halbleitern basierenden Transistor (Q1A), der in einem Ende eines ersten differenziellen Paars (Q2, Q3) angeordnet ist, von der Fähigkeit, eine Stromquelle bereitzustellen, zu einer Fähigkeit zu ändern, dem Ende des ersten differenziellen Paars (Q2, Q3) einen Widerstand bereitzustellen; und
  - selektiv einen zweiten auf komplementären Metall-Oxid-Halbleitern basierenden Transistor (Q1B), der in einem Ende eines zweiten differenziellen Paars (Q4, Q5) angeordnet ist, von der Fähigkeit, eine Stromquelle bereitzustellen, zu einer Fähigkeit zu ändern, dem Ende des zweiten differenziellen Paars (Q4, Q5) einen Widerstand bereitzustellen.

2. Vorrichtung nach Anspruch 1, weiter umfassend:

- einen ersten Eingangsknoten (i1) und einen zweiten Eingangsknoten (i2), die mit einem ersten beziehungsweise einem zweiten Eingang eines doppelten differenziellen Paars (Q2-Q5) gekoppelt sind, gebildet durch das erste und das zweite differenzielle Paar;
- einen ersten Schalter (S2), der eingerichtet ist, den zweiten Eingangsknoten (i2) selektiv mit einem Spannungsteiler (Q6, Q7) zu koppeln; und
- einen zweiten Satz von Schaltern (S11), der eingerichtet ist, um selektiv einen dritten und einen vierten auf komplementären Metall-Oxid-Halbleitern basierenden Transistor (Q21, Q22) zu umgehen, wobei der dritte und der vierte auf komplementären Metall-Oxid-Halbleitern basierende Transistor mit einem ersten Ausgang beziehungsweise einem zweiten Ausgang des doppelten differenziellen Paars (Q2-Q5) in Reihe geschaltet ist.

3. Vorrichtung, umfassend eine Empfängerschaltung (14), die eingerichtet ist, um Daten von einer integrierten Schaltung (1) zu empfangen, wobei die Empfängerschaltung mehrere auf komplementären Metall-Oxid-Halbleitern basierende Transistoren (Q8-Q18) umfasst, die durch mehrere Schalter (S3, S6, S7) selektiv miteinander verbunden sind, um betriebsfähig zu sein als jedes von:

- zwei einpolige Strom- oder Spannungsmodus-Verbindungen; und
- eine einzelne differenzielle Strom- oder Spannungsmodus-Verbindung;

wobei die Empfängerschaltung (14) umfasst:

- einen ersten Satz von Schaltern (S3), der eingerichtet ist, um einen Rückkoppelungswiderstand (Q8, Q9; Q11, Q12) selektiv zwischen die Eingänge und Ausgänge (o1, o2) der Empfängerschaltung zu koppeln;
- einen zweiten Satz von Schaltern (S6), der eingerichtet ist, um einen Widerstand (Q8, Q9; Q11, Q12) selektiv mit einem Spannungsteiler

(Q10, Q13) zu koppeln; und
- einen dritten Satz von Schaltern (S7), der eingerichtet ist, um:

- selektiv einen ersten auf komplementären Metall-Oxid-Halbleitern basierenden Transistor (Q14A), der in einem Ende eines ersten differenziellen Paars (Q15, Q16) angeordnet ist, von der Fähigkeit, eine Stromquelle bereitzustellen, zu einer Fähigkeit zu ändern, dem Ende des ersten differenziellen Paars (Q15, Q16) einen Widerstand bereitzustellen; und
- selektiv einen zweiten auf komplementären Metall-Oxid-Halbleitern basierenden Transistor (Q14B), der in einem Ende eines zweiten differenziellen Paars (Q17, Q18) angeordnet ist, von der Fähigkeit, eine Stromquelle bereitzustellen, zu einer Fähigkeit zu ändern, dem Ende des zweiten differenziellen Paars (Q17, Q18) einen Widerstand bereitzustellen.

4. Vorrichtung nach Anspruch 3, weiter umfassend:

- einen vierten Satz von Schaltern (S8), der eingerichtet ist, ein Gate eines dritten auf komplementären Metall-Oxid-Halbleitern basierenden Transistors (Q19) selektiv mit einem ersten Ausgang (o1) der Empfängerschaltung zu koppeln und ein Gate eines vierten auf komplementären Metall-Oxid-Halbleitern basierenden Transistors (Q20) selektiv mit einem zweiten Ausgang (o2) der Empfängerschaltung zu koppeln, wobei der dritte Transistor (Q19) zwischen einen ersten Eingang des Empfängers und eine Stromversorgung (VDD2) gekoppelt ist, und der vierte auf komplementären Metall-Oxid-Halbleitern basierende Transistor (Q20) zwischen einen zweiten Eingang des Empfängers und die Stromversorgung (VDD2) gekoppelt ist;
- einen fünften Satz von Schaltern (S9), der eingerichtet ist, um die Gates des dritten und des vierten auf komplementären Metall-Oxid-Halbleitern basierenden Transistors (Q19, Q20) mit der Stromversorgung (VDD2) zu koppeln; und
- einen sechsten Satz von Schaltern (S12), der eingerichtet ist, um einen fünften und einen sechsten auf komplementären Metall-Oxid-Halbleitern basierenden Transistor (Q23, Q24) selektiv zu umgehen, wobei der fünfte und sechste auf komplementären Metall-Oxid-Halbleitern basierende Transistor mit dem ersten beziehungsweise zweiten Eingang des Empfängers in Reihe geschaltet ist.

5. Multimodus-Eingabe/Ausgabe-Schaltung (10), umfassend:

- die Vorrichtung nach einem der Ansprüche 1 oder 2; und
- die Vorrichtung nach einem der Ansprüche 3 oder 4.

6. Multimodus-Eingabe/Ausgabc-Schaltung (10) nach Anspruch 5, wobei die Senderschaltung (12) eingerichtet ist, Daten über ein erstes Paar von benachbart angeordneten Leitern (W1, W2) an die integrierte Schaltung (2) zu senden, und wobei die Empfängerschaltung (14) eingerichtet ist, um Daten über ein zweites Paar von benachbart angeordneten Leitern von der integrierten Schaltung (2) zu empfangen.

7. Multimodus-Eingabe/Ausgabe-Schaltung (10) nach Anspruch 5, wobei die Senderschaltung (12) und die Empfängerschaltung (14) durch Schalter (S1:S3, S6:S9) selektiv eingerichtet werden, um in einem Zustand betrieben zu werden, in dem eine Stromversorgungsspannung (VDD1) der Senderschaltung gleich einer Stromversorgungsspannung (VDD2) der Empfängerschaltung in der integrierten Schaltung (2) ist, um in einem Zustand betrieben zu werden, in dem die Stromversorgungsspannung der Senderschaltung kleiner als die Stromversorgungsspannung der Empfängerschaltung in der integrierten Schaltung ist, und um in einem Zustand betrieben zu werden, bei der die Stromversorgungsspannung der Senderschaltung größer als die Stromversorgungsspannung der Empfängerschaltung in der integrierten Schaltung ist.

8. Multimodus-Eingabe/Ausgabe-Schaltung (10) nach Anspruch 5, wobei die Senderschaltung (12) und die Empfängerschaltung (14) durch Schalter (S1:S3, S6:S9) selektiv eingerichtet werden, um in einem von mehreren doppelt-einpoligen, komplementären Metall- Oxid- Halbleiter- Spannungspegel- Verbindungsmodi betrieben zu werden, wobei in einem ersten Modus eine Stromversorgungsspannung (VDD1) der Senderschaltung gleich einer Stromversorgungsspannung (VDD2) der Empfängerschaltung in der integrierten Schaltung (2) ist, wobei in einem zweiten Modus die Stromversorgungsspannung der Senderschaltung kleiner als die Stromversorgungsspannung der Empfängerschaltung in der integrierten Schaltung ist, und wobei in einem dritten Modus die Stromversorgungsspannung der Senderschaltung größer als die Stromversorgungsspannung der Empfängerschaltung in der integrierten Schaltung ist.

9. Multimodus-Eingabe/Ausgabe-Schaltung (10) nach Anspruch 5, wobei die Senderschaltung (12) und die Empfängerschaltung (14) durch Schalter (S1:S3, S6:S9) selektiv eingerichtet werden, um in einem der mehreren doppelt-einpoligen, komplementären Metall-Oxid-Halbleiter-Spannungspegel-Verbindungs-

modi betrieben zu werden, oder in den differenziellen Spannungs- oder Strommodus-Verbindungen, und wobei die integrierten Schaltungen (1, 2) an jedem Ende der Verbindung mit verschiedenen Versorgungsspannungen betrieben werden können.

10. Multimodus-Eingabe/Ausgabe-Schaltung (10) nach Anspruch 5, wobei die Senderschaltung (12) und die Empfängerschaltung (14) durch Schalter (S1:S3, S6:S9) selektiv eingerichtet werden, um in einer doppelt-einpoligen Spannungsmodus-Verbindung betrieben zu werden.

11. Multimodus-Eingabe/Ausgabe-Schaltung (10) nach Anspruch 5, wobei die Senderschaltung (12) und die Empfängerschaltung (14) selektiv durch Schalter (S1:S3, S6:S9) eingerichtet werden, um in einer doppelt-einpoligen Strommodus-Verbindung betrieben zu werden.

12. Multimodus-Eingahe/Ausgabe-Schaltung (10) nach Anspruch 5, wobei die Senderschaltung (12) und die Empfängerschaltung (14) durch Schalter (S1:S3, S6:S9) selektiv eingerichtet werden, um in einem Modus betrieben zu werden, der durch eine einzelne differenzielle Spannungsmodus-Verbindung mit einer einpoligen Eingangsansteuerung definiert wird.

13. Multimodus-Eingabaltlusgabe-Schaltung (10) nach Anspruch 5, wobei die Sendeischaltung (12) und die Empfängerschaltung (14) selektiv durch Schalter (S1:S3, S6:S9) eingerichtet werden, um in einem Modus betrieben zu werden, der durch eine einzelne differenzielle Spannungsmodus-Verbindung mit einer differenziellen Eingangsansteuerung definiert wird.

14. Multimodus-Eingabe/Ausgabe-Schaltung (10) nach Anspruch 5, wobei die Senderschaltung (12) und die Empfängerschaltung (14) durch Schalter (S1:S3, S6:S9) selektiv eingerichtet werden, um in einem Modus betrieben zu werden, der durch eine einzelne differenzielle Strommodus-Verbindung mit einer einpoligen Eingangsansteuerung definiert wird.

15. Multimodus-Eingabe/Ausgabe-Schaltung (10) nach Anspruch 5, wobei die Senderschaltung (12) und die Empfängerschaltung (14) durch Schalter (S1:S3, S6:S9) selektiv eingerichtet werden, um in einem Modus betrieben zu werden, der durch eine einzelne differenzielle Strommodus-Verbindung mit einer differenziellen Eingangsansteuerung definiert wird.

16. Multimodus-Eingabe/Ausgabe-Schaltung (10) nach Anspruch 5, wobei bestimmte Schalter bereitgestellt sind, um die Eingabe/Ausgabe-Schaltung in entweder die Konfiguration der Senderschaltung (12) oder die Konfiguration der Empfängerschaltung (14) umzuwandeln.

17. Multimodus-Eingahe/Ausgabe-Schaltung (10) nach Anspruch 5, wobei die integrierten Schaltungen (1, 2) in einer drahtlosen Kommunikationsvorrichtung angeordnet sind.

18. Multiinodus-Eingabe/Ausgabe-Schaltung (10) nach Anspruch 5, wobei die integrierten Schaltungen (1, 2) in einer Zubehörvorrichtung für eine drahtlose Kommunikationsvorrichtung angeordnet sind.

19. Multimodus-Eingabe/Ausgabe-Schaltung (10) nach Anspruch 5, wobei die integrierten Schaltungen (1, 2) in einer Schnittstelle zwischen einer drahtlosen Kommunikationsvorrichtung und einer Zubehörvorrichtung für die drahtlose Kommunikationsvorrichtung angeordnet sind.

20. Verfahren, umfassend:

- Bereitstellen von mindestens zwei integrierten Schaltungen (1, 2), so dass jede mindestens eine Eingabe/Ausgabe-Schaltung (10) enthält, wobei die Eingabe/Ausgabe-Schaltung mindestens eine Senderschaltung (12) oder eine Empfängerschaltung (14) umfasst, wobei die Senderschaltung eingerichtet ist, um Daten an eine der mindestens zwei integrierten Schaltungen (2) zu senden, und wobei die Empfängerschaltung (14) eingerichtet ist, um Daten von der anderen der mindestens zwei integrierten Schaltungen (1) zu empfangen, wobei die Eingabe/Ausgabe-Schaltung mit auf komplementären Metall-Oxid-Halbleitern basierenden Transistoren (Q1A;Q24) aufgebaut ist; und
- Selektives Verbinden der auf komplementären Metall-Oxid-Halbleitern basierenden Transistoren miteinander mit Schaltern (S1:S3, S6:S9), um betriebsfähig zu sein als jedes von:
- zwei einpoligen Strom- oder Spannungsmodus-Verbindungen; und
- eine einzelne differenzielle Strom- oder Spannungsmodus-Verbindung;

wobei die Senderschaltung (12) umfasst:

- einen ersten Satz von Schaltern (S1), der eingerichtet ist, um:

  - selektiv einen ersten auf komplementären Metall-Oxid-Halbleitern basierenden Transistor (Q1A), der in einem Ende eines ersten differenziellen Paars (Q2, Q3) angeordnet ist, von der Fähigkeit, eine Stromquelle bereitzustellen, zu einer Fähigkeit zu ändern, dem Ende des ersten differenziellen Paars (Q2, Q3) einen Widerstand bereitzustellen;

und

- selektiv einen zweiten auf komplementären Metall-Oxid-Halbleitern basierenden Transistor (Q1B), der in einem Ende eines zweiten differenziellen Paars (Q4, Q5) angeordnet ist, von der Fähigkeit, eine Stromquelle bereitzustellen, zu einer Fähigkeit zu ändern, dem Ende des zweiten differenziellen Paars (Q4, Q5) einen Widerstand bereitzustellen;

wobei die Empfängerschaltung (14) umfasst:

- einen ersten Satz von Schaltern (S3), der eingerichtet ist, um einen Rückkoppelungswiderstand (Q8, Q9; Q11, Q12) selektiv zwischen die Eingänge und Ausgänge (o1, o2) der Empfängerschaltung zu koppeln; einen zweiten Satz von Schaltern (S6), der eingerichtet ist, um einen Widerstand (Q8, Q9; Q11, Q12) selektiv mit einem Spannungsteiler (Q10, Q13) zu koppeln; und
- einen dritten Satz von Schaltern (S7), der eingerichtet ist, um:

  - selektiv einen ersten auf komplementären Metall-Oxid-Halbleitern basierenden Transistor (Q14A), der in einem Ende eines ersten differenziellen Paars (Q15, Q16) angeordnet ist, von der Fähigkeit, eine Stromquelle bereitzustellen, zu einer Fähigkeit zu ändern, dem Ende des ersten differenziellen Paars (Q15, Q16) einen Widerstand bereitzustellen; und
  - selektiv einen zweiten auf komplementären Metall-Oxid-Halbleitern basierenden Transistor (Q14B), der in einem Ende eines zweiten differenziellen Paars (Q17, Q18) angeordnet ist, von der Fähigkeit, eine Stromquelle bereitzustellen, zu einer Fähigkeit zu ändern, dem Ende des zweiten differenziellen Paars (Q17, Q18) einen Widerstand bereitzustellen.

21. Verfahren nach Anspruch 20, wobei die Senderschaltung (12) Daten über ein erstes Paar von benachbart angeordneten Leitern (W1, W2) an die Empfängerschaltung (14) in der einen der mindestens zwei integrierten Schaltungen (2) sendet, und wobei die Empfängerschaltung Daten über ein zweites Paar von benachbart angeordneten Leitern von der Senderschaltung in der anderen der mindestens zwei integrierten Schaltungen (1) empfängt,

22. Verfahren nach Anspruch 20, wobei die Senderschaltung (12) und die Empfängerschaltung (14) durch die Schalter (S1:S3, S6:S9) selektiv eingerichtet werden, um in einem Zustand betrieben zu werden, in dem eine Stromversorgungsspannung (VDD1) der Senderschaltung gleich einer Stromversorgungsspannung (VDD2) der Empfängerschaltung in der einen der mindestens zwei integrierten Schaltungen (2) ist, um in einem Zustand betrieben zu werden, in dem die Stromversorgungsspannung der Senderschaltung kleiner als die Stromversorgungsspannung der Empfängerschaltung in der einen der mindestens zwei integrierten Schaltungen (2) ist, und um in einem Zustand betrieben zu werden, in dem die Stromversorgungsspannung der Senderschaltung größer als die Stromversorgungsspannung der Empfängerschaltung in der einen der mindestens zwei integrierten Schaltungen (2) ist.

23. Verfahren nach Anspruch 20, wobei die Senderschaltung (12) und die Empfängerschaltung (14) durch die Schalter (S1:S3, S6:S9) selektiv eingerichtet werden, um in einem von mehreren doppelt-einpoligen, komplementären Metall-Oxid-Halbleiter-Spannungspegel-Verbindungsmodi betrieben zu werden, wobei in einem ersten Modus eine Stromversorgungsspannung (VDD1) der Senderschaltung gleich einer Stromversorgungsspannung (VDD2) der Empfängerschaltung in der einen der mindestens zwei integrierten Schaltungen (2) ist, wobei in einem zweiten Modus die Stromversorgungsspannung der Senderschaltung kleiner als die Stromversorgungsspannung der Empfängerschaltung in der einen der mindestens zwei integrierten Schaltungen (2) ist, und wobei in einem dritten Modus die Stromversorgungsspannung der Senderschaltung größer als die Stromversorgungsspannung der Empfängerschaltung in der einen der mindestens zwei integrierten Schaltungen (2) ist.

24. Verfahren nach Anspruch 20, wobei die Senderschaltung (12) und die Empfängerschaltung (14) durch die Schalter (S1:S3, S6:S9) selektiv eingerichtet werden, um in entweder einer doppelt-einpoligan Spannungsmodus-Verbindung oder einer doppelteinpoligen Strornrnadus-Verhindung betrieben zu werden.

25. Verfahren nach Anspruch 20, wobei die Senderschaltung (12) und die Empfängerschaltung (14) durch die Schalter (S1:S3, S6:S9) selektiv eingerichtet werden, um in einem Modus betrieben zu werden, der durch eine einzelne differenzielle Spannungsmodus-Verbindung mit entweder einer einpoligen Eingangsansteuerung oder einer differenziellen Eingangsansteuerung definiert wird.

26. Verfahren nach Anspruch 20, wobei die Senderschaltung (12) und die Empfängerschaltung (14) durch die Schalter (S1:S3, S6:S9) selektiv eingerichtet werden, um in einem Modus betrieben zu werden, der durch eine einzelne differenzielle Strommodus-

Verbindung mit entweder einer einpoligen Eingangsansteuerung oder einer differenziellen Eingangsansteuerung definiert wird.

27. Verfahren nach Anspruch 20, wobei die Senderschaltung (12) und die Empfängerschaltung (14) durch die Schalter (S1:S3, S6:S9) selektiv eingerichtet werden, um in einem der mehreren doppelt-einpoligen, komplementären Metall-Oxid-Halbleiter-Spannungspegel-Verbindungsmodi betrieben zu werden, oder in der differenziellen Spannungs- oder Strommodus-Verbindung, und wobei jede der mindestens zwei integrierten Schaltungen (1, 2) an jedem Ende der Verbindung mit verschiedenen Versorgungsspannungen betrieben werden kann.

28. Verfahren nach Anspruch 20, wobei bestimmte Schalter bereitgestellt sind, um die Eingabe/Ausgabe-Schaltung (10) in entweder die Konfiguration der Senderschaltung (12) oder die Konfiguration der Empfängerschaltung (14) umzuwandeln.

29. Verfahren nach Anspruch 20, wobei die mindestens zwei integrierten Schaltungen (1, 2) in einer drahtlosen Kommunikationsvorrichtung angeordnet sind.

30. Verfahren nach Anspruch 20, wobei die mindestens zwei integrierten Schaltungen (1, 2) in einer Zubehörvorrichtung für eine drahtlose Kommunikationsvorrichtung angeordnet sind.

31. Verfahren nach Anspruch 20, wobei die mindestens zwei integrierten Schaltungen (1, 2) in einer Schnittstelle zwischen einer drahtlosen Kommunikationsvorrichtung und einer Zubehörvorrichtung für die drahtlose Kommunikationsvorrichtung angeordnet sind.

Revendications

1. Appareil comprenant des éléments de circuit d'émetteur (12) configurés pour envoyer des données à un circuit intégré (2), lesdits éléments de circuit d'émetteur comprenant une pluralité de transistors à structure métal oxyde semi-conducteur complémentaire (Q1A, Q1B, Q2 à Q5) qui sont interconnectés de manière sélective les uns aux autres par une pluralité de commutateurs (S1) de manière à pouvoir être exploités en tant que chacun des éléments suivants :

deux liaisons en mode courant ou tension à sortie unique ; et
une unique liaison en mode courant ou tension différentielle ;
dans lequel les éléments de circuit d'émetteur (12) comprennent :
un premier ensemble de commutateurs (S1) configurés pour :
changer de manière sélective un premier transistor à structure métal oxyde semi-conducteur complémentaire (Q1A), situé dans une queue d'une première paire différentielle (Q2, Q3), depuis un état dans lequel il est capable de fournir une source de courant à un état dans lequel il est capable de fournir une résistance à la queue de la première paire différentielle (Q2, Q3), et
changer de manière sélective un deuxième transistor à structure métal oxyde semi-conducteur complémentaire (Q1B), situé dans une queue d'une deuxième paire différentielle (Q4, Q5), depuis un état dans lequel il est capable de fournir une source de courant à un état dans lequel il est capable de fournir une résistance à la queue de la deuxième paire différentielle (Q4, Q5).

2. Appareil selon la revendication 1, comprenant en outre :

un premier naeud d'entrée (i1) et un deuxième noeud d'entrée (i2) couplés respectivement à une première entrée et une deuxième entrée d'une paire différentielle double (Q2 à Q5) formée par les première et deuxième paires différentielles ;
un premier commutateur (S2) configuré pour coupler de manière sélective le deuxième noeud d'entrée (i2) à un diviseur de tension (Q6, Q7) ; et
un deuxième ensemble de commutateurs (S11) configurés pour shunter de manière sélective un troisième et un quatrième transistor à structure métal oxyde semi-conducteur complémentaire (Q21, Q22), dans lequel les troisième et quatrième transistors à structure métal oxyde semi-conducteur complémentaire sont respectivement en série avec une première sortie et une deuxième sortie de la paire différentielle double (Q2 à Q5).

3. Appareil comprenant des éléments de circuit de récepteur (14) configurés pour recevoir des données en provenance d'un circuit intégré (1), lesdits éléments de circuit de récepteur comprenant une pluralité de transistors à structure métal oxyde semi-conducteur complémentaire (Q8 à Q18) qui sont interconnectés de manière sélective les uns aux autres par une pluralité de commutateurs (S3, S6, S7) de manière à pouvoir être exploité en tant que chacun des éléments suivant :

deux liaisons en mode courant ou tension à sortie unique ; et
une unique liaison en mode courant ou tension différentielle ;
dans lequel les éléments de circuit de récepteur

(14) comprennent :
un premier ensemble de commutateurs (S3) configurés pour coupler de manière sélective une résistance de rétroaction (Q8, Q9 ; Q11, 12) entre les entrées et les sorties (o1, o2) des éléments de circuit de récepteur ;
un deuxième ensemble de commutateurs (S6) configurés pour coupler de manière sélective une résistance (Q8, Q9 ; Q11, 12) à un diviseur de tension (Q10, Q13) ; et
un troisième ensemble de commutateurs (S7) configurés pour ;
changer de manière sélective un premier transistor à structure métal oxyde semi-conducteur complémentaire (Q14A), situé dans une queue d'une première paire différentielle (Q15, Q16), depuis un état dans lequel il est capable de fournir une source de courant à un état dans lequel il est capable de fournir une résistance à la queue de la première paire différentielle (Q15, Q16), et
changer de manière sélective un deuxième transistor à structure métal oxyde semi-conducteur complémentaire (Q14B), situé dans une queue d'une deuxième paire différentielle (Q17, Q18), depuis un état dans lequel il est capable de fournir une source de courant à un état dans lequel il est capable de fournir une résistance à la queue de la deuxième paire différentielle (Q17, Q18).

4. Appareil selon la revendication 3, comprenant en outre :

un quatrième ensemble de commutateurs (S8) configurés pour coupler de manière sélective une grille d'un troisième transistor à structure métal oxyde semi-conducteur complémentaire (Q19) à une première sortie (o1) des éléments de circuit de récepteur et pour coupler de manière sélective une grille d'un quatrième transistor à structure métal oxyde semi-conducteur complémentaire (Q20) à une deuxième sortie (o2) des éléments de circuit de récepteur, dans lequel le troisième transistor (Q19) est couplé entre une première entrée du récepteur et une alimentation électrique (VDD2), et le quatrième transistor à structure métal oxyde semi-conducteur complémentaire (Q20) est couplé entre une deuxième entrée du récepteur et le bloc d'alimentation électrique (VDD22) ;
un cinquième ensemble de commutateurs (S9) configurés pour coupler les grilles des troisième et quatrième transistors à structure métal oxyde semi-conducteur complémentaire (Q19, Q20) au bloc d'alimentation électrique (VDD2) ; et
un sixième ensemble de commutateurs (S12) configurés pour shunter de manière sélective un cinquième et un sixième transistor à structure métal oxyde semi-conducteur complémentaire (Q23, Q24), dans lequel les cinquième et sixième transistors à structure métal oxyde semi-conducteur complémentaire sont respectivement en série avec les première et deuxième entrées du récepteur.

5. Circuit d'entrée/sortie multimode (10) comprenant :

le dispositif selon l'une quelconque des revendications 1 et 2, et
le dispositif selon l'une quelconque des revendications 3 et 4.

6. Circuit d'entrée/sortie multimode (10) selon la revendication 5, dans lequel lesdits éléments de circuit d'émetteur (12) sont configurés pour envoyer des données audit circuit intégré (2) sur une première paire de conducteurs (W1, W2) disposés de manière adjacente, et dans lequel lesdits éléments de circuit de récepteur (14) sont configurés pour recevoir des données en provenance dudit circuit intégré (2) sur une deuxième paire de conducteurs disposés de manière adjacente,

7. Circuit d'entrée/sortie multimode (10) selon la revendication 5, dans lequel lesdits éléments de circuit d'émetteur (12) et lesdits éléments de circuit de récepteur (14) sont configurés de manière sélective par des commutateurs (S1:S3, S6:S9) pour fonctionner dans une condition dans laquelle une tension d'alimentation électrique (VDD1) desdits éléments de circuit d'émetteur est égale à une tension d'alimentation électrique (VDD2) desdits éléments de circuit de récepteur dans ledit circuit intégré (2), pour fonctionner dans une condition dans laquelle la tension d'alimentation électrique desdits éléments de circuit d'émetteur est inférieure à la tension d'alimentation électrique desdits éléments de circuit de récepteur dans ledit circuit intégré, et pour fonctionner dans une condition dans laquelle la tension d'alimentation électrique desdits éléments de circuit d'émetteur est supérieure à la tension d'alimentation électrique desdits éléments de circuit de récepteur dans ledit circuit intégré.

8. Circuit d'entrée/sortie multimode (10) selon la revendication 5, dans lequel lesdits éléments de circuit d'émetteur (12) et lesdits éléments de circuit de récepteur (14) sont configurés de manière sélective par des commutateurs (S1:S3, S6:S9) pour fonctionner dans un des modes parmi une pluralité de modes de liaison à niveaux de tension métal oxyde semi-conducteur complémentaire à sortie unique double, dans lequel, dans un premier mode, une tension d'alimentation électrique (VDD1) desdits éléments de circuit d'émetteur est égale à une tension d'ali-

mentation électrique (VDD2) desdits éléments de circuit de récepteur dans ledit circuit intégré (2), dans lequel, dans un deuxième mode, la tension d'alimentation électrique desdits éléments de circuit d'émetteur est inférieure à la tension d'alimentation électrique desdits éléments de circuit de récepteur dans ledit circuit intégré, et dans lequel, dans un troisième mode, la tension d'alimentation électrique desdits éléments de circuit d'émetteur est supérieure à la tension d'alimentation électrique desdits éléments de circuit de récepteur dans ledit circuit intégré.

9. Circuit d'entrée/sortie multimode (10) selon la revendication 5, dans lequel lesdits éléments de circuit d'émetteur (12) et lesdits éléments de circuit de récepteur (14) sont configurés de manière sélective par des commutateurs (S1: S3, S6: S9) pour fonctionner dans un des modes parmi ladite pluralité de modes de liaison à niveaux de tension métal oxyde semi-conducteur complémentaire à sortie unique double, ou dans lesdites liaisons en mode de tension ou de courant différentielles, et dans lequel les circuits intégrés (1, 2) au niveau chaque extrémité de la liaison peuvent fonctionner avec différentes tensions d'alimentation électrique.

10. Circuit d'entrée/sortie multimode selon la revendication 5, dans lequel lesdits éléments de circuit d'émetteur (12) et lesdits éléments de circuit de récepteur (14) sont configurés de manière sélective par des commutateurs (S1:S3, S6:S9) pour fonctionner dans une liaison en mode tension à sortie unique double.

11. Circuit d'entrée/sortie multimode (10) selon la revendication 5, dans lequel lesdits éléments de circuit d'émetteur (12) et lesdits éléments de circuit de récepteur (14) sont configurés de manière sélective par des commutateurs (S1:S3, S6:S9) pour fonctionner dans une liaison en mode courant à sortie unique double.

12. Circuit d'entrée/sortie, multimode (10) selon la revendication 5, dans lequel lesdits éléments de circuit d'émetteur (12) et lesdits éléments de circuit de récepteur (14) sont configurés de manière sélective par des commutateurs (S1:S3, S6:S9) pour fonctionner dans un mode défini par une liaison en mode tension différentielle unique avec une commande d'entrée à sortie unique.

13. Circuit d'entrée/sortie multimode (10) selon la revendication 5, dans lequel lesdits éléments de circuit d'émetteur (12) et lesdits éléments de circuit de récepteur (14) sont configurés de manière sélective par des commutateurs (S1:S3, S6:S9) pour fonctionner dans un mode défini par une liaison en mode tension différentielle unique avec une commande d'entrée différentielle.

14. Circuit d'entrée/sortie multimode (10) selon la revendication 5, dans lequel lesdits éléments de circuit d'émetteur (12) et lesdits éléments de circuit de récepteur (14) sont configurés de manière sélective par des commutateurs (S1:S3, S6:S9) pour fonctionner dans un mode défini par une liaison en mode courant différentielle unique avec une commande d'entrée à sortie unique.

15. Circuit d'entrée/sortie multimode (10) selon la revendication 5, dans lequel lesdits éléments de circuit d'émetteur (12) et lesdits éléments de circuit de récepteur (14) sont configurés de manière sélective par des commutateurs (S1:S3, S6:S9) pour fonctionner dans un mode défini par une liaison en mode courant différentielle unique avec une commande d'entrée différentielle.

16. Circuit d'entrée/sortie multimode (10) selon la revendication 5, dans lequel certains commutateurs sont prévus pour convertir lesdits éléments de circuit d'entrée/sortie soit en ladite configuration d'éléments de circuit d'émetteur (12), soit en ladite configuration d'éléments de circuit de récepteur (14).

17. Circuit d'entrée/sortie multimode (10) selon la revendication 5, dans lequel les circuits intégrés (1, 2) sont situés dans un dispositif de communication sans fil.

18. Circuit d'entrée/sortie multimode (10) selon la revendication 5, dans lequel les circuits intégrés (1, 2) sont situés dans un dispositif accessoire pour un dispositif de communication sans fil.

19. Circuit d'entrée/sortie multimode (10) selon la revendication 5, dans lequel les circuits intégrés, (1, 2) sont situés dans une interface entre un dispositif de communication sans fil et un dispositif accessoire pour le dispositif de communication sans fil.

20. Procédé comprenant les étapes consistant à :

fournir au moins deux circuits intégrés (1, 2) pour contenir chacun au moins un circuit d'entrée/sortie (10), ledit circuit d'entrée/sortie comprenant au moins soit des éléments de circuit d'émetteur (12) soit des éléments de circuit de récepteur (14), les éléments de circuit d'émetteur étant configurés pour envoyer des données à l'un desdits au moins deux circuits intégrés (2), et les éléments de circuit de récepteur étant configurés pour recevoir des données en provenance de l'autre desdits au moins deux circuits intégrés (1), le circuit d'entrée/sortie étant construit à partir de transistors à structure métal oxyde semi-conducteur complémentaire (Q1A: Q24) ; et interconnectant ensembles de manière sélective les transistors à structure métal oxy-

de semi-conducteur complémentaire avec les commutateurs (S1:S3, S6:S9) de manière à ce qu'ils puissent être exploités en tant que chacun des éléments suivants :
deux liaisons en mode courant ou tension à sortie unique ; et
en tant que liaison en mode courant ou tension différentielle unique ;
dans lequel les éléments de circuit d'émetteur (12) comprennent :
un premier ensemble de commutateurs (S1) configurés pour :
changer de manière sélective un premier transistor à structure métal oxyde semi-conducteur complémentaire (Q1A), situé dans une queue d'une première paire différentielle (Q2, Q3), depuis un état dans lequel il est capable de fournir une source de courant à un état dans lequel il est capable de fournir une résistance à la queue de la première paire différentielle (Q2, Q3), et
changer de manière sélective un deuxième transistor à structure métal oxyde semi-conducteur complémentaire (Q1B), situé dans une queue d'une deuxième paire différentielle (Q4, Q5), depuis un état dans lequel il est capable de fournir une source de courant à un état dans lequel il est capable de fournir une résistance à la queue de la deuxième paire différentielle (Q4, Q5).
dans lequel les éléments de circuit de récepteur (14) comprennent :
un premier ensemble de commutateurs (53) configurés pour coupler de manière sélective une résistance de rétroaction (Q8, Q9 ; Q11, 12) entre les entrées et les sorties (o1, o2) des éléments de circuit de récepteur;
un deuxième ensemble de commutateurs (S6) configurés pour coupler de manière sélective une résistance (Q8, Q9 ; Q11, 12) à un diviseur de tension (Q10, Q13) ; et
un troisième ensemble de commutateurs (S7) configurés pour :
changer de manière sélective un premier transistor à structure métal oxyde semi-conducteur complémentaire (Q14A), situé dans une queue d'une première paire différentielle (Q15, Q16), depuis un état dans lequel il est capable de fournir une source de courant à un état dans lequel il est capable de fournir une résistance à la queue de la première paire différentielle (Q15, Q16), et
changer de manière sélective un deuxième transistor à structure métal oxyde semi-conducteur complémentaire (Q14B), situé dans une queue d'une deuxième paire différentielle (Q17, Q18), depuis un état dans lequel il est capable de fournir une source de courant à un état dans lequel il est capable de fournir une résistance à la queue de la deuxième paire différentielle (Q17, Q18).

21. Procédé selon la revendication 20, dans lequel lesdits éléments de circuit d'émetteur (12) envoient des données auxdits éléments de circuit de récepteur (14) dans ledit un desdits au moins deux circuits intégrés (2) sur une première paire de conducteurs (W1, W2) disposés de manière adjacente, et dans lequel lesdits éléments de circuit de récepteur reçoivent des données en provenance desdits éléments de circuit d'émetteur dans ledit autre desdits au moins deux circuits intégrés (1) sur une deuxième paire de conducteurs disposés de manière adjacente.

22. Procédé selon la revendication 20, dans lequel lesdits éléments de circuit d'émetteur (12) et lesdits éléments de circuit de récepteur (14) sont configurés de manière sélective par des commutateurs (S1:S3, S6:S9) pour fonctionner dans une condition dans laquelle une tension d'alimentation électrique (VDD1) desdits éléments de circuit d'émetteur est égale à une tension d'alimentation électrique (VDD2) desdits éléments de circuit de récepteur dans ledit un desdits au moins deux circuits intégrés (2), pour fonctionner dans une condition dans laquelle la tension d'alimentation électrique desdits éléments de circuit d'émetteur est inférieure à la tension d'alimentation électrique desdits éléments de circuit de récepteur dans ledit un desdits au moins deux circuits intégrés (2), et pour fonctionner dans une condition dans laquelle la tension d'alimentation électrique desdits éléments de circuit d'émetteur est supérieure à la tension d'alimentation électrique desdits éléments de circuit de récepteur dans ledit un desdits au moins deux circuits intégrés (2).

23. Procédé selon la revendication 20, dans lequel lesdits éléments de circuit d'émetteur (12) et lesdits éléments de circuit de récepteur (14) sont configurés de manière sélective par des commutateurs (S1:S3, S6-S9) pour fonctionner dans un des modes parmi une pluralité de modes de liaison à niveaux de tension métal oxyde semi-conducteur complémentaire à sortie unique double, dans lequel, dans un premier mode, une tension d'alimentation électrique (VDD1) desdits éléments de circuit d'émetteur est égale à une tension d'alimentation électrique (VDD2) desdits éléments de circuit de récepteur dans ledit un desdits au moins deux circuits intégrés (2), dans lequel, dans un deuxième mode, la tension d'alimentation électrique desdits éléments de circuit d'émetteur est inférieure à la tension d'alimentation électrique desdits éléments de circuit de récepteur dans ledit un desdits au moins deux circuits intégrés (2), et dans lequel, dans un troisième mode, la tension d'alimentation électrique desdits éléments de circuit d'émetteur est supérieure à la tension d'alimentation

électrique desdits éléments de circuit de récepteur dans ledit un desdits au moins deux circuits intégrés (2).

24. Procédé selon la revendication 20, dans lequel lesdits éléments de circuit d'émetteur (12) et lesdits éléments de circuit de récepteur (14) sont configurés de manière sélective par les commutateurs (S1:S3, S6:S9) pour fonctionner soit dans une liaison en mode tension à sortie unique double, soit dans une liaison en mode courant à sortie unique double.

25. Procédé selon la revendication 20, dans lequel lesdits éléments de circuit d'émetteur (12) et lesdits éléments de circuit de récepteur (14) sont configurés de manière sélective par des commutateurs (S1:S3, S6:S9) pour fonctionner dans un mode défini par une liaison en mode tension différentielle unique soit avec une commande d'entrée à sortie unique, soit avec une commande d'entrée différentielle.

26. Procédé selon la revendication 20, dans lequel lesdits éléments de circuit d'émetteur (12) et lesdits éléments de circuit de récepteur (14) sont configurés de manière sélective par les commutateurs (S1:S3, S6:S9) pour fonctionner dans un mode défini par une liaison en mode courant différentielle unique soit avec une commande d'entrée à sortie unique, soit avec une commande d'entrée différentielle,

27. Procédé selon la revendication 20, dans lequel lesdits éléments de circuit d'émetteur (12) et lesdits éléments de circuit de récepteur (14) sont configurés de manière sélective par lesdits commutateurs (S1: S3, S6 : S9) pour fonctionner dans un des modes parmi ladite pluralité de modes de liaison à niveaux de tension métal oxyde semi-couducteur complémentaire à sortie unique double, ou dans lesdites liaisons en mode tension ou courant différentielles, et dans lequel chacun desdits au moins deux circuits intégrés (1, 2) au niveau de chaque extrémité de la liaison peut fonctionner avec différentes tensions d'alimentation électrique.

28. Procédé selon la revendication 20, dans lequel certains commutateurs sont prévus pour convertir lesdits éléments de circuit d'entrée/sortie (10) soit en ladite configuration d'éléments de circuit d'émetteur (12), soit en ladite configuration d'éléments de circuit de récepteur (14).

29. Procédé selon la revendication 20, dans lequel lesdits au moins deux circuits intégrés (1, 2) sont situés dans un dispositif de communication sans fil.

30. Procédé selon la revendication 20, dans lequel lesdits au moins deux circuits intégrés (1, 2) sont situés dans un dispositif accessoire pour un dispositif de communication sans fil.

31. Procédé selon la revendication 20, dans lequel lesdits au moins deux circuits intégrés (1, 2) sont situés dans une interface entre un dispositif de communication sans fil et un dispositif accessoire pour le dispositif de communication sans fil.

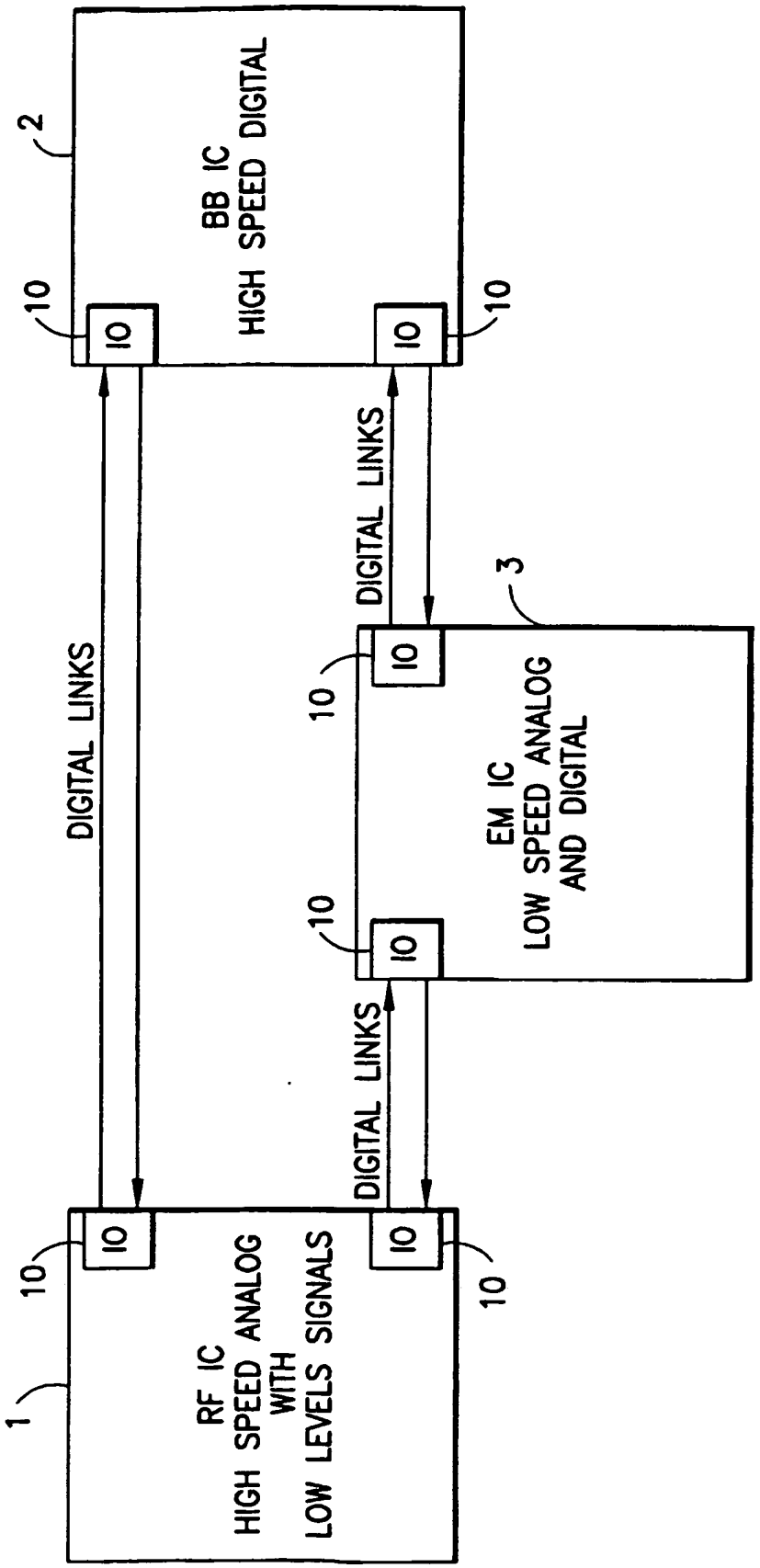

BB IC
HIGH SPEED DIGITAL
2
10
10
DIGITAL LINKS
DIGITAL LINKS
3
10
EM IC
LOW SPEED ANALOG
AND DIGITAL
10
DIGITAL LINKS
10
10
RF IC
HIGH SPEED ANALOG
WITH
LOW LEVELS SIGNALS
1

FIG.1

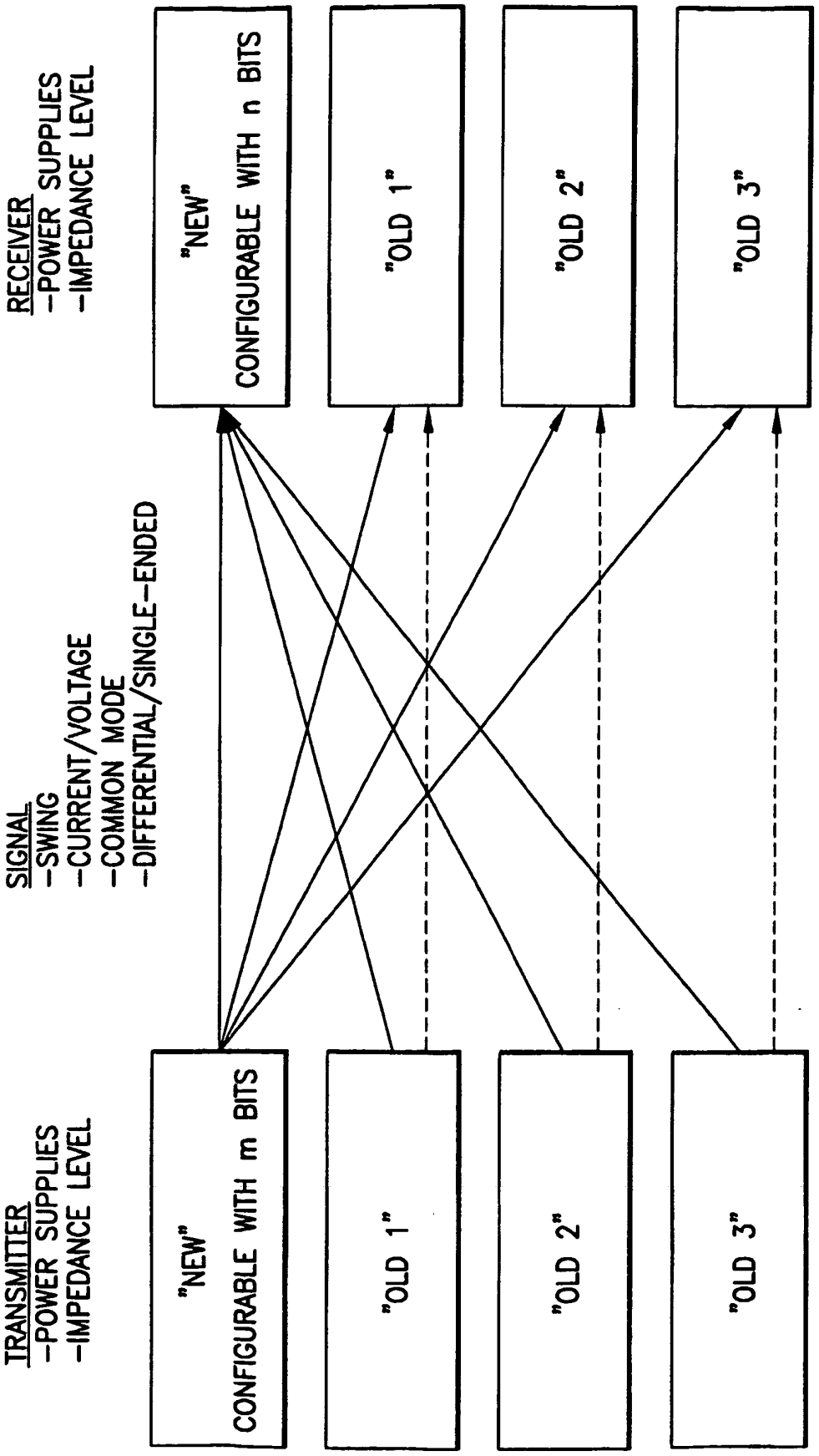

TRANSMITTER
-POWER SUPPLIES
-IMPEDANCE LEVEL
SIGNAL
-SWING
-CURRENT/VOLTAGE
-COMMON MODE
-DIFFERENTIAL/SINGLE-ENDED
RECEIVER
-POWER SUPPLIES
-IMPEDANCE LEVEL
"NEW" CONFIGURABLE WITH m BITS
"OLD 1"
"OLD 2"
"OLD 3"
"NEW" CONFIGURABLE WITH n BITS
"OLD 1"
"OLD 2"
"OLD 3"

FIG.2

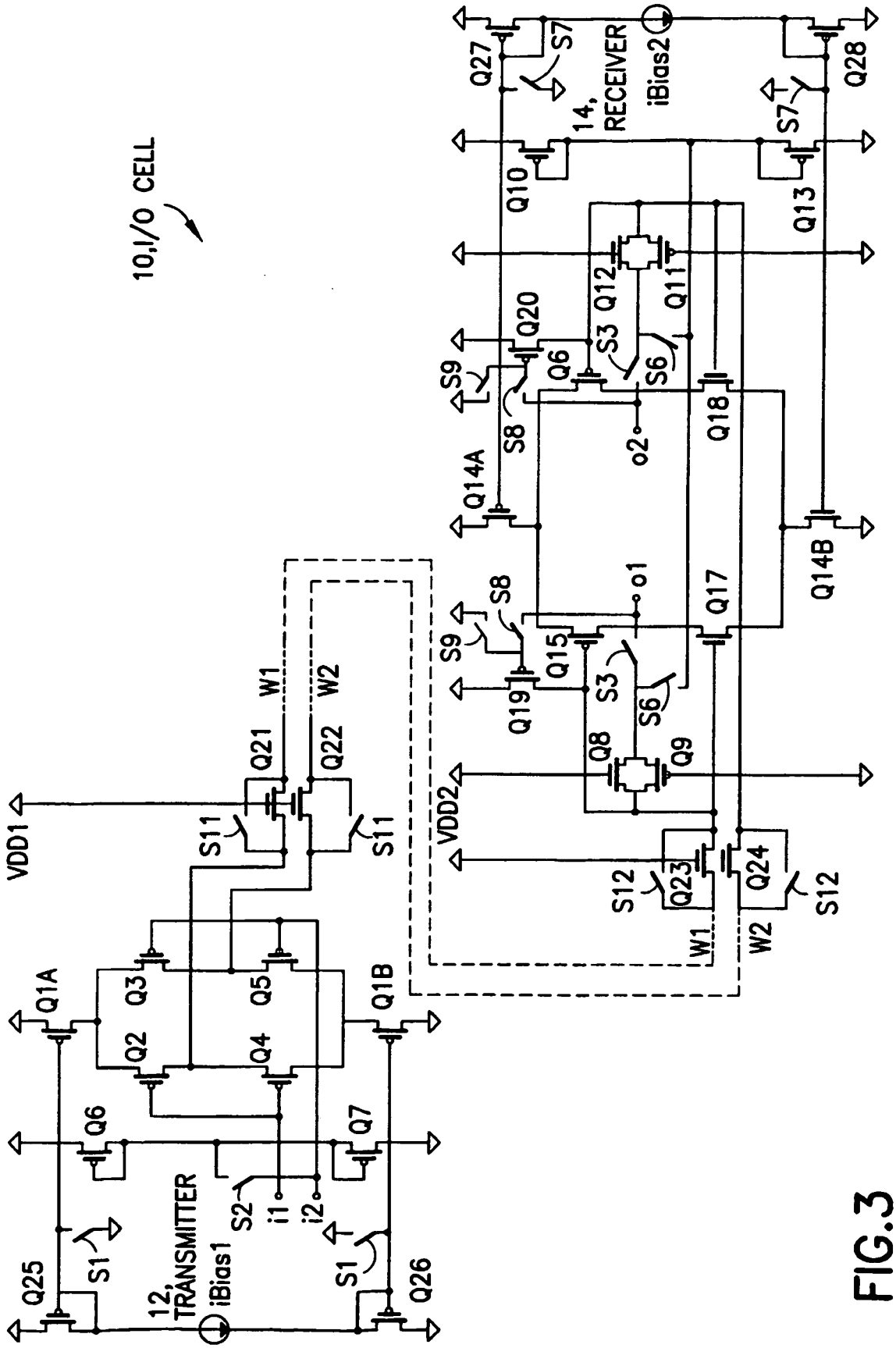

10,I/O CELL
VDD1
VDD2
Q1A
Q1B
Q2
Q3
Q4
Q5
Q6
Q7
Q10
Q11
Q12
Q13
Q14A
Q14B
Q15
Q17
Q18
Q19
Q20
Q21
Q22
Q23
Q24
Q25
Q26
Q27
Q28
Q8
Q9
S1
S2
S3
S6
S7
S8
S9
S11
S12
W1
W2
i1
i2
o1
o2
12,
TRANSMITTER
iBias1
14,
RECEIVER
iBias2

FIG.3

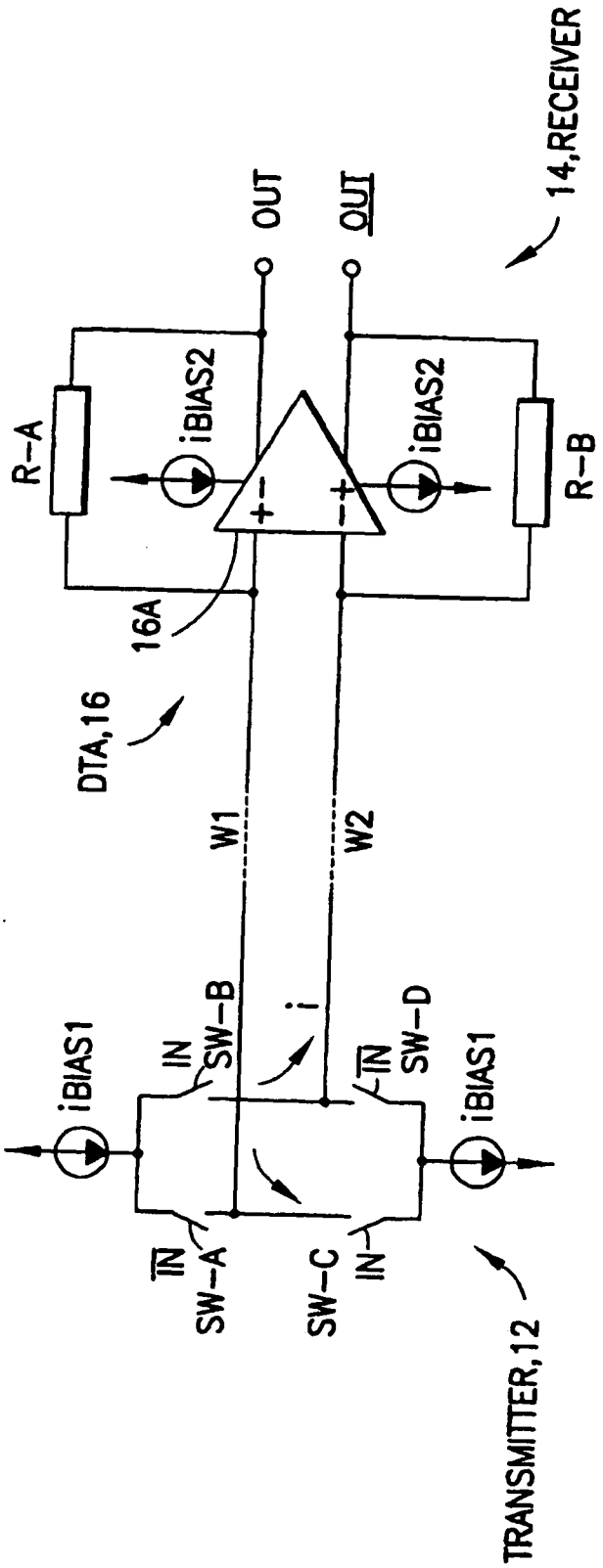

14,RECEIVER
OUT
OUT
R-A
iBIAS2
iBIAS2
R-B
16A
DTA,16
W1
W2
iBIAS1
IN
SW-B
i
IN
SW-D
iBIAS1
IN
SW-A
SW-C
IN
TRANSMITTER,12
OUT
OUT
IN
IN

FIG.4

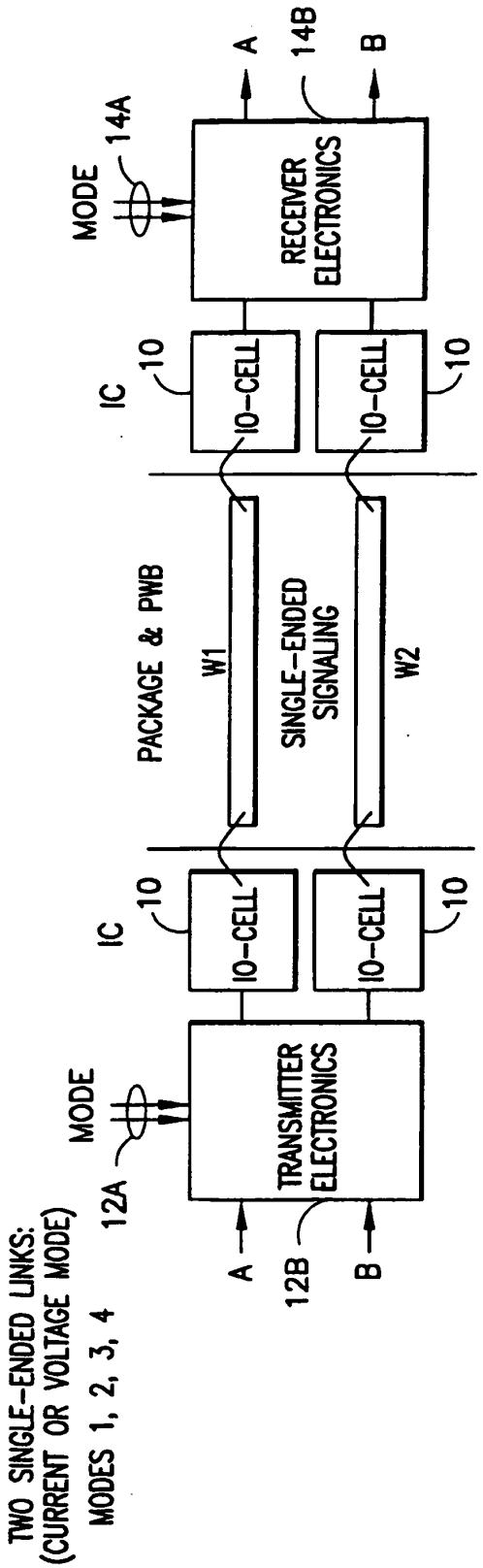

TWO SINGLE-ENDED LINKS:
(CURRENT OR VOLTAGE MODE)
MODES 1, 2, 3, 4
MODE
12A
TRANSMITTER ELECTRONICS
IC
10
IO-CELL
IO-CELL
10
PACKAGE & PWB
W1
SINGLE-ENDED SIGNALING
W2
A
12B
B
MODE
14A
RECEIVER ELECTRONICS
IC
10
IO-CELL
IO-CELL
10
A
14B
B

FIG.5A

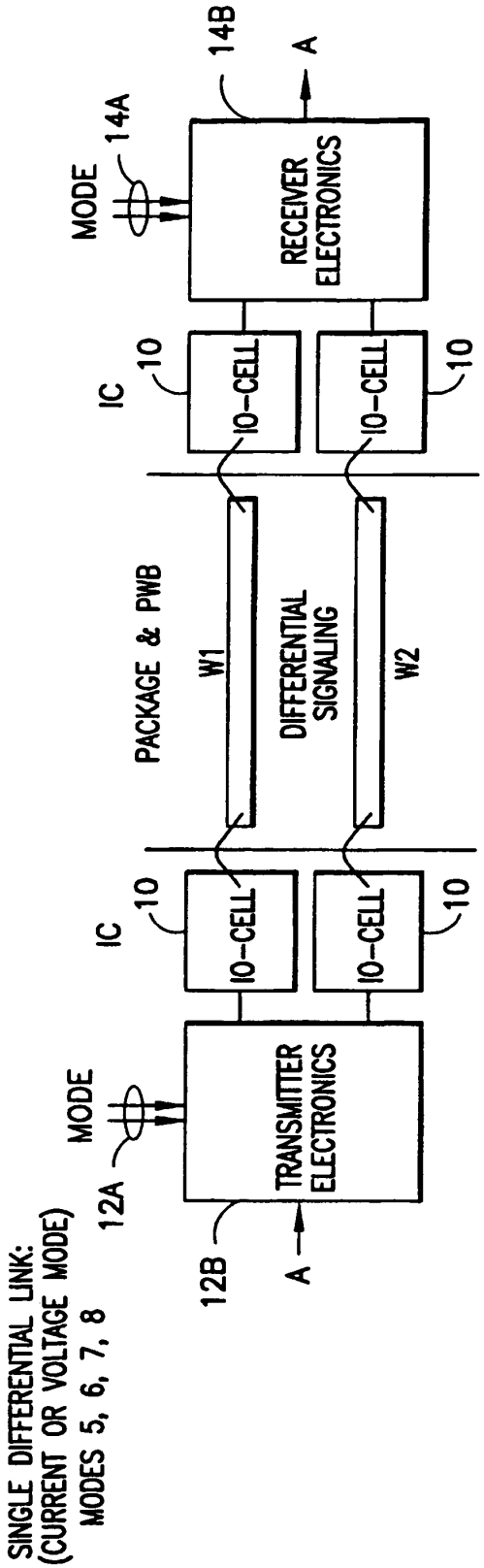

SINGLE DIFFERENTIAL LINK:
(CURRENT OR VOLTAGE MODE)
MODES 5, 6, 7, 8
MODE
12A
TRANSMITTER ELECTRONICS
IC
10
IO-CELL
IO-CELL
10
PACKAGE & PWB
W1
DIFFERENTIAL SIGNALING
W2
12B
A
MODE
14A
RECEIVER ELECTRONICS
IC
10
IO-CELL
IO-CELL
10
A
14B

FIG.5B

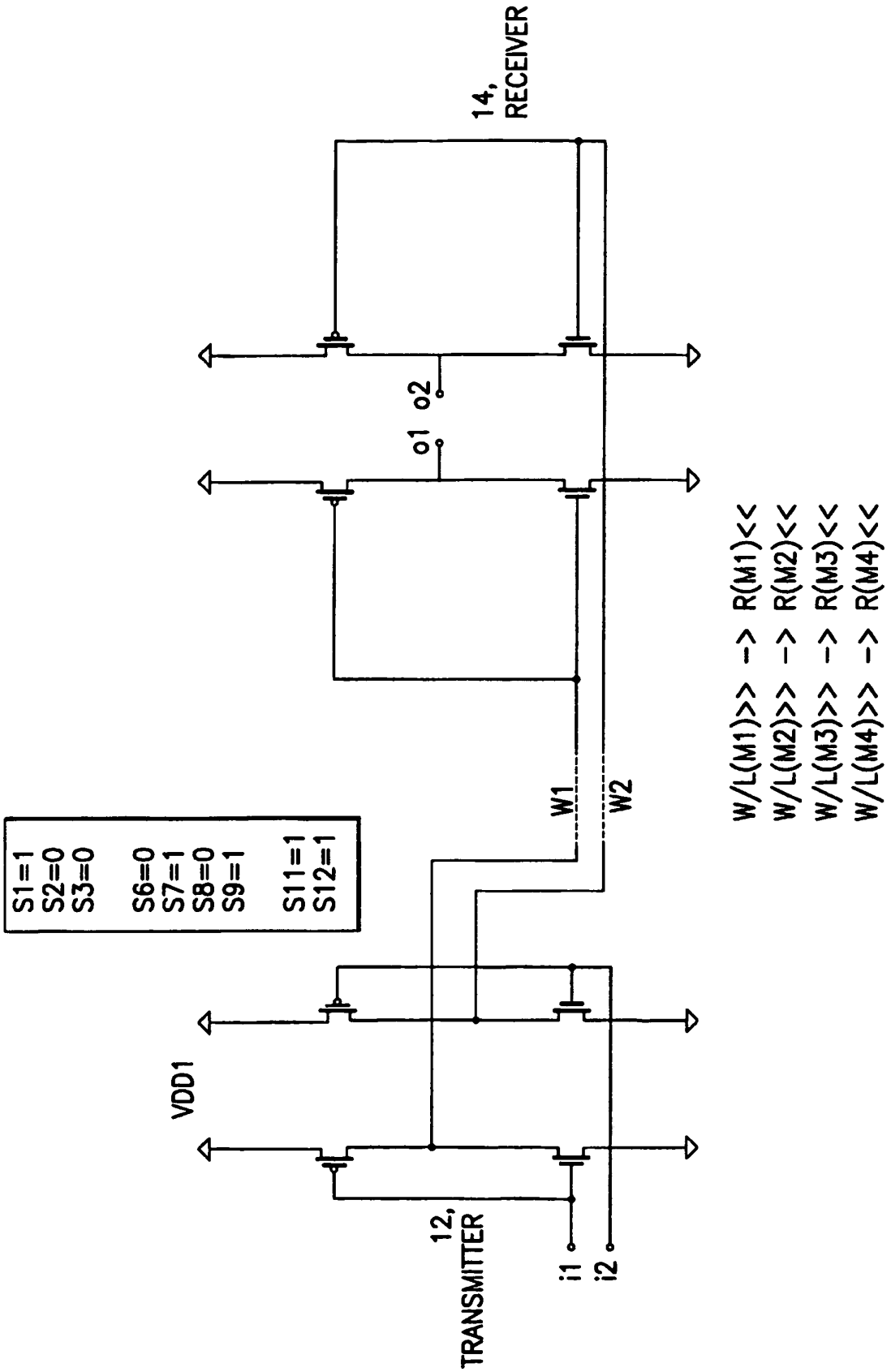

14,
RECEIVER
o2
o1
W1
W2
S1=1
S2=0
S3=0
S6=0
S7=1
S8=0
S9=1
S11=1
S12=1
VDD1
12,
TRANSMITTER
i1
i2
W/L(M1)>> -> R(M1)<<
W/L(M2)>> -> R(M2)<<
W/L(M3)>> -> R(M3)<<
W/L(M4)>> -> R(M4)<<

FIG.6

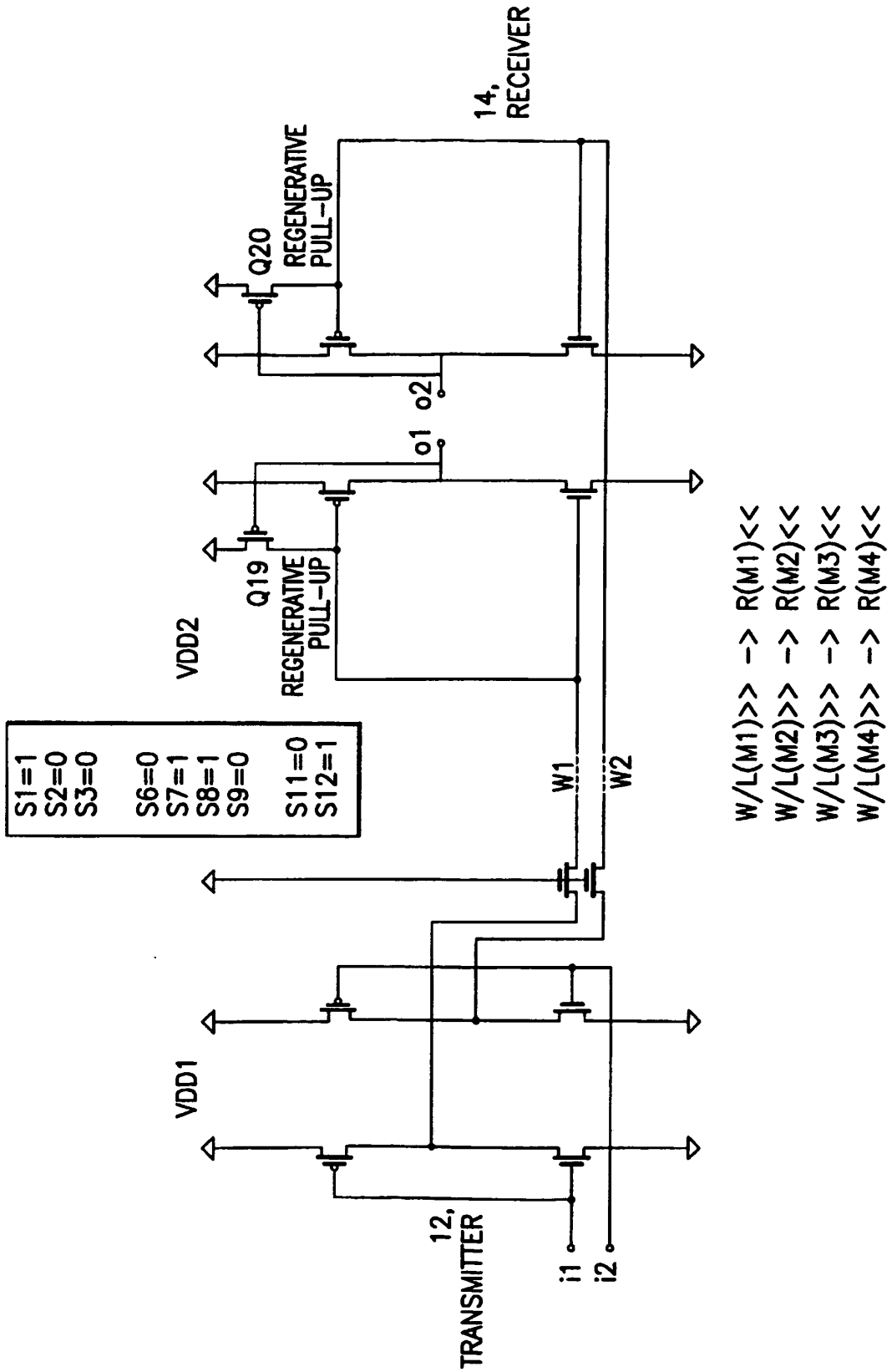

14,
RECEIVER
Q20
REGENERATIVE
PULL-UP
o2
o1
Q19
REGENERATIVE
PULL-UP
VDD2
S1=1
S2=0
S3=0
S6=0
S7=1
S8=1
S9=0
S11=0
S12=1
W1
W2
W/L(M1)>> -> R(M1)<<
W/L(M2)>> -> R(M2)<<
W/L(M3)>> -> R(M3)<<
W/L(M4)>> -> R(M4)<<
VDD1
12,
TRANSMITTER
i1
i2

FIG.7

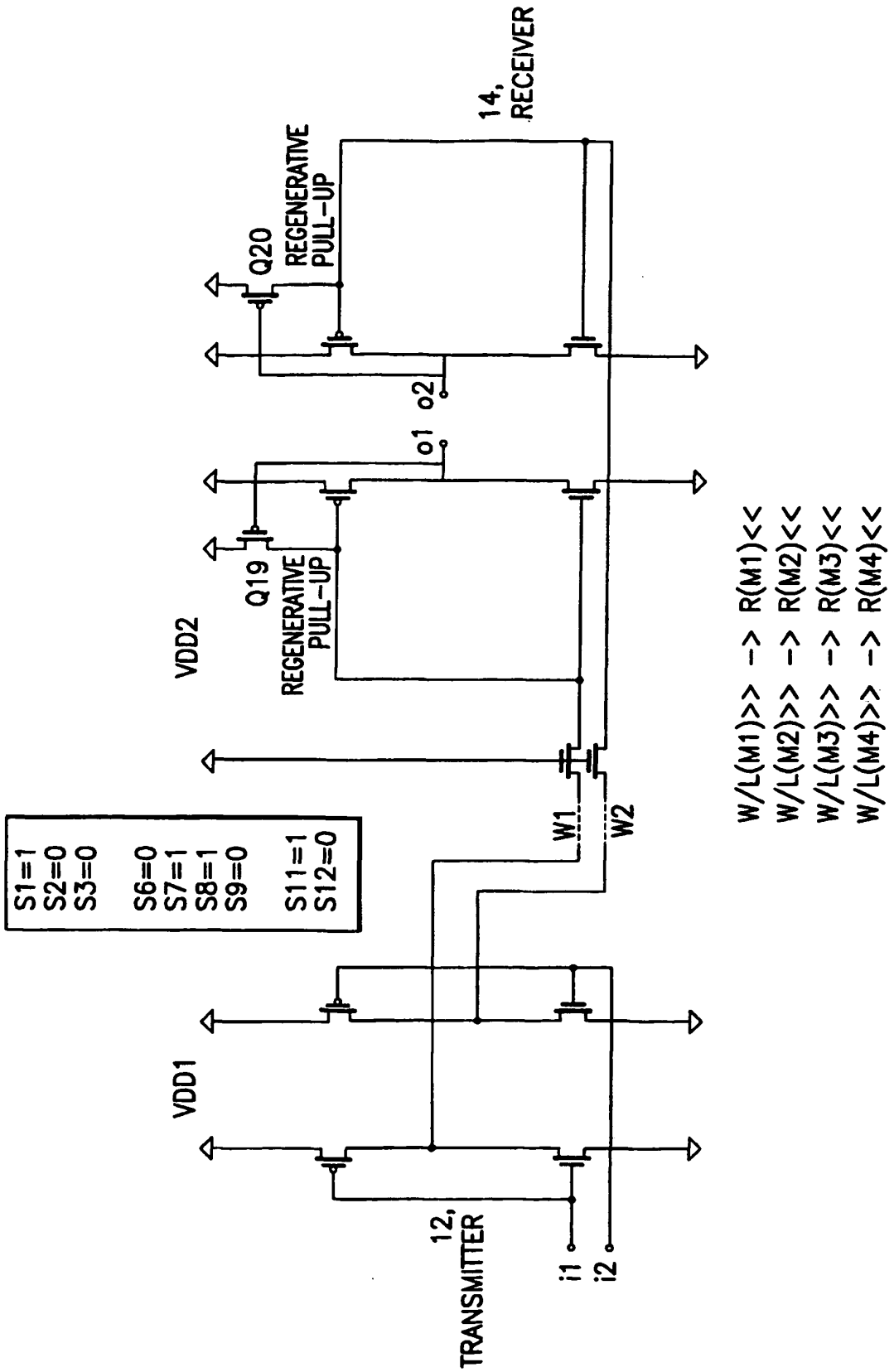

14, RECEIVER
Q20 REGENERATIVE PULL-UP
o2
o1
Q19 REGENERATIVE PULL-UP
VDD2
W1
W2
S1=1 S2=0 S3=0 S6=0 S7=1 S8=1 S9=0 S11=1 S12=0
VDD1
12, TRANSMITTER
i1
i2
W/L(M1)>> -> R(M1)<<
W/L(M2)>> -> R(M2)<<
W/L(M3)>> -> R(M3)<<
W/L(M4)>> -> R(M4)<<

FIG.8

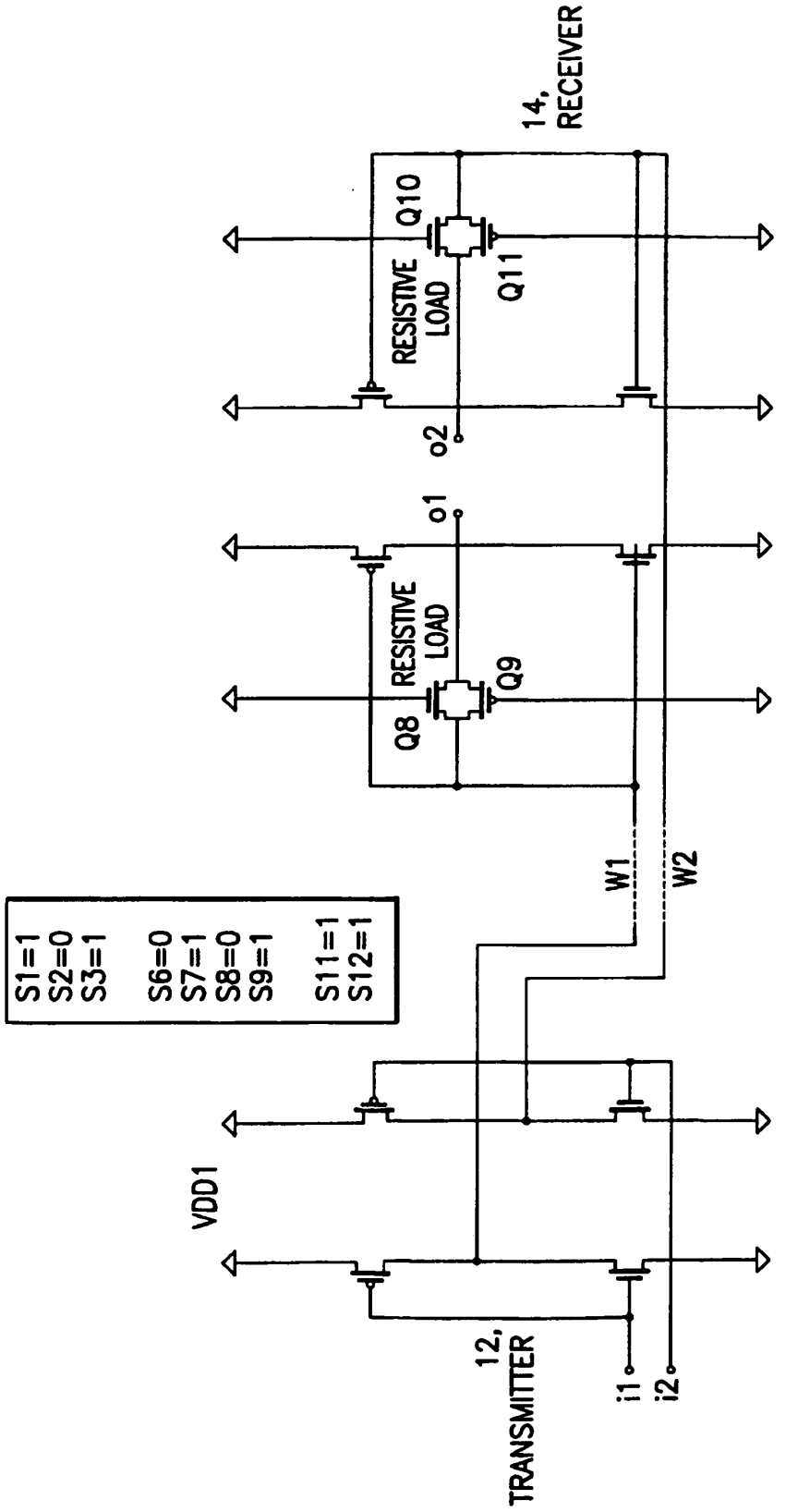

14,
RECEIVER
Q10
Q11
RESISTIVE
LOAD
o2
o1
Q8
Q9
RESISTIVE
LOAD
W1
W2
S1=1
S2=0
S3=1
S6=0
S7=1
S8=0
S9=1
S11=1
S12=1
VDD1
12,
TRANSMITTER
i1
i2
W/L(M1)>> -> R(M1)<<
W/L(M2)>> -> R(M2)<<
W/L(M3)>> -> R(M3)<<
W/L(M4)>> -> R(M4)<<

FIG.9

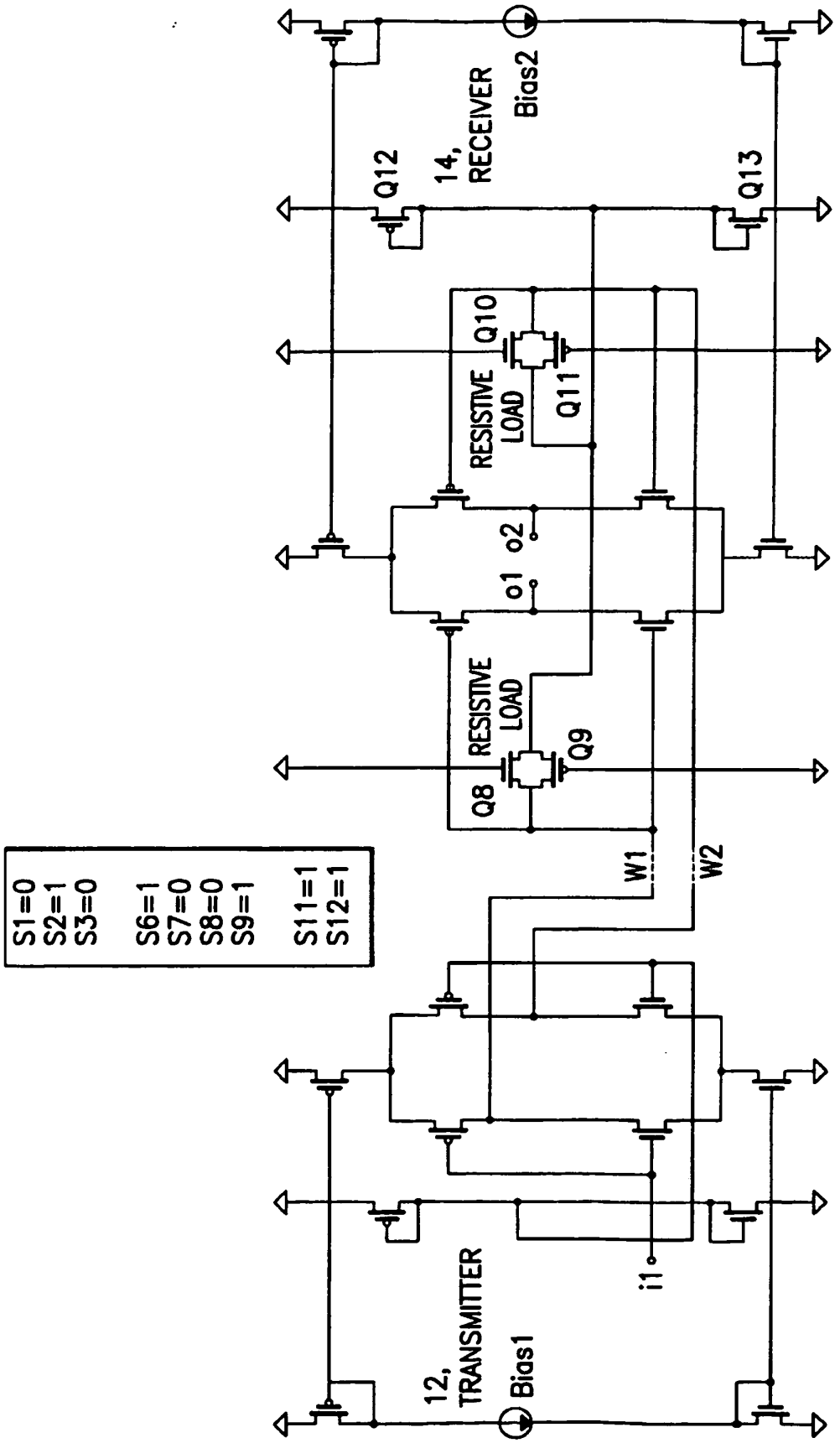

Bias2
14, RECEIVER
Q12
Q13
Q10
Q11
RESISTIVE LOAD
o2
o1
RESISTIVE LOAD
Q9
Q8
W1
W2
i1
12, TRANSMITTER
Bias1
S1=0
S2=1
S3=0
S6=1
S7=0
S8=0
S9=1
S11=1
S12=1

FIG.10

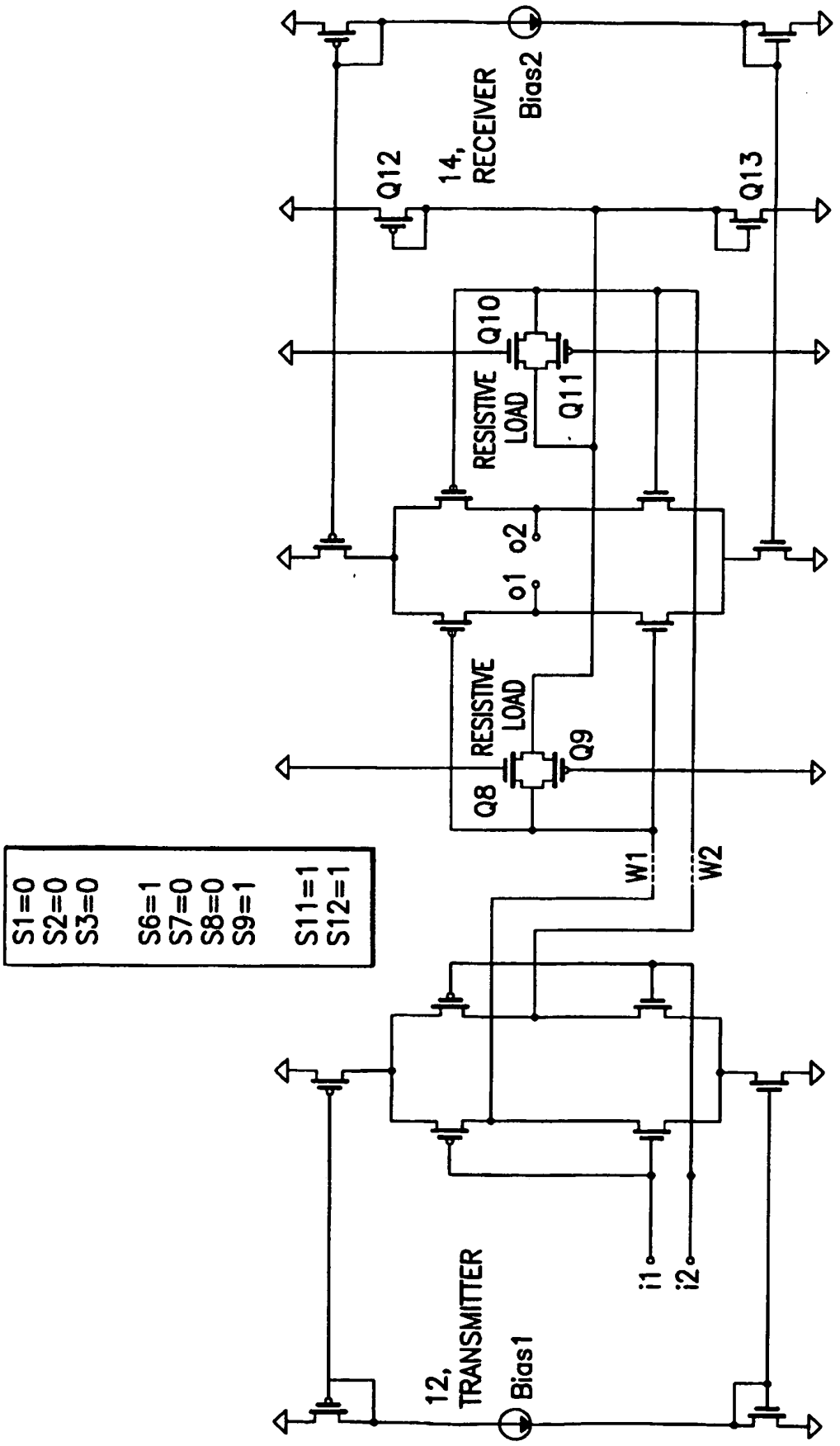

Bias2
14, RECEIVER
Q12
Q13
Q10
Q11
RESISTIVE LOAD
o1
o2
RESISTIVE LOAD
Q8
Q9
W1
W2
S1=0
S2=0
S3=0
S6=1
S7=0
S8=0
S9=1
S11=1
S12=1
i1
i2
12, TRANSMITTER
Bias1

FIG.11

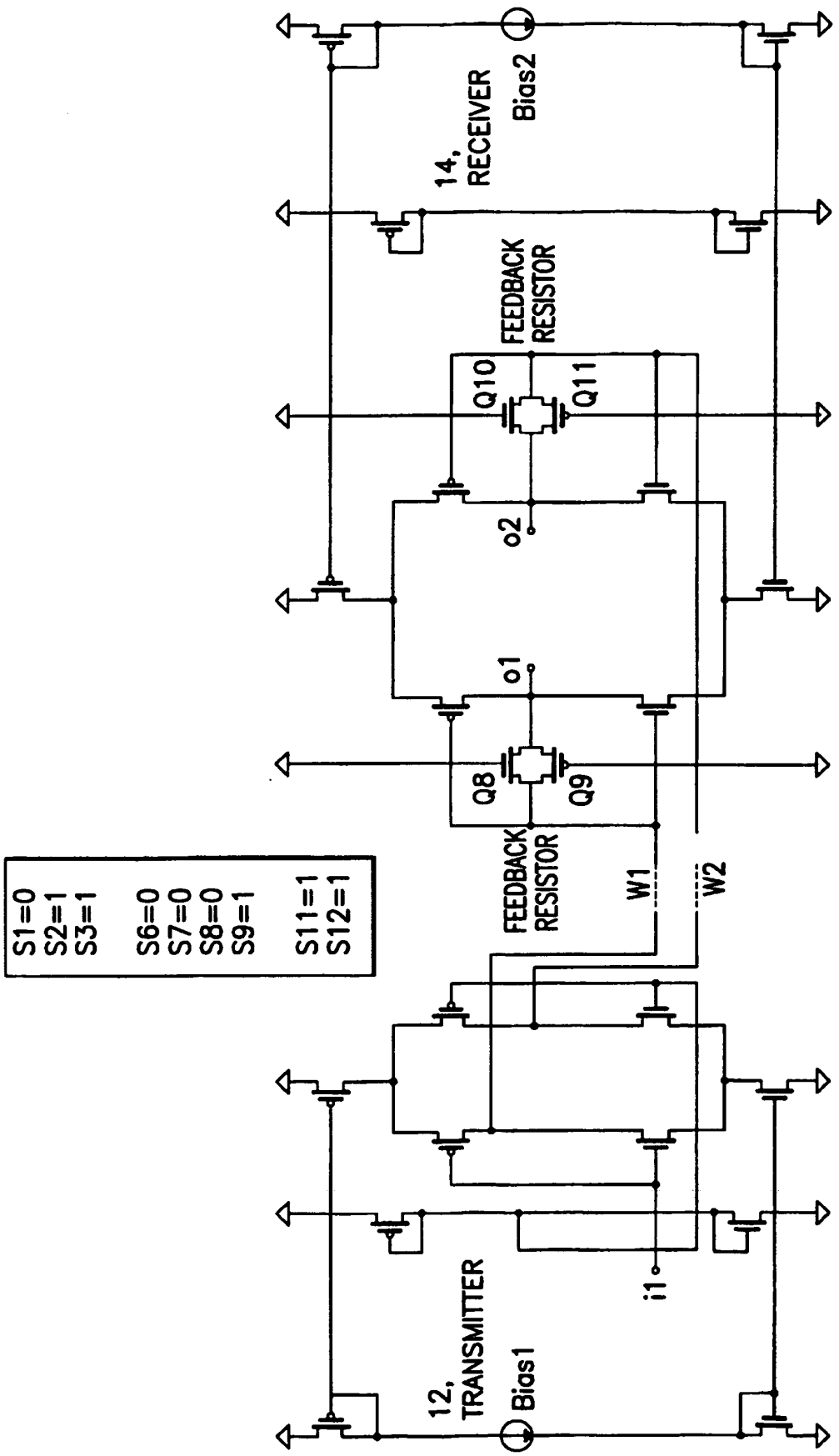

S1=0
S2=1
S3=1
S6=0
S7=0
S8=0
S9=1
S11=1
S12=1
14, RECEIVER
Bias2
FEEDBACK RESISTOR
Q10
Q11
o2
o1
Q8
Q9
FEEDBACK RESISTOR
W1
W2
i1
12, TRANSMITTER
Bias1

FIG.12

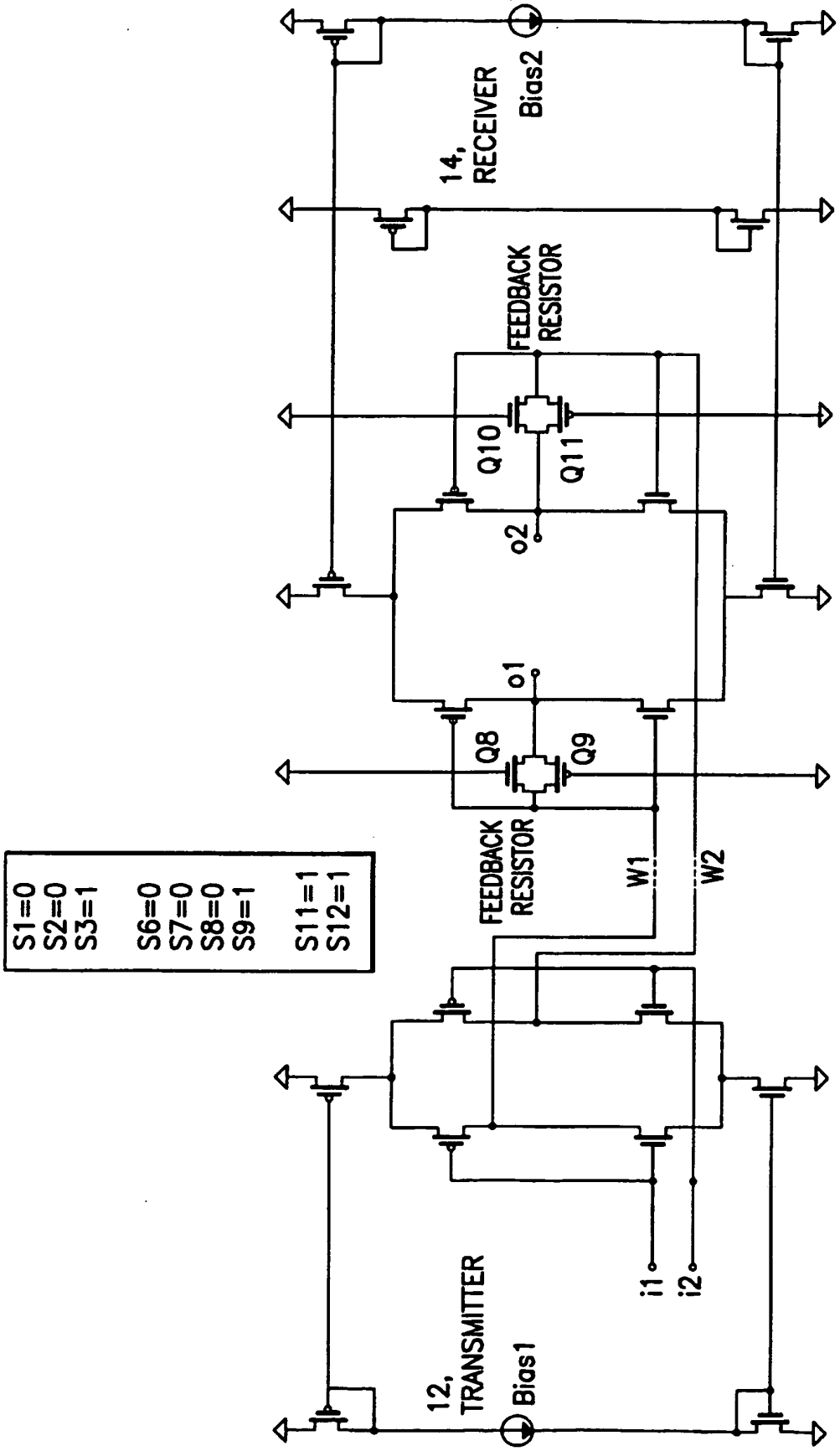

S1=0
S2=0
S3=1
S6=0
S7=0
S8=0
S9=1
S11=1
S12=1
12, TRANSMITTER
Bias1
14, RECEIVER
Bias2
FEEDBACK RESISTOR
FEEDBACK RESISTOR
Q8
Q9
Q10
Q11
o1
o2
W1
W2
i1
i2

FIG.13

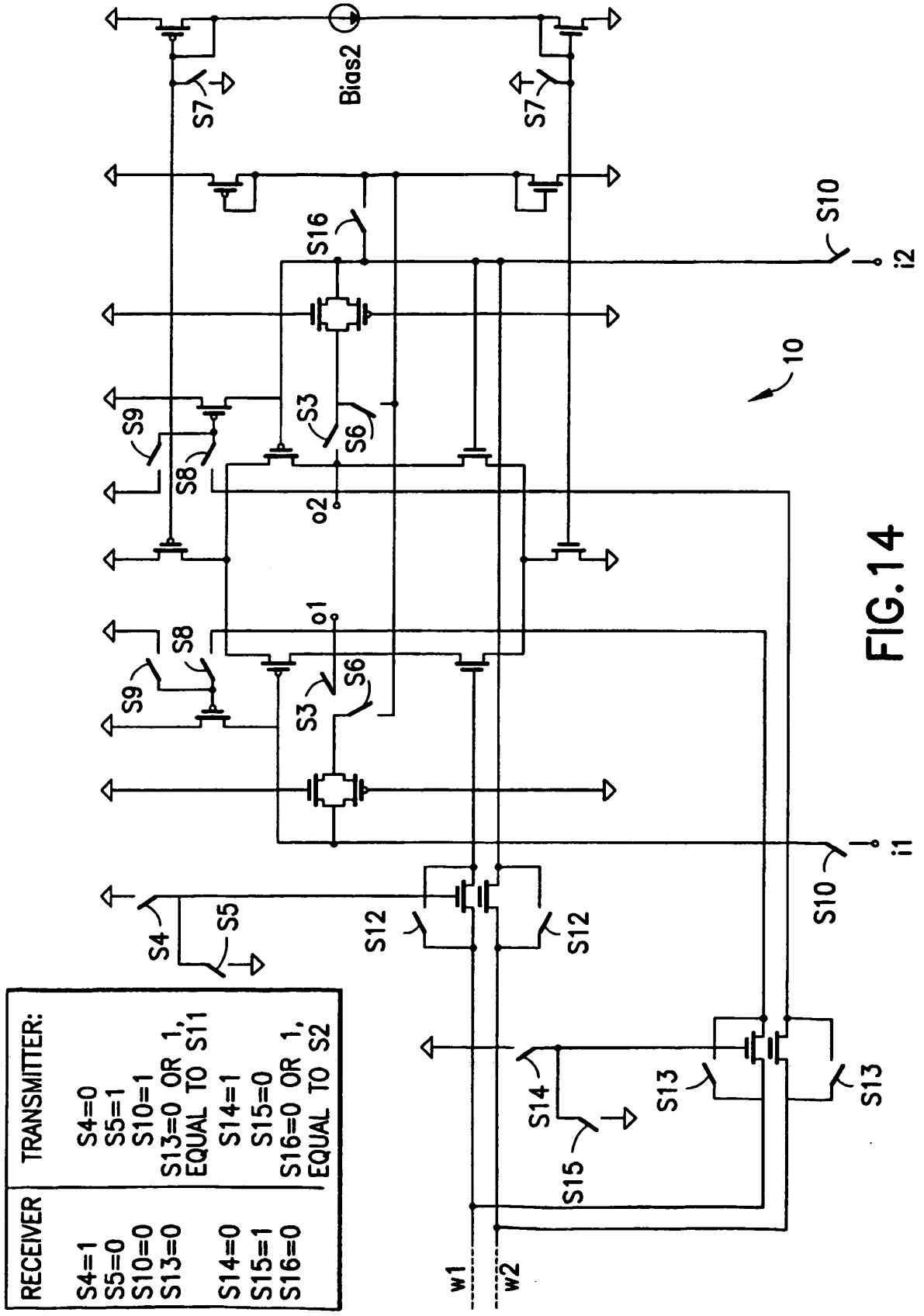

Bias2
S7
S7
S16
S10
i2
10
S9
S8
S3
S6
o2
o1
S8
S9
S3
S6
S4
S5
S12
S12
S10
i1
S14
S15
S13
S13
w1
w2
RECEIVER
S4=1
S5=0
S10=0
S13=0
S14=0
S15=1
S16=0
TRANSMITTER:
S4=0
S5=1
S10=1
S13=0 OR 1, EQUAL TO S11
S14=1
S15=0
S16=0 OR 1, EQUAL TO S2

FIG. 14

REFERENCES CITED IN THE DESCRIPTION

This list of references cited by the applicant is for the reader's convenience only. It does not form part of the European patent document. Even though great care has been taken in compiling the references, errors or omissions cannot be excluded and the EPO disclaims all liability in this regard.

Patent documents cited in the description

- EP 0482336 A1 **[0009]**
- US 6243776 B1 **[0010]**