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(54) **Correction of amplitude and phase imbalance in PSK receivers**

Korrektur von Amplituden- sowie Phasenungleichheiten in PSK-Empfängern

Correction de déséquilibrages d'amplitude et de phase dans des récepteurs MDP

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(56) References cited:
EP-A- 0 568 056 **WO-A-98/32221**
US-A- 4 085 378 **US-A- 5 263 196**

- **HIROSHI SUZUKI, HITOSHI YOSHIMO: "Affine transformations for compensating linear distortion: an application to linear signaling in mobile radio" ELECTRONICS & COMMUNICATIONS IN JAPAN, PART I - COMMUNICATIONS, vol. 75, no. 11, November 1992 (1992-11), pages 47-58, XP000368546 NEW YORK, US**
- **GLAS: "Digital I/Q imbalance compensation in a low-IF receiver" IEEE GLOBAL TELECOMMUNICATIONS CONFERENCE, 8 November 1998 (1998-11-08), pages 1461-1466, XP000805154 NEW YORK, US**

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Description

BACKGROUND OF THE INVENTION

Field of the Invention

[0001] The present invention relates generally to digital communication techniques. More specifically, the invention relates to an apparatus for balancing the amplitude and phase of a received, quadrature-phase modulated signal according to claim 1.

Description of the Prior Art

[0002] One of the common methods for modulating digital signals is the use of multilevel systems or *M*-ary techniques. *M*-ary modulation techniques are natural extensions of binary modulation techniques and apply to *L*-level amplitude or phase shift keying. A commonly used quadriphase scheme is called quadrature phase shift keying or QPSK. Like all of the *M*-ary amplitude or phase schemes, its principle advantage is bandwidth reduction.

[0003] Since pulse rate f_p is:

Equation 1

$$f_p = f_s \log_L M,$$

where f_s is the symbol rate and *M* is the number of messages; with *L* representing the number of modulation levels, the larger *L* is, the smaller the pulse rate and hence, the smaller the bandwidth.

[0004] In telecommunication applications, QPSK modulates two different signals into the same bandwidth creating a two-dimensional signal space. This is accomplished by creating a composite phase modulated signal using two carriers of the same frequency but having a phase difference of 90 degrees as shown in **Figure 1A.** By convention, the cosine carrier is called the in-phase component *I* and the sine carrier is the quadrature component *Q*. The *I* component is the real component of the signal and the *Q* component is the imaginary component of the signal. Each of the *I* and *Q* components are bi-phase modulated. A QPSK symbol consists of at least one sample from both the in-phase *I* and quadrature *Q* signals. The symbols may represent a quantized version of an analog sample or digital data.

[0005] All phase modulated schemes must overcome the inevitable problem of phase synchronization. For proper operation of QPSK signaling, the *I* and *Q* channels should have the same gain throughout processing both received channels, keeping the *I* and *Q* channels uncorrelated. Mismatched signal gains or magnitudes between the uncorrelated *I* and *Q* channels create errors when processing. Phase differences other than 90 degrees between the signals cause spillover between the channels and similarly result in degraded performance.

[0006] Typical receivers exhibit different overall gains for the separate *I* and *Q* channels due to mismatched gains in the mixers, filters, and A/D converters caused by variations in component values due in part to temperature, manufacturing tolerances and other factors. Amplitude and phase imbalance between the *I* and *Q* channels result in the distortions shown in **Figures 1B** and **1C**, decreasing overall signal-to-noise ratio (SNR).

[0007] Prior art approaches taken to avoid amplitude and phase imbalance rely upon very precise circuitry controlling each gain stage with active temperature compensation. These expensive designs require components that are manufactured with extremely low temperature coefficients and with the mixers for the *I* and *Q* channels custom matched during manufacture.

[0008] Accordingly, there exists a need for a system that balances the amplitude and phase of a QPSK signal upon reception increasing signal integrity and thereby reducing bit error rate (BER).

SUMMARY OF THE INVENTION

[0009] The present invention balances the amplitude and phase of a received QPSK signal that may have been corrupted during transmission. The output from the system is a signal corrected in both amplitude and phase. The system determines the amplitude of the *I* and *Q* channels of a received signal, compares them, and applies a correction to one or both channels correcting amplitude imbalance. For phase imbalance, the system calculates the cross-correlation of the *I* and *Q* channels which should average to zero. A correction factor is derived from the cross-correlation product and is applied to both channels, returning the phase cross-correlation to zero.

[0010] Accordingly, it is an object of the invention to provide a system which balances the amplitude of a received QPSK signal.

[0011] It is a further object of the invention to provide a system which balances the phase of a received QPSK signal.
[0012] Other objects and advantages of the system and method will become apparent to those skilled in the art after reading the detailed description of the preferred embodiment.

BRIEF DESCRIPTION OF THE DRAWINGS

[0013]

Figure 1A is a plot of a QPSK symbol, balanced in both amplitude and phase.
Figure 1B is a plot of a QPSK symbol, amplitude imbalanced.
Figure 1C is a plot of a QPSK symbol, phase imbalanced.
Figure 2 is a block diagram of an amplitude balancing system in accordance with the present invention.
Figure 3 is a block diagram of a phase balancing system in accordance with the present invention.
Figure 4 is a vector representation showing phase correction.
Figure 5 is a block diagram of a combined amplitude and phase balancing system in accordance with the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0014] The preferred embodiment will be described with reference to the drawing figures where like numerals represent like elements throughout.
[0015] An embodiment showing the amplitude balancing system **17** of the present invention is shown in **Figure 2** where two bi-phase modulated signals **19** are input **21I, 21Q**. Quantizing is the process of measuring the intensity of a signal in each sample and assigning a digital number to that measured value. Each time the sampling circuit samples the signal, it measures the intensity of the varying analog signal at that discrete moment in time. The input **23I, 23Q** data streams represent the discrete samples of data assembled into finite words each having a plurality of bits. The number of bits that define each word determine the total quantization of each sample or symbol. For example, six-bit quantization:

Equation 2

$$\text{quantization levels} = 2^n - 1$$

with *n* equal to 6 would yield a resolution of 63 levels. Desired signal resolution determines *n*.
[0016] Each signal **23I, 23Q** component, *I* and *Q*, is coupled to an input of an amplifier **25I, 25Q** which has an adjustable gain. The output **27I, 27Q** of the amplifiers **25I, 25Q** are coupled to an absolute value processor **29I, 29Q** to obtain the relative magnitudes of each incoming symbol **23I, 23Q**. The output **31I**, **31Q** of the absolute value processors **29I, 29Q** are coupled to inputs of respective low pass filters **33I, 33Q**.
[0017] The low pass filters **33I, 33Q** time-average the received component symbols **23I, 23Q**, giving additional weight to recent samples and decreasing weight to previous samples. In the present embodiment **17, IIR** (infinite impulse response) filters **33I, 33Q** with one pole are used, however, other types of filters or different order IIR filters can also be used without deviating from the principle of the invention. The low pass filter outputs **35I, 35Q** present averaged estimates of the sample amplitudes output from the absolute value processors **29I, 29Q**.
[0018] A summer **37** obtains the difference from the outputs **35I, 35Q** of the low pass filters **33I, 33Q** producing an error reference signal **39**. If the *I* and *Q* components of an input signal **23I, 23Q** are orthogonal to each other, the error reference signal **39** will have zero magnitude, indicating a balanced symbol. If the error reference signal **39** produces a value other than zero, the symbols are not amplitude balanced.
[0019] A non-zero-value error reference signal **39** becomes an error correction value. The reference signal **39** is coupled to an input of a hard limiter processor **41**. The hard limiter **41** outputs a signal **43** smaller in magnitude, either positive or negative, in dependence upon the error reference signal **39**. The hard limiter processor **41** clips the error reference signal **39** magnitude thereby making the sign of the error reference signal **39** a correction factor. This is done for simplifying the implementation, the hard limiter is not essential to the invention.
[0020] The output **43** of the hard limiter processor **41** is coupled to a leaky integrator which is an accumulator **45**. The accumulator **45** adds the present value input with an accumulated value from previous input values and outputs 47 a sum. Since the accumulator **45** has a finite bit width, over time, the accumulated value will self-limit in magnitude and plateau if errors persist and are great. The accumulated plurality of error reference signals **39** in the internal accumulator of the accumulator **45** will average to zero when the system reaches stasis.
[0021] The output **47** from the accumulator **45** is coupled to a gain input **49I, 49Q** on each adjustable gain amplifier **25I, 25Q**. The amplifiers **25I, 25Q** balance the amplitudes of the received *I* and *Q* symbols **23I, 23Q**, increasing or

attenuating their gains in dependence with the accumulator **45** output signal **47**. As can be seen, the reference signal **39** is negative feedback to the upstream amplification stages **25I, 25Q**. A positive control voltage at the gain input **49I, 49Q** indicates a gain increase for that amplifier; a negative control voltage indicates attenuation.

[0022] If the amplitudes of the input signals **23I, 23Q** are not balanced, the system will adjust the variable amplifiers **25I, 25Q** (attenuating one component while boosting the other) according to the accumulator **45** output signal **47** until the *I* and *Q* symbol amplitudes are within a predetermined tolerance. If the symbol gains are equal, but vary between received symbols, the system **17** will not effect correction. A downstream automatic gain control (AGC)(not shown) equalizes the system output **51I, 51Q** for further signal processing (not shown).

[0023] An embodiment showing the phase correction system **61** of the present invention is shown in Figure 3. Two bi-phase modulated signals **19** are input **63I, 63Q** into the system **61**. The input **63I, 63Q** data streams **65I, 65Q** for the *I* and *Q* symbols are coupled to a first input **67I, 67Q** of parallel summers **69I, 69Q**. The output **71I, 71Q** of each summer **69I, 69Q** are the system output **73I, 73Q** and feedback for the phase correction system **61**. Both feedback lines **71I, 71Q** are coupled to a mixer **75** for correlation. The mixer **75** cross-correlated output signal **77** is coupled to an integrator **79.** The integrator **79** time-averages the cross-correlation product **77**. The integrator output is coupled to a hard limiter processor **83**. The hard decision processor **83** limits the magnitude of the integrated cross-correlation product. The hard decision processor **83** output **85** retains sign. The hard limiter processor **83** output **85** is coupled to an accumulator input **87.** The hard decision processor **83** reduces implementation complexity, one skilled in this art would recognize that it is not essential.

[0024] As previously discussed, the function of an accumulator is to accumulate, over-time, the present input value with previous inputs. The sum is output as a correction signal.

[0025] The correction signal **89** is coupled to a first input **91I** of a variable gain amplifier **93I** coupling the *Q* input **65Q** with the *I* input **63I**. The correction signal **89** also is coupled to a first input **91Q** of a variable gain amplifier **93Q** coupling the *I* symbol input **65I** with the *Q* input **63Q**.

[0026] The correction signal **89** adjusts both amplifiers **93I, 93Q** increasing or decreasing their gain. The amplifier outputs **95I, 95Q** are coupled to a second input **97I, 97Q** of the input adders **69I, 69Q**.

[0027] The phase correction is shown as a vector representation in **Figure 4**. The adders **69I, 69Q** subtract the portion of *Q* component **63Q** from the *I* component **65I**;

Equation 3 $$I = x - r\,y,$$

Equation 4 $$-I = -x - r\,y,$$

where $r \triangleq$ *cross correlation,*

and the portion of *I* component **63I** from the *Q* component **65Q**;

$$Q = y - xr,$$ Equation 5

$$-Q = -y - xr,$$ Equation 6

where $r \triangleq$ *cross correlation*,

in order to remove the cross correlation contribution from each. Once the parts of the signals that result in the cross correlation are removed, the outputs **71I** and **71Q** of the adders **69I, 69Q** become uncorrelated *I*, *Q* and orthogonal in signal space.

[0028] An alternative embodiment combining both systems correcting amplitude **17** and phase **61** imbalance is shown in **Figure 5.** The system **101** is a simple series connection outputting **103I, 103Q** a symbol corrected in both amplitude and phase. Another combined embodiment where the amplitude balancer **17** follows the phase balancer **61** is also possible.

[0029] While specific embodiments of the present invention have been shown and described, many modifications and variations could be made by one skilled in the art without departing from the scope of the invention. The above description serves to illustrate and not limit the particular form in any way.

Claims

1. An apparatus (61) for amplitude and phase balancing a signal having I and Q components (23I, 23Q), wherein, the apparatus comprises:

   a correlator for correlating (75) phase and amplitude balanced I and Q components (71I, 71Q) to produce a cross correlation product (77);
   a first adjuster for adjusting (93I, 93Q) a gain of each amplitude balanced I and Q component (63I, 63Q) in accordance with said cross correlation product (77); and
   an adder for adding (69I, 69Q) the amplitude balanced I component (63I) with an adjusted Q component (95I), and the amplitude balanced Q component (63Q) with an adjusted I component (95Q) each adjusted by the first adjuster
   (93Q, 93I) to produce an amplitude and a phase-balanced signal (73I, 73Q).

2. The apparatus (61) of claim 1, **characterized in that** the apparatus further comprises:

   a comparer for comparing (37) the magnitudes of the amplitude balanced I and Q components (27I, 27Q);
   a generator for generating (33I, 33Q, 37) a correction signal (39) for both the I and Q components based on the magnitude comparison;
   a second adjuster for adjusting (25I, 25Q) a gain of the I and Q components in dependence upon said correction signal (39) to produce the amplitude balanced signal (27I, 27Q);
   wherein the correlator (75) uses the gain adjusted I (71I) and Q (71Q) components of said amplitude balanced signal to derive said cross correlation product (77); and
   wherein the adder (69I, 69Q) produces an amplitude and phase balance signal (103I, 103Q).

3. The apparatus (61) of claim 2, **characterized in that** said second adjuster (25I, 25Q) includes I (25I) and Q (25Q) amplifiers, and said apparatus further comprises:

   respective I and Q low pass filters (33I, 33Q) coupled to said comparer (37); and
   an absolute value processor (29I, 29Q) having an output coupled to said low pass filters (33I, 33Q) and an input coupled to said first adjuster (25I, 25Q).

4. The apparatus (61) of claim 1, **characterized in that**:

   the first adjuster comprises:

      an I adjustable gain amplifier (93I) for receiving said amplitude balanced I component (63I) and having an I output (95Q); and
      a Q adjustable gain amplifier (93Q) for receiving said amplitude balanced Q component (63Q) and having a Q output (95I); and

   the adder comprises:

      an I summer (69I) having a first summer input (67I) coupled to said amplitude balanced I component (63I) and a second summer input (97I) coupled to said Q output (95I), and having an I summer output (71I); and
      a Q summer (69Q) having a first summer input (67Q) coupled to said amplitude balanced Q component (63Q) and a second summer input (97Q) coupled to said I output (95Q) and having a Q summer output (71Q);
      said apparatus further comprising a controller (79, 83, 87) for controlling gain of each said I adjustable gain amplifier (93I) and Q adjustable gain amplifier (93Q).

5. The apparatus (61) of claim 4, **characterized in that**:

   said correlator for correlating (75) the phase and amplitude balanced I and Q components (71I, 71Q) has as an output of a cross correlation product (77);
   said cross correlation product (77) coupled to said I adjustable gain amplifier (93I) and Q adjustable gain amplifier (93Q) to control gain of said I adjustable gain amplifier (93I) and Q adjustable gain amplifier (93Q); and
   whereby amplitude and phase balanced I and Q signals (73I, 73Q) are output from said I mixer output (71I) and said Q mixer output (71Q), respectively.

Patentansprüche

1. Vorrichtung (61) zum Amplituden- und Phasenabgleich eines über I- und Q-Komponenten (23I, 23Q) verfügenden Signals, wobei die Vorrichtung umfasst:

   einen Korrelator zum Korrelieren (75) von phasen- und amplitudenabgeglichenen I- und Q-Komponenten (71I, 71Q), um ein Kreuzkorrelationsprodukt (77) zu erzeugen;
   eine erste Einstelleinrichtung zum Einstellen (93I, 93Q) einer Verstärkung jeder amplitudenabgeglichener I- und Q-Komponente (63I, 63Q) in Übereinstimmung mit dem Kreuzkorrelationsprodukt (77);
   ein Addierglied zum Addieren (69I, 69Q) der amplitudenabgeglichenen I-Komponente (63I) mit einer eingestellten Q-Komponente (95I), und der amplitudenabgeglichenen Q-Komponente (63Q) mit einer eingestellten I-Komponente (95Q), die jeweils durch die erste Einstelleinrichtung (93Q, 93I) eingestellt wurden, um ein amplituden- und phasenabgeglichenes Signal (73I, 73Q) zu erzeugen.

2. Vorrichtung (61) nach Anspruch 1, **dadurch gekennzeichnet, dass** die Vorrichtung darüber hinaus umfasst:

   eine Vergleichseinrichtung zum Vergleichen (37) der Größenordnungen der amplitudenabgeglichenen I- und Q-Komponenten (27I, 27Q);
   einen Generator zum Generieren (33I, 33Q, 37) eines Korrektursignals (39) für sowohl die I- als auch die Q-Komponenten auf Grundlage des Größenordnungsvergleichs;
   eine zweite Einstelleinrichtung zum Einstellen (25I, 25Q) einer Verstärkung der I- und Q-Komponenten in Abhängigkeit von dem Korrektursignal (39), um ein amplitudenabgeglichenes Signal (27I, 27Q) zu erzeugen;
   wobei der Korrelator (75) die verstärkungseingestellten I-Komponenten (71I) und Q-Komponenten (71Q) des amplitudenabgeglichenen Signals verwendet, um das Kreuzkorrelationsprodukt (77) abzuleiten; und
   wobei das Addierglied (69I, 69Q) ein Amplituden- und Phasenabgleichssignal (103I, 103Q) erzeugt.

3. Vorrichtung (61) nach Anspruch 2, **dadurch gekennzeichnet, dass** die zweite Einstelleinrichtung (25I, 25Q) I-Verstärker (25I) und Q-Verstärker (25Q) umfasst und die Vorrichtung darüber hinaus umfasst:

   jeweilige I- und Q-Tiefpassfilter (33I, 33Q), die an die Vergleichseinrichtung (37) angeschlossen sind; und
   einen Absolutwertprozessor (29I, 29Q) mit einem Ausgang, der an die Tiefpassfilter (33I, 33Q) angeschlossen ist, und einem Eingang, der an die erste Einstelleinrichtung (25I, 25Q) angeschlossen ist.

4. Vorrichtung (61) nach Anspruch 1, **dadurch gekennzeichnet, dass**:

   die erste Einstelleinrichtung umfasst:

      einen I-Verstärker (93I) mit einstellbarer Verstärkung, um die amplitudenabgeglichene I-Komponente (63I) zu empfangen, und mit einem I-Ausgang (95Q); und
      einen Q-Verstärker (95Q) mit einstellbarer Verstärkung, um die amplitudenabgeglichene Q-Komponente (63Q) zu empfangen, und mit einem Q-Ausgang (95I); und

   das Addierglied umfasst:

      ein I-Summierglied (69I) mit einem ersten Summiergliedeingang (67I), der an die amplitudenabgeglichene I-Komponente (63I) angeschlossen ist, und einem zweiten Summiergliedeingang (97I), der an den Q-Ausgang (95I) angeschlossen ist, und mit einem I-Summiergliedausgang (71I); und
      ein Q-Summierglied (69Q) mit einem ersten Summiergliedeingang (67Q), der an die amplitudenabgeglichene Q-Komponente (63Q) angeschlossen ist, und einem zweiten Summiergliedeingang (97Q), der an den I-Ausgang (95Q) angeschlossen ist, und mit einem Q-Summiergliedausgang (71Q);
      wobei die Vorrichtung darüber hinaus eine Regeleinrichtung (79, 83, 87) umfasst, um jeweils eine Verstärkung des I-Verstärkers (93I) mit einstellbarer Verstärkung und Q-Verstärkers (93Q) mit einstellbarer Verstärkung zu regeln.

5. Vorrichtung (61) nach Anspruch 4, **dadurch gekennzeichnet, dass**:

   der Korrelator zum Korrelieren (75) der phasen- und amplitudenabgeglichenen I- und Q-Komponenten (71I, 71Q) ein Kreuzkorrelationsprodukt (77) als Ausgang hat;

das Kreuzkorrelationsprodukt (77) in den I-Verstärker (93I) mit einstellbarer Verstärkung und den Q-Verstärker (93Q) mit einstellbarer Verstärkung eingekoppelt wird, um eine Verstärkung des I-Verstärkers (93I) mit einstellbarer Verstärkung und Q-Verstärkers (93Q) mit einstellbarer Verstärkung zu regeln; und
wodurch amplituden- und phasenabgeglichene I- und Q-Signale (73I, 73Q) aus dem I-Mischerausgang (71I) bzw. Q-Mischerausgang (71Q) ausgegeben werden.

Revendications

1. Dispositif (61) destiné à équilibrer en amplitude et en phase un signal présentant des composants I et Q (23I, 23Q), le dispositif comportant :

   un corrélateur destiné à corréler (75) des composants I et Q équilibrés en phase et en amplitude (71I, 71Q) pour produire un produit de corrélation croisée (77) ;
   un premier régleur destiné à régler (93I, 93Q) un gain de chaque composant I et Q équilibré en amplitude (63I, 63Q) en fonction dudit produit de corrélation croisée (77) ; et
   un additionneur destiné à additionner (69I, 69Q) le composant I équilibré en amplitude (63I) à un composant Q réglé (95I), et le composant Q équilibré en amplitude (63Q) à un composant I réglé (95Q), chacun étant réglé par le premier régleur (93Q, 93I) pour produire un signal équilibré en amplitude et en phase (73I, 73Q).

2. Le dispositif (61) de la revendication 1, **caractérisé en ce que** le dispositif comporte en outre :

   un comparateur destiné à comparer (37) les magnitudes des composants I et Q équilibrés en amplitude (27I, 27Q) ;
   un générateur destiné à générer (33I, 33Q, 37) un signal de correction (39) pour à la fois les composants I et Q sur la base de la comparaison de magnitude ;
   un deuxième régleur destiné à régler (25I, 25Q) un gain des composants I et Q en fonction dudit signal de correction (39) pour produire le signal équilibré en amplitude (27I, 27Q) ;
   où le corrélateur (75) utilise les composants I (71I) et Q (71Q) réglés en gain dudit signal équilibré en amplitude pour dériver ledit produit de corrélation croisée (77) ; et
   où l'additionneur (69I, 69Q) produit un signal équilibré en amplitude et en phase (103I, 103Q).

3. Le dispositif (61) de la revendication 2, **caractérisé en ce que** ledit deuxième régleur (25I, 25Q) inclut des amplificateurs I (25I) et Q (25Q), et ledit dispositif comporte en outre :

   des filtres passe-bas I et Q respectifs (33I, 33Q) couplés audit comparateur (37) ; et
   un processeur de valeur absolue (29I, 29Q) présentant une sortie couplée auxdits filtres passe-bas (33I, 33Q) et une entrée couplée audit premier régleur (25I, 25Q).

4. Le dispositif (61) de la revendication 1, **caractérisé en ce que** :

   le premier régleur comporte :

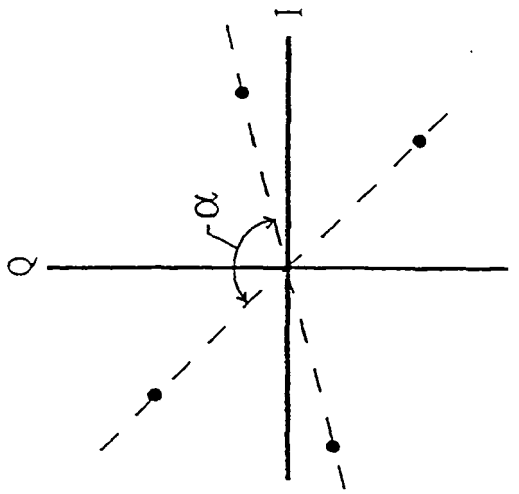
      un amplificateur de gain réglable I (93I) destiné à recevoir ledit composant I équilibré en amplitude (63I) et présentant une sortie I (95Q) ; et
      un amplificateur de gain réglable Q (93Q) destiné à recevoir ledit composant Q équilibré en amplitude (63Q) et présentant une sortie Q (95I) ; et

   l'additionneur comporte :

      un sommateur I (69I) présentant une première entrée de sommateur (67I) couplée audit composant I équilibré en amplitude (63I) et une deuxième entrée de sommateur (97I) couplée à ladite sortie Q (95I), et présentant une sortie de sommateur I (71I) ; et
      un sommateur Q (69Q) présentant une première entrée de sommateur (67Q) couplée audit composant Q équilibré en amplitude (63Q) et une deuxième entrée de sommateur (97Q) couplée à ladite sortie I (95Q) et présentant une sortie de sommateur Q (71Q) ;
      ledit dispositif comportant en outre un régulateur (79, 83, 87) destiné à réguler le gain de chaque dit amplificateur de gain réglable I (93I) et amplificateur de gain réglable Q (93Q).

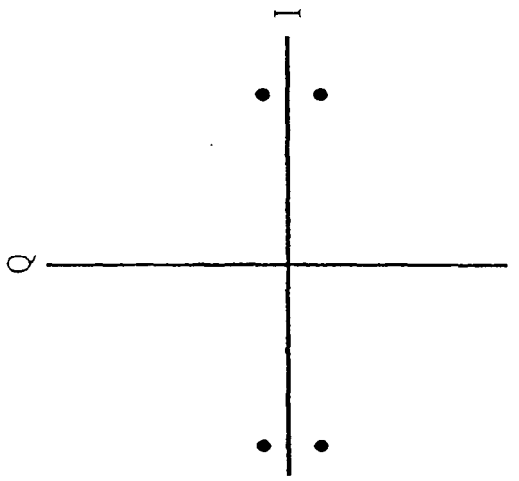
5. Le dispositif (61) de la revendication 4, **caractérisé en ce que** :

ledit corrélateur destiné à corréler (75) les composants I et Q équilibrés en phase et en amplitude (71I, 71Q) a comme sortie un produit de corrélation croisée (77) ;
ledit produit de corrélation croisée (77) étant couplé audit amplificateur de gain réglable I (93I) et amplificateur de gain réglable Q (93Q) pour réguler le gain dudit amplificateur de gain réglable I (93I) et amplificateur de gain réglable Q (93Q) ; et
où des signaux I et Q équilibrés en amplitude et en phase (73I, 73Q) sont sortis de ladite sortie de mélangeur I (71I) et de ladite sortie de mélangeur Q (71Q), respectivement.



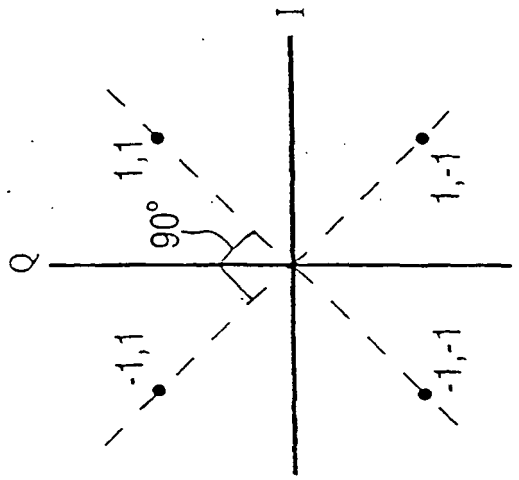
PHASE IMBALANCE

FIG. 1C



AMPLITUDE IMBALANCE

FIG. 1B



BALANCED

FIG. 1A

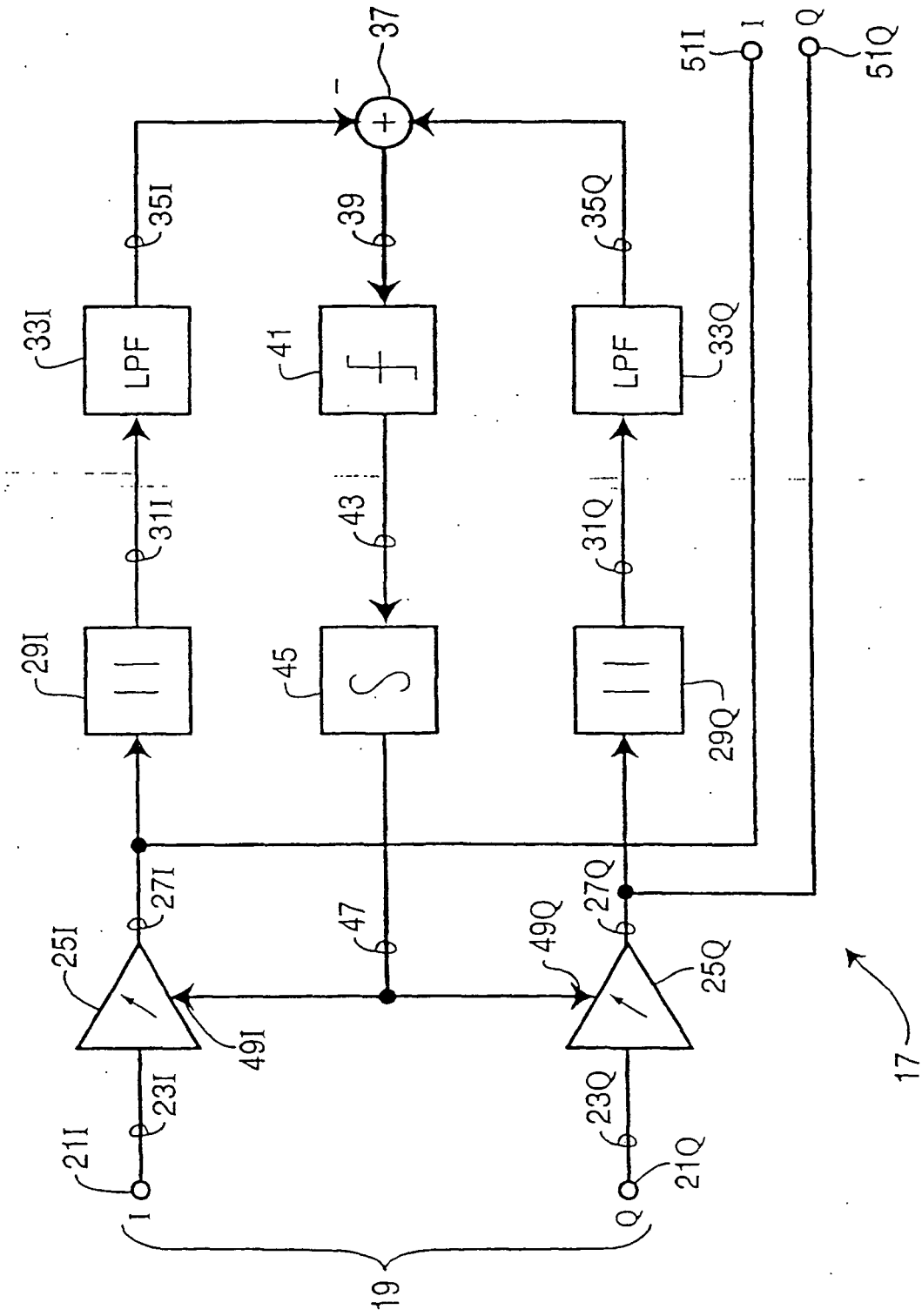

37
51I
I
Q
51Q
35I
39
35Q
33I
LPF
41
LPF
33Q
31I
43
31Q
29I
45
29Q
27I
47
49Q
27Q
25I
25Q
49I
23I
23Q
21I
21Q
I
Q
19
17

FIG. 2

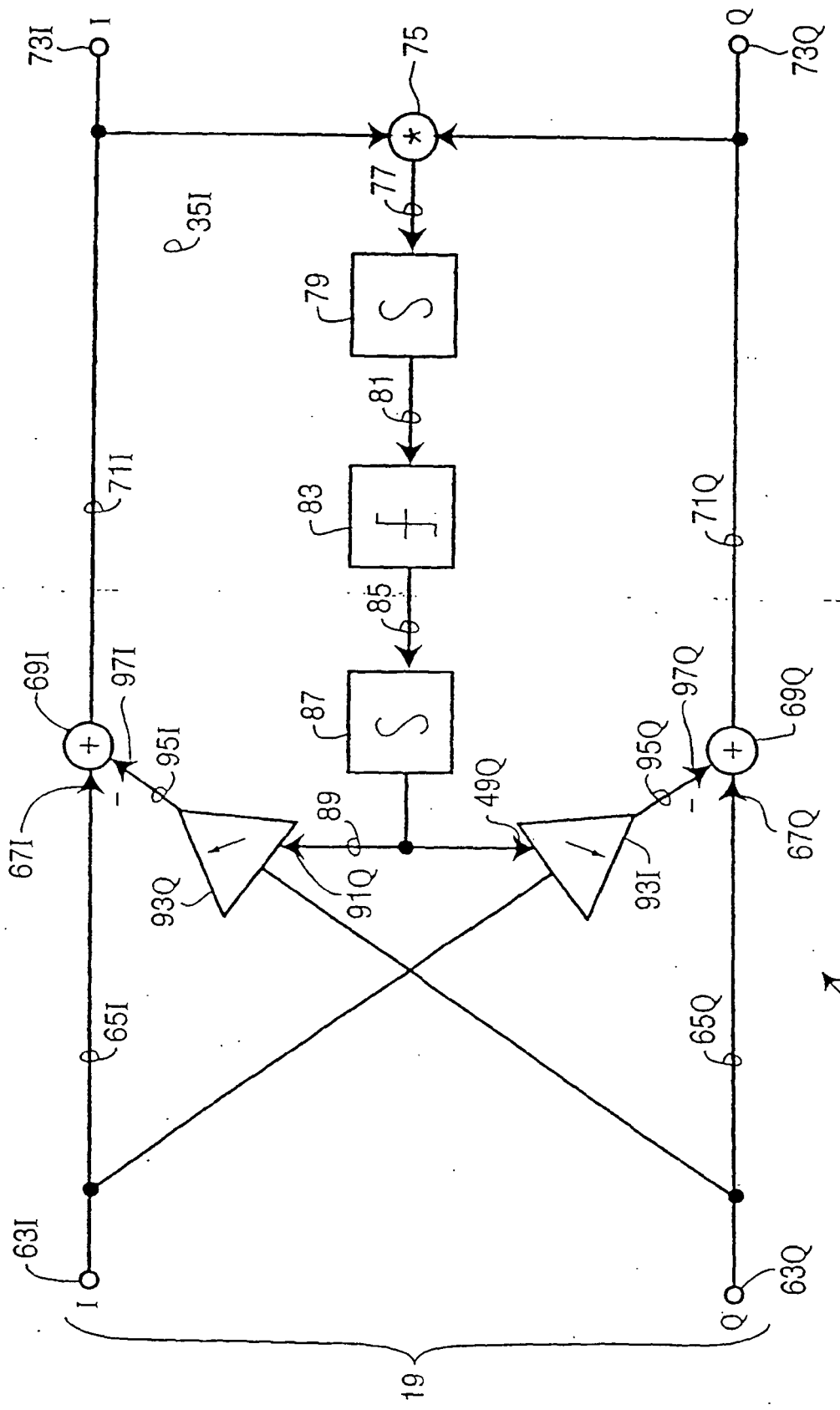

I
Q
73I
73Q
75
77
35I
79
81
83
85
87
71I
71Q
69I
69Q
97I
97Q
95I
95Q
67I
67Q
89
49Q
91Q
93Q
93I
65I
65Q
61
63I
63Q
19

FIG. 3

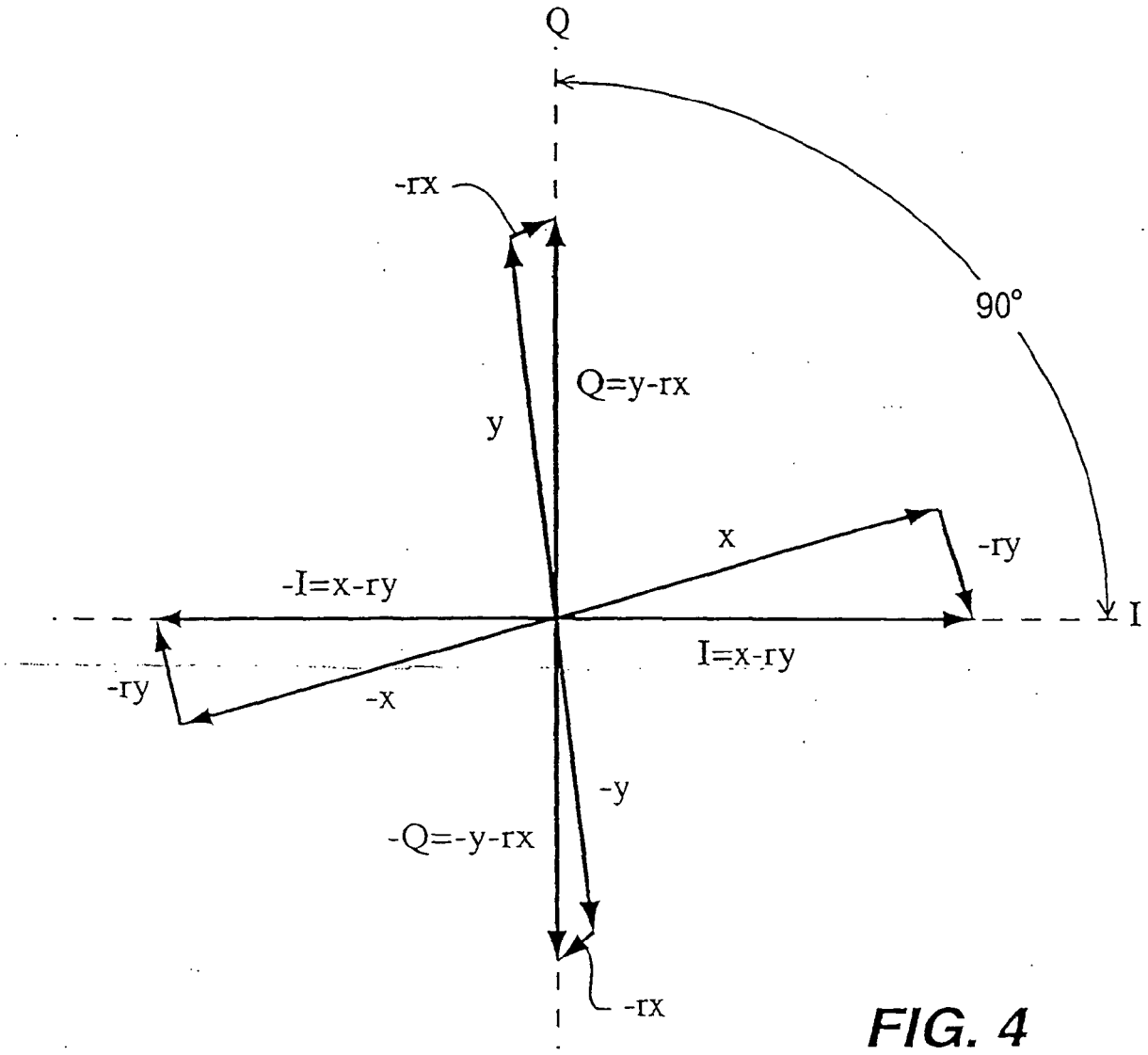

Q
-rx
90°
Q=y-rx
y
x
-ry
-I=x-ry
I
I=x-ry
-ry
-x
-y
-Q=-y-rx
-rx

FIG. 4

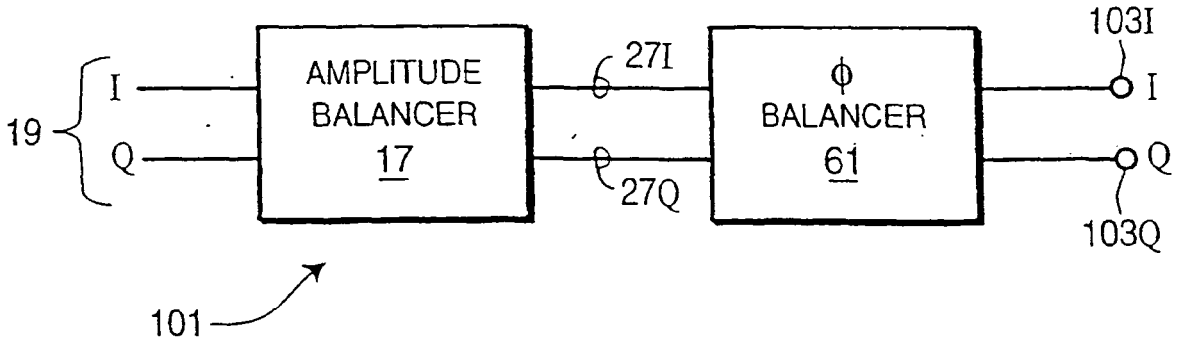

19
I
Q
AMPLITUDE BALANCER 17
27I
27Q
ϕ BALANCER 61
103I
I
Q
103Q
101

FIG. 5