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(54) **Monotonic precise current DAC**

Ein stromgesteuerter Digital Analog Wandler mit gleichbleibender Genauigkeit

Un convertisseur numérique-analogique courant de précision monotone

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(73) Proprietor: **AMI Semiconductor Belgium BVBA**
9700 Oudenaarde (BE)

(72) Inventors:
• **Horsky, Pavel**
638 00 Brno (CZ)
• **Koudar, Ivan**
664 51 Slapanice u Brna (CZ)

(74) Representative: **Bird, William Edward et al**
Bird Goën & Co.
Klein Dalenstraat 42A
3020 Winksele (BE)

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Description

Technical field of the invention

[0001]   The present invention relates to data conversion, and more particularly to a method of digital-to-analog (D/A) data conversion and corresponding digital-to-analog data converters (DACs).

Background of the invention

[0002]   Description of prior art monotonic DAC can be found in H.J. Schouwenaars et al., "A low-power stereo 16-bit CMOS D/A converter for digital audio", IEEE J. Solid-State Circuits, vol. 23, no. 6, pp. 1290-1297, December 1988.
[0003]   A basic diagram of a segmented current dividing DAC is shown in Fig. 1. An array of C linearly weighted coarse current sources is used. To increase the resolution, one of the current sources, in the case presented in Fig. 1 current source I_C, can be divided into more fine levels by a passive current divider. Depending on the value of the data signal, a number of the currents are switched to the output terminal I_{out}, and the remaining currents are dumped to signal ground.
[0004]   To guarantee monotonicity of such a DAC, a principle as shown in Fig. 2 may be used. The coarse current sources are connected to three way switches. A decoder transforms the binary information of the most significant bits of the digital input signal into a thermometer code, which controls the coarse current switches. The first unselected coarse current source is connected by the three way switches to a fine bit divider stage, which divides the applied current into binary weighted current levels. These binary currents are switched to the output line by two-way switches controlled by the least significant bits. The coarse and fine output currents are added, thus forming an output current signal which is converted to an output voltage which is an analog equivalent of the digital input signal.
[0005]   EP 0 359 315 discloses a digital-to-analog converter comprising a current source arrangement. The current source arrangement comprises a number of current sources and a switching network. The most significant bits of a digital input are sent to a first block comprising a decoding device, a current source for generating substantially equal currents and a switching network comprising two-way switches. A current coming from the first block is then sent to the second block comprising a current dividing circuit and a switching network. The current dividing circuit supplies the currents for the 10 least significant bits. The 10 least significant bits directly control the switches of the switching network.
[0006]   The above described DAC's have a voltage output. If it is desired to obtain a current output, then the amplifier converting the current output to a voltage output may be left out. However, when doing this and when working in a wide range of output voltages, the current output is not precise due to a changing voltage at the outputs of coarse and fine blocks.
[0007]   In US 4,292,625 a monotonic digital-to-analog converter is described for converting a binary number in an analog signal. The converter comprises a segment generator and a step generator. The segment generator is disposed for providing a first signal proportional to the values of the most significant digits of the binary numbers. Further, a step generator is disposed for providing a second signal proportional to the values of the least significant digits of the same binary numbers. Additionally, means for combining the first and second signals is provided to form an analog signal proportional to the value of the binary number to be converted. The output of the converter is a current.

Summary of the invention

[0008]   It is an object of the present invention to provide a DAC which delivers a current output which can be used in a wide range of output voltages.
[0009]   The above objective is accomplished by a method and device according to the present invention.
[0010]   The present invention provides a monotonic digital-to-analog converter (DAC) for converting a digital input signal into an analog output signal. The converter comprises:

an input node for receiving the digital input signal having at least M+L bits,
an output node for delivering the analog output signal corresponding to the received digital input signal,
a coarse conversion block comprising current sources and first switching means for switching current of a first number of selected current sources as a coarse block output current to an output node, the number depending on a value of M more significant bits of the digital input signal, and from a first of N unselected current sources in the coarse conversion block into a fine conversion block, the fine conversion block comprising means for receiving current from the first of N unselected current sources of the coarse conversion block, a current divider comprising current division means and second switching means forswitching current of a second number of selected current division means in the fine conversion block to the output node, the second number depending on a value of L less significant bits of the digital input signal,
characterised in that the monotonic digital-to-analog converter furthermore comprises:

- a first cascode means for active cascoding of the coarse block output current, and
- a second cascode means comprising at least the current divider, for active cascoding of the current from the first of N unselected current sources.

[0011]   It is an advantage of the present invention that the coarse block current outputs connected to the fine block and to the output node see the same voltage, so that monotonicity is not offended.

[0012]   The first switching means may consist of two switching devices with three states: two ways where the current can flow (switching to the output node or switching to the fine conversion block) and one open state (no current can flow; preferably current sources are switched OFF).

[0013]   Alternatively, the first switching means may be three way switches, i.e. there are three ways where the current can flow: switching to the output node, switching to the fine conversion block and switching to the power supply level or to another voltage level. Also three way switches with four states may be used: three ways where the current can flow (switching to the output node, switching to the fine conversion block or switching to a complementary output node), and one open state (no current can flow, preferably the current sources are switched OFF).

[0014]   Unselected current sources may be switched off in order to save power consumption.

[0015]   The coarse conversion block may comprise linearly weighted current sources. The fine conversion block may comprise a linearly weighted current divider for dividing the current coming from the coarse conversion block.

[0016]   The monotonic digital-to-analog converter according to the present invention may furthermore be provided with means for carrying out pulse width modulation (PWM) to current from the first unselected current division means of the fine conversion block. The PWM may be applied to an unselected fine bit, for example the first unselected fine bit in order to keep monotonicity. A monotonic digital-to-analog converter according to the present invention may furthermore comprise an output follower loop for buffering the voltage on the output node.

[0017]   The present invention also provides a method for converting a digital input signal comprising at least M+L bits into an analog signal. The method comprises:

providing the digital input signal at an input node,
selecting a first number of coarse current sources in a coarse conversion block, the first number depending on a value of M more significant bits of the digital input signal,
switching current of the selected first number of current sources to an output node,
switching current from a first of N unselected current sources in the coarse conversion block to a fine conversion block,
dividing the current from the switched first of N unselected current sources by means of a current divider comprising current division means in the fine conversion block,
selecting a second number of current division means in the fine conversion block, the second number depending on a value of L less significant bits of the digital input signal,
switching current of the selected current division means in the fine conversion block to the output node,
characterised in that the method furthermore comprises:

actively cascoding the coarse block output current, and
actively cascoding the current of the first of N unselected current sources in the coarse conversion block by means of at least the current divider.

A method according to the present invention may further comprise applying pulse width modulation on current from an unselected current division means in the fine conversion block, and switching this pulse width modulated current to the output node.

[0018]   A method according to the present invention may furthermore comprise switching off the second to Nth unselected current sources in the coarse conversion block.

[0019]   Dividing the current from the switched unselected current source in the coarse conversion block by means of a current divider in the fine conversion block may be such that the current is equally divided over different branches in the fine conversion block, or in other words, may comprise linearly weighted dividing of said current.

[0020]   A method according to the present invention may furthermore comprise buffering a voltage on the output node.

[0021]   These and other characteristics, features and advantages of the present invention will become apparent from the following detailed description, taken in conjunction with the accompanying drawings, which illustrate, by way of example, the principles of the invention. This description is given for the sake of example only, without limiting the scope of the invention. The reference figures quoted below refer to the attached drawings.

Brief description of the drawings

[0022]

Fig. 1 is a schematic circuit diagram of a current dividing DAC according to the prior art.
Fig. 2 is a block diagram of a segmented DAC according to the prior art.
Fig. 3 is a block diagram of a current DAC according to an embodiment of the present invention.
Fig. 4 illustrates and example of separation between coarse and fine blocks and PWM modulation.

[0023] In the different figures, the same reference figures refer to the same or analogous elements.

Description of illustrative embodiments

[0024] The present invention will be described with respect to particular embodiments and with reference to certain drawings but the invention is not limited thereto but only by the claims. The drawings described are only schematic and are non-limiting. In the drawings, the size of some of the elements may be exaggerated and not drawn on scale for illustrative purposes.

[0025] The terms first, second, third and the like in the description and in the claims, are used for distinguishing between similar elements and not necessarily for describing a sequential or chronological order. It is to be understood that the terms so used are interchangeable under appropriate circumstances and that the embodiments of the invention described herein are capable of operation in other sequences than described or illustrated herein.

[0026] Furthermore, it is to be noticed that the term "comprising", used in the claims, should not be interpreted as being restricted to the means listed thereafter; it does not exclude other elements or steps.. Thus, the scope of the expression "a device comprising means A and B" should not be limited to devices consisting only of components A and B. It means that with respect to the present invention, the only relevant components of the device are A and B.

[0027] Similarly, it is to be noticed that the term "coupled" discloses both direct and indirect coupling and should not be interpreted as being restricted to direct connections only. Thus, the scope of the expression "a device A coupled to a device B" should not be limited to devices or systems wherein an output of device A is directly connected to an input of device B. It means that there exists a path between an output of A and an input of B which may be a path including other devices or means.

[0028] The diagram of Fig. 3 shows the principles of a DAC 1 according to an embodiment of the present invention. This DAC 1 is a current DAC, i.e. it utilises current sources controlled by a digital input signal value which is being converted into an analog equivalent. The output of the DAC 1 according to the present invention is a current signal.

[0029] The DAC 1 according to the present invention is a segmented or dual DAC for conversion of a digital word or signal having a number of bits into an analog value. As a first embodiment, a DAC 1 for converting a digital word having M+L bits is considered.

[0030] At the left hand side of Fig. 3, a reference voltage V_{ref}, for example 0.5 Volts, is generated, for example by a current I_{b1} which is sent through a reference resistor R_{ref}. The current I_{b1} is chosen proportional to the value of the resistance R_{ref}, and therefore is preferably generated on-chip. As the current I_{b1} is only used for generating the reference voltage V_{ref}, it does not need to be highly accurate. Instead of a current flowing to a reference resistor R_{ref}, any voltage source can be used for V_{ref}.

[0031] It is tried to keep the same voltage V_{ref} at node N_{ref} by means of a source follower circuit 3, comprising an input transistor and an output transistor. At the side of the output transistor of the source follower circuit 3, a reference input current I_{ref} flows through a diode 5. This diode 5 may comprise a number of transistors, e.g. eight transistors. I_{ref} is proportional to the number of transistors in the diode 5. The overall precision of the DAC depends on this current I_{ref}, therefore this current I_{ref} needs to be very precise. At the gate of the transistors in the diode 5, a voltage V_G is generated. The gates of the transistors of the diode 5 are connected to the drain of the output transistor of the source follower circuit 3 in order to provide a low voltage drop circuit. A conventional current mirror, without connection between the gates of the transistors of the diode 5 and the drain of the output transistor of the source follower circuit 3, may also be used, but in that case another output voltage range is obtained.

[0032] A first block, a coarse block 2, provides a coarse conversion of a part of the input digital signal by means of switching means, such as e.g. switching transistors, controlled by a decoder decoding the M most significant bits of the digital signal having M+L bits. A second block, a fine block 4, provides a fine conversion in response to the L least significant bits of the digital signal. The use of a coarse (M-bit) converter cascaded with a fine (L-bit) converter instead of an N-bit converter (wherein N=M+L) produces a very great saving in the number of devices which are required for the conversion, and accordingly a very great saving in the area of the converter.

[0033] Coarse block 2 comprises a number of current sources 6. If the course block 2 is provided for conversion of M bits of the incoming digital signal, then it comprises 2^M current sources 6; for example for conversion of a 7-bits signal, 128 current sources are needed. In the embodiment described with respect to Fig. 3, the current sources 6 are transistors, the gates of which are connected to the gates of the transistors forming the diode 5. The current sources are formed as linearly weighted, low voltage drop, current mirrors. This decreases matching requirements for the transistors forming the current sources 6. The currents delivered by the current sources 6 of the coarse block 2 are thus substantially equal

to each other. By providing current sources 6 which each provide substantially the same amount of current and controlling these currents by a thermometer signal, a monotonic converter is provided. Linearly weighted converters require more switches and/or more current sources than binary weighted converters (wherein each current source provides a different amount of current, each value being a binary two multiple) to implement the same resolution. However, monotonic converters are characterised by the fact that, when increasing input signal values are applied to the converter, the output never decreases in value. Although binary weighted converters can be monotonic if a high enough precision of the current sources is provided, they are often not monotonic due to errors in precisely implementing each current source value. To create a monotonic binary weighted converter requires high accuracy for all current sources mainly for higher number of bits, on the other hand a linearly weighted converter is intrinsically monotonic. In coarse block 2 as shown in Fig. 3, the reference current I_{ref} is mirrored to each of the current sources 6, which each deliver a current I_{ref}, or a part or a multiple thereof, depending on the number and the dimensions of the transistors forming the current sources 6.

[0034] Coarse block 2 furthermore comprises a number of switching devices 8. On the outputs of the current sources 6 of the coarse block 2, two way switches 8 are used, according to one embodiment, as represented in Fig. 3. Such two way switch 8 provides two ways in which the current can flow, and one open state. Therefore, each two way switch 8 comprises two switches 10, 12.

[0035] A first switch 10 is controlled by a thermometer code delivered by a binary-to-thermometer converter part of a converting means 9. A binary-to-thermometer converter has a data input for receiving M bits of the digital input signal to be converted into an analog signal, where M is an integer. The M bits represent the most significant bits of the digital input signal which is desired to be converted to an equivalent analog value. The binary-to-thermometer converter provides a conventional conversion from binary code to thermometer code. For facilitating the understanding of such converter, an example of the conventional binary-to-thermometer code conversion is provided in table 1 for three input bits (M = 3).

Binary input	Thermometer output	Code 1 of Nc
000	00000000	00000001
001	00000001	00000010
010	00000011	00000100
011	00000111	00001000
100	00001111	00010000
101	00011111	00100000
110	00111111	01000000
111	01111111	10000000

For an M-bit input word, 2^M-1 thermometer coded signals are required, for example for a 3-bit input word, 7 thermometer coded signals are required. A binary-to-thermometer encoder is such that the number of bits turned on at its output is the same as the numeric value presented at its input.

[0036] The first switches 10 thus switch current from activated current sources 6 through cascode transistor MC1 to an output node N_{OUT}.

[0037] A first switch 10 is controlled by a thermometer code delivered by a binary-to-thermometer converter part of a first converting means 9. A second switch 12 of the two way switches 8 is controlled by a code 1 of Nc, Nc being the number of coarse currents (Nc = 2^M), which code is delivered by a binary-to-1-of-N converter which may also be, but does not need to be, part of the first converting means 9. The code 1 of Nc is illustrated in the table hereinabove in case of a 3-bit digital input signal. The second switches 12 switch the current of the first unselected current source of the coarse block 2 so as to flow into the fine block 4. Other unselected current sources are switched off to decrease current consumption.

[0038] Very careful routing of the ground node is needed to guarantee negligible ground shifts in the coarse current mirror. If not, the sources of different transistors forming the current sources are at a different voltage level, and the current sources will not deliver a same current as expected. When switching between coarse bits, the ground shifts will change (due to change of the current flowing through the ground connection) and monotonicity of the converter can be lost.

[0039] Alternatively, three way switches (not represented in the drawings) can also be used to improve accuracy. In that case, each three-way switch comprises a first, a second and a third switch. The first switch switches selected or activated current sources to the output node, the second switch switches the current of the first unselected current source to the fine block, and the third switch switches non-activated current sources to the supply, or preferably to a level substantially equal to V_{ref}. By switching current sources off instead of letting the current flow to a voltage level such the

supply or V_{ref}, current consumption is saved. However, if the current sources are switched off and need to be switched on at a certain moment in time, more time is needed to settle the DAC because it is needed to charge the drains of the transistors forming said current sources and monotonicity could be influenced.

[0040]   The output of the first unselected coarse bit is connected to the fine block 4, where the current is further divided by current division means, e.g. by means of current dividing transistors. When the DAC digital input signal is increased in such a way that the coarse bit value is increased by one, then the coarse bit, which was previously connected to fine bits input node N_{fine} is now added to the other selected outputs on the output node N_{coarse} and goes to the output via cascode MC1. The next coarse current source is taken as an input for the fine bits on node N_{fine}.

[0041]   The fine block 4 is constructed as a linearly weighted current divider. This means that current coming in from the coarse block is equally divided e.g. by current dividing transistors, over the different branches 14 in the fine block 4. This principle makes the current DAC intrinsically monotonic. Each branch 14 of the fine block 4 is again provided with switching means, for example with two way switches 16. The two way switches 16 comprise a first switch 17 for switching the current of the corresponding current source to the output node N_{OUT}, and a second switch 18 for switching the current of the corresponding current source to a dummy node N_{dummy}.

[0042]   The L least significant bits of the digital input signal are again thermometer coded in a binary-to-thermometer converter part of a second converting means 15 to provide a control signal for controlling the first switch 17 of the two way switches 16, as illustrated in the table below for a 3-bit input signal. The second switches 18 are controlled by an inverted converter part of the second converting means 15. This inverted converter outputs a control signal which is the inverse of the control signal outputted by the binary-to-thermometer converter, i.e. current from current sources not flowing to the output node N_{OUT} is flowing to the dummy node N_{dummy}.

Binary input	Thermometer output	Inversion
000	0000000	1111111
001	0000001	1111110
010	0000011	1111100
011	0000111	1111000
100	0001111	1110000
101	0011111	1100000
110	0111111	1000000
111	1111111	0000000

[0043]   For the fine block, if L least significant bits are to be coded, for the present embodiment 2^L-1 current sources are needed, for example for a 3-bit digital input, 7 current sources are needed.

[0044]   The switches 16 are used to connect the output of the fine block current dividers to the output node N_{OUT} or to connect them to a dummy branch N_{dummy} where the current may be dumped.

[0045]   According to a second embodiment of the present invention, pulse width modulation (PWM) can be applied to the first unselected fine current source in order to increase or enhance resolution while substantially keeping the same number of current sources and switches, i.e. by substantially the same number of transistors. In fact, only a control signal and decoder (and one more switch) is needed in the fine conversion block compared to the first embodiment as explained above. In case PWM may be applied, the digital signal coming in comprises M+L+K bits, whereby the M more significant bits are used for controlling the switches of the coarse conversion block, the L less significant bits are used for controlling the switches of the fine conversion block, and the K least significant bits are used for controlling the PWM. The controlling of the switches of the coarse conversion block 2 and of the fine conversion block 4 is done as described in the first embodiment above, and is therefore not repeated in detail here.

[0046]   The L least significant bits of the digital input signal are again thermometer coded in a binary-to-thermometer converter part of a second converting means 15 to provide a control signal for controlling the first switch 17 of the two way switches 16, as illustrated in the table below for a 3-bit input signal. The second switches 18 are controlled by an inverted converter part of the second converting means 15. This inverted converter outputs a control signal which is the inverse of the control signal outputted by the binary-to-thermometer converter, i.e. current from current sources not flowing to the output node N_{OUT} is flowing to the dummy node N_{dummy}.

Binary input	Thermometer output	Inversion	Bit for applying PWM
000	00000000	11111111	00000001
001	00000001	11111110	00000010
010	00000011	11111100	00000100
011	00000111	11111000	00001000
100	00001111	11110000	00010000
101	00011111	11100000	00100000
110	00111111	11000000	01000000
111	01111111	10000000	10000000

[0047]   For the fine block, if L least significant bits are to be coded, for the present embodiment 2^L current sources are needed, for example for a 3-bit digital input, 8 current sources are needed.

[0048]   For the PWM, a modulation is applied to the first unselected current source of the fine block 4. For example, if there are K least significant bits in the digital input signal, which K least significant bits are used for applying the PWM, then the switches of the first unselected current source of the fine block are controlled so that current flows to the output node for $\dfrac{X}{2^K}$ of a time period, X depending on the value of the K least significant bits used for applying PWM. As an example, it is considered that 2 least significant bits of the digital input signal are used for applying PWM. In that case, depending on the value of those 2 least significant bits, the output of the PWM is as follows, i.e. the current of the first unselected current source is switched to the output node N_{OUT} as follows:

Binary input	PWM
00	0
01	1/4
10	2/4
11	3/4

[0049]   This means that, if the binary input is e.g. 01, the current of the first unselected current source is switched for 1/4 of a period to the output node N_{OUT}, and for 3/4 of a period to the dummy node N_{dummy}. If the PWM code, i.e. the value of the K least significant bits, is increased, this corresponds to switching the current of the first unselected current source to the output node N_{OUT} for a longer time.

[0050]   Applying PWM results in an output signal which has a DC value which has, at certain moments in time, a step on it. It is clear that, after filtering, the mean value of the analog output signal has risen.

[0051]   According to a third embodiment, not represented in the drawings, current from the first unselected fine current source in the fine conversion block is fed to a current divider of a further, still finer, conversion block. PWM may then for example be applied to an unselected current source of this finer conversion block. The bits of the incoming digital signal need then to be divided so that a part of them control the switches of the coarse conversion block, another part control the switches of the fine conversion block, another part control the switches of the finer conversion block and still another part controls the PWM means.

[0052]   To guarantee a low voltage drop, high output impedance and high precision, three active cascoding loops are used. By using active cascoding, better results are obtained on a smaller area, which is important both in view of precision and in view of miniaturisation of devices. Furthermore, the voltage at the output may change in a wide range. Because the transistors of the coarse conversion block are close to linear region, the output impedance decreases and the transistors are more sensitive to voltage variations on their drains. If instead of active cascoding, passive cascoding would be used, a bigger area would be needed because a separate cascoding transistor would be needed for each branch to be precise, and a lower output impedance would be obtained. Furthermore, passive cascoding is not good when switching the current.

[0053]   The fine block 4 functions as an active cascode for the first unselected coarse bit, i.e. for cascoding of the coarse current source which is connected to the fine current divider. This makes efficient use of the voltage available

("voltage room", e.g. 1 Volt) for delivering a correct output current. A first operational amplifier OA2 is provided, the positive input of which is coupled to node N_{ref}, which carries the reference voltage for the current mirror, which reference voltage is approximately equal to the voltage V_{ref}. The negative input of first amplifier OA2 is coupled to node N_{fine}. The output of the first amplifier OA2 is connected to the gates of the fine block current dividing transistors. The gate voltages of the current dividing transistors are thus regulated so that the voltage on node N_{fine} is kept the same as the reference voltage V_{ref}. Voltage drops on switches inside the coarse block may be compensated by a dummy switch 19 inside the reference current branch.

[0054]   Active cascoding (OA1, MC1) for the coarse block output current is used because of the high dynamic range of this current and the required precision. By doing this, a high output impedance, precision and monotonicity are ensured. A second operational amplifier OA1 is connected with its positive input to node N_{fine}, which is kept at the reference voltage V_{ref} by means of the first operational amplifier OA2, and with its negative input to node N_{coarse} and with its output to the gate of a cascoding transistor MC1. This structure keeps the same voltage on the outputs of the coarse current sources connected to the output, node N_{coarse}, as is on the output of the first unselected current source which is connected into the fine current divider, node N_{fine}, i.e. also the same voltage as on node N_{ref}. An advantage of this structure compared to directly connecting the positive input of second operational amplifier OA1 to node N_{ref} is that the voltage difference between nodes N_{fine} and N_{coarse} is given by the offset of second operational amplifier OA1 only, and is independent of the offset of the first operational amplifier OA2, but a structure with directly connecting the positive input of second operational amplifier OA1 to node N_{ref} is also possible according to the present invention. The voltage difference between nodes N_{fine} and N_{coarse} is important to guarantee monotonicity. If the voltages on nodes N_{fine} and N_{coarse} would be different, the transistors forming the current sources would work in slightly different conditions, and monotonicity might be lost. This is mainly important when the coarse block current sources 6 work close to linear region. With monotonicity is meant that the output signal goes always up for higher input values. Furthermore, if the positive input of second amplifier OA1 would be connected to node N_{ref}, and positive input of first amplifier OA2 would be connected to N_{coarse}, then for currents below 1 coarse LSB, no current would be flowing through MC1 cascode, and the voltage on N_{coarse} would not be correctly defined. This problem is solved by the interconnection scheme of the first and the second operational amplifier OA1, OA2 according to the present invention.

[0055]   A third operational amplifier OA3 buffers the voltage on pin N_{OUT} to node N_{dummy}. This is used to make the same conditions for all fine bit transistors, so that they all see the same voltage at their drains, which improves the accuracy. If they would see different voltages, then they would deliver different currents.

[0056]   An advantage of the above circuit is that no additional cascodes are needed for each transistor in the coarse and fine block, which would lead to a need of much more voltage. Cascoding of the coarse block is done by transistor MC1 and the fine block 4 itself; cascoding of the fine block is done by using a dummy node N_{dummy} with the same voltage as is on node N_{OUT}. By using a circuit as explained above, the coarse and/or fine bit transistors can be used in a mode which is close to linear mode without loosing accuracy nor monotonicity.

[0057]   A possible example of used separation of incoming digital bits between coarse and fine blocks 2, 4 and PWM is illustrated in Fig. 4. From an incoming 17-bit digital word, the MSB is a polarity bit, defining whether the incoming digital word has to go to a structure with elements of a first type, for example NMOS transistors, or to a same structure with elements of a second type opposite to the first type, for example PMOS transistors. The next seven MSBs are controlling the the coarse block 2. The next five bits are controlling the fine block. The four LSB are used for PWM.

[0058]   A current mode DAC according to the present invention, as described above, has the following features:

- current mode output
- high number of bits (e.g. 16 bits)
- guaranteed monotonicity and no missing code over the full range; with missing code is meant that, for two different digital input values, the same analog output value is obtained and the maximum step on output when increasing input data by one is below 2 LSBs
- low voltage drop
- high output impedance
- high accuracy over the full range
- PWM modulation possible

[0059]   It is to be understood that although preferred embodiments, specific constructions and configurations, as well as materials, have been discussed herein for devices according to the present invention, various changes or modifications in form and detail may be made without departing from the scope and spirit of this invention. For example, the embodiment shown in Fig. 3 and described hereinabove is for a current sink DAC. It will be clear for a person skilled in the art that the polarity of the devices and the current can be changed so as to create a current source DAC.

Claims

1. A monotonic digital-to-analog converter (1) for converting a digital input signal into an analog output signal, the converter comprising:

   - an input node for receiving the digital input signal having at least M+L bits,
   - an output node (N_{out}) for delivering the analog output signal corresponding to the received digital input signal,
   - a coarse conversion block (2) comprising current sources (6) and first switching means (8) for switching current of a first number of selected current sources (6) as a coarse block output current to the output node (N_{out}), said first number depending on a value of M more significant bits of the digital input signal, and from a first of N unselected current sources in the coarse conversion block (2) into a fine conversion block (4),
   - the fine conversion block (4) comprising means for receiving current from the first of N unselected current sources of the coarse conversion block (2), a current divider comprising current division means, and second switching means (16) for switching current of a second number of selected current division means in the fine conversion block (4) to the output node (N_{out}), said second number of selected current division means depending on a value of L less significant bits of the digital input signal,

   characterised in that the monotonic digital-to-analog converter (1) furthermore comprises:

   - a first cascode means (OA1 + MC1) for active cascoding of the coarse block output current, and
   - a second cascode means (OA2 + 14) comprising at least the current divider, for active cascoding of the current from the first of N unselected current sources in the coarse conversion block (2).

2. - A monotonic digital-to-analog converter (1) according to claim 1, the first switching means (8) being associated with a current branch (14), wherein the first switching means (8) consist of two switching devices (10, 12) with three states on the associated current branch (14), or of three-way switches.

3. - A monotonic digital-to-analog converter (1) according to any of the previous claims, wherein the second to Nth unselected current sources are switched off.

4. - A monotonic digital-to-analog converter(1) according to any of the previous claims, wherein the current sources of the coarse conversion block (2) are linearly weighted current sources (6).

5. - A monotonic digital-to-analog converter (1) according to any of the previous claims, wherein the current divider of the fine conversion block (4) is a linearly weighted current divider.

6. - A monotonic digital-to-analog converter (1) according to any of the previous claims, wherein the digital-to-analog converter (1) is furthermore provided with means for applying pulse width modulation (PWM) to current from a first unselected current division means of the fine conversion block (4).

7. - A monotonic digital-to-analog converter (1) according to any of the previous claims, furthermore comprising an output follower loop (OA3) for buffering a voltage on the output node (N_{out}).

8. - A method for converting a digital input signal comprising at least M+L bits into an analog signal, the method comprising:

   - providing said digital input signal at an input node,
   - selecting a first number of current sources (6) in a coarse conversion block (2), said first number depending on a value of M more significant bits of the digital input signal,
   - switching current of the selected first number of current sources (6) to an output node (N_{out}),
   - switching current from a first of N unselected current sources in the coarse conversion block (2) to a fine conversion block (4),
   - dividing the current from the switched first of N unselected current sources by means of a current divider comprising current division means in the fine conversion block (4),
   - selecting a second number of current division means in the fine conversion block (4), said second number depending on a value of L less significant bits of the digital input signal,
   - switching current of said selected current division means in the fine conversion block (4) to the output node (N_{out}),

characterised in that the method furthermore comprises:

- actively cascoding the coarse block output current, and
- actively cascading the current of the first of N unselected current sources in the coarse conversion block (2) by means of at least the current divider.

9. - A method according to claim 8, further comprising applying pulse width <5> modulation on current from a first unselected current division means in the fine conversion block (4), and switching this pulse width modulated current to the output node (N_{out})

10. - A method according to any of claims 8 to 9, furthermore comprising switching off the second to Nth unselected current sources in the coarse conversion block (2).

11. - A method according to any of claims 8 to 10, wherein dividing the current from the switched unselected current source in the coarse conversion block (2) by means of a current divider in the fine conversion block (4) is such that said current is equally divided over different branches (14) in the fine conversion block (4).

12. - A method according to any of claims 8 to 11, furthermore comprising buffering a voltage on the output node (N_{out}).

Patentansprüche

1. Monotoner Digital-Analog-Wandler (1) zum Wandeln eines digitalen Eingangssignals in ein analoges Ausgangssignal, wobei der Wandler aufweist:

- einen Eingangsknoten zum Empfangen des digitalen Eingangssignals mit zumindest M + L Bits,
- einen Ausgangsknoten (N_{out}) zum Liefern des analogen Ausgangssignals entsprechend dem empfangenen digitalen Eingangssignal,
- einem Grobumwandlungsblock (2) mit Stromquellen (6) und einer ersten Schalteinrichtung (8) zum Schalten des Stroms einer ersten Anzahl ausgewählter Stromquellen (6) als Grobblock-Ausgangsstrom zum Ausgangsknoten (N_{out}), wobei die erste Anzahl von einem Wert von M signifikanteren Bits des digitalen Eingangssignals abhängt, und von einer ersten von N unausgewählten Stromquelle in dem Grobumwandlungsblock (2) in einen Feinumwandlungsblock (4),
- wobei der Feinumwandlungsblock (4) eine Einrichtung zum Empfangen des Stroms von der ersten der N unausgewählten Stromquelle des Grobumwandlungsblocks (2), einen Stromteiler mit Stromteilungseinrichtungen und eine zweite Schalteinrichtung (16) zum Schalten des Stroms einer zweiten Anzahl von ausgewählten Stromteilungseinrichtungen in dem Feinumwandlungsblock (4) in den Ausgangsknoten (N_{out}) aufweist, wobei die zweite Anzahl ausgewählter Stromteilungseinrichtungen von einem Wert von L weniger signifikanten Bits des digitalen Eingangssignals abhängt,

dadurch gekennzeichnet, dass der monotone Digital-Analog-Wandler (1) weiterhin aufweist:

- eine erste Kaskodeneinrichtung (OA1 + MC1) zum aktiven Kaskodieren des Grobblockausgangsstroms, und
- eine zweite Kaskodeneinrichtung (OA1 + 14) mit zumindest dem Stromteiler zum aktiven Kaskodieren des Stroms von den ersten der N unausgewählten Stromquellen in den Grobumwandlungsblock (2).

2. Monotoner Digital-Analog-Wandler (1) nach Anspruch 1,
wobei die erste Schalteinrichtung (8) einem Stromzweig (14) zugeordnet ist,
wobei die erste Schalteinrichtung (8) aus zwei Schaltvorrichtungen (10, 12) mit drei Zuständen auf dem zugeordneten Stromzweig (14) oder aus drei-Weg-Schaltern besteht.

3. Monotoner Digital-Analog-Wandler (1) nach einem der vorhergehenden Ansprüche,
wobei die zweite bis N-te unausgewählte Stromquelle ausgeschaltet sind.

4. Monotoner Digital-Analog-Wandler (1) nach einem der vorhergehenden Ansprüche,
wobei Stromquellen des Grobumwandlerblocks (2) linear gewichtete Stromquellen (6) sind.

5. Monotoner Digital-Analog-Wandler (1) nach einem der vorhergehenden Ansprüche,

wobei der Stromteiler des Feinumwandlungsblocks (4) ein linear gewichteter Stromteiler ist.

6. Monotoner Digital-Analog-Wandler (1) nach einem der vorhergehenden Ansprüche,
   wobei der Digital-Analog-Wandler (1) weiterhin mit einer Einrichtung zum Anwenden einer Impulsbreitenmodulation (PWM) an den Strom von einer ersten unausgewählten Stromteilungseinrichtung des Feinumwandlungsblocks (4) ausgestattet ist.

7. Monotoner Digital-Analog-Wandler (1) nach einem der vorhergehenden Ansprüche,
   welcher weiterhin eine Ausgangsfolgerschleife (OA3) zum Puffern einer Spannung an dem Ausgangsknoten (N_{out}) aufweist.

8. Verfahren zum Umwandeln eines digitalen Eingangssignals mit zumindest M + L Bits in ein analoges Signal, wobei das Verfahren aufweist:

   - Liefern des digitalen Eingangssignals an einem Eingangsknoten,
   - Ausführen einer ersten Anzahl von Stromquellen (6) in einem Grobumwandlungsblock (2), wobei die erste Anzahl von einem Wert M signifikanterer Bits des digitalen Eingangssignals abhängt,
   - Schalten eines Stroms der ersten ausgewählten Anzahl von Stromquellen (6) auf einem Ausgangsknoten (N_{out}),
   - Schalten eines Stroms von einer ersten von N unausgewählten Stromquellen in dem Grobumwandlungsblock (2) auf einen Feinumwandlungsblock (4),
   - Teilen des Stroms von der geschalteten ersten der N unausgewählten Stromquellen mittels eines Stromteilers mit Stromteilungseinrichtungen in den Feinumwandlungsblock (4),
   - Ausführen einer zweiten Anzahl von Stromteilungseinrichtungen in dem Feinumwandlungsblock (4), wobei die zweite Anzahl von einem Wert von L weniger signifikanten Bits des digitalen Eingangssignals abhängt,
   - Schalten des Stroms der ausgewählten Stromteilungseinrichtungen in dem Feinumwandlungsblock (4) auf den Ausgangsknoten (N_{out}),

   dadurch gekennzeichnet, dass das Verfahren weiterhin aufweist:

   - aktives Kaskodieren des Grobumwandlungsblock-Ausgangsstroms, und
   - aktives Kaskodieren des Stroms der ersten der N unausgewählten Stromquellen in den Grobumwandlungsblock (2) zumindest mittels des Stromteilers.

9. Verfahren nach Anspruch 8,
   weiterhin aufweisend das Anlegen einer Impulsbreitenmodulation an einen Strom von einer ersten unausgewählten Stromteilungseinrichtung in dem Feinumwandlungsblock (4) und Schalten dieses impulsbreitenmodulierten Stroms auf den Ausgangsknoten (N_{out}).

10. Verfahren nach einem der vorhergehenden Ansprüche,
    weiterhin aufweisend das Ausschalten der zweiten bis N-ten unausgewählten Stromquellen in dem Grobumwandlungsblock (2).

11. Verfahren nach einem der Ansprüche 8 bis 10,
    wobei das Teilen des Stroms von der geschalteten unausgewählten Stromquelle in dem Grobumwandlungsblock (2) mittels eines Stromteilers in dem Feinumwandlungsblock (4) derart gestaltet ist, dass der Strom gleich über verschiedene Zweige (14) in dem Feinumwandlungsblock (4) geteilt wird.

12. Verfahren nach einem der Ansprüche 8 bis 11,
    weiterhin aufweisend das Puffern einer Spannung an dem Ausgangsknoten (N_{out}).

Revendications

1. Convertisseur numérique / analogique monotone (1) servant à convertir un signal numérique d'entrée en un signal analogique de sortie, le convertisseur comprenant :

   - un noeud d'entrée pour recevoir le signal numérique d'entrée ayant au moins M + L bits,
   - un noeud de sortie (N_{out}) pour fournir le signal analogique de sortie correspondant au signal numérique

appliqué à l'entrée,
- un bloc de conversion grossière (2) comprenant des sources de courant (6) et des premiers moyens de commutation (8) pour commuter le courant provenant d'un premier nombre de sources de courant (6) sélectionnées, en tant que courant de sortie de bloc de conversion grossière, vers le noeud de sortie (N_{out}), ledit premier nombre dépendant d'une valeur de M bits de poids plus fort du signal numérique d'entrée, et le courant provenant d'une première de N sources de courant non sélectionnées dans le bloc de conversion grossière (2), vers un bloc de conversion fine (4),
- le bloc de conversion fine (4) comprenant des moyens pour recevoir du courant provenant de la première des N sources de courant non sélectionnées dans le bloc de conversion grossière (2), un diviseur de courant comprenant des moyens de division de courant, et des deuxièmes moyens de commutation (16) pour commuter le courant provenant d'un deuxième nombre de moyens sélectionnés de division de courant, situés dans le bloc de conversion fine (4), vers le noeud de sortie (N_{out}), ledit deuxième nombre de moyens sélectionnés de division de courant dépendant d'une valeur de L bits de poids moindre du signal numérique d'entrée,

caractérisé en ce que le convertisseur numérique / analogique monotone (1) comprend en outre :

- un premier moyen formant cascode (OA1 + MC1) pour le raccordement actif en cascode du courant de sortie du bloc de conversion grossière, et
- un deuxième moyen formant cascode (OA2 + 14) comprenant au moins le diviseur de courant, pour le raccordement actif en cascode du courant provenant de la première des N sources non sélectionnées de courant dans le bloc de conversion grossière (2).

2. Convertisseur numérique / analogique monotone (1) selon la revendication 1, les premiers moyens de commutation (8) étant associés à une branche de courant (14), dans lequel les premiers moyens de commutation (8) consistent en deux dispositifs de commutation (10, 12) à trois états sur la branche associée de courant (14), ou en des commutateurs à trois positions.

3. Convertisseur numérique / analogique monotone (1) selon l'une des revendications précédentes, dans lequel la deuxième à la Nième sources non sélectionnées de courant sont mises hors fonction.

4. Convertisseur numérique / analogique monotone (1) selon l'une quelconque des revendications précédentes, dans lequel les sources de courant du bloc de conversion grossière (2) sont des sources de courant (6) à pondération linéaire.

5. Convertisseur numérique / analogique monotone (1) selon l'une quelconque des revendications précédentes, dans lequel le diviseur de courant du bloc de conversion fine (4) est un diviseur de courant à pondération linéaire.

6. Convertisseur numérique / analogique monotone (1) selon l'une quelconque des revendications précédentes, dans lequel le convertisseur numérique / analogique (1) est en outre pourvu de moyens pour appliquer une modulation de largeur d'impulsion (PWM) au courant provenant d'un premier moyen, non sélectionné, de division de courant du bloc de conversion fine (4).

7. Convertisseur numérique / analogique monotone (1) selon l'une quelconque des revendications précédentes, comprenant en outre une boucle de régulation de sortie (OA3) servant de tampon pour une tension sur le noeud de sortie (N_{out}).

8. Procédé pour la conversion d'un signal numérique d'entrée, comprenant au moins M + L bits, en un signal analogique, le procédé comprenant :

- la fourniture dudit signal numérique d'entrée à un noeud d'entrée,
- la sélection d'un premier nombre de sources de courant (6) dans un bloc de conversion grossière (2), ledit premier nombre dépendant d'une valeur de M bits de poids plus fort du signal numérique d'entrée,
- la commutation du courant provenant du premier nombre sélectionné de sources de courant (6) vers un noeud de sortie (N_{out}),
- la commutation du courant provenant d'une première de N sources de courant non sélectionnées dans le bloc de conversion grossière (2), vers un bloc de conversion fine (4),
- la division du courant provenant de la première des N sources de courant non sélectionnées, qui a été commutée, au moyen d'un diviseur de courant comprenant des moyens de division de courant, dans le bloc

de conversion fine (4),
- la sélection d'un deuxième nombre de moyens de division de courant, dans le bloc de conversion fine (4), ledit deuxième nombre dépendant d'une valeur de L bits de poids moindre du signal numérique d'entrée,
- la commutation du courant provenant desdits moyens sélectionnés de division de courant, dans le bloc de conversion fine (4), vers le noeud de sortie (N_{out}),

caractérisé en ce que le procédé comprend en outre :

- le raccordement actif en cascode du courant de sortie du bloc de conversion grossière, et
- le raccordement actif en cascode du courant provenant de la première des N sources non sélectionnées de courant dans le bloc de conversion grossière (2), au moyen au moins du diviseur de courant.

9. Procédé selon la revendication 8, comprenant en outre l'application d'une modulation de largeur d'impulsion au courant provenant d'un premier moyen, non sélectionné, de division de courant du bloc de conversion fine (4), et la commutation de ce courant à modulation de largeur d'impulsion vers le noeud de sortie (N_{out}).

10. Procédé selon la revendication 8 ou 9, comprenant en outre la mise hors fonction de la deuxième à la Nième sources non sélectionnées de courant dans le bloc de conversion grossière (2).

11. Procédé selon l'une quelconque des revendications 8 à 10, dans lequel la division du courant provenant de la source de courant non sélectionnée et commutée dans le bloc de conversion grossière (2), au moyen d'un diviseur de courant dans le bloc de conversion fine (4), est telle que ledit courant soit divisé de manière égale sur différentes branches (14), dans le bloc de conversion fine (4).

12. Procédé selon l'une quelconque des revendications 8 à 11, comprenant en outre le tamponnage d'une tension sur le noeud de sortie (N_{out}).
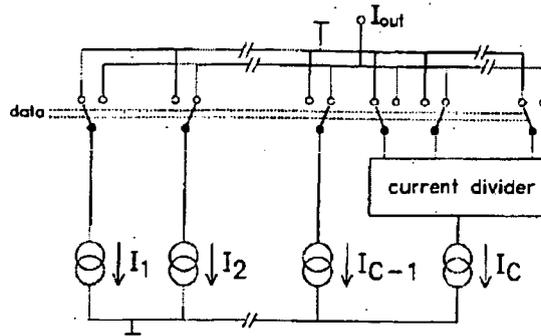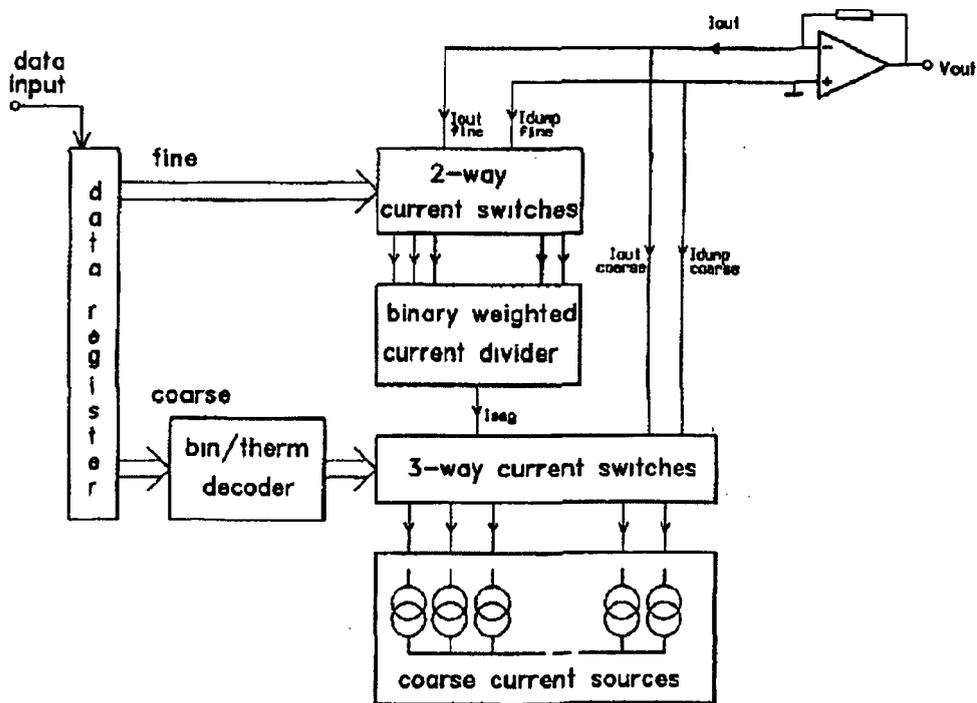
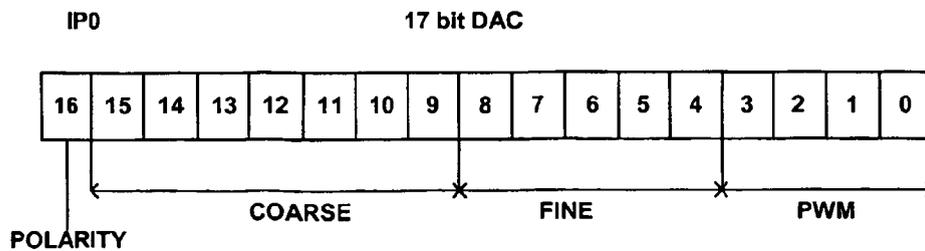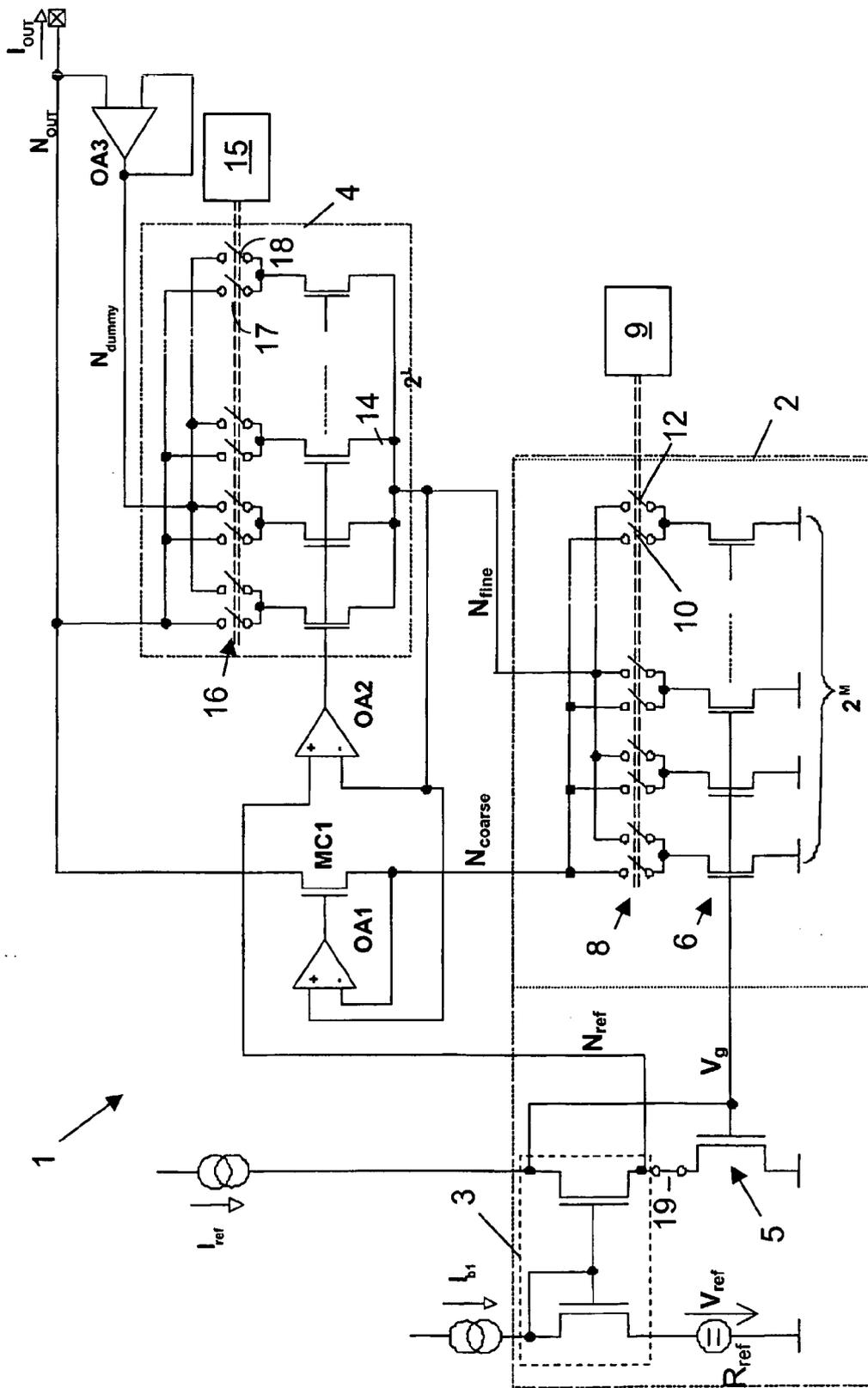# Fig. 1 - PRIOR ART

Fig. 2 - PRIOR ART

Fig. 4

Fig. 3

REFERENCES CITED IN THE DESCRIPTION

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