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(54) Boron phosphide based semiconductor device

Boronphosphid-Halbleiterbauelement

Composant a semi-conducteur a base de phosphure de bore

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- **PATENT ABSTRACTS OF JAPAN vol. 2002, no. 02, 2 April 2002 (2002-04-02) & JP 2001 284643 A (SHOWA DENKO KK), 12 October 2001 (2001-10-12)**

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Description

Technical Field:

[0001] The present invention relates to a boron phosphide-based semiconductor device having crystal structure of a boron phosphide based semiconductor layer formed on a silicon (Si) single crystal (silicon) substrate, which is suitable for obtaining a boron phosphide-based semiconductor device, and to a light-emitting diode.

Background Art:

[0002] There are conventionally known techniques of forming by the use of boron phosphide (BP) a semiconductor light-emitting device, such as a light-emitting diode (LED) and a laser diode (LD), which is one of boron phosphide semiconductors containing boron (B) and phosphorus (P) as constituent elements (see, U.S. Patent No. 6,069,021). Conventional boron phosphide light-emitting devices are fabricated using, for example, a stacked layer structure where a boron phosphide layer is formed as a buffer layer on a substrate composed of a silicon single crystal (silicon) (see, U.S. Patent No. 6,069,021, *supra*). In recent years, there has been invented a stacked layer structure for semiconductor light-emitting devices, which has a light-emitting part comprising a pn-junction double hetero structure that uses as a clad layer a boron phosphide layer with a wide bandgap (see, Japanese Patent Application No. 2001-158282).

[0003] It has been heretofore known that on a silicon substrate, a boron phosphide single crystal layer comprising the same crystal plane as the crystal plane constituting the substrate surface grows. For example, on a {100}-Si single crystal substrate, the surface of which is a {100} crystal plane, a boron phosphide single crystal layer comprising {100} crystal planes stacked in parallel with the substrate surface is known to grow (see, "Semiconductor Technology (First Volume)" by Katsufusa SHONO, 9th imp., page 77, Tokyo University Publishing Association (June 25, 1992)). It is also known that on a silicon substrate, a boron phosphide single crystal layer not containing a twin crystal (twinning) at all can be grown (see, "Semiconductor Technology (First Volume)", supra, page 98). On the other hand, it is known that a {100}-boron phosphide single crystal layer containing twining can also be obtained (see, "Semiconductor Technology (First Volume)", supra, pages 99-100).

[0004] Conventional techniques disclose that the twinning contained in a boron phosphide layer has a property of relaxing the mismatching ratio between crystal lattices (see, "Semiconductor Technology (First Volume)", *supra,* page 100). Accordingly, when a boron phosphide-based semiconductor layer containing twinning is used, this can contribute to the production of an LED having excellent characteristics including high emission intensity, for example. However, as disclosed in conventional techniques, the boron phosphide-based semiconductor layer containing twinning cannot be stably obtained. That is, conditions necessary for producing a boron phosphide based semiconductor layer stably containing twinning are not heretofore clarified and therefore a light-emitting device having excellent emission intensity, for example, cannot be stably obtained.

[0005] Nishinaga and Mizutani in "Japanese Journal of Applied Physics", Vol. 14, No. 6, June 1975, p. 753-760 disclose a semiconductor device comprising a zinc-blende type BP-based polycrystalline layer formed on a {111} surface of a Si substrate.

[0006] Takigawa et al. in "Japanese Journal of Applied Physics", Vol. 13, No. 3, March 1974, p. 411-416 disclose a process of epitaxially forming a BP based polycrystalline layer on a {111} surface of a Si substrate by MOCVD using a temperature of 950-1050°C and a growth rate of about 12-60 nm/min.

[0007] Kumashiro et al. in "Journal of Crystal Growth", 70 (1984), p. 507-514 disclose the growth of BP single crystals on (111) oriented Si substrates.

[0008] US 6069021 discloses a semiconductor device comprising a BP based polycrystalline layer on a {111} surface of a Si substrate.

[0009] An object of the present invention is to provide a boron phosphide- based semiconductor device improved in its properties by having the device provided with a polycrystalline boron phosphide based semiconductor layer stably containing twinning and having a specific crystal surface as a twinning plane.

[0010] Another object of the invention is to provide an LED excellent in efficiency of taking out emitted light toward the outside.

[0011] Here, the boron phosphide based semiconductor layer comprising the crystal structure is not a conventional boron phosphide based semiconductor layer comprising a film-form single crystal, but a boron phosphide based semiconductor comprising a polycrystal that is an aggregate of single crystal entities different in the crystal direction of the twinning interface (twinning plane) (see, "Chemical Crystallography" by C.W. Van, 1st ed., pages 75-76, Baifukan (June 15, 1970)).

Disclosure of the Invention:

[0012] The present invention provides the following.

(1) A boron phosphide based semiconductor device comprising a silicon single crystal substrate (101) and a boron phosphide based polycrystalline layer (103) formed on a {111} surface of said substrate, wherein said boron phosphide based polycrystalline layer (103) is composed of an aggregate of a plurality of triangular pyramidal single crystal entities (13) connected with each other through side faces (16), each of said single crystal entities (13) having a {111} bottom face (13a) being parallel with said {111} surface of said substrate and each of said single crystal entities (13) having {111} side faces (16), characterised in that inside each of said single crystal entities (13) a plurality of twinning interfaces (14) are regulary incorporated, whereby said twinning interfaces (14) are parallel with any one of said {111} side faces (16), whereby said twinning interfaces (14) in different ones of said single crystal entities (13) have different <111> directions, and whereby the intersections of said twinning interfaces (14) with said {111} surface of said substrate forms an angle of 60 degrees relative to a <110> direction in said {111} surface of said substrate.

(2) The boron phosphide based semiconductor device according to (1) above, further comprising a group III-V compound semiconductor layer (104) stacked on said boron phosphide based polycrystalline layer (103) and forming a heterojunction therewith , whereby the lattice spacing constituting said group III-V compound semiconductor layer (104) agrees with the lattice spacing of crystal planes intersecting with surfaces of said single crystal entities constituting the boron phosphide based polycrystalline layer (103).

(3) The boron phosphide based semiconductor device according (2) above, further comprising a second boron phosphide based polycrystalline layer (105) as defined in claim 1 stacked onto said group III-V compound semiconductor layer (104) and forming a heterojunction therewith, whereby said said group III-V compound semiconductor layer (104) is a light emitting layer and said first and second boron phosphide based polycrystalline layers (103, 105) are lower and upper cladding layers forming a double heterojunction light emitting diode.

(4) The boron phosphide based semiconductor device according to any one of (1) to (3) above, wherein each single crystal entity (13) of said boron phosphide based polycrystalline layer (103) consists of a boron monophosphide crystal.

(5) A light-emitting diode comprising a phosphide based semiconductor device according to (3) or (4) above, wherein the lower clad layer (103) has a thickness of d nm and the light emitted from the light-emitting layer (104) has a wavelength of $\lambda = 0.135d + 380$ nm, provided that 420 nm $\leq \lambda \leq$ 490 nm.

[0013] According to the present invention, as described above, since the boron phosphide based polycrystalline layer provided on the Si single crystal substrate is composed of an aggregate of a plurality of connected triangular pyramidal single crystal entities containing twinning interfaces capable of absorbing misfit dislocation and preventing the propagation of dislocation, it is possible to construct a boron phosphide based semiconductor layer excellent in crystallinity and reduced in dislocation density. As a result, it is possible to provide a boron phosphide based semiconductor device using the boron phosphide based semiconductor layer and having excellent characteristics, such as high emission intensity, excellent rectification property and high breakdown voltage.

[0014] In addition, since the upper and lower clad layers sandwiching the light-emitting layer of the light-emitting diode according to the present invention are composed of the polycrystal layer that is an aggregate of a plurality of single crystal entities including twining interfaces and since the lower clad layer is adjusted to have a thickness that can bring about emitted-light reflection of not less than 30%, it is possible to provide a light-emitting diode excellent in efficiency of taking out emitted light toward the outside.

Brief Description of the Drawings:

[0015]

Fig. 1 is a schematic view showing the form of a single crystal entity constituting the polycrystal layer in the device according to the present invention.
Fig. 2 is a schematic plan view showing the structure of the polycrystal layer in the device according to the present invention.
Fig. 3 is a schematic view showing crystal planes intersecting with the {111} crystal plane of the boron phosphide-

based semiconductor layer in the device according to the present invention.

Fig. 4 is a schematic plan view of the LED according to an Example of the present invention.

Fig. 5 is a cross-sectional schematic view of the LED taken along line V-V of Fig. 4.

Fig. 6 is a view showing the electron beam diffraction pattern of the boron phosphide layer according to an Example of the present invention.

Fig. 7 shows an example of the wavelength dependency of the reflectance of a p-type boron phosphide layer.

Best Mode for Carrying Out the Invention:

[0016] In the present invention, the boron phosphide based semiconductor layer is formed on a {111} crystal plane surface of a Si single crystal substrate (in this description, this substrate is referred to as a {111}-Si single crystal substrate). On the {111} crystal plane of a diamond crystal structure Si single crystal, silicon atoms are more densely present than on the {100} or {110} crystal plane. Therefore, the {111}-Si single crystal substrate is advantageous in that the constituent elements of a boron phosphide based semiconductor layer deposited on the substrate can be prevented from diffusing in or penetrating through the interior of the substrate. This is effective in constituting a clear junction interface. Also, when the {111}-Si single crystal substrate has electrical conductivity, this provides an effect of, for example, facilitating the fabrication of a light-emitting device, because an ohmic electrode having either positive or negative polarity can be provided on the back surface as a back electrode. In particular, an electrically conducting single crystal substrate having a low resistivity (specific resistance) of 1 mΩ·cm or less, preferably 0.1 mΩ·cm or less, contributes to the production of an LED having a low forward voltage (so-called Vf). Furthermore, this substrate has excellent heat radiation property and therefore, is effective in fabricating an LD for which stable oscillation is ensured.

[0017] The boron phosphide based semiconductor layer stacked, as a polycrystal layer, on the surface of the {111}-Si substrate is a layer containing boron (B) and phosphorus (P) as constituent elements, such as a layer of $B\alpha Al\beta Ga\gamma In_{1-\alpha-\beta-\gamma}P_{1-\delta}As_{\delta}$ (wherein $0 < \alpha \leq 1$, $0 \leq \beta < 1$, $0 \leq \gamma < 1$, $0 < \alpha+\beta+\gamma \leq 1$ and $0 \leq \delta < 1$). Or, the polycrystal layer can be composed of, for example, a layer of $B_{\alpha}Al_{\beta}Ga_{\gamma}In_{1-\alpha-\beta-\gamma}P_{1-\delta}N_{\delta}$ (wherein $0 < \alpha \leq 1$, $0 \leq \beta < 1$, $0 \leq \gamma < 1$, $0 < \alpha+\beta+\gamma \leq 1$ and $0 \leq \delta < 1$). A boron monophosphide (BP) is particularly preferred because the constituent elements are only boron (B) and phosphorus (P), and the film formation is advantageously easier than the multi-element mixed crystal due to the small number of constituent elements. A boron phosphide, for example, grown by metal organic chemical vapor deposition (MOCVD) means under the conditions such that the growth rate is from 2 to 30 nm/min and the supply ratio (so-called V/III ratio) of raw materials between the group V element, such as phosphorus, and the group III element, such as boron, is from 15 to 60, becomes a wide bandgap semiconductor having a bandgap of about 3 eV at room temperature. The boron phosphide semiconductor layer having such a wide bandgap can be used, for example, as a clad layer for a light-emitting layer in a light-emitting device.

[0018] In the present invention, the boron phosphide based semiconductor layer that is the polycrystal layer is constructed by aggregating a plurality of single crystal entities comprising a boron phosphide based semiconductor crystal. Fig. 1 schematically shows the form of the single crystal entity constituting the polycrystal layer in the device according to the present invention. Each single crystal entity 13 on a {111}-Si single crystal substrate 11 has an outer shape of a regular triangular pyramidal body 13b, the periphery of which is surrounded by planes equivalent to the {111} crystal plane of a boron phosphide-based semiconductor crystal, or a regular triangular pyramidal body 13c, the top part of which has a {111} crystal plane. The bottom face 13a of each single crystal entity 13 is composed of a {111} crystal plane of a boron phosphide based semiconductor crystal disposed in parallel with the {111} crystal plane of the {111}-Si single crystal substrate. The bottom face 13a means a crystal plane contacting the surface of the {111}-Si single crystal substrate 11.

[0019] As shown in a schematic plan view of Fig. 2, the polycrystal layer 12 of the present invention is constructed by connecting a plurality of triangular pyramidal single crystal entities 13 with each other. Respective single crystal entities 13 are connected with each other through a junction face 16. Inside each single crystal entity 13, twinning 15 is present. The direction in which the twinning plane 14 of the twinning incorporated inside each single crystal entity exists is not uniformly constant and therefore, the boron phosphide based semiconductor layer composed of single crystal entities 13 containing twinning in different crystal directions is referred to as a polycrystalline layer 12 in the present invention. Particularly, in the present invention, the polycrystalline layer 12 is constructed by aggregating single crystal entities 13 each having twinning regularly incorporated to direct the twinning plane at an angle of 60° with respect to the <110> crystal direction of the {111}-Si single crystal constituting the substrate. The twinning plane as used herein specifically means a plane equivalent to the {111} crystal plane of the boron phosphide based semiconductor crystal, namely, a crystal plane, such as {111}, {-1.-1.-l.}, {1.-1.1.}, etc. Also, the twinning plane is characterized by running parallel with any one of {111} crystal planes of the boron phosphide-based semiconductor crystal, constituting the periphery of the triangular pyramidal single crystal entity 13. By virtue of the generation of twinning 15 having a twinning plane 14 that is a {111} crystal plane of the boron phosphide-based semiconductor crystal, the generation and propagation of misfit dislocation ascribable to lattice mismatching between the Si single crystal substrate and the boron phosphide based

semiconductor crystal can be effectively suppressed. In the boron phosphide based semiconductor crystal, the twinning having a {111} crystal plane as the twinning plane can be stably and easily formed as compared with twinning having a different crystal plane as the twinning plane. Accordingly, when the polycrystal layer 12 is constructed by aggregating single crystal entities each containing twinning having as the twinning plane a {111} crystal plane of the boron phosphide based semiconductor crystal, an effect of stably suppressing the propagation of misfit dislocation can be provided.

[0020] The presence of twinning is known, for example, by the presence or absence of an abnormal diffraction spot on an electron diffraction pattern photographed using an electron diffraction technique (see, "Crystal Electron Microscopy" by Kimitomo SAKA, 1st ed. pages 111-113, Uchida Rokakuho (November 25, 1997)). Also, by measuring the angle between the <110> crystal direction and the diffraction spot ascribable to twinning on a diffraction pattern photographed by entering an electron beam in parallel with the <110> crystal direction of the boron phosphide-based semiconductor layer, the angle formed by the <110> crystal direction and the twinning can be known. Incidentally, the twinning can be regarded as a kind of stacking fault (see, "Crystal Electron Microscopy", supra, page 112).

[0021] For obtaining the polycrystal layer according to the device of the present invention that is an aggregate of single crystal entities each containing twinning, the conditions at the film formation have to be precisely controlled. In particular, a triangular pyramidal single crystal entity comprising a boron phosphide based semiconductor crystal containing twinning having a {111} crystal plane as the twinning plane is formed by an atmospheric pressure metal organic chemical vapor deposition (MOCVD) method using a starting material system of triethylborane ($(C_2H_5)_3B$)/phosphine (PH_3)/hydrogen (H_2) while precisely controlling the growth temperature. In the MOCVD method, the temperature for obtaining a boron phosphide based semiconductor polycrystal layer, particularly, a polycrystalline layer of boron monophosphide is preferably from 950 to 1,100°C, more preferably from 1,025 to 1,075°C. For forming a boron phosphide based semiconductor polycrystal layer containing indium (In), a lower temperature of about 950 to about 1,000°C is preferred and for forming a boron phosphide-based semiconductor polycrystal layer containing aluminum (Al) as a constituent element, a relatively high temperature of about 1,050 to 1,100°C is preferred. At a high temperature exceeding about 1,200°C, a polyhedral boron phosphide, such as BP_6 or $B_{13}P_2$, is readily generated and this is disadvantageous in obtaining a boron phosphide based semiconductor layer having a homogeneous composition.

[0022] For efficiently forming a single crystal entity having twining therein, the growth rate is preferably from 20 to 60 nm/min. In the case of boron monophosphide (BP), the particularly preferable growth rate is from 30 to 40 nm/min. In a single crystal entity grown at a rate exceeding 60 nm, a large amount of twinning (stacking fault) and additionally, an abrupt increase in the density of other crystal faults, such as point defects and dislocations, are disadvantageously generated and a polycrystal layer having excellent crystallinity can be hardly obtained. On the contrary, if the growth rate is reduced, in other words, if a longer time is necessary for obtaining a boron phosphide based semiconductor layer having a desired layer thickness, the occasion of causing volatilization of phosphorus (P) that is a constituent element increases at the growth time. Therefore, if the growth rate is as small as less than 20 nm/min, non-equilibrium abruptly occurs in the chemical equivalent ratio between the constituent elements of the boron phosphide based semiconductor layer due to vaporization or volatilization of phosphorus (P). A boron phosphide based compound semiconductor layer having a stoichiometrically non-equilibrium composition contains a large amount of point defects and therefore, is not suitable as the polycrystalline layer for use in the present invention.

[0023] The twinning contained inside the single crystal entity has an activity of suppressing the propagation of misfit dislocation generated due to lattice mismatching, for example, between the silicon single crystal of the substrate and the boron phosphide based semiconductor constituting the single crystal entity. For example, a misfit dislocation generated from the junction interface between the Si substrate and the single crystal entity is absorbed by the twinning present inside the single crystal entity and prevented from propagating to the upper part. As a result, the density of dislocations passed through to reach the upper part of the single crystal entity is reduced.

[0024] For obtaining a single crystal entity reduced in the misfit dislocation, technical means of providing a buffer layer in the middle between the Si single crystal substrate and the boron phosphide-based semiconductor layer is also effective. The buffer layer is preferably composed of an amorphous or polycrystalline boron phosphide based compound semiconductor layer. The amorphous or polycrystalline buffer layer exerts an effect of relaxing the lattice mismatching with the Si single crystal constituting the substrate and providing a boron phosphide based semiconductor layer reduced in the density of the crystal defects, such as misfit dislocations. In particular, when the buffer layer is composed of a boron phosphide based semiconductor, this provides an effect of forming a boron phosphide based semiconductor layer having continuity on the buffer layer because boron and phosphorus act as "growth nuclei" accelerating the growth. In the case of constituting the buffer layer of boron phosphide, the layer thickness is preferably from about 1 to 50 nm, more preferably from 2 to 15 nm.

[0025] The surface layer part of the polycrystalline layer constructed by aggregating single crystal entities containing twinning forms a region reduced in the misfit dislocation passed through from the lower Si single crystal substrate side, and favored with excellent crystallinity. Accordingly, on the boron phosphide based semiconductor polycrystal layer having the constitution of the present invention, a deposited layer having excellent crystallinity can be grown. In particular, when the deposited layer is a crystal layer constituted of crystal planes arrayed at the same interval as the spacing

(lattice spacing) of crystal lattices intersecting with the surface of the single crystal entity of the boron phosphide based semiconductor forming the surface of the polycrystal layer, this is effective in obtaining a crystal layer reduced in misfit dislocations and favored with excellent crystallinity. As schematically shown in Fig. 3, a lower Miller index {hkl} plane crossing the surface 17 composed of a {111} crystal plane of the single crystal entity includes {110} and {100} crystal planes in addition to the {111} crystal plane of h = k=l=1. The spacing (= D) of these {hkl} crystal planes on the surface of the {111} crystal plane of the single crystal is given, in the case of a cubic zinc blend-type boron phosphide based semiconductor crystal, as $D (Å) = a/\{(h^2+k^2+l^2)^{1/2} \cdot \sin\theta\}$, wherein a (Å) denotes a lattice constant of the boron phosphide based semiconductor crystal and θ denotes an angle (°) between the {111} crystal surface 17 and the crystal plane crossing it. Examples thereof include a case of depositing on the surface of a boron phosphide (BP) polycrystal layer, a layer of wurtzite-type gallium·indium nitride mixed crystal ($Ga_{0.94}In_{0.06}N$) having arrayed therein hexagonal (1.0.0.0.) crystal planes each agreeing in the lattice spacing (≈ 3.21 Å) with the {110} crystal plane orthogonally meeting the {111} crystal plane of the BP single crystal entity 13 constituting the surface of the BP polycrystal layer. Such a crystal layer having excellent crystallinity can be suitably used, for example, as a light-emitting layer giving high-intensity emission in a light-emitting device.

[0026] Examples of the boron phosphide based semiconductor device that can be fabricated using the polycrystal layer composed of a boron phosphide based semiconductor according to the present invention include an LED: The LED can be fabricated, for example, based on a stacked layer structure comprising a p-type {111}-Si single crystal substrate, a p-type boron phosphide (BP) polycrystal layer as defined in the present invention grown on the substrate through an amorphous buffer layer containing boron (B) and phosphorus (P), an n-type light-emitting layer on the polycrystal layer and an n-type boron phosphide (BP) polycrystal layer as defined in the present invention grown on the light-emitting layer. A polycrystal layer composed of single crystal entities of boron phosphide having a bandgap of about 3 eV at room temperature can be used as clad layers for sandwiching the light-emitting layer.

[0027] When the polycrystalline layer is used as clad layers, the thickness d (nm) of the lower clad layer is set to a value giving high reflectance for the wavelength λ (nm) of light emitted from the light-emitting layer. Here, the wavelength of light emitted from the light-emitting layer is represented by the peak wavelength. The reflectance of the lower clad layer for light at a specific wavelength (= λ) changes depending on the layer thickness (= d). For example, in a boron phosphide (BP) layer provided on a Si single crystal substrate, the layer thickness (= d) giving high reflectance for light in the range of $420 \text{ nm} \leq \lambda \leq 490 \text{ nm}$ can be approximately calculated by the following formula (1):

$$\lambda \text{ (nm)} \approx 0.135 \cdot d + 380 \quad \text{.........................} \quad (1)$$

[0028] For example, the thickness of the lower clad layer giving high reflectance for the emitted violet light at λ, = 420 nm is about 300 nm. A single layer composed of boron phosphide, provided on an Si single crystal substrate and having a thickness of about 300 to 320 nm, gives reflectance exceeding about 30% to about 40% for the emitted violet light at a wavelength of 420 nm. That is, the polycrystalline layer having the thickness adjusted as described above can advantageously constitute, even if it is a single layer, a lower clad layer having high reflectance for light at a wavelength of λ emitted from the light-emitting layer.

[0029] The reflectance can be measured with a general reflectometer, spectral ellipsometer or the like using laser light or visible light as the light source. The reflectance is calculated from the intensity ratio between the incident light at a certain wavelength and the reflected light on the same plane as the incident light. The reflectance is also expressed based on the ratio between the intensity of incident light at a certain wavelength and the intensity of reflected light in all azimuths irrespective of the scattering azimuth. The two are not discriminated but generically called reflectance in some cases. However, the reflectance as used in the present invention is a value calculated from the intensity ratio between the incident light and the reflected light on the same plane. Fig. 7 shows an example of the wavelength dependency of the reflectance of an undoped p-type boron phosphide layer formed on a Si single crystal substrate. When the reflectance of the lower clad layer is less than about 30%, in an LED for example, the intensity of emitted light released in the outside view-field direction is not improved. This is considered to be complicatedly affected by the plane area in the region where the current for driving an LED (LED driving current) can diffuse, the light-shielding effect of the electrode located in the direction for taking out emitted light toward the outside, and the like. When a boron monophosphide layer having reflectance of 30% or more, formed on an Si single crystal substrate, is used as the lower clad layer, an LED having an excellent efficiency for taking out emitted light toward the outside can be fabricated. Actually, a polycrystal layer having a reflectance of 100% can be hardly obtained because there is a possibility of the polycrystal layer absorbing the emitted light. In practice, the reflectance of the lower clad layer, which contributes to the improvement of emission intensity of an LED, is not less than 30% and less than 100%.

[0030] The thickness (= d) of the lower clad layer can be controlled by the adjustment of the time necessary for the film formation of a polycrystal layer. Supposing d = 1,000 nm, the wavelength (= λ) of emitted light, which can be suitably

applied in the present invention, is calculated according to formula (1) above as about 515 nm or less. On the contrary, when the layer thickness is extremely small, a continuous film satisfactorily and evenly covering the surface of an amorphous layer can be hardly obtained. Also, when the growth time is extremely short and the film thickness is small, irregular film growth partly takes place on the amorphous layer and a discontinuous film inhomogeneous in the thickness results. Irregular asperities (inhomogenous thickness) bring about light scattering and inhibit the improvement of reflectance in the constant direction. For constituting a lower clad layer having uniform junction properties with the light-emitting layer and excellent surface flatness giving high reflectance, a lower clad layer having a thickness of about 100 nm or more is suitably used.

[0031] When the upper clad layer is composed of the same boron phosphide polycrystal layer as the lower clad layer, the strains imposed on the light-emitting layer from the lower and upper clad layers sandwiching the light-emitting layer can be made almost equal in the quantity. This enables a light-emitting layer ensuring stable wavelength and excellent intensity of emitted light to be obtained. In particular, when the lower and upper clad layers are composed of the same boron phosphide polycrystal layer and have substantially the same thickness, the strains imposed on the light-emitting layer from the upper and lower sides of the light-emitting layer due to the difference in the coefficient of thermal expansion or the like between the materials of which the light-emitting layer and the clad layers are made, can be rendered more equal in the quantity. The "substantially the same thickness" as used herein means that the difference in the thickness is $\pm$10%. As described above, the layer thickness suitable for constituting the lower clad layer that serves also as the reflecting mirror and is a single layer provided on an Si single crystal substrate and composed of boron phosphide, is determined by formula (1). Accordingly, it is optimal to also determine the thickness of the upper clad layer in accordance with formula (1). By making equal the quantities of strains imposed on the light-emitting layer from the upper and lower clad layers, the wavelength of emitted light can be prevented from unstably becoming a short wavelength, and stable emission of light having a wavelength corresponding to the bandgap of the light-emitting layer can be advantageously obtained.

[0032] The light-emitting layer sandwiched between the upper and lower clad layers can also be composed of a single or multiple quantum well structure having a well layer comprising $GaxIn_{1-X}N$ ($0 \leq X \leq 1$) or $GaN_{1-Y}P_Y$ ($0 < Y \leq 1$). Incidentally, a barrier layer for the well layer can be composed of $Al_XGa_{1-X}N$ ($0 \leq X \leq 1$) or $GaN_{1-Z}P_Z$ ($0 \leq Z < 1$, $Z < Y$). An n-type ohmic electrode is provided on the n-type boron phosphide polycrystal layer forming the surface layer of the stacked layer structure, and a p-type ohmic electrode is disposed on the back surface of the p-type Si single crystal substrate, whereby an LED having a pn-junction hetero structure can be fabricated.

[0033] An electronic device, such as hetero junction field effect transistor (FET), can be fabricated from a stacked layer structure comprising an undoped high-resistance {111}-Si single crystal substrate, an oxygen-containing high-resistance boron phosphide polycrystal layer grown on the substrate through a polycrystalline buffer layer containing boron (B) and phosphorus (P), and a high-purity n-type gallium nitride (GaN) layer provided on the polycrystal layer as an active layer (electron channel layer). The FET is fabricated by providing a Schottky junction gate electrode on the active layer and providing source and drain ohmic electrodes at the positions opposing each other through the gate electrode on the surface of an n-type contact layer stacked on the active layer.

[0034] The single crystal entity containing twinning and composed of a boron phosphide based semiconductor crystal of the present invention has an activity of preventing upward propagation of misfit dislocations ascribable to the lattice mismatching between the Si single crystal substrate and the boron phosphide based semiconductor.

[0035] Examples:

The present invention is described in more detail below with reference to a case where an LED is fabricated from a stacked layer structure comprising a {111}-Si single crystal substrate having provided thereon a boron phosphide (BP) layer comprising a polycrystal layer.

[0036] Fig. 4 is a schematic plan view of an LED 1B according to the present invention, and Fig. 5 a schematic cross section of the LED 1B taken along line V-V in Fig. 4.

[0037] In a stacked layer structure 1A for use in the LED 1B, a boron-doped p-type Si single crystal having a plane offset by 2° from the {111} plane was constructed as a substrate 101. On the substrate 101, a buffer layer 102 composed of boron phosphide mainly comprising an amorphous one in the as-grown state was deposited at 350°C by an atmospheric-pressure MOCVD method using a triethylborane ($(C_2(_5)_3B$)/phosphine (PH_3)/hydrogen (H_2) system. The thickness of the buffer layer 102 thus deposited was about 10 nm.

[0038] On the surface of the buffer layer 102, a p-type boron phosphide (BP) layer 103 composed of a polycrystal layer was stacked as a lower clad layer at 1,050°C with vapor phase growth means used in the aforementioned MOCVD method. The growth rate was set to 40 nm/min. The carrier concentration of the p-type boron phosphide (BP) layer 103 was 1×10^{19} cm^{-3}, the thickness thereof was about 400 nm, and the bandgap thereof at room temperature was about 3.0 eV.

[0039] The crystal structure inside the p-type boron phosphide layer 103 was analyzed from the cross-sectional TEM

image and the electron beam diffraction pattern using a transmission electron microscope (TEM). Fig. 6 is a copy showing a diffraction pattern of the p-type boron phosphide layer 103, obtained by injecting an electron beam in parallel with the <110> crystal direction of the Si single crystal substrate 101. As shown in Fig. 6, a diffraction spot 19 attributable to the {111} crystal plane of each single crystal entity 103a constituting the p-type boron phosphide layer 103 composed of a polycrystal layer was positioned in parallel with the <111> crystal direction and adjacent to a diffraction spot 20 attributable to the (111) crystal plane of the Si single crystal substrate 101. From this, it was revealed that the single crystal entity 103a is a crystal entity where the {111} crystal plane of boron phosphide is stacked in parallel with the <111> crystal direction on the surface of the Si single crystal substrate. Furthermore, as shown in the diffraction pattern of Fig. 6, diffraction spots 21 attributable to twinning having a {111} crystal plane as the twinning plane were also observed in the vicinity of the diffraction spots of the single crystal entity 103a aligning in the <111> crystal direction of the Si single crystal substrate 101 and were symmetrically positioned, with the diffraction spots of the single crystal entity 103a as the symmetrical points. From this, it was confirmed that the single crystal entity 103a contains twinning having a {111} crystal plane as the twinning plane. It was confirmed from the position of the diffraction spot 21 attributable to the twinning that the twinning plane was present in the direction of 60° with respect to the <110> crystal direction of the BP crystal.

[0040] On the surface of the p-type boron phosphide layer 103, a light-emitting layer 104 composed of hexagonal n-type gallium indium nitride ($Ga_{0.90}In_{0.10}N$) was stacked at 850°C by an atmospheric-pressure MOCVD method using a system of trimethyl gallium ($(CH_3)_3Ga$)/trimethyl indium ($(CH_3)_3In$)/ammonia (NH_3)/hydrogen (H_2). The thickness of the light-emitting layer 104 thus stacked was about 10 nm.

[0041] On the surface of the light-emitting layer 104, an undoped n-type boron phosphide layer 105 composed of a polycrystal layer was stacked as an upper clad layer at 1,050°C using vapor phase growth means used in the aforementioned MOCVD method. The growth rate was set to 30 nm/min. Similarly to the p-type boron phosphide layer 103, the n-type boron phosphide layer 105 was constructed by an aggregate of regular tetrahedral single crystal entities 105a comprising the {111} crystal plane of BP. The carrier concentration of the n-type boron phosphide layer 105 was 8×10^{18} cm^{-3} and the thickness thereof was about 300 nm. The bandgap of the n-type boron phosphide layer 105 at room temperature was about 3.0 eV.

[0042] From the electron beam diffraction pattern, it was observed that the {111} crystal planes of the single crystal entities 105a constituting the n-type boron phosphide layer 105 were arrayed in parallel with the <111> crystal direction of the {111}-Si single crystal substrate 101. Inside the single crystal entity 105a, the presence of twinning having a {111} crystal plane of the BP crystal as the twinning plane was confirmed. The twinning plane was present in the direction of 60° with respect to the <110> crystal direction of the BP crystal.

[0043] A light-emitting part 106 of a pn-junction double hetero (DH) structure was constructed from the p-type boron phosphide layer 103 and the n-type boron phosphide layer 105, each having a bandgap of about 3.0 eV at room temperature, and the light-emitting layer 104 composed of a material having the same lattice plane spacing as the layers 103 and 105.

[0044] In the center part on the surface of the n-type boron phosphide layer 105, a circular n-type ohmic electrode 107 serving also as a pad electrode was disposed. The n-type ohmic electrode 107 was composed of a multilayer structure obtained by vacuum depositing films of Au-Ge alloy/Ni/Au. The diameter of the n-type ohmic electrode 107 was about 120 μm. Furthermore, a p-type ohmic electrode 108 was disposed on the almost entire back face of the p-type Si single crystal substrate 101, thereby completing the LED 1B. The p-type ohmic electrode 108 was composed of a vacuum deposited aluminum (Al) film. The Si single crystal substrate 101 was cut in the directions parallel and perpendicular to the [211] direction to form a square LED 1B having a one-side length of about 300 μm.

[0045] After connecting a gold (Au) wire to the n-type ohmic electrode 107, an operating current of 20 mA was passed in the forward direction between the n-type ohmic electrode 107 and the p-type ohmic electrode 108, and the emission properties were examined. The emission center wavelength was about 420 nm, and the full width at half mximum (FWHM) of the emission spectrum was about 32 nm. In the present invention, the light-emitting layer 104 was formed by using the p-type boron phosphide layer 103 reduced in the density of misfit dislocation as the underlying layer, so that a non-emitting dark line (see, "Optical Communication Device Engineering, Light-Emitting/Photo-Diode Device" by Hiroo YONETSU, 5th ed., pages 155-156, Kogaku Tosho (May 20, 1995)) was not discernibly confirmed in the light-emitting region, and light emission almost uniform in the intensity was given from the entire surface in the light-emitting region. The brightness in the chip state as measured using a general integrating sphere was about 8 mcd. Thus, an LED having high emission intensity was provided. With respect to the current-voltage (I-V) characteristics of the LED 1B, no occurrence of local breakdown due to the effect of dislocation was observed, and it was revealed that from the structure of the present invention, a pn-junction light-emitting part 106 exhibiting good pn-junction-property (rectification property) was obtained. The forward voltage (so-called Vf) determined from the I-V characteristics was 3.6 V (forward current = 20 mA) and the reverse voltage was 6 V (reverse current = 10 μA). Thus, an LED having high breakdown voltage was provided.

Industrial Applicability:

[0046] In the present invention, a boron phosphide based polycrystalline semiconductor layer provided on a Si single crystal substrate having a surface of {111}-crystal plane is an aggregate of a plurality of connected triangular pyramidal single crystal entities containing twinning capable of absorbing misfit dislocations and preventing the propagation of dislocations, so that a boron phosphide based polycrystalline layer having excellent crystallinity and reduced in the dislocation density can be constructed. By using this, it is possible to provide a boron phosphide based semiconductor device having excellent characteristics, such as a boron phosphide based semiconductor light-emitting device having high emission intensity, excellent rectification property and high breakdown voltage.

[0047] Furthermore, in the present invention a light-emitting diode is constituted using, as upper and lower clad layers sandwiching a light-emitting layer, a polycrystalline layer that is an aggregate of a plurality of connected triangular pyramidal single crystal entities including twining, and the lower clad layer is adjusted to have a thickness that can bring about emitted-light reflection of not less than 30%. Therefore, it is possible to suppress absorption of emitted light by a Si single crystal substrate and enhance an efficiency of taking out the emitted light toward the outside.

[0048] Moreover, by making the upper and lower clad layers of the same material and forming them to have substantially the same thickness, it is possible to make equal the quantities of strains imposed on the light-emitting layer from the upper and lower directions of the light-emitting layer. This can prevent the wavelength of the emitted light from unstably becoming a short wavelength by virtue of the strains imposed. Thus, it is possible to provide a light-emitting diode that can stably emit light having a wavelength corresponding to the bandgap of the light-emitting layer.

Claims

1. A boron phosphide based semiconductor device comprising a silicon single crystal substrate (101) and a boron phosphide based polycrystalline layer (103) formed on a {111} surface of said substrate, wherein said boron phosphide based polycrystalline layer (103) is composed of an aggregate of a plurality of triangular pyramidal single crystal entities (13) connected with each other through side faces (16), each of said single crystal entities (13) having a {111} bottom face (13a) being parallel with said {111} surface of said substrate and each of said single crystal entities (13) having {111} side faces (16), **characterised in that** inside each of said single crystal entities (13) a plurality of twinning interfaces (14) are regulary incorporated, whereby said twinning interfaces (14) are parallel with any one of said {111} side faces (16), whereby said twinning interfaces (14) in different ones of said single crystal entities (13) have different <111> directions, and whereby the intersections of said twinning interfaces (14) with said {111} surface of said substrate forms an angle of 60 degrees relative to a <110> direction in said {111} surface of said substrate.

2. The boron phosphide based semiconductor device according to claim 1, further comprising a group III-V compound semiconductor layer (104) stacked on said boron phosphide based polycrystalline layer (103) and forming a heterojunction therewith , whereby the lattice spacing constituting said group III-V compound semiconductor layer (104) agrees with the lattice spacing of crystal planes intersecting with surfaces of said single crystal entities constituting the boron phosphide based polycrystalline layer (103).

3. The boron phosphide based semiconductor device according claim 2, further comprising a second boron phosphide based polycrystalline layer (105) as defined in claim 1 stacked onto said group III-V compound semiconductor layer (104) and forming a heterojunction therewith, whereby said said group III-V compound semiconductor layer (104) is a light emitting layer and said first and second boron phosphide based polycrystalline layers (103, 105) are lower and upper cladding layers forming a double heterojunction light emitting diode.

4. The boron phosphide based semiconductor device according to any one of claims 1 to 3, wherein each single crystal entity (13) of said boron phosphide based polycrystalline layer (103) consists of a boron monophosphide crystal.

5. A light-emitting diode comprising a phosphide based semiconductor device according to claim 3 or 4, wherein the lower clad layer (103) has a thickness of d nm and the light emitted from the light-emitting layer (104) has a wavelength of $\lambda = 0.135d + 380$ nm, provided that $420\ \text{nm} \leq \lambda \leq 490\ \text{nm}$.

Patentansprüche

1. Halbleitervorrichtung auf Borphosphidbasis, umfassend ein Siliciumeinkristallsubstrat (101) und eine auf einer

{111}-Oberfläche des Substrats gebildete polykristalline Schicht auf Borphosphidbasis (103), wobei die polykristalline Schicht auf Borphosphidbasis (103) aus einer Aggregation einer Vielzahl dreieckspyramidenförmiger Einkristalleinheiten (13) gebildet ist, die miteinander durch Seitenflächen (16) verbunden sind, wobei jede der Einkristalleinheiten (13) eine {111}-Unterseitenfläche (13a) parallel zu der {111}-Oberfläche des Substrats aufweist, und jede der Einkristalleinheiten (13) {111}-Seitenflächen (16) aufweist, **dadurch gekennzeichnet, dass** innerhalb jeder der Einkristalleinheiten (13) eine Vielzahl von Zwillingsgrenzflächen (14) regelmäßig vorliegt, wobei die Zwillingsgrenzflächen (14) parallel zu einer der {111}-Seitenflächen (16) sind, wobei die Zwillingsgrenzflächen (14) in verschiedenen Einkristalleinheiten (13) unterschiedliche <111>-Richtungen aufweisen, und wobei die Schnitte der Zwillingsgrenzflächen (14) mit der {111}-Oberfläche des Substrats einen Winkel von 60 Grad in Bezug auf eine <110>-Richtung in der {111}-Oberfläche des Substrats bilden.

2. Halbleitervorrichtung auf Borphosphidbasis nach Anspruch 1, weiterhin umfassend eine Gruppe III-V-Verbindungshalbleiterschicht (104), welche auf die polykristalline Schicht auf Borphosphidbasis (103) geschichtet ist und mit dieser einen Heteroübergang bildet, wobei der die Gruppe III-V-Verbindungshalbleiterschicht (104) bildende Gitterabstand mit dem Gitterabstand von Kristallebenen übereinstimmt, welche die Oberflächen der die polykristalline Schicht auf Borphosphidbasis (103) bildenden Einkristalleinheiten schneiden.

3. Halbleitervorrichtung auf Borphosphidbasis nach Anspruch 2, weiterhin umfassend eine zweite polykristalline Schicht auf Borphosphidbasis (105) wie in Anspruch 1 definiert, welche auf die Gruppe III-V-Verbindungshalbleiterschicht (104) geschichtet ist und mit dieser einen Heteroübergang bildet, wobei die Gruppe III-V-Verbindungshalbleiterschicht (104) eine Lichtemissionsschicht ist, und die erste und zweite polykristalline Schicht auf Borphosphidbasis (103, 105) untere und obere Mantelschichten sind, wobei eine Doppel-Heteroübergangs-Leuchtdiode gebildet wird.

4. Halbleitervorrichtung auf Borphosphidbasis nach einem der Ansprüche 1 bis 3, wobei jede Einkristalleinheit (13) der polykristallinen Schicht auf Borphosphidbasis (103) aus einem Bormonophosphidkristall besteht.

5. Leuchtdiode, welche eine Halbleitervorrichtung auf Phosphidbasis nach Anspruch 3 oder 4 aufweist, wobei die untere Mantelschicht (103) eine Dicke von d nm aufweist, und das von der Lichtemissionsschicht (104) emittierte Licht eine Wellenlänge von $\lambda = 0{,}135\ d + 350$ nm aufweist, mit der Maßgabe, dass $420\ \text{nm} \leq \lambda \leq 490\ \text{nm}$ ist.

Revendications

1. Dispositif à semi-conducteurs à base de phosphure de bore comprenant un substrat de monocristal de silicium (101) et une couche polycristalline à base de phosphure de bore (103) formée sur une surface {111} dudit substrat, ladite couche polycristalline à base de phosphure de bore (103) étant composée d'un agrégat d'une pluralité d'entités monocristallines en forme de pyramides triangulaires (13) connectées entre elles par des faces latérales (16), chacune desdites entités monocristallines (13) ayant une face inférieure {111} (13a) qui est parallèle à ladite surface {111} dudit substrat et chacune desdites entités monocristallines (13) ayant des faces latérales {111} (16), **caractérisé en ce qu'**une pluralité d'interfaces de maclage (14) est incorporée selon un agencement régulier à l'intérieur de chacune desdites entités monocristallines (13), lesdites interfaces de maclage (14) étant parallèles à l'une quelconque desdites faces latérales {111} (16), de sorte que lesdites interfaces de maclage (14) se trouvant dans différentes desdites entités monocristallines (13) aient des directions <111> différentes, et les intersections desdites interfaces de maclage (14) avec ladite surface {111} dudit substrat forment un angle de 60° par rapport à une direction <110> dans ladite surface {111} dudit substrat.

2. Dispositif à semi-conducteurs à base de phosphure de bore selon la revendication 1, comprenant en outre une couche semi-conductrice d'un composé du groupe III-V (104) empilée sur ladite couche polycristalline à base de phosphure de bore (103) et formant une hétérojonction avec celle-ci, de sorte que la constante réticulaire constituant ladite couche semi-conductrice d'un composé du groupe III-V (104) s'accorde avec la constante réticulaire des plans cristallins coupant les surfaces desdites entités monocristallines constituant la couche polycristalline à base de phosphure de bore (103).

3. Dispositif à semi-conducteurs à base de phosphure de bore selon la revendication 2, comprenant en outre une deuxième couche polycristalline à base de phosphure de bore (105) telle que définie dans la revendication 1, empilée sur ladite couche semi-conductrice d'un composé du groupe III-V (104) et formant une hétérojonction avec celle-ci, de sorte que ladite couche semi-conductrice d'un composé du groupe III-V (104) soit une couche émettrice de

lumière et que lesdites première et deuxième couches polycristallines à base de phosphure de bore (103, 105) soient des couches de gainage inférieure et supérieure formant une diode électroluminescente à double hétérojonction.

4. Dispositif à semi-conducteurs à base de phosphure de bore selon l'une quelconque des revendications 1 à 3, dans lequel chaque entité monocristalline (13) de ladite couche polycristalline à base de phosphure de bore (103) est constituée d'un cristal à base de monophosphure de bore.

5. Diode électroluminescente comprenant un dispositif à semi-conducteurs à base de phosphure selon la revendication 3 ou 4, dans laquelle la couche de gainage inférieure (103) a une épaisseur de d nm et la lumière émise par la couche émettrice de lumière (104) a une longueur d'onde de $\lambda = 0{,}135d + 380$ nm, avec $420 \text{ nm} \leq \lambda \leq 490$ nm.

FIG. 1

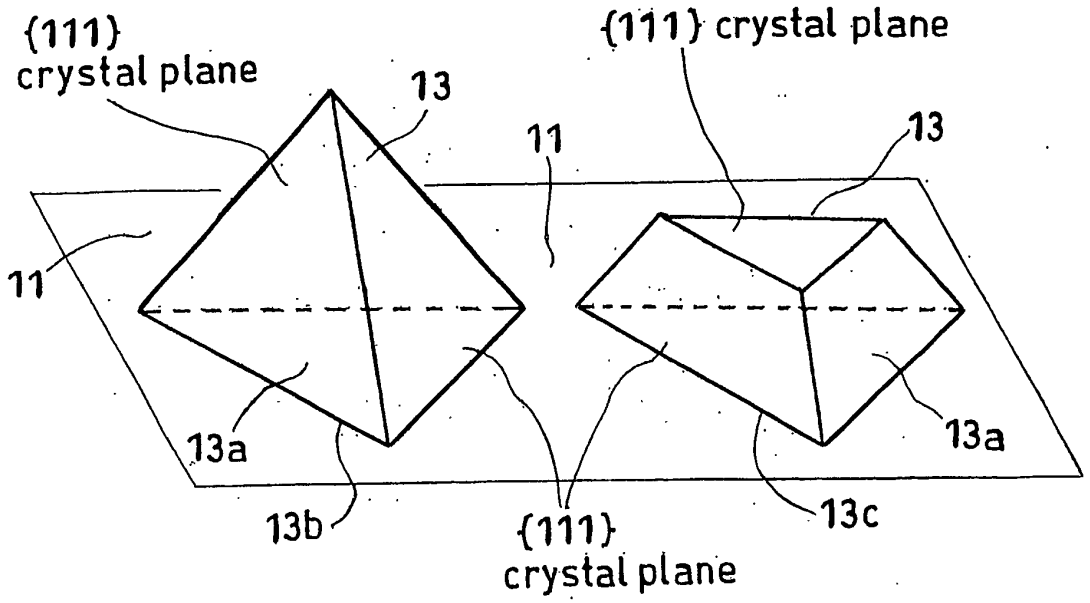

{111}
crystal plane
13
11
{111} crystal plane
13
11
13a
13b
{111}
crystal plane
13c
13a

FIG. 2

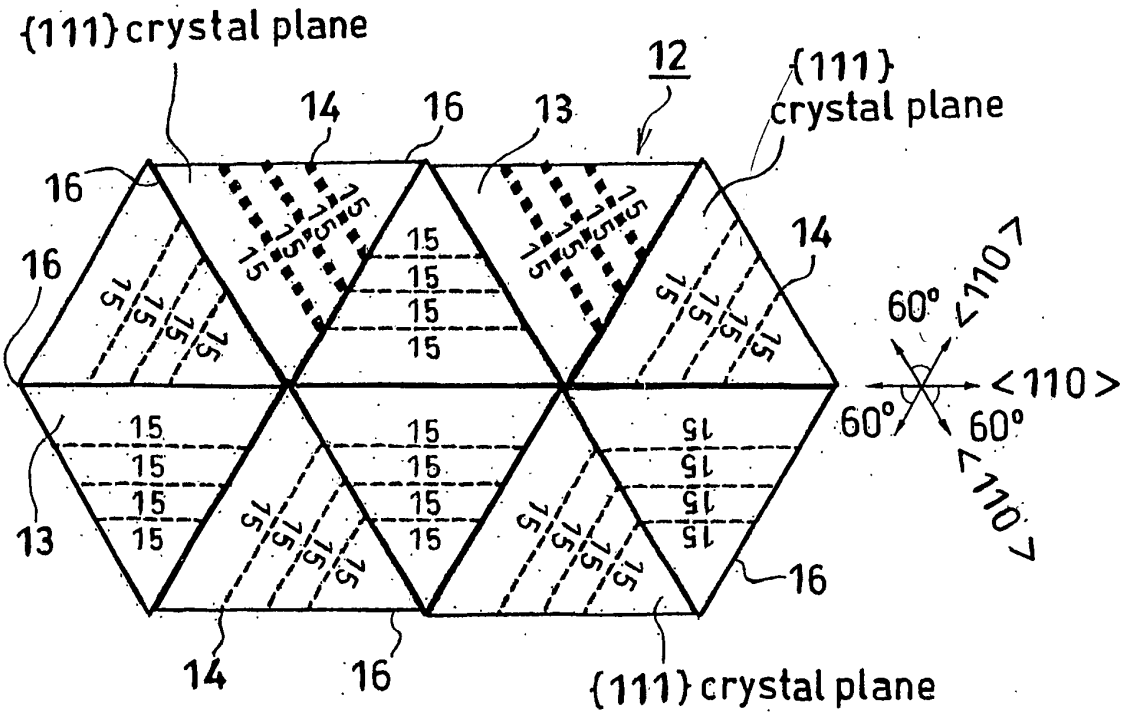

{111} crystal plane
12
{111}
crystal plane
14
16
13
16
16
14
15
13
60°
<110>
60°
60°
<110>
<110>
16
14
16
{111} crystal plane

FIG. 3

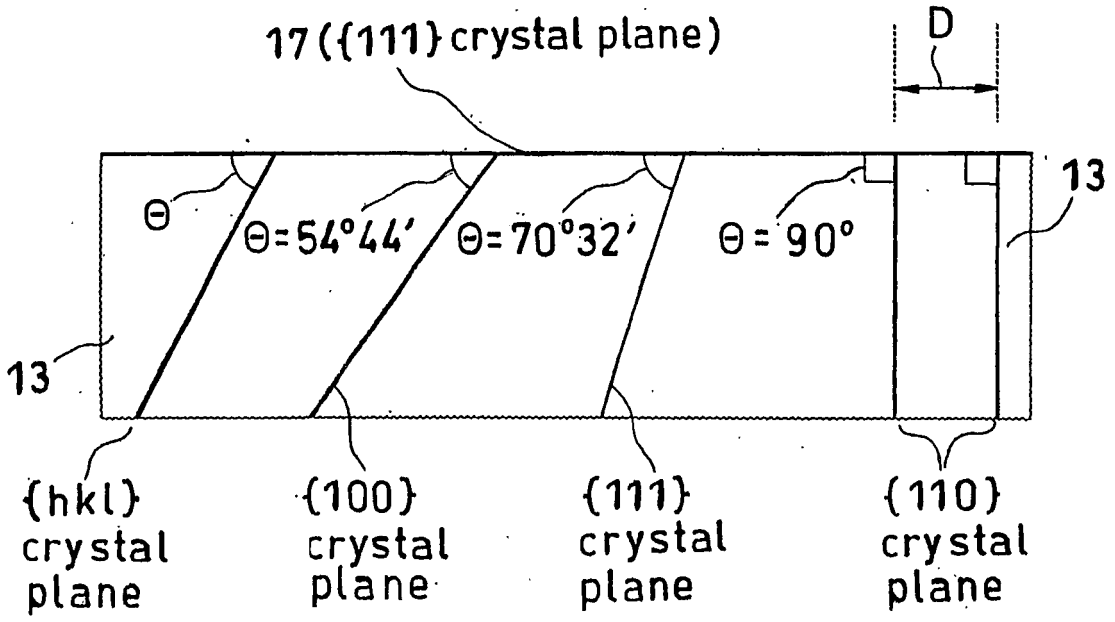

17 ({111} crystal plane)
D
13
Θ
Θ=54°44'
Θ=70°32'
Θ=90°
13
{hkl} crystal plane
{100} crystal plane
{111} crystal plane
{110} crystal plane

FIG. 4

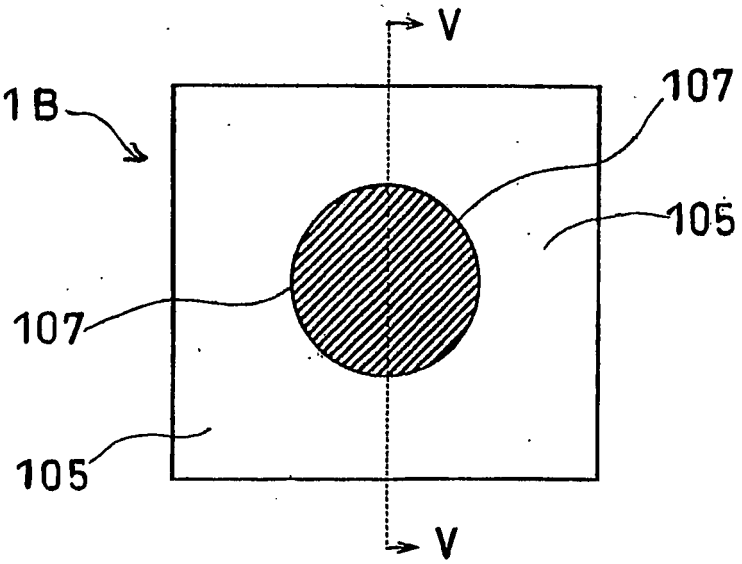

V
1B
107
105
107
105
V

FIG. 5

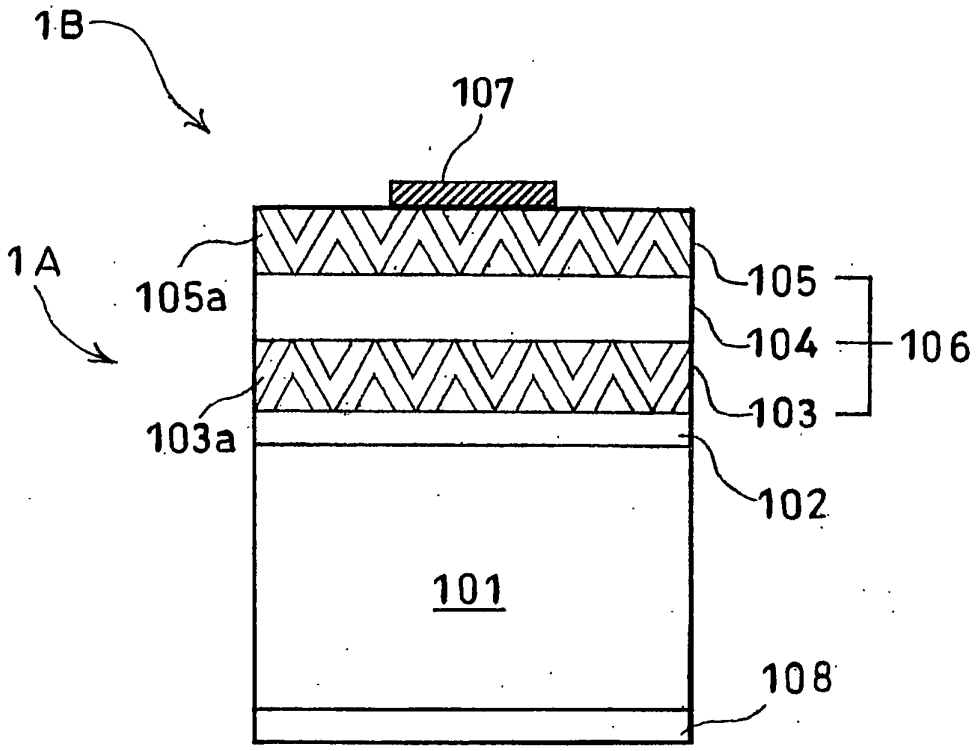

1B
107
1A
105a
105
104
106
103
103a
102
101
108

FIG. 6

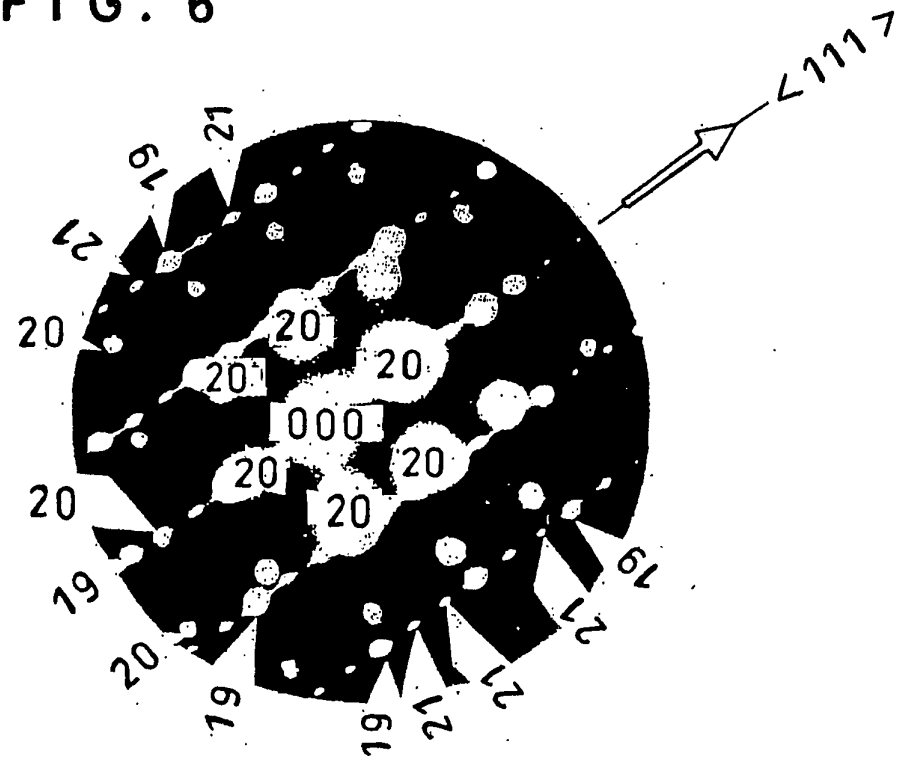
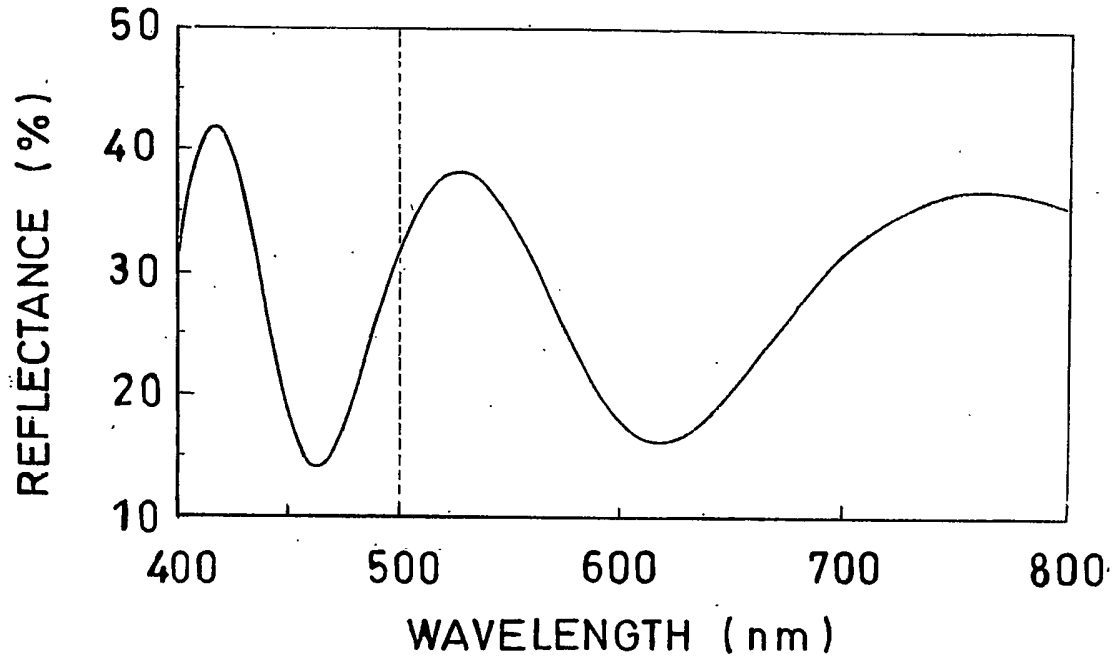

111
21
19
27
20
20
20
20
000
20
20
20
20
19
20
19
21
19
21
21
19

FIG. 7



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