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(54) Combined linear-logarithmic image sensor

(57) An image sensor has an array of pixels each of which comprises a photodiode (P) in circuit with a semiconductor device (M2) to define a node (pix). The pixel can be operated in linear mode with reset voltage (Vrt) applied via device M4. The pixel can also be operated in logarithmic mode by asserting 'logsel' to enable device M2 to conduct the photocurrent. In logarithmic mode, means are provided for calibrating the pixels to remove fixed pattern noise. The pixels may be operated in linear and log modes sequentially, with the linear output being selected for low light signals and the log output being selected for high light signals.

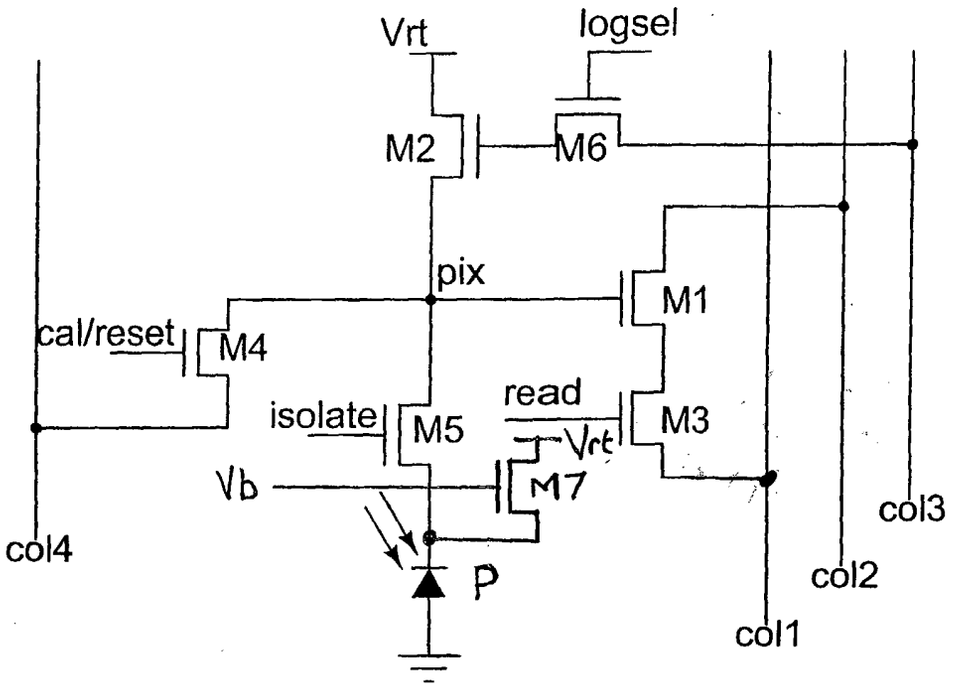

Fig. 2

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Description

[0001] This invention relates to solid state image sensors.

[0002] Dynamic range is a very important parameter of any imaging system. Human vision has the capability to see detail across a wide illumination range in a single scene, and is reported to exhibit around 200dB of dynamic range. Scenes in excess of 100dB are not uncommon in everyday situations. Thus designers of image sensors are continually looking for ways to increase dynamic range.

[0003] In the field of CMOS image sensors, it is known to use sensors having a log characteristic, and these have been shown to image scenes having high dynamic range. In logarithmic mode the pixel voltage is continuously available to the outside world and no integration time is used. The photocurrent which is induced flows through one or more MOS transistors and sets up a gate-source voltage which is proportional to the logarithm of the photocurrent.

[0004] This is exemplified in Figure 1 where the gate-source voltage appears across M2. As the photocurrent is very small, the MOS device(s) will operate in subthreshold, and thus the voltage varies logarithmically with the photocurrent. The voltage is read out by source follower circuitry. Around six decades of light can be captured in logarithmic mode.

[0005] Due to the small devices used in the pixels, a high degree of mismatch results from process variations and produces fixed pattern noise (FPN) across the array. Logarithmic sensors cannot use double sampling (in its conventional form) as a means of mismatch removal as this technique only removes the variation of device M1 and does not alter the effect of M2.

[0006] Another disadvantage of the logarithmic arrangement is a slow response time for low light levels. Increased photocurrent for a given light level can be accomplished by increasing the size of the light sensing element but this is not desirable as the cost for a given resolution will increase accordingly.

[0007] The prior art discloses designs intended to combine features of linear and logarithmic responses, for example US Patent 6,323,479 (Hynecek et al), and Tu et al "CMOS Active Pixel Sensor with Combined Linear and Logarithmic Mode Operation", IEEE Canada conference on Electrical and Computer Engineering 1998, vol. 2, pp 754-757, 1998. However, these prior art proposals do not address the above problems of FPN and slow response.

[0008] An object of the present invention is to provide an image sensor which overcomes or mitigates the problems discussed above.

[0009] The invention, which is defined in claims 1 and 8, is based upon combining conventional integrating mode with logarithmic mode.

[0010] An embodiment of the invention will now be described, by way of example only, with reference to the drawings, in which:

Figure 1 illustrates a prior art arrangement;
Figure 2 is a schematic of one pixel in an image sensor forming an embodiment of the invention;
Figure 3 illustrates the operation of the pixel of Figure 2 in logarithmic mode;
Figure 4 is a schematic of one form of circuitry used in a readout chain; and
Figure 5 illustrates voltage values used in Figure 4.

[0011] The basis of the invention is to combine conventional integrating mode with logarithmic mode. A single frame of image data will have the information for some pixels gathered from the integrating mode and other pixels from logarithmic mode. Those pixels that have saturated during exposure will have a log value (scaled appropriately) put in their place. This keeps the superior performance of the integrating mode in low light conditions but adds the high dynamic range of the logarithmic mode.

[0012] The combined lin-log system can be used without the need for a framestore. After a period of integration the linear result is read before switching the pixel to logarithmic mode and reading the log result. The log result is read in a near instantaneous manner; that is, as soon as the log signal has settled and while no other pixel is addressed. The linear and log results are then combined during the readout phase.

[0013] Logarithmic mode can suffer from image lag due to its slow response time, but by using the linear mode for low light levels the present invention in logarithmic mode only has to process higher photocurrents. Optionally, the addition of an amplifier connected around the pixel will further aid the response time in the logarithmic mode.

[0014] Referring to Figure 2, there is shown a single pixel of an image sensor forming one example of the invention. The pixel comprises a photodiode P connected between earth (ground) and a node 'pix' when device M5 is on.

[0015] For linear operation the reset voltage Vrt (set in col4) can be sampled onto the node 'pix' by pulsing 'cal/reset' high and 'logsel' can be raised to precharge the gate of transistor M2 via col3 low such that it is off and does not affect the integration period. If 'isolate' is on then the photocurrent generated will lower the voltage on 'pix'. After a set integration time 'read' can be turned on such that M1 now acts as a source follower, with column 2 held at a voltage approximately equal to the reset voltage Vrt and column 1 comprising a current source (not shown).

[0016] Optionally, the pixel can include an anti-bloom arrangement to prevent blooming, Blooming is caused by the node 'pix' being driven to near zero volts, allowing leakage of current to adjacent pixels. The anti-bloom arrangement of Figure 2 comprises a transistor M7 which operates to clamp the photodiode voltage if it falls to

some arbitrary low value set by (Vb - Vth_7) where Vth_7 is the threshold voltage of device M7.

[0017] The pixel is operated in logarithmic mode by connecting an amplifier A from the column as shown in Figure 3. The transistor M1 of Figure 2 forms the inverting input of the amplifier A. The noninverting input is held at a reference voltage Vref, and thus the node 'pix' will sit at a level given by:

$$Vpix = Vref + Voff \quad ...(1)$$

where Voff is the offset of the amplifier A. The output voltage is thus given by:

$$Vout = Vpix + Vgs(M2) \quad ...(2)$$

where Vgs(M2) is the gate-source voltage of device M2 which is determined by the photocurrent and has a logarithmic dependence.

[0018] The offset of the amplifier can be removed by performing calibration, that is by bringing the pixels into a reference state so that the FPN can be learnt and cancelled. To do this, the photodiode P is isolated from the load device M2 by turning off device M5; this stops the photocurrent corrupting the calibration. One method of generating a calibration current for device M2 is to use M4 as a switch to an in-column current source C; this allows a matched current to be pulled through the load device of each pixel, placing each pixel into a reference state which should be equivalent to illuminating the sensor with a uniform intensity.

[0019] Other methods of calibration could be used, for example those shown in Kavadias et al, IEEE Journal of solid-state circuits, vol 35, No 8, August 2000 and in Loose et al, *ibid.*, vol 36, No 4, April 2001.

[0020] Referring to Figure 4, one suitable readout scheme for selecting between linear and logarithmic outputs is shown. The linear and log signals for each given pixel are read out sequentially. The linear signal and the corresponding dark reference signal are applied to a difference circuit 40 and the difference is converted to digital format by analog-to-digital converter 42. The log signal and the log calibration signal are applied to a difference circuit 44 and the difference is converted to digital format by analog-to-digital converter 46. The two digital signals are applied to a logic circuit 48 which passes the linear or the log signal in dependence on whether or not the linear signal is saturated.

[0021] However, where a log output is used the actual output must include an offset in order to place it correctly into the linear range. Referring to Figure 5, the log offset is computed to be a value A by comparing a non-saturated linear value with a log value with a log value and taking the difference. All linear values greater than A are then taken to be saturated or near saturation, and are replaced by log values to which the offset A is added.

[0022] The calculation of A can be done once, and need only be changed if the exposure time is altered.

[0023] Thus, the present invention combines features of linear and logarithmic sensors in a manner which avoids or minimises the drawbacks of both types.

Claims

1. An image sensor having an image surface providing an array of pixels, each pixel comprising a photodiode, first output circuit means for deriving a linear output signal by applying a reset signal to the photodiode and reading out the voltage on the photodiode after a predetermined integration time, and second output circuit means for deriving a logarithmic output signal by reading out a near instantaneous illumination-dependent voltage which is a logarithmic function of illumination.

2. An image sensor according to claim 1, in which said first output circuit means comprises a reset switch for applying a reset voltage to the photodiode, a source follower connected to the photodiode, and a readout switch for turning on the source follower at the expiry of said integration time.

3. An image sensor according to any preceding claim, in which the second output circuit means comprises an amplifier and log select switch means for connecting the amplifier around the pixel.

4. An image sensor according to claim 2 and claim 3, in which the amplifier is a differential amplifier the inverting input of which is formed by said source follower and the noninverting input of which is connected to a reference voltage.

5. An image sensor according to any preceding claim, including means for calibrating the pixel before deriving the logarithmic output.

6. An image sensor according to claim 5, in which the calibrating means comprises a constant current source selectively connectable to the pixel.

7. An image sensor according to claim 6, in which the outputs are derived from a node associated with the photodiode, and in which the calibration means includes a switch for isolating the photodiode from the node while calibration takes place.

8. A method of operating an image sensor having an image surface providing an array of pixels, each pixel comprising a photodiode; the method comprising:

deriving a linear output from each pixel;
deriving a logarithmic output from each pixel;

and
selecting the linear output if the pixel has not saturated during generation of the linear output, and otherwise selecting the logarithmic output.

9. A method according to claim 8, in which the linear output from each pixel is derived by applying a reset voltage, allowing a predetermined integration time, and thereafter reading out the voltage on the photodiode.

10. A method according to claim 8 or 9, in which the logarithmic output is derived by connecting an amplifier around the photodiode.

11. A method according to any of claims 8 to 10, in which the pixel is calibrated before the logarithmic output is derived.

12. A method according to claim 11, in which the pixel is calibrated by applying a constant current thereto.

13. A method according to claim 12, in which the photodiode has an associated node from which the logarithmic output is taken, and the photodiode is isolated from said node while the calibration takes place.

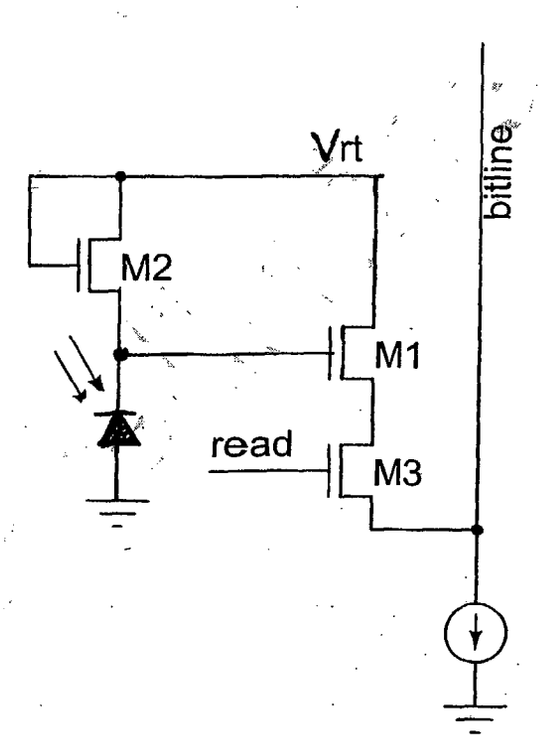

Fig.1

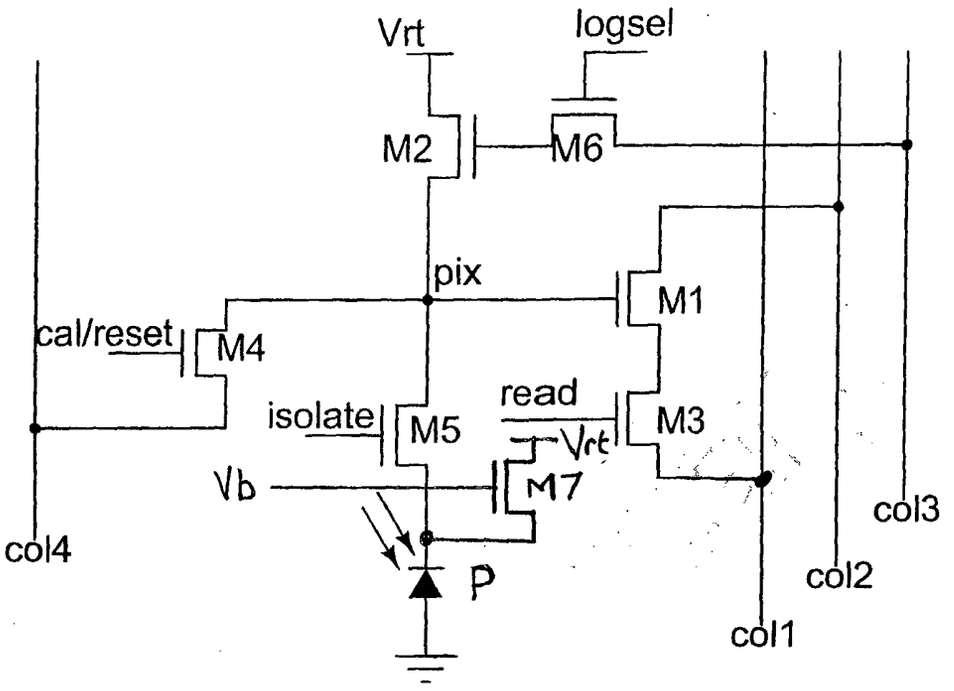
Vrt
logsel
M2
M6
pix
M1
cal/reset
M4
isolate
M5
read
M3
Vrt
Vb
M7
col4
P
col3
col2
col1

Fig. 2

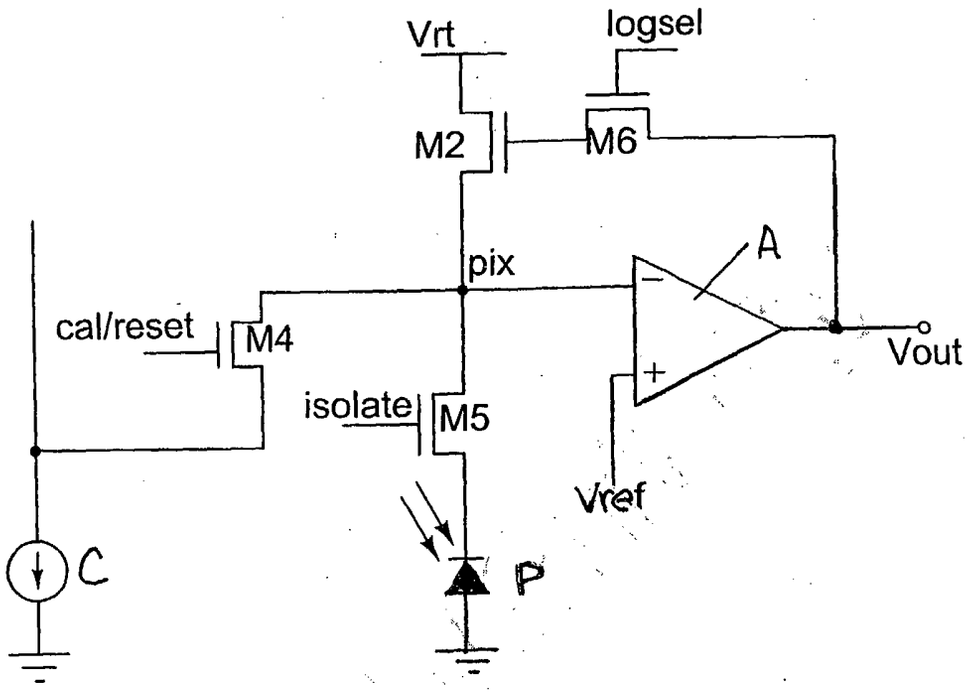
Vrt
logsel
M2
M6
pix
A
cal/reset
M4
Vout
isolate
M5
Vref
C
P

Fig. 3

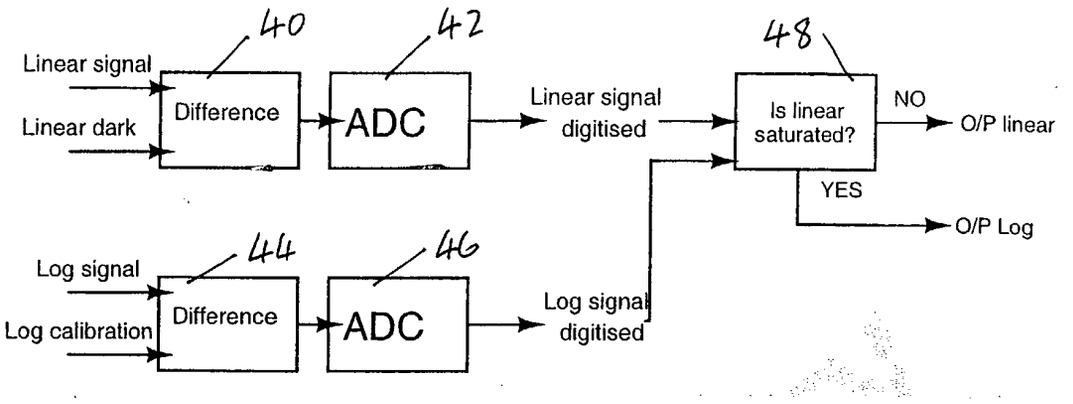
40
42
48
Linear signal
Linear dark
Difference
ADC
Linear signal digitised
Is linear saturated?
NO
O/P linear
YES
O/P Log
44
46
Log signal
Log calibration
Difference
ADC
Log signal digitised

Fig. 4

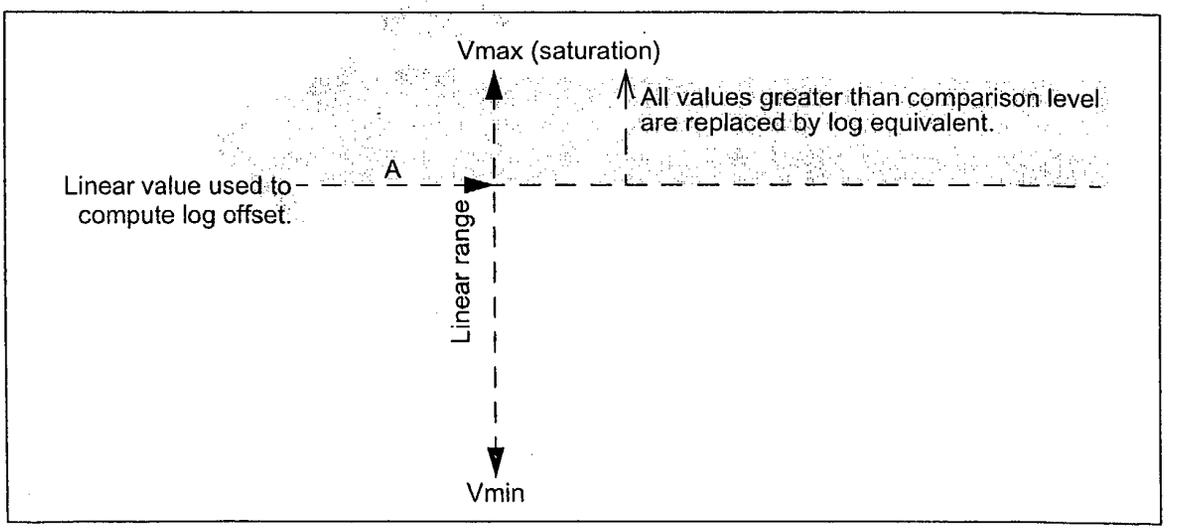
Vmax (saturation)
All values greater than comparison level are replaced by log equivalent.
A
Linear value used to compute log offset.
Linear range
Vmin

Fig. 5

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EUROPEAN SEARCH REPORT

Application Number
EP 03 25 2835

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
D,A	US 6 323 479 B1 (HYNECEK ET AL) 27 November 2001 (2001-11-27) * column 2, line 52 - column 3, line 55; figures 1,2 * ---	1-4,8-10	H04N5/335
A	US 6 133 563 A (CLARK ET AL) 17 October 2000 (2000-10-17) * column 3, line 4 - column 4, line 67; figure 3 * ---	1,8	
D,A	SPYROS KAVADIAS: "A Logarithmic Response CMOS Image Sensor with On-Chip Calibration" IEEE JOURNAL OF SOLID-STATE CIRCUITS, vol. 35, no. 8, August 2000 (2000-08), pages 1146-1152, XP001075115 * page 1146, left-hand column, line 18 - page 1147, right-hand column, line 30; figure 1 * -----	5-7, 11-13	
			TECHNICAL FIELDS SEARCHED (Int.Cl.7) H04N

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
BERLIN	1 October 2003	Dudley, C

CATEGORY OF CITED DOCUMENTS

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01-10-2003

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 6323479 B1	27-11-2001	NONE	
US 6133563 A	17-10-2000	NONE	

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For more details about this annex : see Official Journal of the European Patent Office, No. 12/82