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(54) Method for adaptive recovery

Verfahren zur adaptiven Datenrückgewinnung

Méthode adaptative pour la récupération de bits

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Description

[0001] The present invention relates to a method and a device for bit recovery in a deteriorated data channel, and to an apparatus for reading from and/or writing to recording media using such method or device.

[0002] In many of today's applications large amounts of data need to be stored. In the area of Personal Computers and in addition in the area of consumer electronics harddisks as fixed storage media and optical disks as removable storage media are commonly used for this purpose. Due to emerging incremental data bandwidth needs (HDTV, fast copy) the data throughput of the applications is increasing continuously. Consequently, the corresponding disk devices have to provide the appropriate data and data bandwidth, too. Therefore, a plurality of high density optical recording media have been developed, e.g. the Digital Versatile Disk (DVD) or the Blu-Ray Disk (BD) using blue laser light for reading and recording.

[0003] The readout signal from such high density optical disks is deteriorated mainly by two factors. The first factor is the small ratio between the amplitudes of the shortest run-length symbols and the longest run-length symbols (e.g. the I2/I8 ratio in the case of Blu-Ray disks), which is caused by the high information density, i.e. the ratio between the diameter of the laser spot and the physical length of a channel bit. This ratio is time-variant due to effects like disk tilt or de-focusing. The second factor is the waveform asymmetry, which is caused by an unequal length of the pits and lands due to recording and/or mastering imperfections. This asymmetry is also known as domain bloom.

[0004] In "Combined Adaptive Controlled Partial Response and Maximum Likelihood Signal Processing for High-Density Optical Disks", Jpn. J. Appl. Phys. Vol. 42 (2003), pp. 924-930, Takehara et al. propose to use both an adaptive equalizer and a Viterbi detector with adaptive reference levels in order to allow a highly reliable recovery of the stored user data. However, both adaptation schemes rely on the recovered bit stream and are in fact gain control loops. Therefore, the adaptation is difficult to control and tends to instability. Furthermore, this detector arrangement has problems at start-up, i.e. it needs a proper pre-setting of all coefficients and a complicated range checking during the adaptation process. Finally, an additional automatic gain control loop, which is also necessarily present, forms a third loop which modifies the gain.

[0005] It is an object of the invention to propose an improved method for adaptive bit recovery.

[0006] According to the invention, a method for bit recovery in a data channel comprises the steps of:

- inputting a read channel signal coming from a recording medium;
- providing a main signal processor for adaptive bit recovery from the read channel signal;
- providing an auxiliary signal processor for bit recovery from the read channel signal;
- using an output of the auxiliary signal processor for adaptation of the main signal processor; and
- selectively outputting a recovered binary bit stream.

The bit stream for the adaptation circuits is generated by an additional, more simple but very robust signal processor. In this way the interacting control loops are decoupled. Start-up problems are avoided since the auxiliary signal processor delivers an acceptable bit error rate for the adaptation of the main signal processor without any adjustment. This adaptation is basically a low-pass filtering process and is hence not strongly affected by occasional bit errors.

[0007] Favourably, an adaptive equalizer and an adaptive detector are used for the main signal processor. This allows a highly reliable recovery of the stored user data even if the read channel signal is disturbed by the high information density, by effects like disk tilt or de-focusing, or by signal asymmetry.

[0008] Advantageously, the adaptive equalizer has different middle coefficients for mark, zero and space. This allows to compensate a possible asymmetry in the read channel signal very well. In known systems different coefficients are only used for mark and space. Using different middle coefficients for mark, zero and space is not limited to the present invention, it can also be employed for improving the method known from prior art as described above or other methods.

[0009] According to a further aspect of the invention, the data stream from the main signal processor is used for fine-adaptation of the main signal processor. Though this fine adaptation is not necessary under standard conditions, it might be advantageous for further improving the signal quality or the operation speed.

[0010] According to a refinement of the invention, the data stream from the auxiliary signal processor is used as the recovered binary bit stream until the output from the main signal processor is reliable. In this case a multiplexer is used for choosing the appropriate signal depending on the adaptation. Using the data stream from the auxiliary signal processor as the recovered binary bit stream reduces the time needed until an output signal is obtained from the circuit arrangement after start-up.

[0011] Favourably, the data stream from the auxiliary signal processor is used as the recovered binary bit stream for high-speed operation. For high-speed read operation, the main signal processor might be too slow due to its complicated processing. In this case the data stream coming from the auxiliary signal processor is used. Since high-speed operation is only possible with a good signal quality, this signal processor is sufficient in this case. A multiplexer is used for choosing either the data stream from the auxiliary signal processor or the data stream from the main signal processor depending on the operation mode.

[0012] Advantageously a limit equalizer block and a bit-by-bit detector is used for the auxiliary signal proces-

sor. This type of signal processor is well known. Although the bit error rate delivered by this auxiliary signal processor is not as good as the bit error rate of the main signal processor after proper adaptation of the equalizer coefficients and the Viterbi detector reference levels, it is still sufficient for the adaptation of the main signal processor.

[0013] Favourably, a slicer is inserted between a pre-equalizer and a limit equalizer of the limit equalizer block of the auxiliary signal processor. Since a limit equalizer is very susceptible to signal asymmetry, the insertion of such an additional slicer results in a significant performance improvement in case of strong asymmetry.

[0014] According to the invention, a device for bit recovery in a data channel comprises:

- an input for inputting a read channel signal coming from a recording medium;
- a main signal processor for adaptive bit recovery from the read channel signal;
- an auxiliary signal processor for bit recovery from the read channel signal, whereby an output of the auxiliary signal processor is used for adaptation of the main signal processor; and
- an output for selectively outputting a recovered binary bit stream.

Such a device is well suited for performing a method according to the invention. Favourably, the main signal processor comprises an adaptive equalizer and an adaptive detector, which allows a highly reliable recovery of the stored user data. In order to compensate a possible asymmetry in the read channel signal, the adaptive equalizer advantageously has different middle coefficients for mark, zero and space.

[0015] Favourably, the auxiliary signal processor comprises a limit equalizer block and a bit-by-bit detector. Although this auxiliary signal processor has an increased bit error rate compared with the bit error rate of the main signal processor after proper adaptation, it is still sufficient for the adaptation of the main signal processor. By providing a slicer between a pre-equalizer and a limit equalizer of the limit equalizer block, a significant performance improvement in case of strong asymmetry is achieved.

[0016] According to a further aspect of the invention, an apparatus for reading from and/or writing to recording media uses a method according to the invention or comprises a device according to the invention for bit recovery in a data channel. Favourably, the apparatus is used for reading from and/or writing to optical recording media. However, the invention is not limited to these types of recording media.

[0017] For a better understanding of the invention, an exemplary embodiment is specified in the following description with reference to the figures. It is understood that the invention is not limited to this exemplary embodiment and that specified features can also expediently be combined and/or modified without departing from the scope of the present invention. In the figures:

Fig. 1 shows an arrangement of an adaptive detector; and

Fig. 2 shows a detector arrangement according to the invention.

[0018] In Fig. 1 an arrangement of an adaptive signal processor 3 is shown. An analog read channel signal A_RDCH, which is a summation of the four quadrants of a photo detector (not shown in the figure), is first processed by a variable gain amplifier and offset adder block 1. The variable gain amplifier is an amplifier with a controllable gain factor. The analog signal A_RDCH coming from the recording medium varies both in amplitude and in offset, e.g. due to fingerprints or scratches. The adaptive signal processor 3, however, delivers the best performance, i.e. the lowest bit error rate, when the input signal is constant both in amplitude and offset. Therefore, a gain and offset control block 7 varies the gain of the variable gain amplifier and adds an offset to the input signal A_RDCH. The gain- and offset-corrected signal is digitised by an analog-to-digital converter 2 to obtain a digitised read channel signal D_RDCH. This digitised read channel signal D_RDCH is input to the gain and offset control block 7 to form a closed loop. The analog-to-digital converter 2 is either clocked with a varying clock synchronous with the bit stream coming from the recording medium or asynchronously at a fixed clock rate. In the latter case the signal is re-sampled by a sample rate converter (not shown). For the sake of simplicity, the whole phase locked loop is omitted in the figure. In either case the digitised read channel signal D_RDCH after the analog-to-digital converter 2 is synchronous with the channel bit clock and more or less constant in amplitude and offset due to the gain and offset control loop.

[0019] The digitised read channel signal D_RDCH is modified by an adaptive equalizer 4 and converted to a binary data stream UD by an adaptive Viterbi detector 5 for further processing. The adaptive equalizer 4 changes the waveform of the incoming signal D_RDCH so that it resembles as much as possible a partial-response target waveform. The equalizer 4 is made adaptive since the frequency characteristic of the incoming signal D_RDCH differs for different recording media, for different recordings, or even during the playback of one recording medium due to changes in reflectivity. The coefficients for the equalizer 4 are calculated by a coefficient and reference level adaptation block 6, which favourably is a hardware implementation of the well known least-mean-square algorithm. In fact this is a feedback control system with the output signal E_RDCH of the equalizer 4, i.e. the equalized read channel signal, as the actual value. The necessary target value is derived from the recovered binary bit stream UD, i.e. the output from the adaptive Viterbi detector 5. This bit stream UD is converted to the partial response target waveform with a finite impulse

response filter, the so-called target filter. The equalized signal E_RDCH is delivered to the adaptive Viterbi detector 5, which in principal corresponds to a well-known Viterbi detector. The main problem of Viterbi detection for optical storage channels is an asymmetry of the eye-pattern. Therefore, the reference levels of the Viterbi detector 5 are not fixed, but are obtained from the coefficient and reference level adaptation block 6. This is described in more detail by Ide in "Adaptive Partial-Response Maximum-Likelihood Detection in Optical Recording Media", Jpn. J. Appl. Phys. Vol. 41 (2002), pp. 1789-1790. The coefficient and reference level adaptation block 6 adapts the reference levels based on the recovered binary bit stream NRZ1, i.e. the output of the adaptive Viterbi detector 5. Of course, the variable gain amplifier and offset adder block 1, the analog-to-digital converter 2, and the gain and offset control block 7 can also be included in the signal processor 3.

[0020] Fig. 2 shows a detector arrangement according to the invention. The arrangement corresponds largely to the arrangement shown in Fig. 1. However, in the signal processor 3 the coefficient and reference level adaptation block 6 is divided into a coefficient adaptation block 9 and a reference level adaptation block 8. The main difference is that an additional bit stream NRZ2 for the adaptation circuits is generated by an additional, more simple but very robust auxiliary signal processor 10. This auxiliary signal processor 10 comprises a limit equalizer block 11 and a succeeding bit-by-bit detector 12, which favourably is a threshold detector. Since a limit equalizer is very susceptible to signal asymmetry, an additional slicer (not shown) is inserted between a pre-equalizer and the actual limit equalizer in the limit equalizer block 11. This results in a significant performance improvement in case of strong asymmetry. Although the bit error rate delivered by the auxiliary signal processor 10 is not as good as the bit error rate from the main signal processor 3 after proper adjustment of the equalizer coefficients and the Viterbi detector reference levels, it is still sufficient for the adaptation of the main signal processor 3, since this adaptation is basically a low-pass filtering process and is hence not strongly affected by occasional bit errors. Of course, as in Fig. 1 it is also possible to use the output NRZ1 of the main signal processor 3 for fine adatation of the main signal processor 3 after a preliminary adaptation based on the output NRZ2 of the auxiliary signal processor 10.

[0021] For high-speed read operation, the main signal processor 3 might be too slow due to its complicated processing. In this case the data stream NRZ2 coming from the auxiliary signal processor 10 is advantageously used as the user data output signal UD. Since high-speed operation is only possible with a sufficient signal quality, this signal processor 10 is satisfactory in this case. A multiplexer 14 is used for choosing either the data stream NRZ2 from the auxiliary signal processor 10 or the data stream NRZ1 from the main signal processor 3 depending on the operation mode. Of course, this approach is also applicable if an increased bit error rate can be tolerated.

[0022] Favourably, the Viterbi detector 5 has a constraint length of 3 and a path memory length of 16. For recording media of the Blu-ray disk type the partial-response equalization adaptation is either done for PR(1,2,2,1) or for PR(2,3,3,2). PR(1,2,2,1) has the advantage that the target levels are evenly spaced. However, a stronger boost of the 2T symbols is needed in this case than for PR(2,3,3,2), i.e. 13dB instead of 10dB for a worst case 25GByte Blu-ray disk with an I2pp/I8pp ratio of 5%. PR(2,3,3,2) on the other hand needs a stronger boost at higher frequency and has the drawback that the target levels are not evenly spaced. For DVD, PR(1,1,1,1) is advantageously used.

[0023] The equalizer 4 consists of a symmetrical finite impulse response filter with seven or more taps and a least-mean-square coefficient adaptation. The centre tap favourably has separated coefficients for mark, zero and space, which compensates the asymmetry very well.

Claims

1. Method for bit recovery in a data channel including the steps of:

   - inputting a read channel signal (A_RDCH, DRDCH) coming from a recording medium;
   - providing a main signal processor (3) for adaptive bit recovery from the read channel signal (A_RDCH, D_RDCH);
   - providing an auxiliary signal processor (10);
   - using an output (NRZ2) of the auxiliary signal processor (10) for adaptation of the main signal processor (3); and
   - outputting a recovered binary bit stream (UD), **characterized in that** the auxiliary signal processor (10) is for bit recovery from the read channel signal (A_RDCH, D_RDCH) and includes a limit equalizer block (11) and a succeeding bit-by-bit detector (12) providing the output (NRZ2) of the auxiliary signal processor (10), wherein either the output (NRZ2) from the auxiliary signal processor (10) or an output from the main signal processor (NRZ1) is chosen as the recovered binary bit stream depending on an operation mode.

2. Method according to claim 1, further including the step of using an adaptive equalizer (4) and an adaptive detector (5) for the main signal processor (3).

3. Method according to claim 1 or 2, further including the step of using the data stream (NRZ1) from the main signal processor (3) for fine- adaptation of the main signal processor (3).

4. Method according to one of claims 1 to 3, further including the step of choosing the data stream (NRZ2) from the auxiliary signal processor (10) as the output recovered binary bit stream (UD) until the output (NRZ1) from the main signal processor (3) is reliable.

5. Method according to one of claims 1 to 4, further including the step of choosing the data stream (NRZ2) from the auxiliary signal processor (10) as the output recovered binary bit stream (UD) for high-speed operation.

6. Method according to claim 1, further including the step of using a slicer between a pre-equalizer and a limit equalizer of the limit equalizer block (11) of the auxiliary signal processor (10).

7. Device for bit recovery in a data channel including:

- an input for inputting a read channel signal (A_RDCH, D_RDCH) coming from a recording medium;
- a main signal processor (3) for adaptive bit recovery from the read channel signal (A_RDCH, D_RDCH);
- an auxiliary signal processor (10), whereby an output (NRZ2) of the auxiliary signal processor (10) is used for adaptation of the main signal processor (3); and
- an output for outputting a recovered binary bit stream (UD),

characterized in that the auxiliary signal processor (10) is for bit recovery from the read channel signal (A_RDCH, D_RDCH) and includes a limit equalizer block (11) and a succeding bit-by-bit detector (12) providing the output (NRZ2) of the auxiliary signal processor, wherein either the output (NRZ2) from the auxiliary signal processor (10) or an output from the main signal processor (NRZ1) is chosen as the recovered binary bit stream depending on an operation mode.

8. Device according to claim 7, **characterized in that** the main signal processor (3) includes an adaptive equalizer (4) and an adaptive detector (5).

9. Device according to claim 7, **characterized in that** a slicer is provided between a pre-equalizer and a limit equalizer of the limit equalizer block (11) of the auxiliary signal processor (10).

10. Apparatus for reading from and/or writing to recording media, **characterized in that** it uses a method according to anyone of claims 1 to 6 or includes a device according to anyone of claims 7 to 9 for bit recovery in a data channel.

Patentansprüche

1. Verfahren für die Bitrückgewinnung in einem Datenkanal, wobei das Verfahren die folgenden Schritte enthält:

- Eingeben eines von einem Aufzeichnungsmedium kommenden gelesenen Kanalsignals (A_RDCH, D_RDCH),
- Bereitstellen eines Hauptsignalprozessors (3) für die adaptive Bitrückgewinnung aus dem gelesenen Kanalsignal (A_RDCH, D_RDCH);
- Bereitstellen eines Hilfssignalprozessors (10);
- Verwenden einer Ausgabe (NRZ2) des Hilfssignalprozessors (10) für die Adaptation des Hauptsignalprozessors (3); und
- Ausgeben eines rückgewonnenen binären Bitstroms (UD),

dadurch gekennzeichnet, dass der Hilfssignalprozessor (10) für die Bitrückgewinnung aus dem gelesenen Kanalsignal (A_RDCH, D RDCH) dient und einen Grenzwertentzerrerblock (11) und einen nachfolgenden Bit-für-Bit-Detektor (12), der die Ausgabe (NRZ2) des Hilfssignalprozessors (10) bereitstellt, enthält, wobei in Abhängigkeit von einer Betriebsart entweder die Ausgabe (NRZ2) von dem Hilfssignalprozessor (10) oder eine Ausgabe von dem Hauptsignalprozessor (NRZ1) als der rückgewonnene binäre Bitstrom gewählt wird.

2. Verfahren nach Anspruch 1, das **ferner** den Schritt des Verwendens eines adaptiven Entzerrers (4) und eines adaptiven Detektors (5) für den Hauptsignalprozessor (3) enthält.

3. Verfahren nach Anspruch 1 oder 2, das **ferner** den Schritt des Verwendens des Datenstroms (NRZ1) von dem Hauptsignalprozessor (3) für die Feinadaptation des Hauptsignalprozessors (3) enthält.

4. Verfahren nach einem der Ansprüche 1 bis 3, das **ferner** den Schritt des Wählens des Datenstroms (NRZ2) von dem Hilfssignalprozessor (10) als den ausgegebenen rückgewonnenen binären Bitstrom (UD), bis die Ausgabe (NRZ1) von dem Hauptsignalprozessor (3) zuverlässig ist, enthält.

5. Verfahren nach einem der Ansprüche 1 bis 4, das **ferner** den Schritt des Wählens des Datenstroms (NRZ2) von dem Hilfssignalprozessor (10) als den ausgegebenen rückgewonnenen binären Bitstrom (UD) für den Hochgeschwindigkeitsbetrieb enthält.

6. Verfahren nach Anspruch 1, das **ferner** den Schritt des Verwendens eines Doppelbegrenzers zwischen einem Vorentzerrer und einem Grenzwertentzerrer des Grenzwertentzerrerblocks (11) des Hilfssignal-

prozessors (10) enthält.

7. Vorrichtung für die Bitrückgewinnung in einem Datenkanal, wobei die Vorrichtung enthält:

- einen Eingang zum Eingeben eines von einem Aufzeichnungsmedium kommenden gelesenen Kanalsignals (A_RDCH, D RDCH) ;
- einen Hauptsignalprozessor (3) für die adaptive Bitrückgewinnung aus dem gelesenen Kanalsignal (A_RDCH, D_RDCH);
- einen Hilfssignalprozessor (10), wobei ein Ausgang (NRZ2) des Hilfssignalprozessors (10) für die Adaptation des Hauptsignalprozessors (3) verwendet wird; und
- einen Ausgang zum Ausgeben eines rückgewonnenen binären Bitstroms (UD)

dadurch gekennzeichnet, dass der Hilfssignalprozessor (10) für die Bitrückgewinnung aus dem gelesenen Kanalsignal (A_RDCH, D_RDCH) dient und einen Grenzwertentzerrerblock (11) und einen nachfolgenden Bit-für-Bit-Detektor (12), der die Ausgabe (NRZ2) des Hilfssignalprozessors bereitstellt, enthält, wobei in Abhängigkeit von einer Betriebsart entweder die Ausgabe (NRZ2) von dem Hilfssignalprozessor (10) oder eine Ausgabe von dem Hauptsignalprozessor (NRZ1) als der rückgewonnene binäre Bitstrom gewählt wird.

8. Vorrichtung nach Anspruch 7, **dadurch gekennzeichnet, dass** der Hauptsignalprozessor (3) einen adaptiven Entzerrer (4) und einen adaptiven Detektor (5) enthält.

9. Vorrichtung nach Anspruch 7, **dadurch gekennzeichnet, dass** zwischen einem Vorentzerrer und einem Grenzwertentzerrer des Grenzwertentzerrerblocks (11) des Hilfssignalprozessors (10) ein Doppelbegrenzer bereitgestellt ist.

10. Vorrichtung zum Lesen von einem und/oder zum Schreiben auf ein Aufzeichnungsmedium, **dadurch gekennzeichnet, dass** sie ein Verfahren nach einem der Ansprüche 1 bis 6 verwendet oder eine Vorrichtung nach einem der Ansprüche 7 bis 9 für die Bitrückgewinnung in einem Datenkanal enthält.

Revendications

1. Procédé pour la récupération de bits dans un canal de données comprenant les étapes suivantes :

- saisie d'un signal de canal de lecture (A RDCH, D_RDCH) en provenance d'un support d'enregistrement ;
- fourniture d'un processeur de signal principal (3) pour la récupération adaptative de bits en provenance du signal de canal de lecture (A_RDCH, D_RDCH) ;
- fourniture d'un processeur de signal auxiliaire (10) ;
- utilisation d'une sortie (NRZ2) du processeur du signal auxiliaire (10) pour l'adaptation du processeur du signal principal (3) ; et
- sortie d'un flux récupéré de bits binaires (UD),

caractérisé en ce que le processeur de signal auxiliaire (10) permet la récupération des bits en provenance du signal de canal de lecture (A_ROCH, D_RDCH) et comprend un bloc égalisateur de limite (11) et un détecteur bit-par-bit de bits successifs (12) permettant la sortie (NRZ2) du processeur de traitement auxiliaire (10), dans lequel soit la sortie (NRZ2) du processeur de signal auxiliaire (10) soit une sortie du processeur de signal principal (NRZ1) est sélectionnée en tant que flux de bits binaire récupéré en fonction d'un mode de fonctionnement.

2. Procédé selon la revendication 1, comprenant en outre l'étape d'utilisation d'un égalisateur adaptatif (4) et d'un détecteur adaptatif (5) pour le processeur de signal principal.

3. Procédé selon une des revendications 1 ou 2, comprenant en outre l'étape d'utilisation du flux de données (NRZ1) en provenance du processeur de signal principal (3) pour l'adaptation fine du processeur de signal principal (3).

4. Procédé selon une des revendications 1 à 3, comprenant en outre l'étape de sélection du flux de données (NRZ2) en provenance du processeur de signal auxiliaire (10) en tant que flux de bits binaire (UD) jusqu'à ce que la sortie (NRZ1) en provenance du processeur de signal principal (3) soit fiable.

5. Procédé selon une des revendications 1 à 4, comprenant en outre l'étape de sélection du flux de données (NRZ2) en provenance du processeur de signal auxiliaire (10) en tant que flux de bits binaire (UD) pour le fonctionnement à vitesse rapide.

6. Procédé selon la revendication 1, comprenant en outre l'étape d'utilisation d'un éminceur entre un pré-égalisateur et un égalisateur de limite du bloc égalisateur de limite (11) du processeur de signal auxiliaire (10).

7. Procédé pour la récupération de bits dans un canal de données comprenant :

- une saisie d'un signal de canal de lecture (A RDCH, D_RDCH) en provenance d'un support d'enregistrement,

- un processeur de signal principal (3) pour la récupération adaptative de bits en provenance du signal de canal de lecture (A_RDCH, D_RDCH) ;
- un processeur de signal auxiliaire (10) permettant l'utilisation d'une sortie (NRZ2) du processeur du signal auxiliaire (10) pour l'adaptation du processeur du signal principal (3) ; et
- une sortie pour la sortie d'un flux récupéré de bits binaires (UD),

caractérisé en ce que le processeur de signal auxiliaire (10) permet la récupération des bits en provenance du signal de canal de lecture (A_ROCH, D_RDCH) et comprend un bloc égalisateur de limite (11) et un détecteur bit-par-bit de bits successifs (12) permettant la sortie (NRZ2) du processeur de traitement auxiliaire, dans lequel soit la sortie (NRZ2) du processeur de signal auxiliaire (10) ou une sortie du processeur de signal principal (NRZ1) est sélectionnée en tant que flux de bits binaire récupéré en fonction d'un mode de fonctionnement.

8. Dispositif selon la revendication 7, **caractérisé en ce que** le processeur de signal principal (3) comprend un égalisateur adaptatif (4) et un détecteur adaptatif (5).

9. Dispositif selon la revendication 7, **caractérisé en ce qu'**un éminceur est placé entre un pré-égalisateur et un égalisateur de limite du bloc égalisateur de limite (11) du processeur de signal auxiliaire (10).

10. Appareil permettant de lire et/ou d'écrire sur des supports d'enregistrement, **caractérisé en ce qu'**il utilise un procédé selon l'une quelconque des revendications 1 à 6 ou qu'il comprend un appareil selon l'une quelconque des revendications 7 à 9 pour la récupération de bits dans un canal de données.

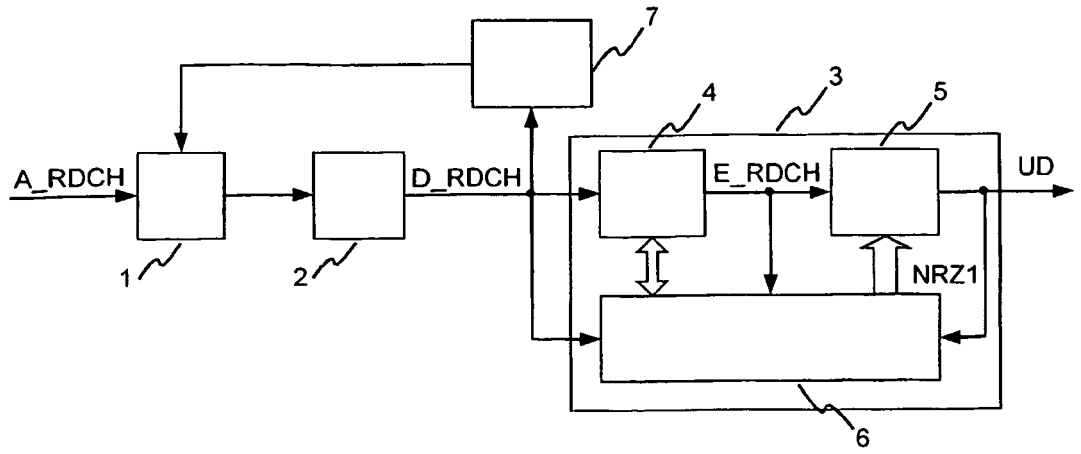

7
4
3
5
A_RDCH
D_RDCH
E_RDCH
UD
1
2
NRZ1
6

Fig. 1

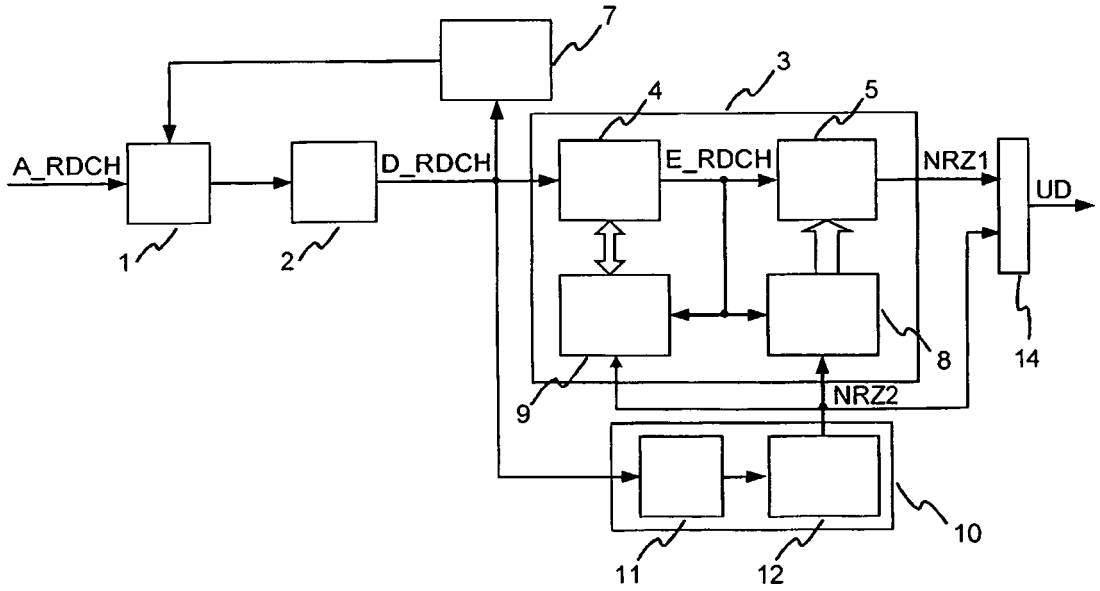

7
3
4
5
A_RDCH
D_RDCH
E_RDCH
NRZ1
UD
1
2
8
14
9
NRZ2
10
11
12

Fig. 2

REFERENCES CITED IN THE DESCRIPTION

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Non-patent literature cited in the description

- **TAKEHARA.** Combined Adaptive Controlled Partial Response and Maximum Likelihood Signal Processing for High-Density Optical Disks. *Jpn. J. Appl. Phys.,* 2003, vol. 42, 924-930 **[0004]**
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