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(54) **METHODS FOR STORING DATA IN NON-VOLATILE MEMORIES**

VERFAHREN ZUM SPEICHERN VON DATEN IN NICHTFLÜCHTIGEN SPEICHERN

PROCEDES DE MEMORISATION DE DONNEES DANS DES MEMOIRES NON VOLATILES

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Description

[0001] The present invention concerns methods for storing data in a non-volatile ferroelectric random access memory (FRAM), particularly a memory wherein a ferroelectric memory material is a ferroelectric polymer, wherein memory locations are provided as elements of a matrix and accessed via electrodes forming word and bit lines of the matrix, and wherein destructive read-out operations to the memory locations are followed by re-write operations.

[0002] Ferroelectric memories are becoming commercially important because they are non-volatile, can be made at relatively low cost, and can be written to and read at voltages from 1 to 5 volts and at speeds in the order of 10 to 100 nanoseconds, which is typical of conventional DRAM and SRAM computer memories.

[0003] Placing ferroelectric material between the plates of a capacitor on a semiconductor substrate causes the capacitor to exhibit a memory effect in the form of charge polarization. When the capacitor is charged with the field lines running in one direction across the capacitor plates, a residual charge polarization remains after the charge is removed from the capacitor plates. If an opposite charge is placed on the capacitor plates, an opposite residual polarization remains. A plot of the applied field voltage across the plates of the capacitor against the polarization of the ferroelectric material between the plates of the capacitor exhibits a classic hysteresis curve as shown in Figure 1. P_s and $-P_s$ are the spontaneous polarization values whereas P_r and $-P_r$ are the remnant polarization values indicating the polarization in the ferroelectric material at zero field value. In an ideal ferroelectric P_s should equal P_r but these values differ in actual ferroelectrics due to linear dielectric and non-linear ferroelectric behaviour.

[0004] Ferroelectric memories utilize a ferroelectric capacitor as the storage medium and an electric field must be placed across the storage capacitor in order to read it. A pulse is applied to the ferroelectric capacitor and the amount of resultant charge is either low if the pulse polarity agreed with the previous one, or the resultant charge is higher if the charge placed on the capacitor is of the opposite polarity of the one last placed across the plates of the capacitor. This minute difference between charge that agreed with the previous memory charge and an opposite charge can be measured to determine what the previous polarization on the ferroelectric capacitor was when it was last written. The reading electric field alters the state of the memory cell in many cases. This means that ferroelectric memories are destructively read-out memories which must include a rewrite function in which the data read out is restored to the memory cell after it has been read. The rewrite operation takes time, and if the memory function is truncated, for instance by a power loss, during or immediately after a cell is read and before the rewrite cycle can be completed, the data of that cell will be lost. Such data losses are not acceptable for non-volatile memories.

[0005] A ferroelectric random access memory (RAM) which uses ferroelectric memory cells to store data is disclosed in U.S. Pat. No. 5,682,344. The ferroelectric memory is a static memory in which data stored in the ferroelectric memory cells can be destroyed during read operations. The memory comprises circuitry which latches a current memory address during an access operation and prevents the memory from jumping to a new memory address until the destroyed data has been replaced. The memory also includes circuitry which can detect a transition in address data provided on address inputs.

[0006] A circuit including a ferroelectric capacitor that can be used to store the value of nodes of volatile logic elements in a logic circuit is disclosed in U.S. Pat. No. 5,815,431. In this manner, the state of a complex logic circuit, such as a CPU or an I/O device, can be stored in the non-volatile ferroelectric capacitors. After an accidental or planned power outage, the non-volatile ferroelectric capacitors can be used to restore the values of the nodes. Additionally, a planned power loss can be used for saving system power in circuits that are power-consumption sensitive.

[0007] An apparatus and method for maintaining non-volatility in a ferroelectric random access memory is disclosed in U.S. Pat. No. 5,892,705. The apparatus for maintaining non-volatility includes a control section for a write-back function, a power source voltage sensing unit for sensing a failure in the power source voltage and providing a power failure signal to the control section, such that the control section completes a write-back cycle before power failure. The power source voltage-sensing unit generates a control signal by sensing a failure in power source voltage, and provides a power failure signal to the control section such that a write-back process is completed before power failure, thereby maintaining non-volatility of the memory device.

[0008] In U.S. Pat. No. 6,201,731, the ferroelectric destructive read-out memory system includes a power source, a memory array including a memory cell, and a logic circuit for applying a signal to the memory array. Whenever a low power condition is detected in said power source, a disturb prevent circuit prevents unintended voltages due to the low power condition from disturbing the memory cell. The disturb prevent circuit also stops the operation of the logic circuit for a time sufficient to permit a rewrite cycle to be completed, thereby preventing loss of the data being rewritten.

[0009] In U.S. Pat. No. 6,211,710, a circuit for ensuring stabilized configuration information upon power-up is disclosed. In one embodiment, a semiconductor device includes a configuration information stored in a number of non-volatile storage elements (fuse bits). A configuration power-on reset circuit generates a signal for latching the configuration data into volatile configuration registers on power-up. The configuration data signals are generated in response to a power-on reset (POR) pulse, and not latched until a predetermined delay after the POR pulse

is terminated. The predetermined delay allows time for the data signals from the fuse bits to "settle." Subsequent POR pulses will not result in another latching action.

[0010] European patent application EP 0 803 813 A1 discloses a data-backup apparatus for a semiconductor memory, particularly a non-volatile semiconductor memory, for instance of the type EEPROM (electrical erasable read only memory). The purpose of this apparatus is to prevent data loss or incorrect data if a write operation unintentionally is interrupted, for instance if the power is turned off during a write operation. The semiconductor memory has a plurality of memory locations storing values of variables. A write unit writes a value to a plurality of memory locations in the memory one by one and a read unit reads the values from these memory locations. A coincidence determining means is used to decide whether more than half of the read values from the memory locations in the memory are identical, and assigning means then determines a coincidence value if the coincidence determining means has found that more than half of the values are identical. Thus, a determined coincidence value can be assigned each variable.

[0011] The object of the present invention is to provide methods that ensures a non-volatile storage of data in matrix-addressable memories, particularly ferroelectric memories, and maintain the integrity of the stored data by detecting bit errors in the readout data and effecting a correction thereof.

[0012] This object as well as further features and advantages are realized according to the present invention with a first method which is characterized by successive steps for

(a) storing a plurality of identical copies of said data in a plurality of memory locations, said memory locations not having any common word lines;
(b) reading a first word line in its entirety, said first word line comprising at least a first copy of said identical copies of said data, rewriting the data read from said first word line back into said first word line and, transferring the data read from said first word line to a memory control logic circuit;
(c) reading a subsequent word line in its entirety, said subsequent word line comprising at least a subsequent copy of said identical copies of said data, rewriting the data read from said subsequent word line back into said subsequent word line, and transferring the data read from said subsequent word line to said memory control logic circuit;
(d) repeating step (c) until said data read from said word lines comprising copies of said identical copies of said data, have been transferred to said memory control logic circuit;
(e) detecting any bit errors by comparing said data read from said word lines comprising copies of said identical copies of said data, bit-wise in said memory control logic circuit, or by including an error correction code (ECC) with said data; and
(f) writing corrected data to the memory cells in said memory locations that hold bit errors, when bit errors have been detected in step (e).

[0013] The same object as well as further features and advantages are realized according to the present invention with a second method which is characterized by successive steps for

(a) storing a plurality of identical copies of said data in a plurality of memory locations, said memory locations having neither common word lines nor common bit lines;
(b) reading a segment of a first word line, said segment of a first word line comprising at least a first copy of said identical copies of said data, rewriting the data read from said segment of a first word line back into said segment of a first word line, transferring said data read from said segment of a first word line to a first segment of data latches, and retaining said data read from said segment of a first word line in said first segment of data latches;
(c) reading a segment of a subsequent word line, said segment of a subsequent word line comprising at least a subsequent copy of said identical copies of said data, rewriting the data read from said segment of a subsequent word line back into said segment of a subsequent word line, transferring said data read from said segment of a subsequent word line to a subsequent segment of data latches, and retaining said data read from said segment of a subsequent word line in said subsequent segment of data latches;
(d) repeating step (c) until said identical copies of said data have been transferred to said segments of data latches;
(e) transferring said data retained in said segments of data latches to a memory control logic circuit;
(f) detecting any bit errors by comparing said identical copies of said data bit-wise in said memory control logic circuit, or by including an error correction code (ECC) with said data; and
(g) writing corrected data to the memory cells in said memory locations that hold bit errors, when bit errors have been detected in step (f).

[0014] In both methods according to the invention the data preferably are timing data for controlling the read and rewrite operations, or redundancy data for identifying redundancy memory cells.

[0015] The invention shall now be explained in greater detail with discussions of exemplary embodiments and with reference to the accompanying drawing figures, of which

figure 1 shows a hysteresis curve of a ferroelectric capacitor as known in the art and mentioned above,

figure 2 a block diagram of a memory circuit wherein the methods according to the invention may be implemented,

figure 3a a schematic block diagram of an array of ferroelectric memory cells connecied to sense amplifiers and which can be used with the methods according to the invention,

figure 3b a schematic block diagram of an array similar to the one in fig. 3a and comprising ferroelectric memory cells with diodes between the electrodes in the crossings thereof,

figure 4 two diagrams of a ferroelectric thin-film capacitor as used in ferroelectric memory devices,

figure 5 a flow chart of a first method according to the invention,

figure 6 a flow chart of a second method according to the invention, and

figure 7 a diagram of a memory array as used with a preferred embodiment of the second method according to the invention.

[0016] The present invention concerns related methods expressing the same inventive idea. These methods will now be described in terms of preferred embodiments.

[0017] Figure 2 illustrates a simple block diagram that demonstrates the elements of the memory as used with both methods according to the invention. The memory macro 210 comprises a memory matrix or array 200, row and column decoders 22, 202, sense amplifiers 206, data latches 208 and redundant word and bit lines 204, 24. The row and column decoders 22, 202 decode the addresses of memory locations or memory cells which are located at the crossings of the memory array electrodes, i.e. the word lines (abbreviated WL) forming the rows of the memory array and the bit lines (abbreviated BL) forming the columns of the memory macros. Readout of data stored in the memory cells is performed by the sense amplifiers 206 connected to the bit lines. The data latches 208 hold the data until a part thereof or all is transferred to the memory control logic 220. The data read from the memory macro 210 shall have a certain bit error rate (BER) which can be decreased by replacing defective word and bit lines in the memory array 200 with redundant word and bit lines 204, 24. In order to perform error detection the memory macro 210 must have data fields containing error correction code (ECC) information.

[0018] A module for the memory control logic 220 provides a digital interface for the memory macro 210 and controls the read and write of the memory array 200. Memory initialisation and logic for replacing defective word and bit lines with redundant word and bit lines 204, 24 will be found in the memory control logic 220 as well.

[0019] The device controller 230 connects the memory control logic 220 to external bus standards. The ECC unit 240 performs error correction on the full memory array 200. It can be a simple error detection or include error correction as well. The charge pumps 242 generate some of the voltages needed to read and write of the memory cells. A separate clock input, given by the device controller 230 via an oscillator (not shown), will be used by the charge pumps 242 for charge pumping in order to remain independent of the bit rate of the application using the memory macro 210.

[0020] Figure 3a shows a ferroelectric memory device 300 comprising a matrix or array of ferroelectric memory cells 302. Each memory cell comprises one ferroelectric capacitor and one access control transistor, but there may well be arrangements with two capacitors and two transistors. In the first case the memory macro then is an active matrix-addressable memory device of the type 1T-1C, while in the other case it is of the type 2T-2C. A memory cell 302 is accessed by an enabling word line 310 and is subsequently read by a pulsing drive line 312. Sense amplifiers 206 provided at the end of each bit line 314 generate data out signals. The sense amplifiers also include data regeneration circuits for rewriting data to the ferroelectric memory cells 302. A row decoder 22 decodes a part of the incoming address signals into word line selection signals and the memory control logic 220 generates a sequence of timing signals required for operating the memory array 200.

[0021] Figure 3b shows a memory array 200 comprising word line 310 and bit line 314 electrodes. A ferroelectric insulating material is located between these electrodes which therefore do not connect electrically or physically. The ferroelectric material could, however, also be provided above the electrodes, i.e. the word and bit lines, in contact therewith, but beyond that the word and bit lines shall be mutually insulated by a non-ferroelectric dielectric. - At each intersection 320 between the word lines 310 and bit lines 314, diodes 322 are generated. The ferroelectric material together with the word and bit lines 310;314 forms ferroelectric capacitors or memory cells 315 with the word and bit lines 310;314 as the plates of the capacitors.

[0022] Figure 4 illustrates a typical structure and a commonly used symbol for a ferroelectric thin film capacitor 315. The symbol was also used in the schematic block diagram in figure 3a as mentioned above. A ferroelectric capacitor of this kind has metallic conductive plates separated by about 50 nm to 100 micrometers of a ferroelectric material constituting the dielectric of the capacitor.

[0023] In a non-volatile passive matrix memory system as described above some data, such as configuration data, are very important and need to be protected from a power loss. Timing data for controlling read and rewrite operations as well as redundancy data for identifying redundant memory cells are examples thereof, and if these data get lost, that could render the entire memory useless. Data of this kind could be permanently stored in e.g.

fused cells, i.e. fuses melted by lasers, but this comports rather large area penalties. Therefore, important data can be stored in destructive read-out memory cells anyway if other measures are taken to maintain their safety.

[0024] Figure 5 presents in the form of a flow diagram the first method of the present invention, which solves the problem of having important data eradicated by e.g. a power failure. In step 500, the data that require special attention is stored in several locations in the memory array 200. If some of these locations are defective the redundant word and bit lines 204, 24 are used instead. Whenever the data is about to be used, or on a regular basis, the word lines (WL);(see fig. 7) where these data are stored are read, followed by a rewrite, also known as write-back, automatic in most cases, and transferred to the memory control logic 220 in steps 502 and 504. The number of instances or copies of said data will be around four to ten and some form of counter will in step 506 make sure that all instances are read. Three copies is obviously too little since a power failure in combination with a bit error could cause fatal damage. The different copies of the data are compared in step 508 bit by bit. Another option is to use an ECC unit 240 which requires ECC data to be stored together with the data itself. Finally, in step 510 the portions of the data that were found to be incorrect are corrected and written to the memory cells 302;315 holding the erroneous data.

[0025] The amount of data that needs to be protected in this way may be quite limited and the word lines 310 used for safety storage can be quite long. This leads to an inefficient use of the memory array 200. In order to remedy this problem the second method according to the invention could be used. It is shown in the flow diagram in fig. 6 and will ensure that smaller portions of the data deemed important are transferred and that these portions are transferred to data latches 208 in steps 602 and 604. This results in memory cells 302;315 being freed up for other data since the entire word lines 310 no longer have to hold identical data. Steps 606, 608 and 610 correspond to the steps 506, 508 and 510 in fig. 5 with the only difference that less data are handled. However, a step 607 must be inserted between steps 606 and 608 in order to have the data stored in the data latches 208 transferred to the memory control logic 220. As a result, memory cells in the memory control logic 220 do not need to store as much data since there is no data transfer in steps 602 and 604. Thus the area cost is reduced and similarly the requirement on the data processing capabilities for performing the error detection are reduced.

[0026] Bit lines 314 are sometimes shorted and data is then stored in redundant bit lines 24. An unexpected shortage problem may eradicate important data. Although a smaller problem, it can be circumvented by storing the important data on different bit lines 314 as well as on different word lines 310. This variant of the second method of the invention is rendered in figure 7, which shows word lines (WL) 700 and bit lines (BL) 702 for memory cells 704 storing important data. These copies of important data constitute data blocks 706, and are transferred to storage elements such as the data latches 208 in accordance with the second method of the invention as described above in connection with figure 6.

[0027] Persons skilled in the art will realize that the methods according to the invention can be used with active as well as passive matrix-addressable electric memory devices and handle bit errors which are generated in addressing operation on both types. But as the readout operation is destructive and hence requires a write-back or rewrite, it will in any case of particular importance to prevent the loss of data content due to bit errors which are generated in the rewrite operation which is required for restoring the destructively readout data.

Claims

1. A method for storing data in a non-volatile ferroelectric random access memory (FRAM), particularly a memory wherein a ferroelectric memory material is a ferroelectric polymer, wherein memory locations are provided as elements of a matrix and accessed via electrodes forming word and bit lines of the matrix and wherein destructive read-out operations to the memory locations are followed by rewrite operations, the method being
characterized by successive steps for

(a) storing a plurality of identical copies of said data in a plurality of memory locations, said memory locations not having any common word lines;
(b) reading a first word line in its entirety, said first word line comprising at least a first copy of said identical copies of said data, rewriting the data read from said first word line back into said first word line and, transferring the data read from said first word line to a memory control logic circuit;
(c) reading a subsequent word line in its entirety, said subsequent word line comprising at least a subsequent copy of said identical copies of said data, rewriting the data read from said subsequent word line back into said subsequent word line, and transferring the data read from said subsequent word line to said memory control logic circuit;
(d) repeating step (c) until said data read from said word lines comprising copies of said identical copies of said data, have been transferred to said memory control logic circuit;
(e) detecting any bit errors by comparing said data read from said word lines comprising copies of said plurality of identical copies of said data, bit-wise in said memory control logic circuit or by including an error correction code (ECC) with said data; and

(f) writing corrected data to the memory cells in said memory locations that hold bit errors, when bit errors have been detected in step (e).

2. The method according to claim 1, **characterized by** said data being timing data for controlling the read and rewrite operations, or redundancy data for identifying redundant memory cells.

3. A method for storing data in a non-volatile ferroelectric random access memory (FRAM), particularly a memory wherein a ferroelectric memory material is a ferroelectric polymer, wherein memory locations are provided as elements of a matrix and accessed via electrodes forming word and bit lines of the matrix, and wherein destructive read-out operations to the memory locations are followed by rewrite operations, the method being
characterized by successive steps for

(a) storing a plurality of identical copies of said data in a plurality of memory locations, said memory locations having neither common word lines nor common bit lines;
(b) reading a segment of a first word line, said segment of a first word line comprising at least a first copy of said identical copies of said data, rewriting the data read from said segment of a first word line back into said segment of a first word line, transferring said data read from said segment of a first word line to a first segment of data latches, and retaining said data read from said segment of a first word line in said first segment of data latches;
(c) reading a segment of a subsequent word line, said segment of a subsequent word line comprising at least a subsequent copy of said identical copies of said data, rewriting the data read from said segment of a subsequent word line back into said segment of a subsequent word line, transferring said data read from said segment of a subsequent word line to a subsequent segment of data latches, and retaining said data read from said segment of a subsequent word line in said subsequent segment of data latches;
(d) repeating step (c) until said identical copies of said data have been transferred to said segments of data latches;
(e) transferring said data retained in said segments of data latches to a memory control logic circuit;
(f) detecting any bit errors by comparing said identical copies of said data bit-wise in said memory control logic circuit, or by including an error correction code (ECC) with said data; and
(g) writing corrected data to the memory cells in said memory locations that hold bit errors, when bit errors have been detected in step (f).

4. The method according to claim 3, **characterized by** said data being timing data for controlling the read and rewrite operations, or redundancy data for identifying redundant memory cells.

Patentansprüche

1. Verfahren zum Speichern von Daten in einem nichtflüchtigen ferroelektrischen Direktzugriffsspeicher (FRAM), vorzugsweise ein Speicher, in dem ein ferroelektrisches Speichermaterial ein ferroelektrisches Polymer ist, wobei Speicherstellen als Elemente einer Matrix vorgesehen sind und auf die zugegriffen wird über Elektroden, die Wort- und Bitzeilen der Matrix bilden, und wobei auf zerstörende Ausleseoperationen auf die Speicherstellen Umschreibeoperationen folgen, wobei das Verfahren durch aufeinander folgende Schritte **gekennzeichnet** ist zum

(a) Speichern einer Vielzahl von identischen Kopien der Daten in einer Vielzahl von Speicherstellen, wobei die Speicherstellen keine gemeinsamen Wortzeilen haben;
(b) Lesen einer ersten Wortzeile in ihrer Gesamtheit, wobei die erste Wortzeile wenigstens eine erste Kopie der identischen Kopien der Daten umfasst, Umschreiben der Daten, die von der ersten Wortzeile zurück in die erste Wortzeile gelesen wurden, und Übertragen der Daten, die von der ersten Wortzeile in eine Speichersteuer-Logikschaltung gelesen wurden;
(c) Lesen einer anschließenden Wortzeile in ihrer Gesamtheit, wobei die anschließende Wortzeile wenigstens eine anschließende Kopie der identischen Kopien der Daten umfasst, Umschreiben der Daten, die von der anschließenden Wortzeile zurück in die anschließende Wortzeile gelesen wurden, und Übertragen der Daten, die von der anschließenden Wortzeile in die Speichersteuer-Logikschaltung gelesen wurden;
(d) Wiederholen des Schrittes (c) bis die Daten, die von Wortzeilen, die Kopien der identischen Kopien der Daten umfassen, gelesen wurden, zu der Speichersteuer-Logikschaltung übertragen worden sind;
(e) Erkennen von beliebigen Bitfehlern durch bitweises Vergleichen der Daten, die von den Wortzeilen, die Kopien der Vielzahl von identischen Kopien der Daten umfassen, gelesen wurden, in der Speichersteuer-Logikschaltung oder durch Beinhalten eines Fehlerkorrekturcodes (ECC) mit den Daten; und
(f) Schreiben der korrigierten Daten in die Speicherzellen an den Speicherstellen, die Bitfehler enthalten, wenn Bitfehler in Schritt (e) detektiert

wurden.

2. Verfahren nach Anspruch 1, **dadurch gekennzeichnet, dass** die Daten Zeitsteuerungsdaten sind, um die Lese- und Umschreibeoperationen zu steuern, oder Redundanzdaten, um redundante Speicherzellen zu identifizieren.

3. Verfahren zum Speichern von Daten in einem nichtflüchtigen ferroelektrischen Direktzugriffsspeicher (FRAM), vorzugsweise ein Speicher, in dem ein ferroelektrisches Speichermaterial ein ferroelektrisches Polymer ist, wobei Speicherstellen als Elemente einer Matrix vorgesehen sind und auf die zugegriffen wird über Elektroden, die Wort- und Bitzeilen der Matrix bilden, und wobei auf zerstörende Ausleseoperationen auf die Speicherstellen Umschreibeoperationen folgen, wobei das Verfahren durch aufeinander folgende Schritte **gekennzeichnet** ist zum

(a) Speichern einer Vielzahl von identischen Kopien der Daten in einer Vielzahl von Speicherstellen, wobei die Speicherstellen weder gemeinsame Wortzeilen noch gemeinsame Bitzeilen haben;
(b) Lesen eines Segmentes einer ersten Wortzeile, wobei das Segment einer ersten Wortzeile wenigstens eine erste Kopie der identischen Kopien der Daten umfasst, Umschreiben der Daten, die von dem Segment einer ersten Wortzeile zurück in das Segment einer ersten Wortzeile gelesen wurden, Übertragen der Daten, die von dem Segment einer ersten Wortzeile in ein anschließendes erstes Segment von Datensignalspeichern gelesen wurden, und Zurückhalten der Daten, die von dem Segment einer ersten Wortzeile in das erste Segment der Datensignalspeicher gelesen wurden;
(c) Lesen eines Segmentes einer anschließenden Wortzeile, wobei das Segment einer anschließenden Wortzeile wenigstens eine anschließende Kopie der identischen Kopien der Daten umfasst, Umschreiben der Daten, die von dem Segment einer anschließenden Wortzeile zurück in das Segment einer anschließenden Wortzeile gelesen wurden, Übertragen der Daten, die von dem Segment einer anschließenden Wortzeile in ein anschließendes erstes Segment von Datensignalspeichern gelesen wurden, und Zurückhalten der Daten, die von dem Segment einer anschließenden Wortzeile in das anschließende Segment der Datensignalspeicher gelesen wurden;
(d) Wiederholen des Schrittes (c), bis die identischen Kopien der Daten zu den Segmenten der Datensignalspeicher übertragen wurden;
(e) Übertragen der Daten, die in den Segmenten der Datensignalspeicher zurückgehalten werden zu einer Speichersteuer-Logikschaltung
(f) Erkennen beliebiger Bitfehler durch bitweises Vergleichen der identischen Kopien der Daten in der Speichersteuer-Logikschaltung oder durch Beinhalten eines Fehlerkorrekturcodes (ECC) mit den Daten; und
(g) Schreiben der korrigierten Daten in die Speicherzellen an den Speicherstellen, die Bitfehler enthalten, wenn Bitfehler in Schritt (f) detektiert wurden.

4. Verfahren nach Anspruch 3, **dadurch gekennzeichnet, dass** die Daten Zeitsteuerungsdaten sind, um die Lese- und Umschreibeoperationen zu steuern, oder Redundanzdaten, um redundante Speicherzellen zu identifizieren.

Revendications

1. Procédé pour enregistrer les données dans une mémoire vive ferroélectrique (FRAM) non volatile, en particulier une mémoire dans laquelle une matière de mémoire ferroélectrique est un polymère ferroélectrique, dans lequel les emplacements de mémoire sont prévus sous la forme d'éléments d'une matrice et auxquels on accède par des électrodes formant des lignes de mots et de bits de la matrice et dans lequel les opérations de lecture destructive des emplacements de mémoire sont suivies d'opérations de réécriture, le procédé étant **caractérisé par** les étapes successives :

(a) d'enregistrement d'une pluralité de copies identiques desdites données dans une pluralité d'emplacements de mémoire, lesdits emplacements de mémoire ne comprenant pas de lignes de mots communes ;
(b) de lecture d'une première ligne de mots dans sa totalité, ladite première ligne de mots comprenant au moins une première copie desdites copies identiques desdites données, de réécriture des données lues dans ladite première ligne de mots de nouveau dans ladite première ligne de mots, et de transfert des données lues dans ladite première ligne de mots dans un circuit logique de contrôle de mémoire ;
(c) de lecture d'une ligne de mots ultérieure dans sa totalité, ladite ligne de mots ultérieure comprenant au moins une copie ultérieure desdites copies identiques desdites données, de réécriture des données lues dans ladite ligne de mots ultérieure de nouveau dans ladite ligne de mots ultérieure, et de transfert des données lues dans ladite ligne de mots ultérieure dans ledit circuit logique de contrôle de mémoire ;
(d) de répétition de l'étape (c) jusqu'à ce que les

données lues dans lesdites lignes de mots comprenant les copies desdites copies identiques desdites données aient été transférées dans ledit circuit logique de contrôle de mémoire ;
(e) de détection de bits d'erreur en comparant lesdites données lues dans lesdites lignes de mots comprenant les copies de ladite pluralité de copies identiques desdites données, bit par bit dans ledit circuit logique de contrôle de mémoire ou en incluant un code correcteur d'erreurs (ECC) avec lesdites données ; et
(f) écriture des données corrigées dans les cellules de mémoire dans lesdits emplacements de mémoire qui contiennent des bits d'erreur, quand les bits d'erreur ont été détectés à l'étape (e).

2. Procédé selon la revendication 1, **caractérisé en ce que** lesdites données sont des données d'horloge pour contrôler les opérations de lecture et de réécriture, ou des données de redondance pour identifier les cellules de mémoire redondantes.

3. Procédé pour enregistrer les données dans une mémoire vive ferroélectrique non volatile (FRAM), en particulier une mémoire dans laquelle une matière de mémoire ferroélectrique est un polymère ferroélectrique, dans lequel les emplacements de mémoire sont prévus sous la forme d'éléments d'une matrice et accédés par des électrodes formant des lignes de mots et de bits de la matrice et dans lequel les opérations de lecture destructive des emplacements de mémoire sont suivies par des opérations de réécriture, le procédé étant **caractérisé par** les étapes successives :

(a) d'enregistrement d'une pluralité de copies identiques desdites données dans une pluralité d'emplacements de mémoire, lesdits emplacements de mémoire ne comprenant ni des lignes de mots communes, ni des lignes de bits communes ;
(b) de lecture d'un segment d'une première ligne de mots, ledit segment d'une première ligne de mots comprenant au moins une première copie desdites copies identiques desdites données, de réécriture des données lues dans ledit segment d'une première ligne de mots de nouveau dans ledit segment d'une première ligne de mots, et de transfert des données lues dans ledit segment d'une première ligne de mots dans un premier segment de verrous de données, et de conservation dans ledit premier segment de verrous de données, desdites données lues dans ledit segment d'une première ligne de mots ;
(c) de lecture d'un segment d'une ligne de mots ultérieure, ledit segment d'une ligne de mots ultérieure comprenant au moins une copie ultérieure desdites copies identiques desdites données, de réécriture des données lues dans ledit segment d'une ligne de mots ultérieure de nouveau dans ledit segment d'une ligne de mots ultérieure, de transfert desdites données lues dans ledit segment d'une ligne de mots ultérieure dans un segment ultérieur de verrous de données, et de conservation dans ledit segment ultérieur de verrous de données, desdites données lues dans ledit segment d'une ligne de mots ultérieure ;
(d) de répétition de l'étape (c) jusqu'à ce que lesdites copies identiques desdites données aient été transférées dans lesdits segments de verrous de données ;
(e) de transfert desdites données conservées dans lesdits segments de verrous de données dans un circuit logique de contrôle de mémoire ;
(f) de détection de bits d'erreur en comparant lesdites copies identiques desdites données bit par bit dans ledit circuit logique de contrôle de mémoire, ou en incluant un code correcteur d'erreurs (ECC) avec lesdites données ; et
(g) d'écriture des données corrigées dans les cellules de mémoire dans lesdits emplacements de mémoire qui contiennent des bits d'erreur, quand les bits d'erreur ont été détectés à l'étape (f).

4. Procédé selon la revendication 3, **caractérisé en ce que** lesdites données sont des données d'horloge pour contrôler les opérations de lecture et de réécriture, ou des données de redondance pour identifier les cellules de mémoire redondantes.

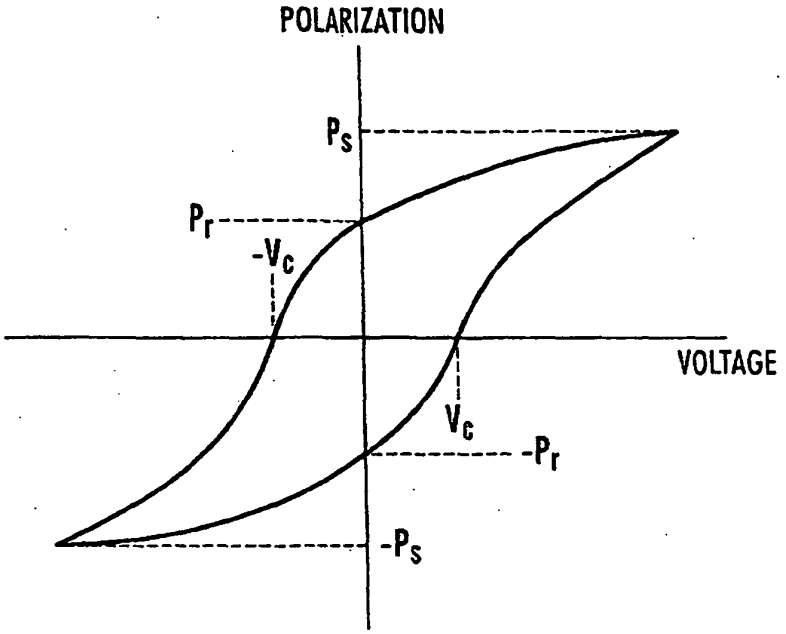
POLARIZATION
P_S
P_r
$-V_C$
VOLTAGE
V_C
$-P_r$
$-P_S$

Fig.1

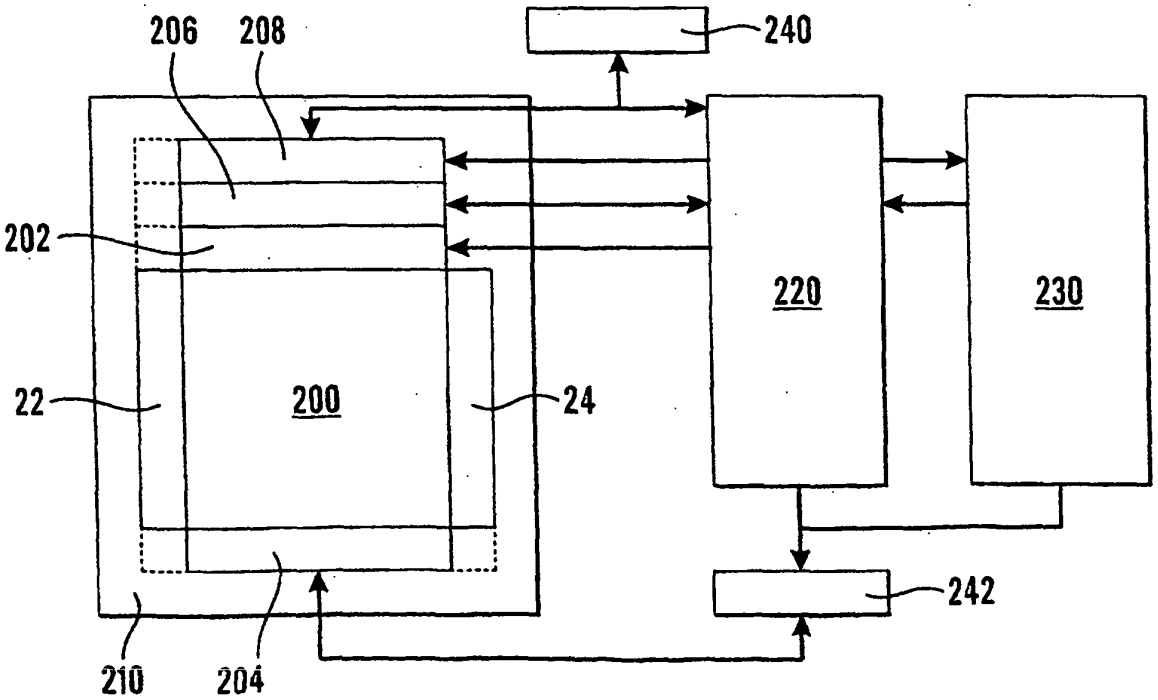
206
208
240
202
220
230
22
200
24
242
210
204

Fig.2

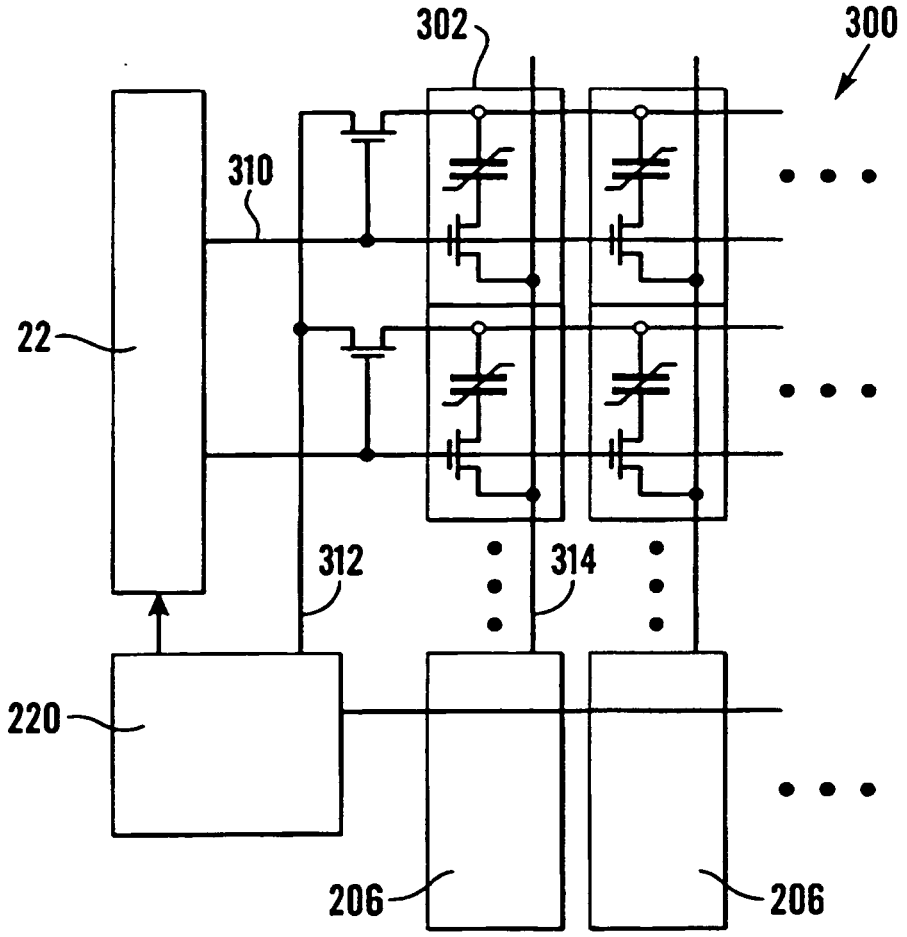

Fig.3a

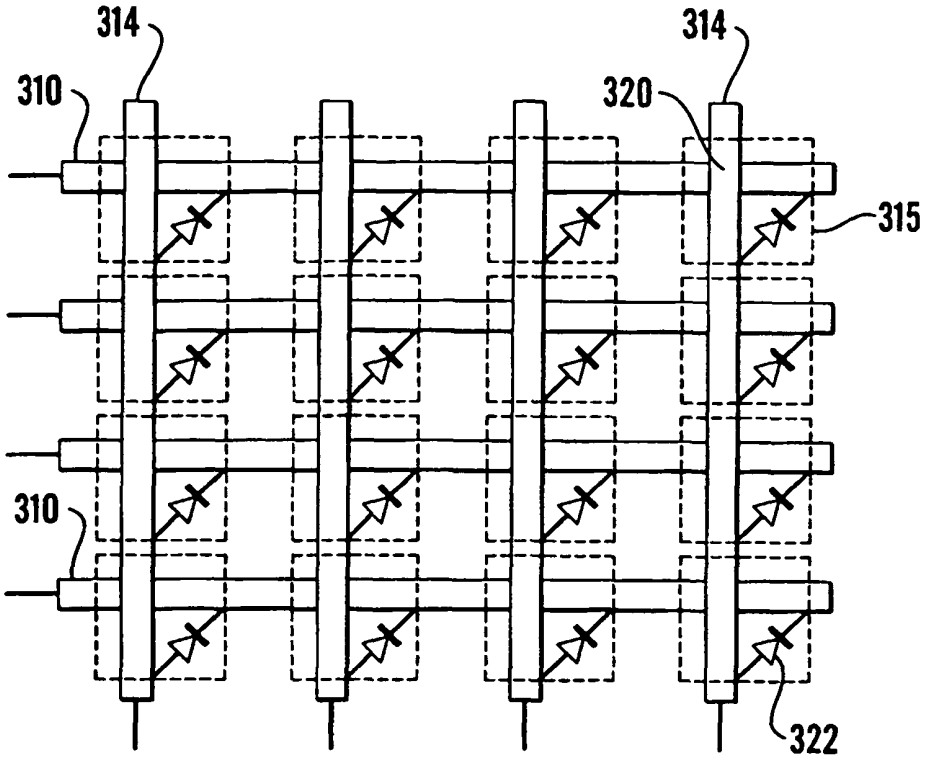
314
314
310
320
315
310
322

Fig.3b

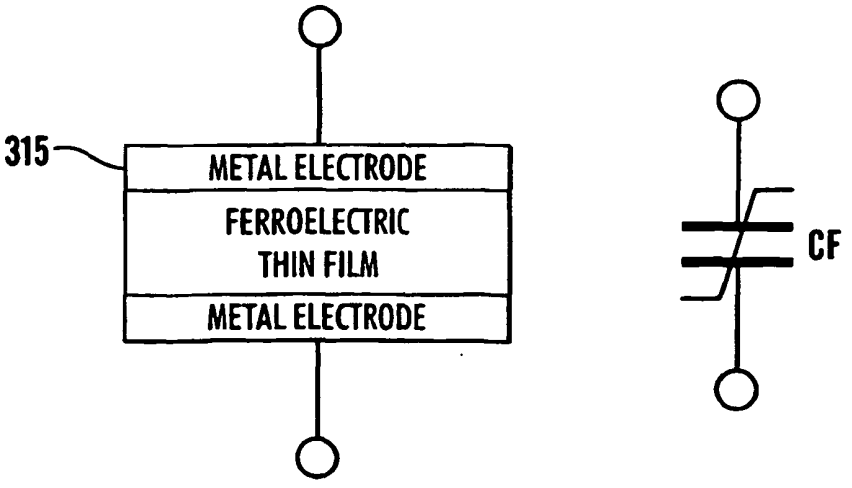
315
METAL ELECTRODE
FERROELECTRIC
THIN FILM
METAL ELECTRODE
CF

Fig.4

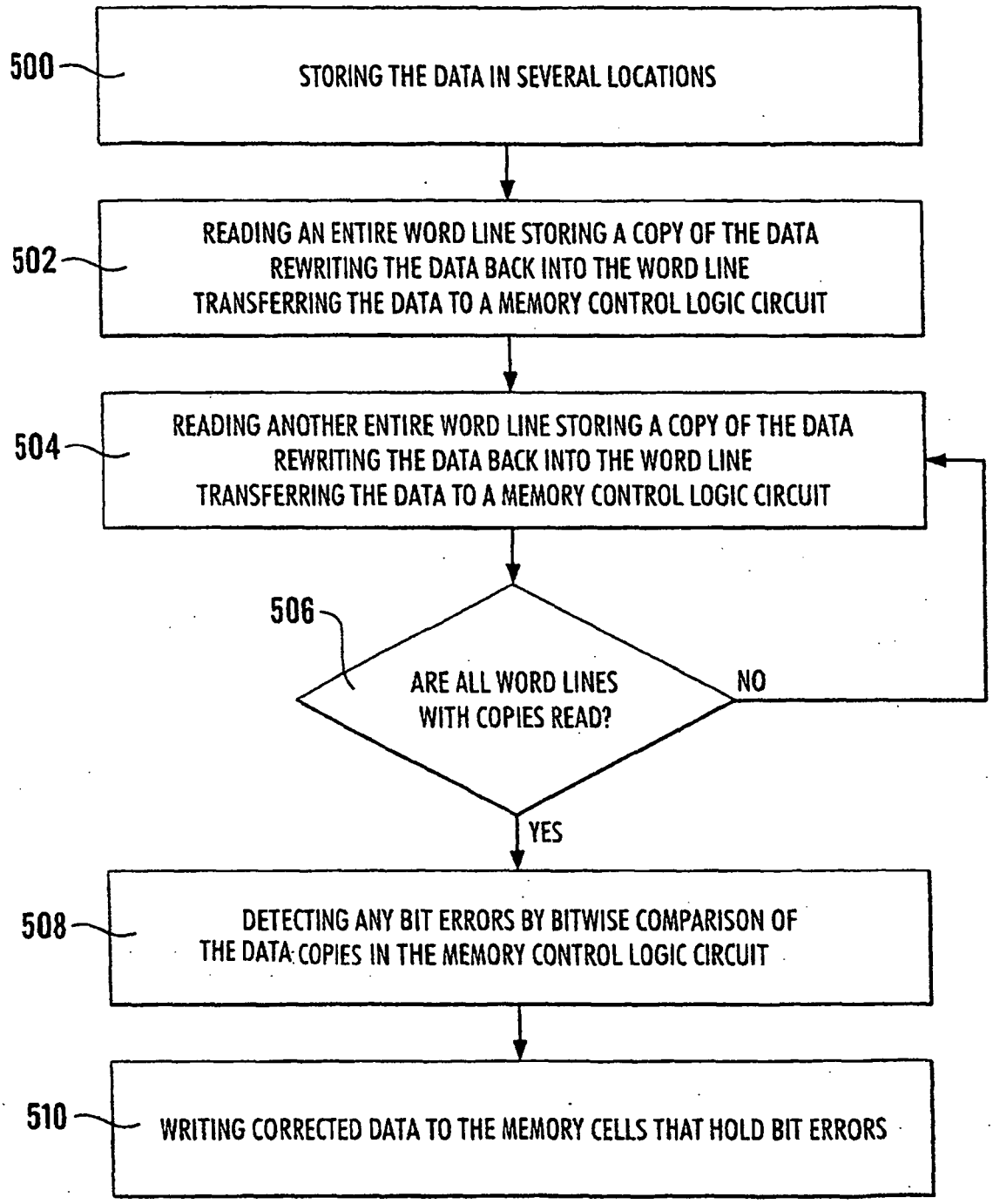
500
STORING THE DATA IN SEVERAL LOCATIONS
502
READING AN ENTIRE WORD LINE STORING A COPY OF THE DATA
REWRITING THE DATA BACK INTO THE WORD LINE
TRANSFERRING THE DATA TO A MEMORY CONTROL LOGIC CIRCUIT
504
READING ANOTHER ENTIRE WORD LINE STORING A COPY OF THE DATA
REWRITING THE DATA BACK INTO THE WORD LINE
TRANSFERRING THE DATA TO A MEMORY CONTROL LOGIC CIRCUIT
506
ARE ALL WORD LINES WITH COPIES READ?
NO
YES
508
DETECTING ANY BIT ERRORS BY BITWISE COMPARISON OF THE DATA COPIES IN THE MEMORY CONTROL LOGIC CIRCUIT
510
WRITING CORRECTED DATA TO THE MEMORY CELLS THAT HOLD BIT ERRORS

Fig.5

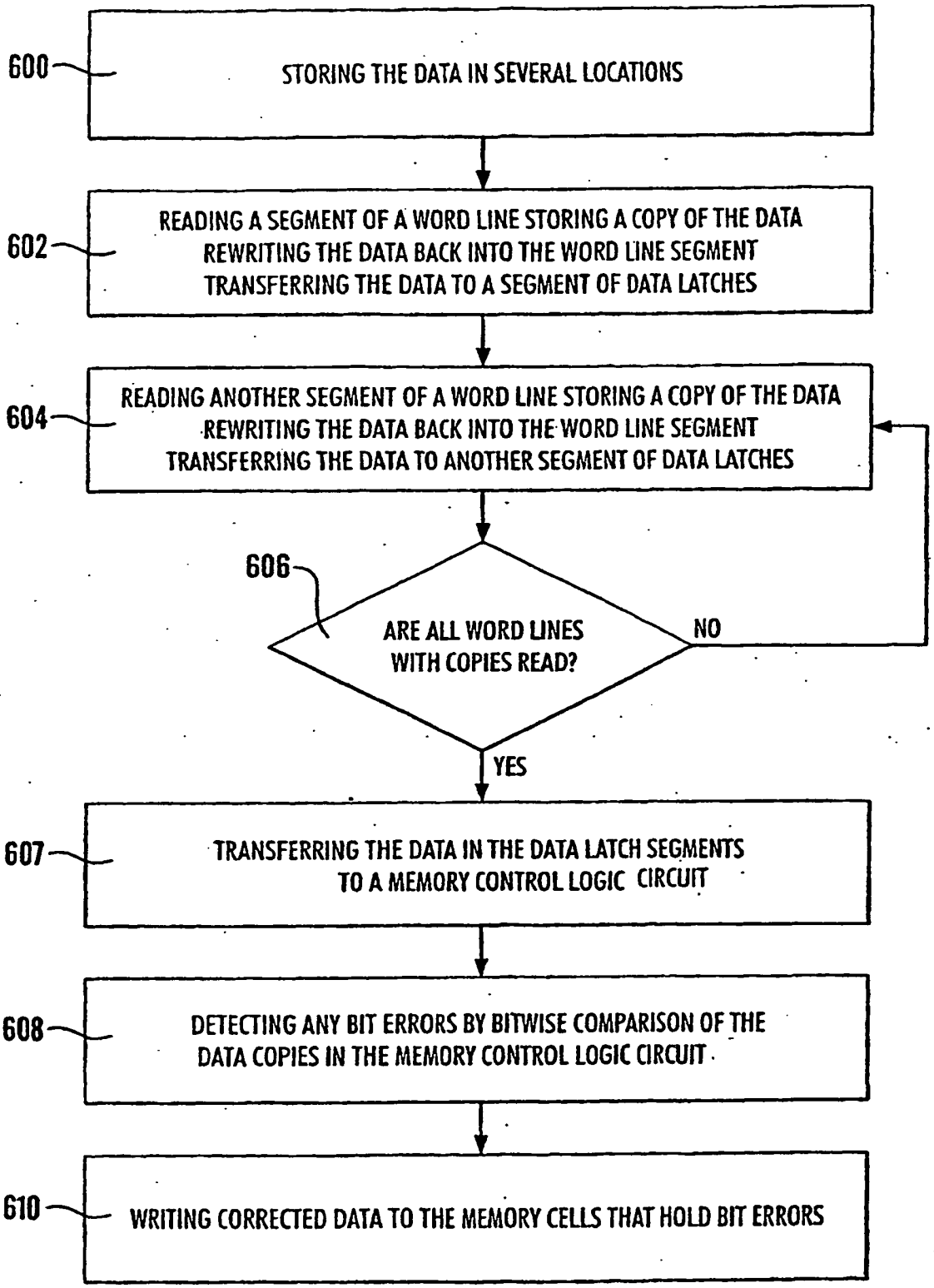
600
STORING THE DATA IN SEVERAL LOCATIONS
602
READING A SEGMENT OF A WORD LINE STORING A COPY OF THE DATA
REWRITING THE DATA BACK INTO THE WORD LINE SEGMENT
TRANSFERRING THE DATA TO A SEGMENT OF DATA LATCHES
604
READING ANOTHER SEGMENT OF A WORD LINE STORING A COPY OF THE DATA
REWRITING THE DATA BACK INTO THE WORD LINE SEGMENT
TRANSFERRING THE DATA TO ANOTHER SEGMENT OF DATA LATCHES
606
ARE ALL WORD LINES WITH COPIES READ?
NO
YES
607
TRANSFERRING THE DATA IN THE DATA LATCH SEGMENTS TO A MEMORY CONTROL LOGIC CIRCUIT
608
DETECTING ANY BIT ERRORS BY BITWISE COMPARISON OF THE DATA COPIES IN THE MEMORY CONTROL LOGIC CIRCUIT
610
WRITING CORRECTED DATA TO THE MEMORY CELLS THAT HOLD BIT ERRORS

Fig.6

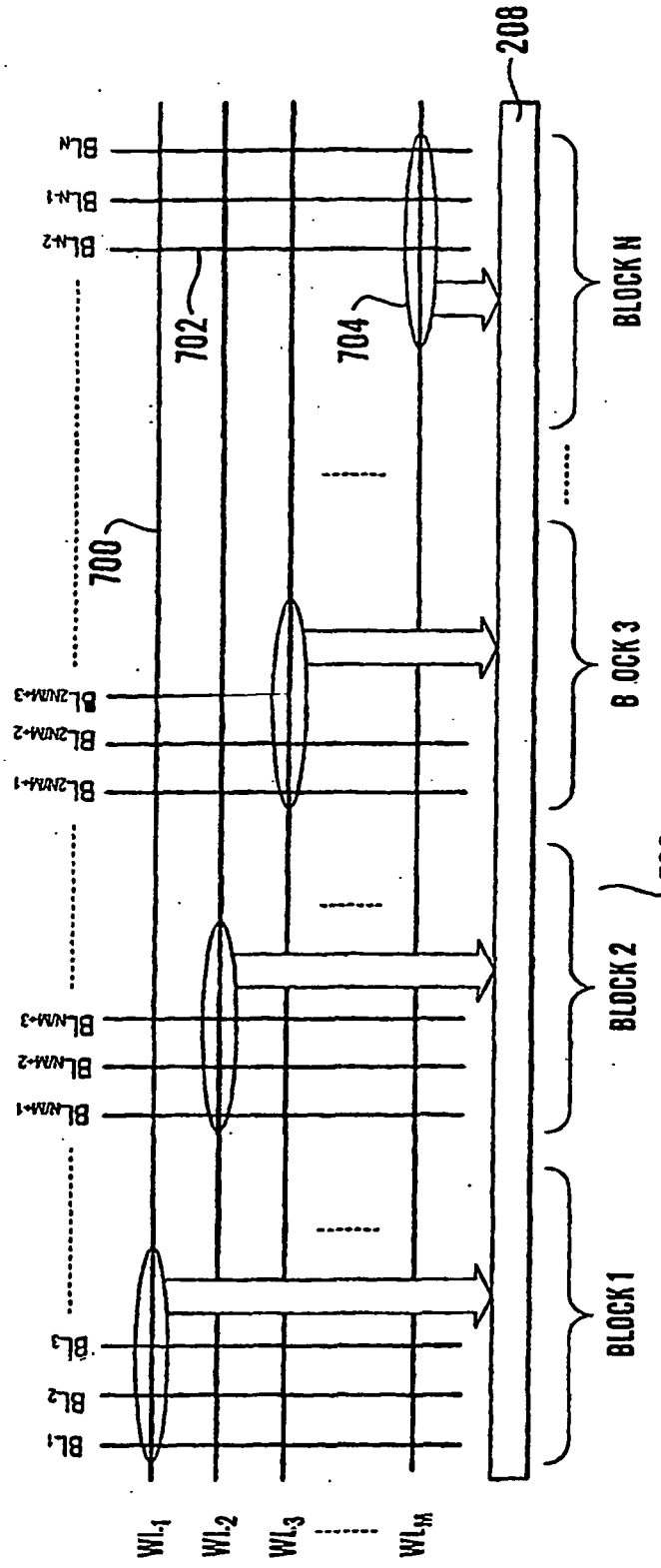
208
BLN
BLN-1
BLN-2
702
704
700
BLOCK N
BLOCK 3
BLOCK 2
BLOCK 1
706
BL1
BL2
BL3
WL1
WL2
WL3
WLM

Fig.7