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(54) MIS power semiconductor device and method of making the same

(57) A power device (D) integrated on a semiconductor substrate (1) with double thickness of a gate dielectric layer (S) and a corresponding manufacturing method for said power device (D), said method comprising the following steps:

- forming first dielectric portions (3) having a first thickness;
- forming on the whole semiconductor substrate (1) a first dielectric layer (4) thinner than the first dielectric portions (3);
- forming a conductive layer (5) on the first dielectric layer (4);
- forming a second dielectric layer (6,13) on the conductive layer (5);
- performing an etching step of the second dielectric layer (6,13) and of the conductive layer (5) to form first spacers (7,14) and a gate electrode (5a), to define, between the gate electrode (5a) and the substrate (1), second dielectric portions (4a) in the first dielectric layer (4), the second dielectric portions (4a) being auto-aligned with the first portions (3).

An etching step may be carried out to remove the portion of the conductive layer (5) overlying the thick dielectric portions (3).
A body contact trench (12) may be formed using second spacers (11).

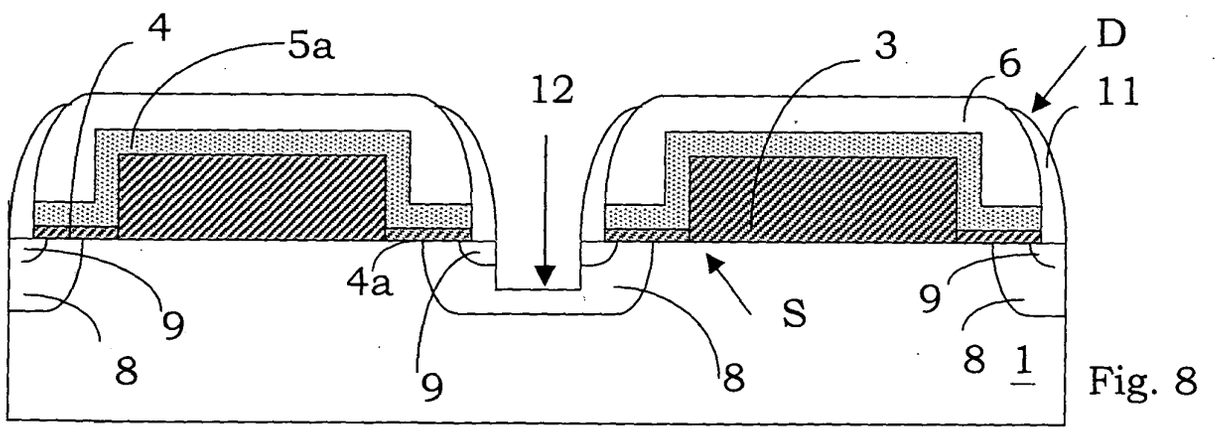

Fig. 8

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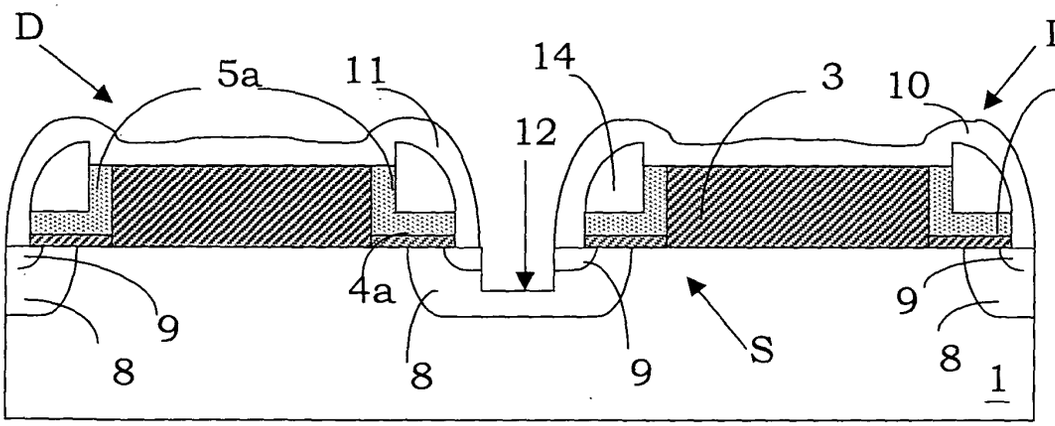

Fig. 12

Description

Field of application

[0001] The present invention relates to a manufacturing method for a power device having an auto-aligned double thickness gate dielectric layer and corresponding device.

[0002] The invention also relates to a power device integrated on a semiconductor substrate comprising a gate electrode formed above a channel region formed in said semiconductor substrate and insulated therefrom by means of a gate dielectric layer.

[0003] The invention particularly, but not exclusively, relates to a manufacturing method of a VDMOS power device and the following description is made with reference to this field of application for convenience of illustration only.

Prior art

[0004] As it is well known, the planar and vertical size decrease and the subsequent power device integration density increase involves the need to reduce the driving potentials of these devices in order to save the strength and integrity thereof. A particularly important class of silicon power devices are PowerMOSFETs which must generally meet very strict requirements in terms of minimum on state resistance and high switching speed in switching applications.

[0005] Moreover, it is important to succeed in driving these devices with very low voltages (logic or superlogic level) in order to reduce also the power consumption.

[0006] On the technological level, the need to reduce more and more a PowerMOSFET operating resistance has led to a new design of the MOS capacitor structure which is formed between the gate electrode, the substrate and the gate dielectric layer interposed between these layers, and which is responsible for the switching functions themselves.

[0007] In particular, the gate dielectric layer thickness, traditionally silicon oxide, is more and more reduced in order to obtain threshold voltage values being even lower than 1 Volt without degrading excessively the breakdown strength of the diffused channel, channel which is moreover designed in order to be always as short as possible.

[0008] Nevertheless, such a technological choice as the just mentioned one has some important drawbacks. In terms of switching speed, in fact, the reduction of the gate dielectric layer thickness, together with the increase in the gate electrode area being intrinsic in the higher integration density, involves lower transistor device performances because of the increased input and transition capacitive components.

[0009] Moreover, in some more and more important applications wherein the device must integrally support the action of ionised environmental agents, for example in satellites or high nuclear radiation concentration environments, an excessive reduction of the involved geometries and of the gate dielectric layer thickness can generate a considerable device weakening with respect to the action of very energetic heavy ions passing through the device and capable of depositing very high amounts of energy/ charge in the active region of the device itself.

[0010] A prior art solution to meet this requirement to form thin, but radiation-resistant, gate dielectric layers, provides the integration in traditional MOS devices of gate dielectric layers being different from thermal silicon oxide (SiO_2) such as for example hafnium oxide, aluminium oxide or silicon oxide/silicon nitride multilayers.

[0011] Although advantageous under many aspects, this first solution has several drawbacks connected to the use of alternative materials whose use at industrial level involves long implementation steps being subject to tests which might require prohibitive times for the present market of the devices concerned.

[0012] The technical problem underlying the present invention is to manufacture a power device having a fast switching and a high tolerance to the trigger of gate dielectric layer hard breakdown mechanisms, this device being manufactured with the lowest number of process steps and having such structural and functional features as to allow a very compact device to be obtained, overcoming the limits and drawbacks still affecting prior art devices.

Summary of the invention

[0013] The solution idea underlying the present invention is to manufacture a power transistor device having a "totally auto-aligned" double thickness gate dielectric layer in active area. Advantageously, in the transistor device manufacturing, a single photolithography step is used to define the configuration of a thick gate dielectric layer portion.

[0014] On the basis of this solution idea the technical problem is solved by a manufacturing method as previously indicated and defined in the characterising part of claim 1.

[0015] The problem is also solved by a device as previously indicated and defined in the characterising part of claim 11.

[0016] The features and advantages of the method and device according to the invention will be apparent from the following description of an embodiment thereof given by way of non-limiting example with reference to the attached drawings.

Brief description of the drawings

[0017] In the drawings:

- Figures 1 to 8 show schematical views in vertical section and in enlarged scale respectively of a ver-

tical-type MOS device undergoing different steps of a first embodiment of the manufacturing method according to the invention;

- Figures 9 to 12 show schematical views in vertical section and in enlarged scale respectively of a MOS device undergoing different steps of a second embodiment of the manufacturing method according to the invention.

Detailed description

[0018] With reference to these drawings, a MOS transistor electronic device, in particular of the VDMOS type, manufactured according to the method of the present invention, is globally and schematically indicated with D.

[0019] The process steps and the structures described hereinafter do not form a complete process flow for manufacturing integrated circuits. In fact, the present invention can be implemented together with the integrated circuit manufacturing techniques presently used in this field and only those commonly used process steps which are necessary to understand the invention are described hereinafter.

[0020] The figures representing cross sections of device portions during the manufacturing are not drawn to scale, but they are drawn instead in order to show the important features of the invention.

[0021] With reference to figure 7, a transistor device D formed on a semiconductor material substrate 1 is shown. In particular, the device D can be a power device formed in the MOS technology with a central gate electrode 5a and respective source regions 9 located on opposite sides with respect to the gate electrode 5a.

[0022] These source regions 9 are completely comprised in respective body regions 8.

[0023] The gate electrode 5a is formed above a channel region 1a formed in the semiconductor substrate 1 and insulated from the latter by interposing a gate dielectric layer S.

[0024] According to the invention, this gate dielectric layer S comprises a first dielectric portion 3 of a first thickness and a second dielectric portion 4a of a second thickness. In other words, the gate dielectric layer S has a double thickness.

[0025] In particular, the first dielectric portion 3 has a higher thickness than the second dielectric portion 4a. Moreover, the first dielectric portion 3 and the second dielectric portion 4a are auto-aligned with each other.

[0026] The second portion 4a is also aligned with the gate electrode 5a in correspondence with the source 9 and channel 1a regions.

[0027] The whole gate electrode 5a is covered on top by a dielectric layer 6. The device D is then completed by spacers 11 formed on the side walls of the electrode 5a and on the dielectric layer 6.

[0028] Advantageously, a soft trench 12 is formed in the substrate 1 aligned with spacers 11.

[0029] The device D is then traditionally completed by forming a drain electrode behind the substrate 1, not shown in the drawings.

[0030] With reference to figure 11, a second embodiment of the device D according to the invention is described.

[0031] In this embodiment, the gate electrode 5a is not present on the upper surface of the first dielectric portion 3, but it is present only on the side walls of this first dielectric portion 3.

[0032] First spacers 14 are then formed on the gate electrode 5a. The device D is then completed by second spacers 11 formed on the side walls of the electrode 5a and they cover at least partially the first spacers 14. These second spacers 11 are formed in a dielectric layer 10 covering the top of both the gate electrode 5a and the first dielectric portions 3.

[0033] In this embodiment too, advantageously, a soft trench 12 is formed in the substrate 1 aligned with the second spacers 11.

[0034] A first embodiment of the manufacturing method of the device D according to the invention is now described.

[0035] Convenient edge terminals, not shown in the figures, are traditionally formed on a semiconductor substrate 1.

[0036] A thin dielectric layer, for example thermal oxide with a thickness being lower or equal to 100 nm, can be formed on the semiconductor substrate 1, not shown in the figures.

[0037] According to the invention, a thick gate dielectric layer 2 is formed on the substrate 1, for example through CVD (Chemical Vapor Deposition) deposition.

[0038] The thick dielectric layer 2 is for example a USG (Undoped Silicon Glass), PSG (Phospho-Silicate Glass), BPSG (Boro-Phospho-Silicate Glass), TEOS (Tetraethyl Ortosilicate), SOG (Spin on Glass), silicon nitride layer, or a multilayer comprising a sequence of these layers.

[0039] Advantageously, the thickness of this dielectric layer 2 ranges from 100 to 1000 nm.

[0040] A thermal densifying process of the thick dielectric layer 2 is then advantageously performed.

[0041] As shown in figure 1, through a traditional photolithographic technique, a first plurality of dielectric portions 3 is defined from the thick dielectric layer 2.

[0042] Advantageously, the etching step of this thick dielectric layer 2 is performed through a unidirectional etching with final end point on the semiconductor substrate 1.

[0043] Advantageously, a cleaning step is performed on the whole semiconductor device to prepare the manufacture of a second dielectric layer.

[0044] A thin gate dielectric layer 4 is then formed on the whole substrate in the regions not covered by the first portions 3. For example this thin gate dielectric layer 4 is formed through thermal oxidation or it can be formed by means of an oxinitride layer or an oxide/nitride/oxide

multilayer. Advantageously, the thickness of the thin gate dielectric layer 4 is lower or equal to 100 nm.

[0045] A conductive layer 5 is then formed on the whole device to manufacture gate electrodes as shown in figure 3. For example, a doped polysilicon layer, or a double polysilicon/metallic silicide layer is deposited. The thickness of this conductive layer 5 is compatible with the planar geometries and the auto-alignment requirements of the manufacturing process.

[0046] A further dielectric layer 6 is formed on the whole device for example through CVD (Chemical Vapor Deposition) deposition.

[0047] The dielectric layer 6 is for example a low-conformality dielectric layer or multilayer like for example USG (Undoped-Silicate Glass), PSG (Phospho-Silicate Glass), TEOS (Tetraethyl Orthosilicate) formed through convenient deposition techniques. The thickness of this dielectric layer 6 depends on the planar geometry and the project channel length.

[0048] Advantageously, having the dielectric layer 6 a low conformality, the thickness of this dielectric layer 6 in correspondence with the thin layer 4 is lower than the layer formed in correspondence with the portions 3 of the thick dielectric layer 2, as shown in figure 3.

[0049] An etching step of the dielectric layer 6 is then performed. For example this etching step is of the unidirectional type, with end point on the conductive layer 5. First spacers 7 are formed therefore on the conductive layer 5 in correspondence with the side walls of the portions 3, as shown in figure 4.

[0050] Advantageously, this dielectric layer 6, after the etching step, covers also a portion of the conductive layer 5 located in correspondence with the upper surface of the first portions 3, while it is completely removed from further portions of the conductive layer 5 located in correspondence with the thin dielectric layer 4 being uncovered by the first spacers 7.

[0051] An etching step of the conductive layer 5 being uncovered by the first spacers 7 is then performed. A portion 5a of the conductive layer 5 which is therefore defined between these spacers 7 and the substrate forms the gate electrode of the final device, as shown in figure 4.

[0052] Advantageously, this etching step is of the unidirectional type and it is timed or end point performed on the thin gate dielectric layer 4.

[0053] Second dielectric portions 4a of the thing gate dielectric layer 4 are then defined and comprised between the gate electrode 5a and the semiconductor substrate 1, as shown in figure 5.

[0054] The first dielectric portions 3 and the second dielectric portions 4a form the gate dielectric layer S of the final device D.

[0055] A body region 8 is then formed for example by performing a ionic implant in the substrate 1 and further diffusing said implanted region 8.

[0056] Advantageously, an etching step of the residual thin gate dielectric layer 4 is then performed up to uncover the substrate 1. This etching step is for example of the dry type and timed.

[0057] A source region 9 is then formed, for example by performing a further ionic implant F in the substrate 1, as shown in figure 5.

[0058] A further dielectric layer 10 is formed, on the whole device, for example through CVD (Chemical Vapor Deposition) deposition, as shown in figure 6.

[0059] The dielectric layer 10 is for example a low-conformality dielectric layer or multilayer, like for example USG (Undoped-Silicate Glass), PSG (Phospho-Silicate Glass), TEOS (Tetraethyl Orthosilicate) formed through convenient deposition techniques.

[0060] The thickness of this dielectric layer 10 depends on the planar geometry of the device D.

[0061] A diffusion step of the source region 9 and a densifying step of the last dielectric layer 10 are then performed, as shown in figure 6.

[0062] An etching step of this last dielectric layer 10 is then performed to form second spacers 11. This etching step is for example of the unidirectional type with final end point on the semiconductor substrate, as shown in figure 7.

[0063] An advantageous embodiment of the device according to the invention provides the formation of a body/ source contact soft trench 12 which is auto-aligned with the second spacers 11.

[0064] The presence of a soft trench in the source/ body diffusion region allows a metalization contact to be formed on both source and body wells being extended on the whole active cell perimeter. Therefore, it avoids a previous photolithographic step to be performed, which selects the active cell area fraction being concerned by the source implant. Therefore the periphery of said channel region, which will obviously be equal to the perimeter of the gate electrode, is maximised.

[0065] Finally, a strengthening of the device with respect to the destructive triggering of parasite elements in the active area is basically obtained.

[0066] The device D according to the invention is then completed with traditional process steps providing:

- pad contact photolithography;
- front device metalization;
- preparation and metalization of the back wafer to form the device drain region.

[0067] This first embodiment allows a device D to be obtained with low resistance of the gate electrode 5a, covering completely the first portions 3.

[0068] A second embodiment of the manufacturing method of the device D according to the invention is now described.

[0069] In particular the process steps up to the deposition of the conductive layer 5 on the whole semiconductor substrate are the same as in the previous em-

bodiment.

[0070] A first dielectric layer 13 is then formed on the conductive layer 5, for example through CVD deposition, as shown in figure 9.

[0071] The first dielectric layer 13 is for example a high-conformality dielectric layer or multilayer like for example USG (Undoped-Silicate Glass), PSG (Phospho-Silicate Glass), TEOS (Tetraethyl Orthosilicate) formed through convenient deposition techniques. The thickness of this dielectric layer 13 depends on the planar geometry and the project channel length.

[0072] Having the first dielectric layer 13 a high conformality, the thickness of this layer is uniform on the whole device D.

[0073] An etching step, for example unidirectional, of the first dielectric layer 13is performed at end point on the conductive layer 5 to form a first spacer 14, as shown in figure 10.

[0074] This etching step is then followed by an etching step, for example unidirectional, of the gate electrode (multi)layer, timed or with end point on the thin gate dielectric layer 4.

[0075] The process flow is completed as in the previous embodiment starting from the deposition of the dielectric layer 10 to form second spacers 11.

[0076] In particular, in this embodiment the dielectric layer 10 is not removed from the upper surface of the first dielectric portion 3 and it covers the top of both the gate electrode 5a and the first dielectric portions 3.

[0077] Advantageously, in this second embodiment the removal of the gate electrode overlapped to the thick dielectric portions 3 ensures a better gate/source side insulation quality because of the higher usable thickness of the second dielectric layer 10.

[0078] The present invention applies to VDMOS power devices of both types of polarity with any edge terminal structure and with cell in active area of any shape and size.

[0079] The method according to the invention can be advantageously applied to signal VDMOS, IGBT and VDMOSFET devices, both of the P- and of the N- type.

[0080] Both embodiments described can be also used to define photolithographically active area contacts, i.e. without auto-aligned formation of the second spacer. Obviously in this case size limits of the width of the device D or elementary cell are largely imposed by the definition and alignment specifications of the photoexposure equipment used. Nevertheless, an evident advantage mainly in the second embodiment, wherein the gate electrode overlapped to the thick dielectric portion 3 also called intercell is removed, is the higher insulation quality between gate electrode and source region because of, as already mentioned, the higher dielectric layer 10 thickness which can be used in this embodiment.

[0081] In conclusion, by manufacturing a device D, with a gate dielectric layer S comprising two portions 3, 4a with different thickness and auto-aligned with each other, photolithographic steps are not used for defining single elements composing the device, such as for example the gate electrode. This allows a very compact device D to be manufactured with no need to provide alignment tolerances required to perform the following photolithographic steps thus allowing a device D with a symmetrical diffused channel and lengths of even 0.1=0.5 μm to be manufactured.

[0082] In particular, the removal of the photolithographic definition step of the gate electrode is allowed by exploiting the low conformality of the CVD silicon oxide layer 4, for example USG, connected in turn to the thick dielectric layer 2 height and to the width of the device D or active cell (aspect ratio).

[0083] Moreover the self-alignment of the pattern of the gate electrode and mainly of the source and body region diffusions makes the definition of the photolithography itself forming initial thick dielectric layer portions 3 less critical.

Claims

1. A manufacturing method for a power device (D) integrated on a semiconductor substrate (1) with double thickness of a gate dielectric layer (S) comprising the following steps:

   - forming first dielectric portions (3) having a first thickness;
   - forming on whole said semiconductor substrate (1) a first dielectric layer (4) thinner than said first dielectric portions (3);
   - forming a conductive layer (5) on said first dielectric layer (4);
   - forming a second dielectric layer (6, 13) on said conductive layer (5);.
   - performing an etching step of said second dielectric layer (6, 13) and of said conductive layer (5) to form first spacers (7, 14) and a gate electrode (5a), to define, between said gate electrode (5a) and said substrate (1), second dielectric portions (4a) in said first dielectric layer (4), said second dielectric portions (4a) being auto-aligned with said first portions (3).

2. A manufacturing method according to claim 1, **characterised in that** said second dielectric layer (6) is formed in a non conforming manner.

3. A manufacturing method according to claim 2, **characterised in that** said etching step leaves portions of said second dielectric layer (6) to cover the top of said gate electrode (5a).

4. A manufacturing method according to claim 1, **characterised in that** said second dielectric layer (13) is formed in a conforming manner.

5. A manufacturing method according to claim 4, **characterised in that** said etching step removes said second dielectric layer (13) and said conductive layer (5) in correspondence with said first portions (3).

6. A manufacturing method according to claim 3, **characterised in that** it further comprises the steps of:

   - depositing a third dielectric layer (10) on whole said semiconductor substrate (1).

7. A manufacturing method according to claim 6, **characterised in that** it further comprises the steps of:

   - etching said third dielectric layer (10) in order to form second spacers (11) on the side walls of said gate electrode (5a) and on said first spacers (7, 14) and to leave said second dielectric layer (6) to cover the top of said gate electrode (5a).

8. A manufacturing method according to claim 5, **characterised in that** it further comprises the steps of:

   - depositing a third dielectric layer (10) on whole said semiconductor substrate (1).

9. A manufacturing method according to claim 8, **characterised in that** it further comprises the steps of:

   - etching said third dielectric layer (10) in order to form second spacers (11) on the side walls of said gate electrode (5a) and on said first spacers (7, 14) and to leave said third dielectric layer (10) to cover the top of said gate electrode (5a) and of said first dielectric portions (3).

10. A manufacturing method according to claim 7 or 9, **characterised in that** it comprises the step of forming a soft trench (12) in the semiconductor substrate (1) being aligned with said second spacers (11).

11. A power device (D) integrated on a semiconductor substrate (1) comprising a gate electrode (5a) formed above a channel region (1a) formed in said semiconductor substrate (1) and insulated from the latter by means of a gate dielectric layer (S) **characterised in that** said gate dielectric layer (S) comprises at least a first dielectric portion (3) having a first thickness and a second dielectric portion (4a) having a second thickness being lower than the first one, said first dielectric portion (3) and second dielectric portion (4a) being auto-aligned with each other.

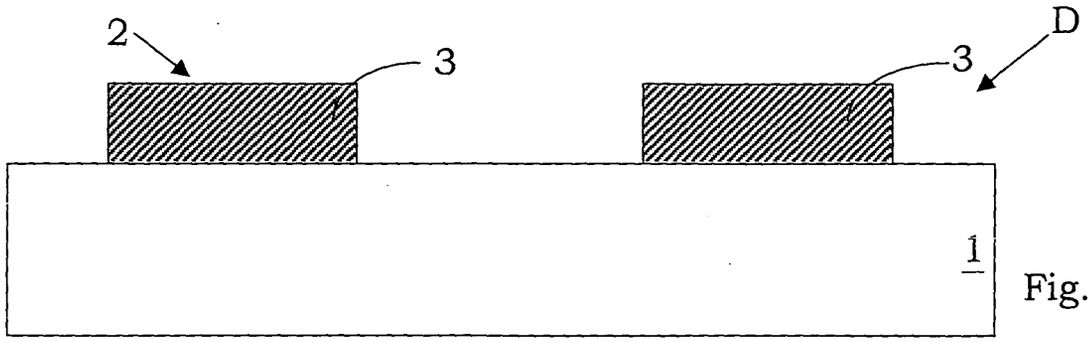

Fig. 1

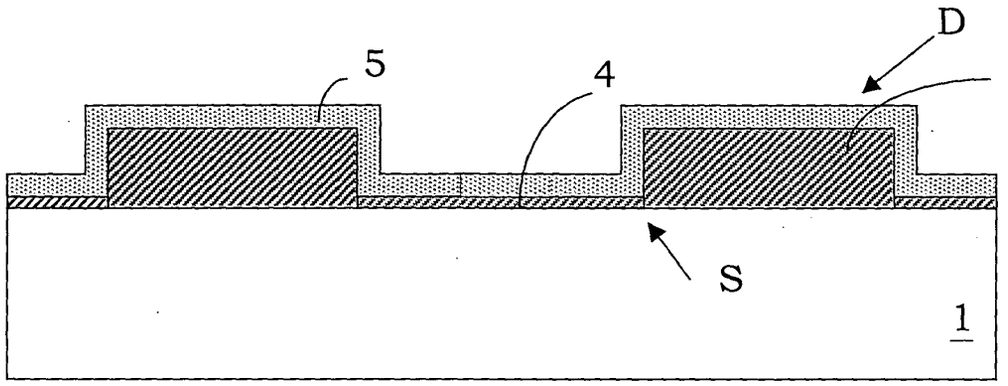

Fig. 2

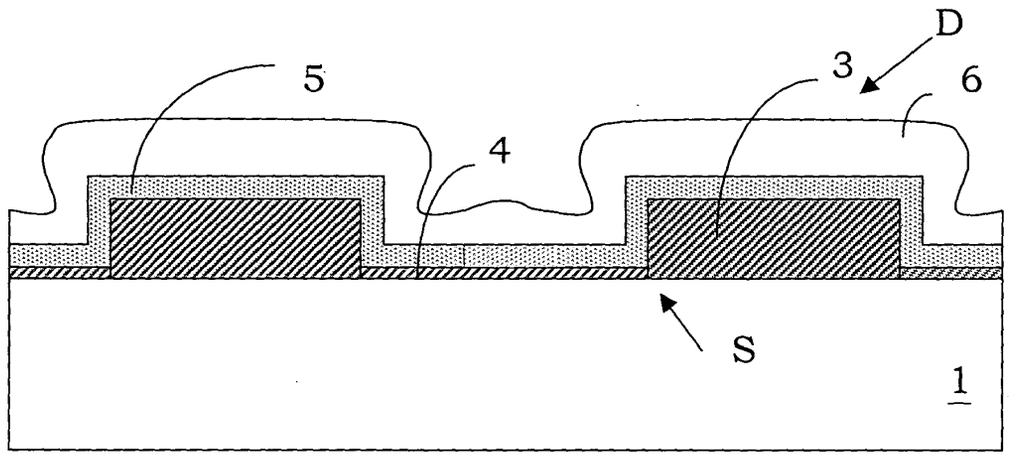

Fig. 3

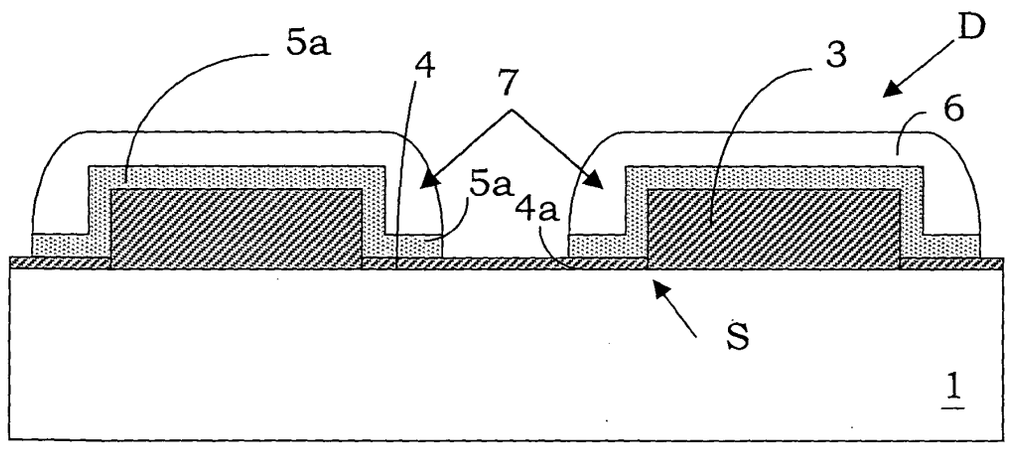

Fig. 4

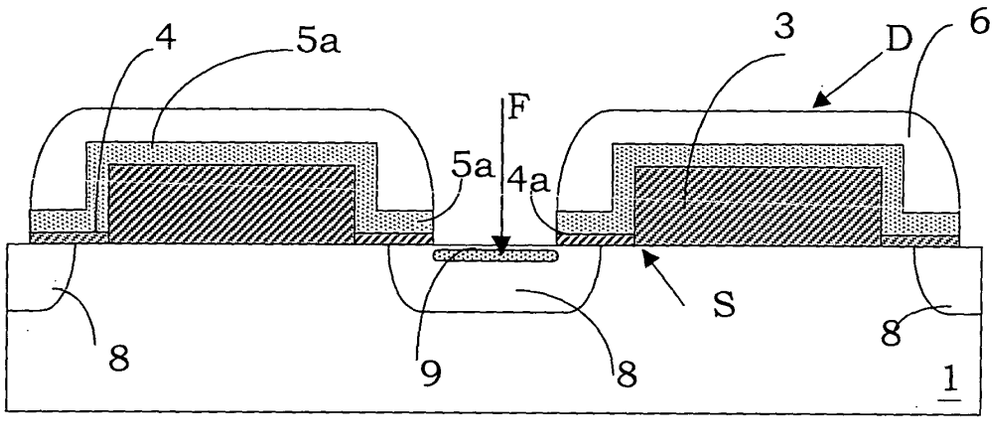

Fig. 5

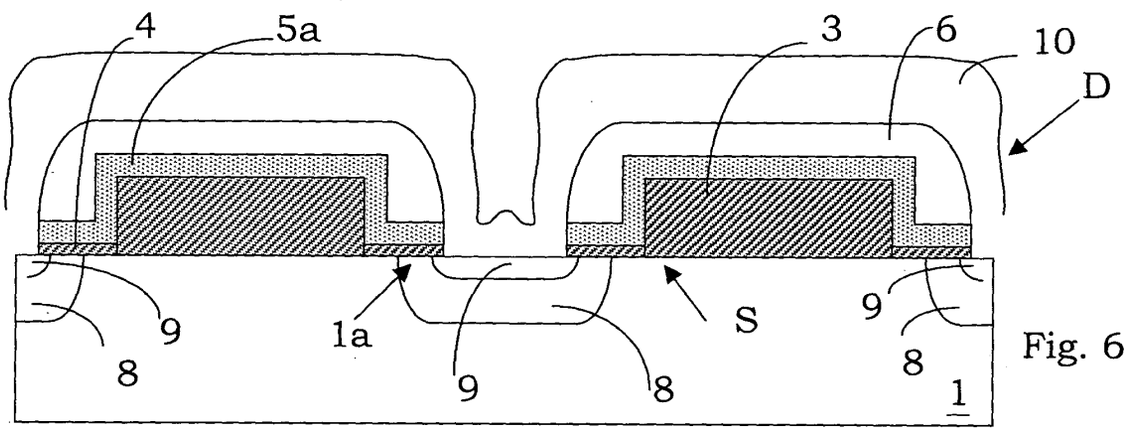

Fig. 6

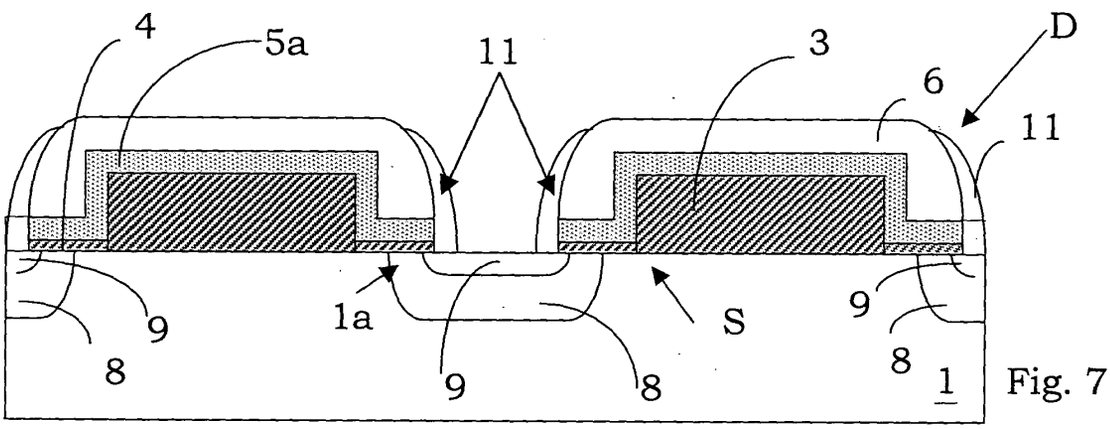

Fig. 7

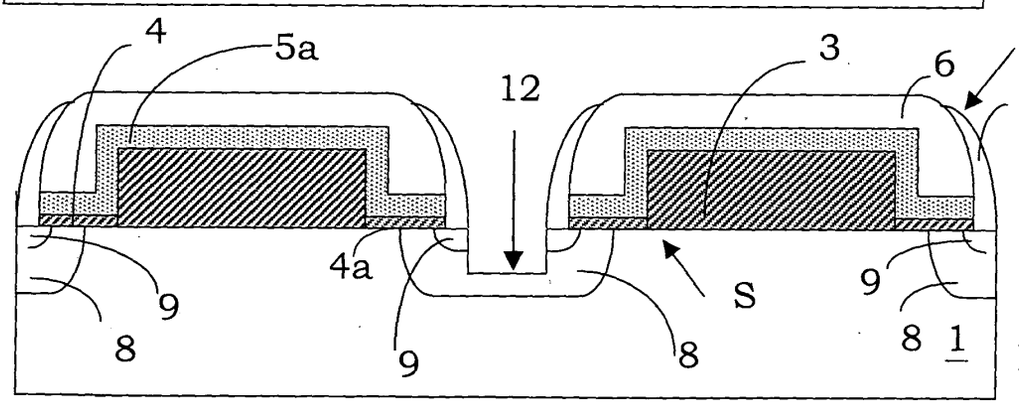

Fig. 8

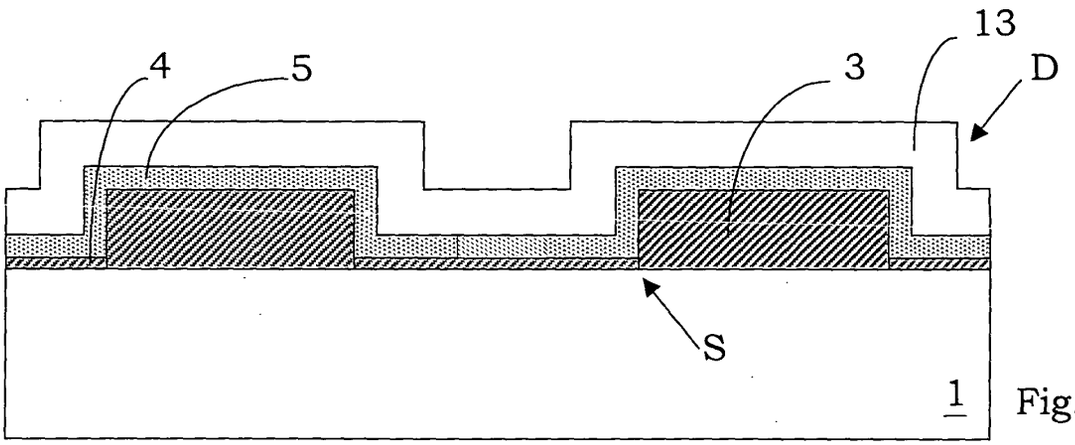

Fig. 9

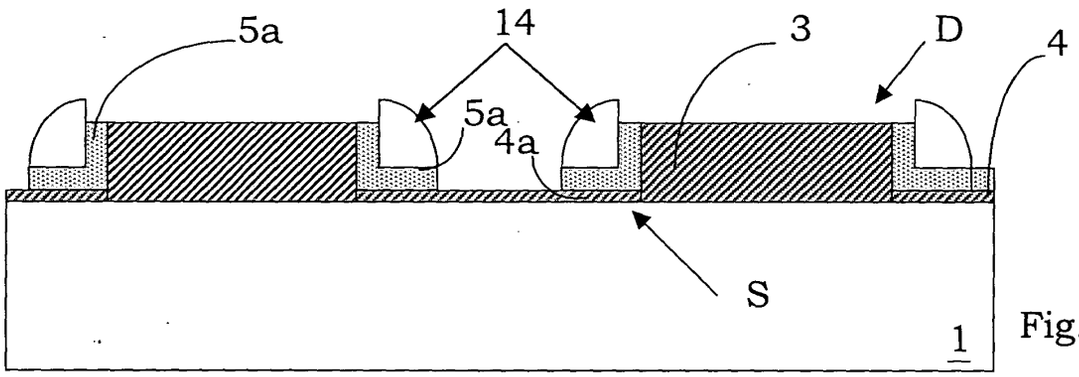

Fig. 10

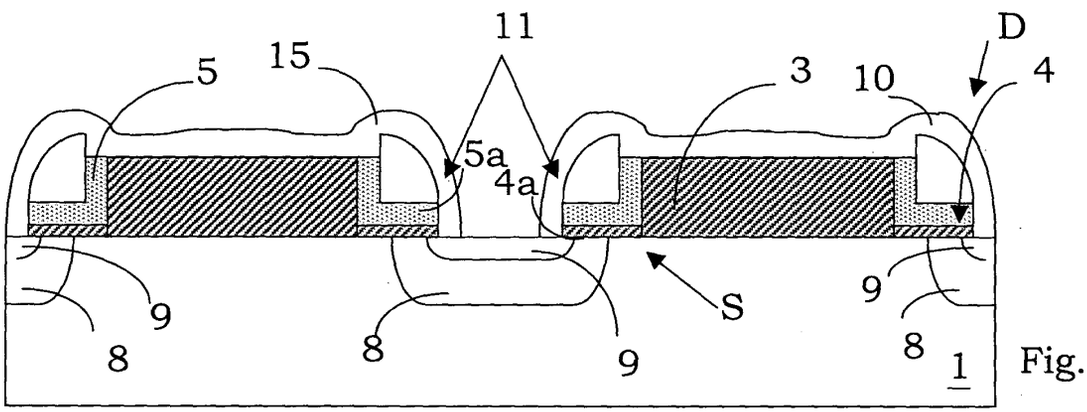

Fig. 11

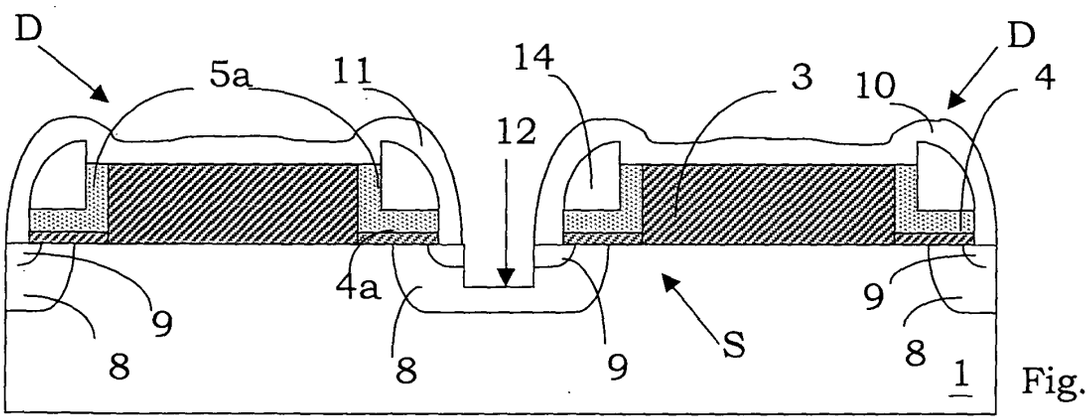

Fig. 12

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 03 42 5526

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
X	US 2002/140042 A1 (STOUT J) 3 October 2002 (2002-10-03)	11	H01L29/78 H01L29/423
A	* page 1, paragraph 0016 - page 2, paragraph 0035; figures 2,4,5-14 *	1,3,4, 6-8,10	H01L21/336 H01L29/739 H01L21/331

TECHNICAL FIELDS SEARCHED (Int.Cl.7)

H01L

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
MUNICH	27 January 2004	Morvan, D

CATEGORY OF CITED DOCUMENTS

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Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2002140042 A1	03-10-2002	NONE	

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