(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 1 529 645 B1

(12) **EUROPEAN PATENT SPECIFICATION**

(45) Date of publication and mention of the grant of the patent:
19.12.2007 Bulletin 2007/51

(51) Int Cl.:
B41J 2/175 *(2006.01)*

(21) Application number: **03024578.1**

(22) Date of filing: **28.10.2003**

(54) **Apparatus and method for determining status of inkjet print head identification circuit**

Anordnung und Verfahren zur Bestimmung des Zustands einer Tintenstrahldruckkopf-Identifizierungsschaltung

Dispositif et procédé pour déterminer l'état d'un circuit d'identification d'une tête d'impression à jet d'encre

(84) Designated Contracting States:
DE FR GB

(43) Date of publication of application:
11.05.2005 Bulletin 2005/19

(73) Proprietor: **International United Technology Co., Ltd.**
Chu-Pei City,
Hsin-Chu Hsien,
Taiwan R.O.C. (TW)

(72) Inventors:
- **Hung, Lieh Hu**
  Hsinchu City 300, R.O.C. (TW)
- **Chieh-Wen, Wang**
  Hsinchu, R.O.C. (TW)
- **Linyean, Lin**
  Dadu Township
  Taichung County 432, R.O.C (TW)

(74) Representative: **Becker Kurig Straus**
Patentanwälte
Bavariastrasse 7
80336 München (DE)

(56) References cited:
US-A1- 2003 030 687
US-B1- 6 179 401
US-B1- 6 325 483

EP 1 529 645 B1

Description

BACKGROUND OF THE INVENTION

Field of the Invention

[0001] This invention generally relates to an inkjet print head, and more particularly to a circuit and method for determining statuses of inkjet print head identification circuit.

Description of the Related Art

[0002] As the technology advances, more and more computer peripherals have been developed. Taking the inkjet printer as an example, to meet the different print requirements, several inkjet printers have been developed. Each inkjet printer has its specific inkjet print heads. The function of the inkjet print head is to spray the ink from the nozzle. There are two types of inkjet print heads - continuous and drop-on-demand type respectively - based on the different droplet ejection principles. To implement the different droplet ejection principles, each inkjet print head has its own structure, such as one inkjet print head for black ink and one inkjet print head for color ink, or inkjet print heads with different numbers of nozzles. For the purpose of identifying each inkjet print head, an identification code corresponding to the specific inkjet print head will be written into the print head. Hence, the inkjet printer can control the inkjet print head according to the identification code for printing works.

[0003] As mentioned above, the inkjet printer has to identify the type of the inkjet print head. Hence, an identification circuit is required in the inkjet print head for the inkjet printer to read the identification code. Techniques for increasing ink-jet pen identification information in an interconnect limited environment is e.g. disclosed in document US6325483. Document US6325483 discloses an inkjet print head in which multiple links with series resistors are connected to address select transistors and a sense line in a printhead encoding circuit. This arrangement provides an increased number of possible states, thereby increasing the amount of information which can be encoded for such purposes as pen identification. This identification circuit will be used when the inkjet print head is installed for the first time in the inkjet printer. After the inkjet printer identifies the inkjet print head, the identification circuit will not be used. Hence, the identification circuit will read the identification code via the signal lines for controlling the print head array circuit.

SUMMARY OF THE INVENTION

[0004] An object of the present invention is to provide a circuit for setting the value of a status bit in an identification circuit of an inkjet print head with the features of claim 1 and a method of setting the value of a status bit in an identification circuit of an inkjet print head with the features of claim 17. Advantageous embodiments of the present invention are disclosed in the dependent claims 2 to 16 and 18. The identification circuit can acquire the complete identification code without the limitation of the number of the signal lines. The circuit provided by the present invention is suitable for an inkjet print head with a plurality of signal lines, comprising: a status output terminal for outputting a one bit data of the status of the inkjet print head identification circuit; a first blowing terminal electrically coupled to the status output terminal via a first programmable switch; and a second blowing terminal electrically coupled to the status output terminal via a second programmable switch; and a switch circuit controlled by the signal lines for conducting an external power supply to program the first and second programmable switches.

[0005] In a preferred embodiment of the present invention, the switch circuit comprises: a first transistor, a first signal line of the plurality of signal lines determining whether to turn on/off the first transistor; and a second transistor, wherein when the first transistor is on, the voltage level of a second signal line of the plurality of signal lines determines whether to apply the external power supply to the first programmable switch and the second programmable switch. The first signal line may be or may not be the second signal line. The first and second switches include fuses or low-power resistor to store data bit 0 or 1 used for identification code output by inkjet print head.

[0006] In another embodiment of the present invention, the circuit further comprises a status input circuit having a third blowing terminal, the status input circuit being electrically coupled to the plurality of signal lines, the status input circuit being controlled by the plurality of signal lines to conduct the external power supply to the third blowing terminal. The status input circuit further comprises: a third transistor, a third signal line of the plurality of signal lines for determining whether to turn on/off the third transistor; and a fourth transistor, when the third transistor is on, the voltage level of a fourth signal line of the plurality of signal lines determines whether to apply the external power supply to the third blowing terminal. The third signal line may be or may not be the fourth signal line. The first, second, third and fourth signal lines can be the same signal line or different.

[0007] The present invention also provides a method of determining statuses of inkjet print head identification circuit, for an inkjet print head with a plurality of signal lines, comprising: enabling two of the plurality of signal lines to conduct an external power supply; and coupling the external power supply to a first programmable switch and a second programmable switch which are electrically coupled to different voltages respectively, to turn off one of the first programmable switch and a second programmable switch; wherein the plurality of signal lines are not enabled simultaneously when the inkjet print head operates.

[0008] In another embodiment of the present inven-

tion, the step of coupling the external power supply to the first programmable switch and the second programmable switch comprises: floating one terminal of one of the first programmable switch and the second programmable switch, and applying the external power supply to another terminal of the one of the first programmable switch and the second programmable switch; and grounding one terminal of another first programmable switch and the second programmable switch, and applying the external power supply to another terminal of the other first programmable switch and the second programmable switch; wherein the grounded first programmable switch and the second programmable switch is off due to a voltage difference between the one terminal and the another terminal.

[0009] The present invention uses a pair of fuses or low power resistors less than approximately 0.3W, or uses a fuse and a low power resistor less than approximately 0.3W. The status output terminal will output 1 or 0 based on which one of the fuses (or resistors, or a fuse and a resistor) is blown. The circuit provided by the present invention can be controlled by the signal line to determine which one of the fuses (or resistors, or a fuse and a resistor) is going to be blown, and receive the applied power supply to blow the fuse.

[0010] The above is a brief description of some deficiencies in the prior art and advantages of the present invention. Other features, advantages and embodiments of the invention will be apparent to those skilled in the art from the following description, accompanying drawings and appended claims. It is intended that the scope of the invention be limited by the claims and not by the preceding summary or the following detailed description.

BRIEF DESCRIPTION OF THE DRAWINGS

[0011] FIG. 1 is a block diagram of an identification system of an inkjet printer.

[0012] FIG. 2 is a conventional identification circuit of an inkjet print head.

[0013] FIG. 3 is another conventional identification circuit of an inkjet print head.

[0014] FIG. 4 is an explanatory figure depicting an explanatory identification circuit of an inkjet print head.

[0015] FIG. 5 is a timing sequence of the explanatory identification circuit of an explanatory inkjet print head of FIG. 4.

[0016] FIG. 6 is another explanatory figure depicting an explanatory identification circuit of an inkjet print head.

[0017] FIG. 7A is a circuit for determining the status of a one bit identification circuit of an inkjet print head in accordance with the first preferred embodiment of the present invention.

[0018] FIG. 7B is a circuit for determining the status of a one bit identification circuit of an inkjet print head in accordance with another preferred embodiment of the present invention.

[0019] FIG. 7C shows how the status output terminal 605 outputs one bit data of the status of the inkjet print head identification circuit to the corresponding input terminal 605''' of one-bit shift registers.

[0020] FIG. 8A is a circuit for determining the status of a one bit identification circuit of an inkjet print head in accordance with the second preferred embodiment of the present invention.

[0021] FIG. 8B shows the circuit of FIG. 8A connected to the circuit of FIG. 4.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0022] In the following description of the invention, reference is made to the accompanying drawings, which form a part thereof, and in which is shown by way of illustration a specific example whereby the invention may be practiced. It is to be understood that other embodiments may be utilized and structural changes may be made without departing from the scope of the present claims. Before illustrating the present invention, to make one skilled in the art understanding the present invention, the structure of the current inkjet print head is described. FIG. 1 is a block diagram of an identification system of an inkjet printer. As shown in FIG. 1, the identification system includes a printer electronic 110 connected to the signal lines 133 and the temperature sensing output line 136, and a print head electronic 120. The printer electronic 110 includes the controller 113 and the driving circuit 116. The print head electronic 120 includes the print head array 123, the identification circuit 126 and the temperature sensing circuit 129.

[0023] The identification circuit 126 can be the one that has been disclosed in U.S. Patent Number 5,363,134 (= EP 0 571 093) as shown in FIG. 2. The identification circuit 200 uses a plurality of fuses F1-F13 connected to the gates of a plurality of transistors Q1-Q13, respectively, to control the turning on of the transistors Q1-Q13. The identification code of the inkjet print head is stored by programming the fuses F1-F13. For example, assuming that the high level reading signal is sent via A13, if the fuse F13 is not blown, the transistor Q13 will be turned on. Hence, the temperature sensing output line 136 will be pulled to a low level and the data bit is "0". If the fuse F13 is blown, the transistor Q13 is turned off. Hence, the temperature sensing output line 136 will be pulled to high level and the data bit is "1". The other lines can also be read by the same way. However, each signal line of the identification circuit can only represent one bit. Hence, the number of bits for the identification code will be limited by the number of the signal lines.

[0024] To overcome this drawback, U.S. Patent Number 5,940,095 (= EP 0 765 762) discloses another identification circuit as shown in FIG. 3. The identification circuit 300 uses a plurality of one-bit mask programmed shift registers 320a - 320d to implement the parallel-in-series-out identification circuit. The printer electronic 110 sends the control signal "Load" via the signal line 305, and the identification code was stored into the one-bit

mask programmed shift registers 320a - 320d. Those shift registers are dynamic shift registers. When the first clock signal CLK1 and the second clock signal CLK2 are received via the signal lines 310 and 315, the data bit stored in the one-bit mask programmed shift register 320d will be shifted out via the signal line 330. The data bit stored in the one-bit mask programmed shift register 320c will be shifted out to the one-bit mask programmed shift register 320d. The data bit stored in the one-bit mask programmed shift register 320b will be shifted out to the one-bit mask programmed shift register 320c. The data bit stored in the one-bit mask programmed shift register 320a will be shifted out to the one-bit mask programmed shift register 320b. Then the printer electronic 110 sends the control signal "Load" via the signal line 305, and sends the signal CLK1 and the second clock signal CLK2 via the signal lines 310 and 315. Then the identification code stored in the one-bit mask programmed shift registers 320a - 320d will be serially outputted. Hence, this parallel-in-series-out identification circuit only requires three signal lines 305, 310, and 315 to read the identification code without the limitation of the number of the signal lines. It should be noted that this identification circuit is fabricated by mask programming. Hence the identification code is determined during the chip fabrication and cannot be changed later on.

[0025] FIG. 4 is an explanatory figure depicting an explanatory identification circuit of an inkjet print head. The explanatory identification circuit 420 includes the counter 410, OR logic unit 430, and the programmable unit 420 consisting of fuses. The identification circuit 420 only requires four signal lines including a reset signal line 401 for transmitting Reset signal, a first clock signal line 402 for transmitting CLK1 signal, a second clock signal line 403 for transmitting CLK2 signal, and an identification code signal line 405 for transmitting ID signal. Hence, this identification circuit can expand the bit number based on the identification code and will not be limited by the number of the signal lines.

[0026] The counter 410 is electrically coupled to the reset signal 401, the first clock signal line 402 and the second clock signal line 403. The counter 410 is an 8-bit counter with 8 output terminals b0-b7 for required number of identification codes. Each of output terminals b0-b7 is connected to the input terminals of the OR gate unit 430 via the fuses of the programmable unit 420. The input terminals of the OR gate unit 430 is electrically connected to the ground via the fuses of the programmable unit 420. Further, the OR gate unit 430 includes an enable terminal EN to receive the second clock signal CLK2. For example, if the identification code is 11101000, the fuses F10, F1 1, F12, F3, F14, F5, F6, and F7 have to be blown and the fuses F0, F1, F2, F13, F4, F15, F16, and F17 are kept intact, thereby programming the identification code into the programmable unit 420. The timing sequence is shown in FIG. 5.

[0027] When the counter 410 receives the reset signal Reset via the reset signal line 401, the counter 410 is reset to "0". When the counter receives the first and second clock signals CLK1 and CLK2 via the first and second clock signal line 402 and 403 respectively in sequence, the output terminals b0-b7 of the counter 410 will be set to "1" in sequence as shown in FIG. 5. When b0 is "1" and b1-b7 are "0", because the fuse F0 is intact when programming, the output terminal of the OR gate unit 430 will output the one bit data "1". Likewise, when b1 is "1" and the other output terminals are "0", because the fuse F1 is intact when programming, the output terminal of the OR gate unit 430 will output the one bit data "1"; when b2 is "1" and the other output terminals are "0", because the fuse F2 is intact when programming, the output terminal of the OR gate unit 430 will output the one bit data "1". When b3 is "1" and the other output terminals are "0", because the fuse F3 is blown when programming, the output terminal of the OR gate unit 430 will output the one bit data "0". Hence, the OR gate unit 430 can output the identification code 11101000 in sequence. The timing sequence is shown in FIG. 5.

[0028] FIG. 6 is another explanatory identification circuit of another explanatory inkjet print head. The identification circuit 700 includes a counter 710, a programmable unit 720 consisting of a plurality of fuses, and several NMOSFET switches 731-737.

[0029] The identification circuit 700 only requires three signal lines including a reset signal line 701 for transmitting Reset signal, a first clock signal line 702 for transmitting CLK1 signal, a second clock signal line 703 for transmitting CLK2 signal. The counter 710 is electrically coupled to the reset signal line 701, the first clock signal line 702 and the second clock signal line 703. The counter 710 is a 8-bit counter with 8 output terminals b0-b7 for required number of identification codes. Each of output terminals b0-b7 is connected to the gates of the switches 730-737 respectively to control the on/off of the switches 730-737. One of the source/drain of the switches 730-737 are connected to the power supply or ground via the fuses of the programmable unit 720 for inputting the identification code. The other source/drain of the switches 730-737 is connected to the identification code line to output the identification code.

[0030] For example, if the identification code is 11101000, the fuses F10, F11, F12, F3, F14, F5, F6, and F7 have to be blown and the fuses F0, F1, F2, F13, F4, F15, F16, and F17 are kept intact, thereby programming the identification code into the programmable unit 720. The timing sequence is shown in FIG. 5.

[0031] When the counter 710 receives the reset signal Reset via the reset signal line 701, the counter 710 is reset to "0". When the counter receives the first and second clock signals CLK1 and CLK2 via the first and second clock signal lines 702 and 703 respectively in sequence, the output terminals b0-b7 of the counter 710 will be set to "1" in sequence as shown in FIG. 5.

[0032] When b0 is "1" and b1-b7 are "0", because the fuse F0 is intact when programming, the switch 730 will be turned on and the one bit data "1" will be outputted.

Likewise, when b1 is "1" and the other output terminals are "0", because the fuse F1 is intact when programming, the switch 731 will be turned on and the one bit data "1" will be outputted; when b2 is "1" and the other output terminals are "0", because the fuse F2 is intact when programming, the switch 732 will be turned on and the one bit data "1" will be outputted. When b3 is "1" and the other output terminals are "0", because the fuse F3 is blown when programming, the switch 733 will be turned on and the one bit data "0" will be outputted. Hence, the identification code 11101000 will be outputted in sequence. The timing sequence is shown in FIG. 5.

[0033] In addition, Applicant also discloses several identification circuits in the European patent application (03250724.6).

First Embodiment

[0034] FIG. 7A is a circuit for determining the status of one bit identification circuit of an inkjet print head in accordance with the first preferred embodiment of the present invention. The circuit is applied to an inkjet print head as shown in FIG. 3 with a plurality of signal lines. The circuit comprises a status output terminal 605, a first blowing terminal 601, a second blowing terminal 603, and a switch circuit 620. The status output terminal 605 outputs one bit data of the status of the inkjet print head identification circuit to the corresponding input terminal 605''' of one-bit shift registers as exemplified in Fig. 7C. It is noted that the input terminal 605''' of one-bit shift registers can be inside or outside the one-bit shift registers. For practical application, it can be connected to a one-bit shift register 320a-320d to provide the predetermined output for the one-bit shift register. The first blowing terminal 601 is electrically coupled to the status output terminal 605 via a first programmable switch 610. The second blowing terminal 603 is electrically coupled to the status output terminal 605 via a second programmable switch 615. The switch circuit 620 is controlled by the signal lines to conduct an external power supply Pin to program the first programmable switch 610 and said second programmable switch 615. The external power supply Pin can be a voltage supply or a current supply.

[0035] In a preferred embodiment of the present invention, the switch circuit 620 comprises a first transistor 623 and a second transistor 626. The first signal line A_{n+1} determines whether to turn on/off the first transistor 623, and when the first transistor 623 is on, the voltage level of the second signal line A_{n+2} determines whether to apply the external power supply Pin to the first programmable switch 610 and the second programmable switch 615. The first programmable switch 610 and the second programmable switch 615 can be fuses or low power resistors as shown in FIG. 7B.

[0036] The method to implement the embodiment mentioned above comprises the steps as follows. First, two of the signal lines, such as A_{n+1}, and A_{n+2} will be enabled to conduct the external power supply Pin. Then the power supply Pin is used to program the first programmable switch 610 and the second programmable switch 615. By this step, one of the first programmable switch 610 and the second programmable switch 615 (such as a fuse or a low power resistor) will be blown. Hence, one of (a) the electrically connection between the first blowing terminal 601 and the status output terminal 605 and (b) the electrically connection between the second blowing terminal 603 and the status output terminal 605 is open. The first programmable switch 610 and the second programmable switch 615 are connected to the different voltage levels. To blow the second programmable switch 615, the second blowing terminal 603 connected to the second programmable switch 615 is connected to the ground and the other terminal of the second programmable switch 615 is connected to the power supply Pin. The first blowing terminal 601 connected to the first programmable switch 610 is floated, and the other terminal of the first programmable switch 610 is connected to the power supply Pin. Hence, because the second blowing terminal 603 is grounded, the second programmable switch 615 will be blown due to the voltage difference so that the connection between the second blowing terminal 603 and the status output terminal 605 is broken.

[0037] Likewise, to blow the first programmable switch 610, the first blowing terminal 601 connected to the first programmable switch 610 is connected to the ground and the other terminal of the first programmable switch 610 is connected to the power supply Pin. The second blowing terminal 603 connected to the second programmable switch 615 is floated, and the other terminal of the second programmable switch 615 is connected to the power supply Pin. Hence, because the first blowing terminal 601 is grounded, the first programmable switch 610 will be blown due to the voltage difference so that the connection between the first blowing terminal 601 and the status output terminal 605 is broken.

[0038] It should be noted that when the inkjet print head operates under normal condition, the first blowing terminal 601 is connected to the operational voltage V_{DD}, and the second blowing terminal 603 is connected to the ground. If the first programmable switch 610 is blown, the output is "0" as the one bit of the identification code. If the second programmable switch 615 is blown, the output is "1" as the one bit of the identification code.

Second Embodiment

[0039] The apparatus shown in FIGs. 7A and 7B can also be applied to the identification circuit of FIG. 6. The first programmable switch and the second programmable switch can be deemed a pair of fuses (e.g., F0 and F10, F1 and F11, F2 and F12, F3 and F13, F4 and F14, F5 and F15, F6 and F16, and F7 and F17) of FIG. 6. Taking F7 and F17 as an example, the status output terminal of FIG.7 is connected to the logic gate input terminal 605' of FIG. 6. The first programmable switch is F7, and the second programmable switch is F17. Hence, to blow one

of the fuses, it can be performed as follows: First, two of the signal lines, such as A_{n+1} and A_{n+2} will be enabled to conduct the external power supply Pin. Then the power supply Pin is used to program the first programmable switch 610 and the second programmable switch 615. By this step, one of the first programmable switch 610 and the second programmable switch 615 (such as a fuse or a low power resistor) will be blown. Hence, one of (a) the electrically connection between the first blowing terminal 601 and the status output terminal 605 and (b) the electrically connection between the second blowing terminal 603 and the status output terminal 605 is open. The first programmable switch 610 and the second programmable switch 615 are connected to the different voltage levels. To blow the second programmable switch 615, the second blowing terminal 603 connected to the second programmable switch 615 is connected to the ground and the other terminal of the second programmable switch 615 is connected to the power supply Pin. The first blowing terminal 601 connected to the first programmable switch 610 is floated, and the other terminal of the first programmable switch 610 is connected to the power supply Pin. Hence, because the second blowing terminal 603 is grounded, the second programmable switch 615 will be blown due to the voltage difference so that the connection between the second blowing terminal 603 and the status output terminal 605 is broken.

[0040] Likewise, to blow the first programmable switch 610, the first blowing terminal 601 connected to the first programmable switch is connected to the ground and the other terminal of the first programmable switch 610 is connected to the power supply Pin. The second blowing terminal 603 connected to the second programmable switch 615 is floated, and the other terminal of the second programmable switch 615 is connected to the power supply Pin. Hence, because the first blowing terminal 601 is grounded, the first programmable switch 610 will be blown due to the voltage difference so that the connection between the first blowing terminal 601 and the status output terminal 605 is broken.

[0041] When the inkjet print head operates under normal condition, the first blowing terminal 601 is connected to the operational voltage V_{DD}, and the second blowing terminal 603 is connected to the ground. If the first programmable switch 610 is blown, the output is "0" as the one bit of the identification code. If the second programmable switch 615 is blown, the output is "1" as the one bit of the identification code.

Third Embodiment

[0042] FIG. 8A is a circuit for determining the status of one bit identification circuit of an inkjet print head in accordance with the third preferred embodiment of the present invention. This circuit can be applied to the one-bit identification circuit of FIG. 4. Compared to the first embodiment, this embodiment further includes a status input circuit 630. The status input circuit 630 is controlled by the signal lines A_{n+3} and A_{n+4} to conduct the external power supply to the third blowing point 607. The status input circuit 630 includes a third transistor 633 and a fourth transistor 636. The third signal line A_{n+3} determines whether to turn on/off the third transistor 633. When the third transistor 633 is on, the voltage level of the fourth signal line A_{n+4}, determines whether to apply the external power supply to the third blowing terminal 607. The first, second, third, and fourth signal lines can be the same signal line or different signal lines.

[0043] FIG. 8B shows the circuit of FIG. 8A connected to the circuit of FIG. 4, wherein the status output terminal 605 is coupled to the corresponding input terminal 605"of the OR gate

[0044] To blow one of the first and second programmable switches 610, 615, first, two of the signal lines, such as A_{n+1} and A_{n+2} will be enabled to conduct the external power supply Pin. Then the power supply Pin is used to program the first programmable switch 610 and the second programmable switch 615. By this step, one of the first programmable switch 610 and the second programmable switch 615 (such as a fuse or a low power resistor) will be blown. Hence, one of (a) the electrically connection between the second blowing terminal 603 and the status output terminal 605 and (b) the electrically connection between the third blowing terminal 607 and the status output terminal 605 is open. The first programmable switch 610 and the second programmable switch 615 are connected to the different voltage levels. To blow the second programmable switch 615, the second blowing terminal 603 connected to the second programmable switch 615 is connected to the ground and the other terminal of the second programmable switch 615 connected to the power supply Pin. The third blowing terminal 607 connected to the first programmable switch 610 is floated, and the other terminal of the first programmable switch 610 is connected to the power supply Pin. Hence, because the second blowing terminal 603 is grounded, the second programmable switch 615 will be blown due to the voltage difference so that the connection between the second blowing terminal 603 and the status output terminal 605 is broken.

[0045] Likewise, to blow the first programmable switch 610, the third blowing terminal 607 connected to the first programmable switch 610 is connected to the ground and the other terminal of the first programmable switch 610 is connected to the power supply Pin. The second blowing terminal 603 connected to the second programmable switch 615 is floated, and the other terminal of the second programmable switch 615 is connected to the power supply Pin. Hence, because the first blowing terminal 601 is grounded, the first programmable switch 610 will be blown due to the voltage difference so that the connection between the third blowing terminal 607 and the status output terminal 605 is broken.

[0046] It should be noted when the inkjet print head operates under normal condition, the third blowing terminal 607 is floated and the second blowing terminal is

connected to the ground. If the first programmable switch 610 is blown, the output is "0" as the one bit of the identification code. If the second programmable switch 615 is blown, the status output terminal 605 is electrically coupled to the output terminals b0-b7 of the counter so that the voltage level of the status output terminal 605 is the same as the output terminals b0-b7 of the counter.

[0047] Further, when the printer prints the works, no more than two signal lines will be enabled. Only when blowing the fuses and storing the identification code, more than two signal lines can be enabled.

[0048] The present invention uses a pair of fuses or low power resistors approximately less than 0.3W, or uses a fuse and a low power resistor approximately less than 0.3W. The status output terminal 605 will output 1 or 0 based on which one of the fuses (or resistors, or a fuse and a resistor) is blown by applying an external power supply Pin. The identification circuit of the present invention is programmable by inputting signals and external power supply for blowing the fuse. The identification circuit of the present invention uses programmable fuses or low power resistors to change the identification code. Hence, it provides flexibility by using the existent signal line pins to blow the fuses without additional pins. Hence the present invention can be used for mass production because it is much simpler than the conventional identification circuit.

[0049] The foregoing description of the preferred embodiment of the present invention has been presented for purposes of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise form or to exemplary embodiments disclosed. Accordingly, the foregoing description should be regarded as illustrative rather than restrictive. Obviously, many modifications and variations will be apparent to practitioners skilled in this art. Similarly, any process steps described might be interchangeable with other steps in order to achieve the same result. The embodiment was chosen and described in order to best explain the principles of the invention and its best mode practical application, thereby to enable others skilled in the art to understand the invention for various embodiments and with various modifications as are suited to the particular use or implementation contemplated. It is intended that the scope of the invention be defined by the claims appended hereto. It should be appreciated that variations may be made in the embodiments described by workers skilled in the art without departing from the scope of the present invention as defined by the following claims. Moreover, no element, component, nor method step in the present disclosure is intended to be dedicated to the public regardless of whether the element, component, or method step is explicitly recited in the following claims.

Claims

1. A circuit for setting the value of a status bit in an identification circuit of an inkjet print head with a plurality of signal lines, wherein said identification circuit has at least one input terminal (605"'), comprising:

a status output terminal (605), outputting one bit data of said status of said inkjet print head identification circuit to said at least one input terminal (605"') corresponding to said status output terminal (605);

a first blowing terminal (601), electrically coupled to said status output terminal (605) via a first programmable switch (610), connected to a logic high voltage and transmitting the logic high voltage to said status output terminal (605) when said circuit outputs said one bit data and when the first programmable switch (610) is on; and

a second blowing terminal (603), electrically coupled to said status output terminal (605) via a second programmable switch (615), connected to a logic low voltage and transmitting the logic low voltage to said status output terminal (605) when said circuit outputs said one bit data and when the second programmable switch (615) is on;

wherein one of said first programmable switch (610) and said second programmable switch (615) being off to set the logic high or low voltage level of said status output terminal,

wherein when the first programmable switch (610) and the second programmable switch (615) are being programmed, a programming voltage is applied to the first programmable switch (610) and the second programmable switch (615) and one of said first programmable switch (610) and said second programmable switch (615) is set to be off.

2. The circuit of claim 1, further comprising a switch circuit (620), controlled by said plurality of said signal lines, conducting an external power supply (Pin) to program said first programmable switch (610) and said second programmable switch (615).

3. The circuit of claim 2, wherein said switch circuit (620) comprises: a first transistor (623), a first signal line (A_{n+1}) of said plurality of signal lines determining whether to turn on/off said first transistor (623); and a second transistor (626), wherein when said first transistor (623) is on, the voltage level of a second signal line (A_{n+2}) of said plurality of signal lines determines whether to apply said external power supply (Pin) to said first programmable switch (610) and said second programmable switch (615).

4. The circuit of claim 3, wherein said first signal lineis and said second signal line transmits the same signal.

5. The circuit of claim 1, wherein said first and second programmable switches include fuses.

6. The circuit of claim 1, further comprising a status input circuit (630) having a third blowing terminal (607), said status input circuit (630) being electrically coupled to said plurality of signal lines, said status input circuit (630) being controlled by said plurality of signal lines to conduct said external power supply (Pin) to said third blowing terminal (607).

7. The circuit of claim 6, wherein said status input circuit (630) further comprises:

a third transistor (633), a third signal line (A_{n+3}) of said plurality of signal lines determining whether to turn on/off said third transistor (633); and
a fourth transistor (636), wherein when said third transistor (633) is on, the voltage level of a fourth signal line (A_{n+4}) of said plurality of signal lines determines whether to apply said external power supply (Pin) to said third blowing terminal (607).

8. The circuit of claim 7, wherein said third signal line-4s and said fourth signal line transmits the same signal.

9. The circuit of claim 3, further comprising a status input circuit having a third blowing terminal, said status input circuit being electrically coupled to said plurality of signal lines, said status input circuit being controlled by said plurality of signal lines to conduct said external power supply to said third blowing terminal.

10. The circuit of claim 9, wherein said status input circuit further comprises:

a third transistor, a third signal line of said plurality of signal lines determining whether to turn on/off said third transistor; and
a fourth transistor, wherein when said third transistor is on, the voltage level of a fourth signal line of said plurality of signal lines determines whether to apply said external power supply to said third blowing terminal.

11. The circuit of claim 10, wherein said first, second, third, and fourth signal lines transmits the same signal.

12. Combination of the circuit of claim 1 and the identification circuit, wherein said identification circuit of said inkjet print head includes a shift register.

13. Combination of the circuit of claim 1 and the identification circuit, wherein said identification circuit of said inkjet print head includes a counter.

14. The circuit of claim 13, wherein said identification circuit of said inkjet print head includes a logic gate.

15. The circuit of claim 1, wherein said first programmable switch and said second programmable switch include resistors.

16. The circuit of claim 1, wherein one of said first programmable switch and said second programmable switch is a resistor.

17. A method of setting the value of a status bit in an identification circuit of an inkjet print head with a plurality of signal lines, comprising:

enabling two of said plurality of signal lines to conduct an external power supply; and
coupling said external power supply to a first programmable switch and a second programmable switch to blow one of said first programmable switch and said second programmable switch;

wherein said plurality of signal lines are not enabled simultaneously when said inkjet print head operates, and the status is sent to said identification circuit via one of said first and second programmable switch by supplying a logic high voltage to said first programmable switch and a logic low voltage to said second programmable switch.

18. The method of claim 17, wherein said step of coupling said external power supply to said first programmable switch and said second programmable switch comprises:

grounding one terminal of said first programmable switch and applying said external power supply to another terminal of said first programmable switch when said first programmable switch is to be turned off; and
grounding one terminal of said second programmable switch and applying said external power supply to another terminal of said second programmable switch when said second programmable switch is to be turned off.

Patentansprüche

1. Schaltung zum Setzen eines Wertes eines Zustandsbits in einer Identifikationsschaltung eines Tintenstrahl-Druckkopfs mit einer Vielzahl von Signalleitungen, wobei die Identifikationsschaltung mindestens eine Eingabe-Endstelle (605''') aufweist, umfassend:

eine Zustandsausgabe-Endstelle (605), die einen Bit-Wert des Zustands der Tintenstrahl-Druckkopf-Identifikationsschaltung an die mindestens eine Eingabe-Endstelle (605"') entsprechend der Zustandsausgabe-Endstelle (605) ausgibt;
eine erste Zerstör-Endstelle (601), die elektrisch an die Zustandsausgabe-Endstelle (605) über einen ersten programmierbaren Schalter (610) gekoppelt ist, der mit einer logischen Hochspannung verbunden ist und die logische Hochspannung an die Zustandsausgabe-Endstelle (605) überträgt, wenn die Schaltung den einen Bit-Wert ausgibt und wenn der erste programmierbare Schalter (610) eingeschaltet ist; und
eine zweite Zerstör-Endstelle (603), die elektrisch an die Zustandsausgabe-Endstelle (605) über einen zweiten programmierbaren Schalter (615) gekoppelt ist, der mit einer logischen Niederspannung verbunden ist und die logische Niederspannung an die Zustandsausgabe-Endstelle (605) überträgt, wenn die Schaltung den einen Bit-Wert ausgibt und wenn der zweite programmierbare Schalter (615) eingeschaltet ist;

wobei entweder der erste programmierbare Schalter (610) oder der zweite programmierbare Schalter (615) ausgeschaltet ist, um das logische Hoch- oder Niederspannungsniveau der Zustandsausgabe-Endstelle festzusetzen,
wobei eine Programmierspannung an den ersten programmierbaren Schalter (610) und den zweiten programmierbaren Schalter (615) angelegt wird, wenn der erste programmierbare Schalter (610) und der zweite programmierbare Schalter (615) programmiert werden, und es wird festgesetzt, dass entweder der erste programmierbare Schalter (610) oder der zweite programmierbare Schalter (615) ausgeschaltet ist.

2. Schaltung gemäß Anspruch 1 weiter umfassend eine Schalterschaltung (620), die durch die Vielzahl von Signalleitungen gesteuert wird, die eine externe Stromversorgung (Pin) leiten, um den ersten programmierbaren Schalter (610) und den zweiten programmierbaren Schalter (615) zu programmieren.

3. Schaltung gemäß Anspruch 2, wobei die Schalterschaltung (620) umfasst:

einen ersten Transistor (623),
eine erste Signalleitung (A_{n+1}) der Vielzahl von Signalleitungen, die bestimmen, ob der erste Transistor (623) ein- oder ausgeschaltet werden soll; und
einen zweiten Transistor (626), wobei wenn der erste Transistor (623) eingeschaltet ist, das Spannungsniveau der zweiten Signalleitung (A_{n+2}) der Vielzahl von Signalleitungen bestimmt, ob die externe Stromversorgung (Pin) an den ersten programmierbaren Schalter (610) und den zweiten programmierbaren Schalter (615) angelegt wird.

4. Schaltung gemäß Anspruch 3, wobei die erste Signalleitung und die zweite Signalleitung das gleiche Signal übertragen.

5. Schaltung gemäß Anspruch 1, wobei die ersten und zweiten programmierbaren Schalter Sicherungen beinhalten.

6. Schaltung gemäß Anspruch 1 weiter umfassend eine Zustandseingabeschaltung (630) mit einer dritten Zerstör-Endstelle (607), wobei die Zustandseingabeschaltung (630) elektrisch an die Vielzahl der Signalleitungen gekoppelt ist, wobei die Zustandseingabeschaltung (630) durch die Vielzahl von Signalleitungen gesteuert wird, um die externe Stromversorgung (Pin) an die dritte Zerstör-Endstelle (607) zu leiten.

7. Schaltung gemäß Anspruch 6, wobei die Zustandseingabeschaltung (630) weiter umfasst:

einen dritten Transistor (633),
eine dritte Signalleitung (A_{n+3}) der Vielzahl von Signalleitungen, die bestimmen, ob der dritte Transistor (633) ein- oder ausgeschaltet werden soll; und
einen vierten Transistor (636), wobei wenn der dritte Transistor (633) eingeschaltet ist, das Spannungsniveau der vierten Signalleitung (A_{n+4}) der Vielzahl von Signalleitungen bestimmt, ob die externe Stromversorgung (Pin) an die dritte Zerstör-Endstelle (607) angelegt wird.

8. Schaltung gemäß Anspruch 7, wobei die dritte Signalleitung und die vierte Signalleitung das gleiche Signal übertragen.

9. Schaltung gemäß Anspruch 3 weiter umfassend eine Zustandseingabeschaltung mit einer dritten Zerstör-Endstelle, wobei die Zustandseingabeschaltung elektrisch an die Vielzahl der Signalleitungen gekoppelt ist, wobei die Zustandseingabeschaltung durch die Vielzahl von Signalleitungen gesteuert wird, um die externe Stromversorgung an die dritte Zerstör-Endstelle zu leiten.

10. Schaltung gemäß Anspruch 9 weiter umfassend:

einen dritten Transistor,
eine dritte Signalleitung der Vielzahl von Signalleitungen, die bestimmen, ob der dritte Transi-

stor ein- oder ausgeschaltet werden soll; und
einen vierten Transistor, wobei wenn der dritte Transistor eingeschaltet ist, das Spannungsniveau der vierten Signalleitung der Vielzahl von Signalleitungen bestimmt, ob die externe Stromversorgung an die dritte Zerstör-Endstelle angelegt wird.

11. Schaltung gemäß Anspruch 10, wobei die erste, zweite, dritte und vierte Signalleitung das gleiche Signal übertragen.

12. Kombination der Schaltung aus Anspruch 1 und der Identifikationsschaltung, wobei die Identifikationsschaltung des Tintenstrahl-Druckkopfes ein Schieberegister beinhaltet.

13. Kombination der Schaltung aus Anspruch 1 und der Identifikationsschaltung, wobei die Identifikationsschaltung des Tintenstrahl-Druckkopfes einen Zähler beinhaltet.

14. Schaltung gemäß Anspruch 13, wobei die Identifikationsschaltung des Tintenstrahl-Druckkopfes ein logisches Gate beinhaltet.

15. Schaltung gemäß Anspruch 1, wobei der erste programmierbare Schalter und der zweite programmierbare Schalter Widerstände beinhalten.

16. Schaltung gemäß Anspruch 1 wobei der erste programmierbare Schalter und der zweite programmierbare Schalter ein Widerstand ist.

17. Verfahren zum Setzen eines Wertes eines Zustandsbits in einer Identifikationsschaltung eines Tintenstrahl-Druckkopfs mit einer Vielzahl von Signalleitungen, umfassend:

Ermöglichen zweier der Vielzahl von Signalleitungen eine externe Stromversorgung zu leiten, und
Koppeln der externen Stromversorgung an einen ersten programmierbaren Schalter und einen zweiten programmierbaren Schalter, um entweder den ersten programmierbaren Schalter oder den zweiten programmierbaren Schalter zu zerstören,

wobei die Vielzahl von Signalleitungen nicht gleichzeitig eingeschaltet werden, wenn der Tintenstrahl-Druckkopf in Betrieb ist, und der Zustand an die Identifikationsschaltung über entweder den ersten oder zweiten programmierbaren Schalter durch Anlegen einer logischen Hochspannung an den ersten programmierbaren Schalter und einer logischen Niederspannung an den zweiten programmierbaren Schalter gesendet wird.

18. Verfahren gemäß Anspruch 17, wobei der Schritt des Koppelns der externen Stromversorgung an den ersten programmierbaren Schalter und den zweiten programmierbaren Schalter umfasst:

Erden einer Endstelle des ersten programmierbaren Schalters und Anlegen der externen Stromversorgung an eine andere Endstelle des ersten programmierbaren Schalters, wenn der erste programmierbare Schalter ausgeschaltet werden soll; und
Erden einer Endstelle des zweiten programmierbaren Schalters und Anlegen der externen Stromversorgung an eine andere Endstelle des zweiten programmierbaren Schalters, wenn der zweite programmierbare Schalter ausgeschaltet werden soll.

Revendications

1. Circuit en vue de régler la valeur d'un bit d'état dans un circuit d'identification d'une tête d'impression à jet d'encre avec une pluralité de lignes de signaux, dans lequel ledit circuit d'identification présente au moins un terminal d'entrée (605"), comportant :

un terminal de sortie d'état (605), générant des données de un bit dudit état dudit circuit d'identification de tête d'impression à jet d'encre audit au moins un terminal d'entrée (605"') correspondant audit terminal de sortie d'état (605) ;
un premier terminal de commutation (601), couplé électriquement audit terminal de sortie d'état (605) par l'intermédiaire d'un premier commutateur programmable (610), connecté à une tension de logique élevée et transmettant la tension de logique élevée audit terminal de sortie d'état (605) lorsque ledit circuit génère lesdites données de un bit et lorsque le premier commutateur programmable (610) est sous tension ; et
un second terminal de commutation (603), couplé électriquement audit terminal de sortie d'état (605) par l'intermédiaire d'un second commutateur programmable (615), connecté à une tension de logique basse et transmettant la tension de logique basse audit terminal de sortie d'état (605) lorsque ledit circuit génère lesdites données de un bit et lorsque le second commutateur programmable (610) est sous tension ;

dans lequel l'un parmi lesdits premier commutateur programmable (610) et second commutateur programmable (615) est hors tension en vue d'établir le niveau de tension de logique élevé ou bas dudit terminal de sortie d'état,
dans lequel lorsque le premier commutateur programmable (610) et le second commutateur pro-

grammable (615) sont en programmation, une tension de programmation est appliquée au premier commutateur programmable (610) et au second commutateur programmable (615) et l'un parmi lesdits premier commutateur programmable (610) et second commutateur programmable (615) est réglé pour être hors tension.

2. Circuit selon la revendication 1, comportant en outre un circuit de commutation (620), commandé par ladite pluralité desdites lignes de signaux, pilotant une alimentation électrique externe (Pin) pour programmer ledit premier commutateur programmable (610) et ledit second commutateur programmable (615).

3. Circuit selon la revendication 2, dans lequel ledit circuit de commutation (620) comporte : un premier transistor (623), une première ligne de signaux (A_{n+1}) de ladite pluralité de lignes de signaux déterminant s'il est nécessaire de mettre sous tension ou hors tension ledit premier transistor (623) ; et un second transistor (626), dans lequel lorsque ledit premier transistor (623) est sous tension, le niveau de tension d'une seconde ligne de signaux (A_{n+2}) de ladite pluralité de lignes de signaux détermine s'il est nécessaire d'appliquer ladite alimentation électrique externe (Pin) audit premier commutateur programmable (610) et audit second commutateur programmable (615).

4. Circuit selon la revendication 3, dans lequel ladite première ligne de signaux et ladite seconde ligne de signaux transmettent le même signal.

5. Circuit selon la revendication 1, dans lequel lesdits premier et second commutateurs programmables comportent des fusibles.

6. Circuit selon la revendication 1, comportant en outre un circuit d'entrée d'état (630) présentant un troisième terminal de soufflage (607), ledit circuit d'entrée d'état (630) étant électriquement couplé à ladite pluralité de lignes de signaux, ledit circuit d'entrée d'état (630) étant commandé par ladite pluralité de lignes de signaux pour piloter ladite alimentation électrique externe (Pin) audit troisième terminal de soufflage (607).

7. Circuit selon la revendication 6, dans lequel ledit circuit d'entrée d'état (630) comporte en outre :

un troisième transistor (633), une troisième ligne de signaux (A_{n+3}) de ladite pluralité de lignes de signaux déterminant s'il est nécessaire de mettre sous tension ou hors tension ledit troisième transistor (633) ; et
un quatrième transistor (636), dans lequel lorsque ledit troisième transistor (633) est sous tension, le niveau de tension d'une quatrième ligne de signaux (A_{n+4}) de ladite pluralité de lignes de signaux détermine s'il est nécessaire d'appliquer ladite alimentation électrique externe (Pin) audit troisième terminal de soufflage (607).

8. Circuit selon la revendication 7, dans lequel ladite troisième ligne de signaux et ladite quatrième ligne de signaux transmettent le même signal.

9. Circuit selon la revendication 3, comportant en outre un circuit d'entrée d'état ayant un troisième terminal de soufflage, ledit circuit d'entrée d'état étant électriquement couplé à ladite pluralité de lignes de signaux, ledit circuit d'entrée d'état étant commandé par ladite pluralité de lignes de signaux pour piloter ladite alimentation électrique externe audit troisième terminal de soufflage.

10. Circuit selon la revendication 9, dans lequel ledit circuit d'entrée d'état comporte en outre :

un troisième transistor, une troisième ligne de signaux de ladite pluralité de lignes de signaux déterminant s'il est nécessaire de mettre sous tension ou hors tension ledit troisième transistor ; et
un quatrième transistor, dans lequel lorsque ledit troisième transistor est sous tension, le niveau de tension d'une quatrième ligne de signaux de ladite pluralité de lignes de signaux détermine s'il est nécessaire d'appliquer ladite alimentation électrique externe audit troisième terminal de soufflage.

11. Circuit selon la revendication 10, dans lequel lesdites première, deuxième, troisième, et quatrième lignes de signaux transmettent le même signal.

12. Combinaison du circuit selon la revendication 1 et du circuit d'identification, dans lequel ledit circuit d'identification de ladite tête d'impression à jet d'encre inclut un registre à décalage.

13. Combinaison du circuit selon la revendication 1 et du circuit d'identification, dans lequel ledit circuit d'identification de ladite tête d'impression à jet d'encre inclut un compteur.

14. Circuit selon la revendication 13, dans lequel ledit circuit d'identification de ladite tête d'impression à jet d'encre inclut une porte logique.

15. Circuit selon la revendication 1, dans lequel ledit premier commutateur programmable et ledit second commutateur programmable incluent des résistances.

16. Circuit selon la revendication 1, dans lequel l'un desdits premier commutateur programmable et second commutateur programmable est une résistance.

17. Procédé de réglage de la valeur d'un bit d'état dans un circuit d'identification d'une tête d'impression à jet d'encre avec une pluralité de lignes de signaux, comportant les étapes consistant à :

activer deux de ladite pluralité de lignes de signaux pour piloter une alimentation électrique externe ; et
coupler ladite alimentation électrique externe à un premier commutateur programmable et à un second commutateur programmable pour commuter l'un parmi lesdits premier commutateur programmable et second commutateur programmable ;

dans lequel lesdites lignes de ladite pluralité de lignes de signaux ne sont pas activées simultanément lorsque ladite tête d'impression à jet d'encre fonctionne, et l'état est transmis audit circuit d'identification par l'intermédiaire de l'un parmi lesdits premier et second commutateurs programmables en délivrant une tension de logique élevée audit premier commutateur programmable et une tension de logique basse audit second commutateur programmable.

18. Procédé selon la revendication 17, dans lequel ladite étape de couplage de ladite alimentation électrique externe audit premier commutateur programmable et audit second commutateur programmable comporte les étapes consistant à :

mettre à la terre un terminal dudit premier commutateur programmable et appliquer ladite alimentation électrique externe à un autre terminal dudit premier commutateur programmable lorsque ledit premier commutateur programmable doit être mis hors tension ; et
mettre à la terre un terminal dudit second commutateur programmable et appliquer ladite alimentation électrique externe à un autre terminal dudit second commutateur programmable lorsque ledit second commutateur programmable doit être mis hors tension.

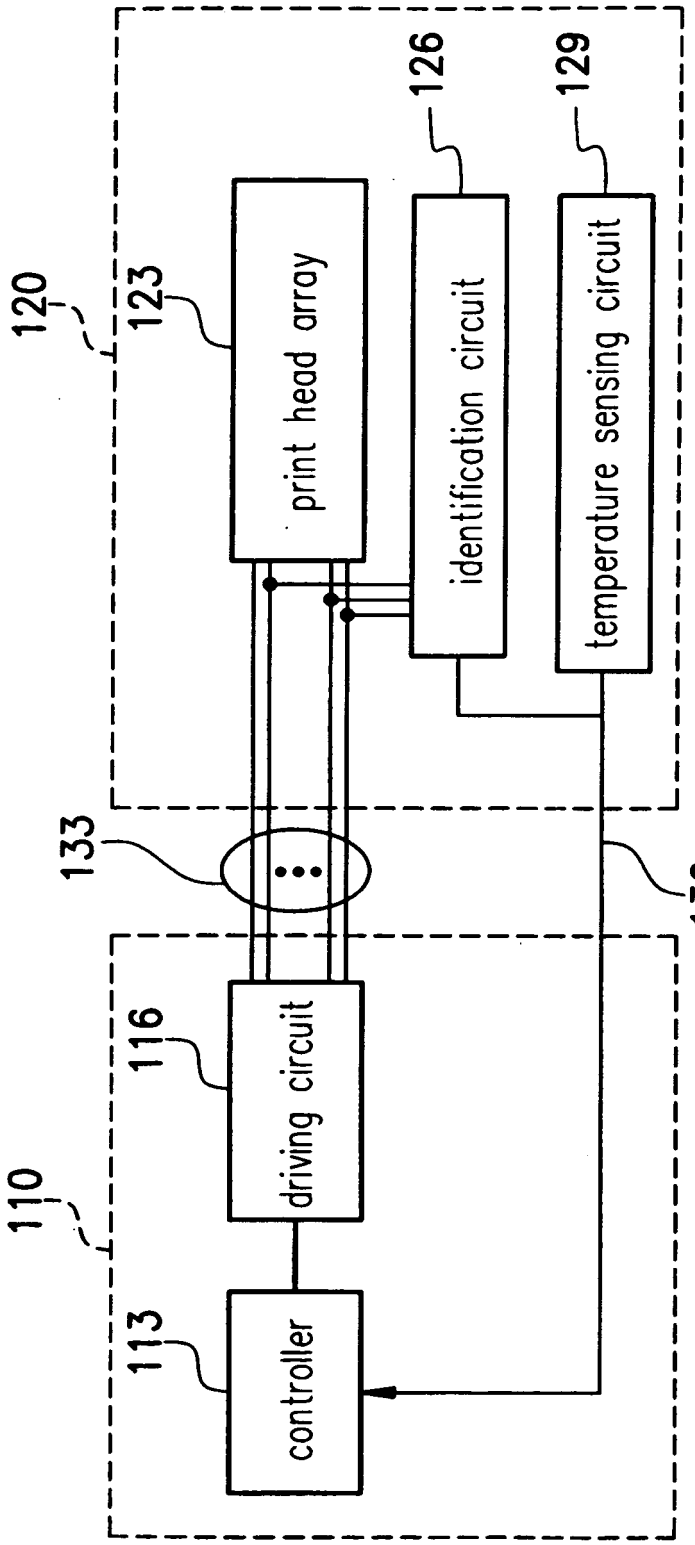

FIG. 1 (PRIOR ART)

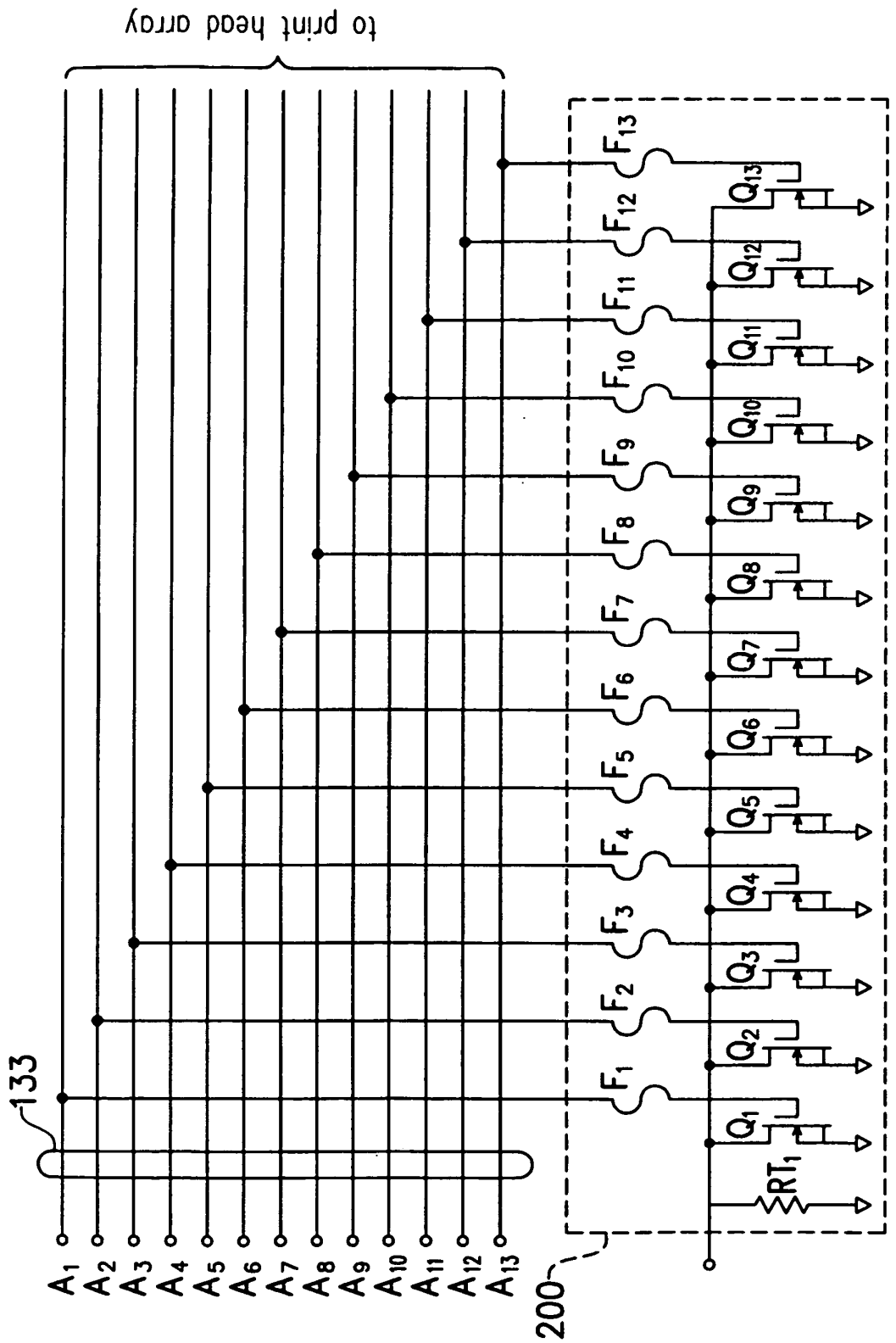

FIG. 2 (PRIOR ART)

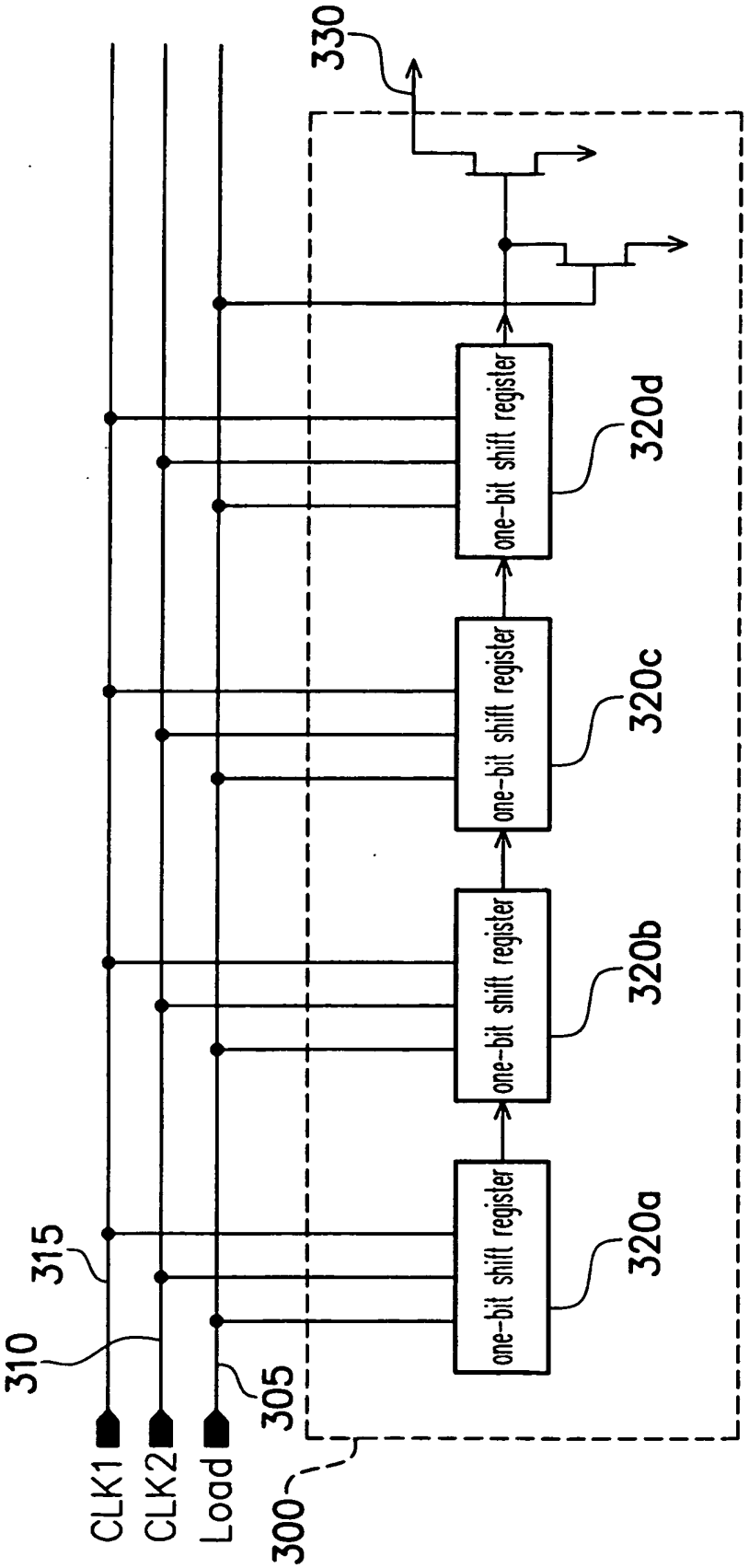

FIG. 3 (PRIOR ART)

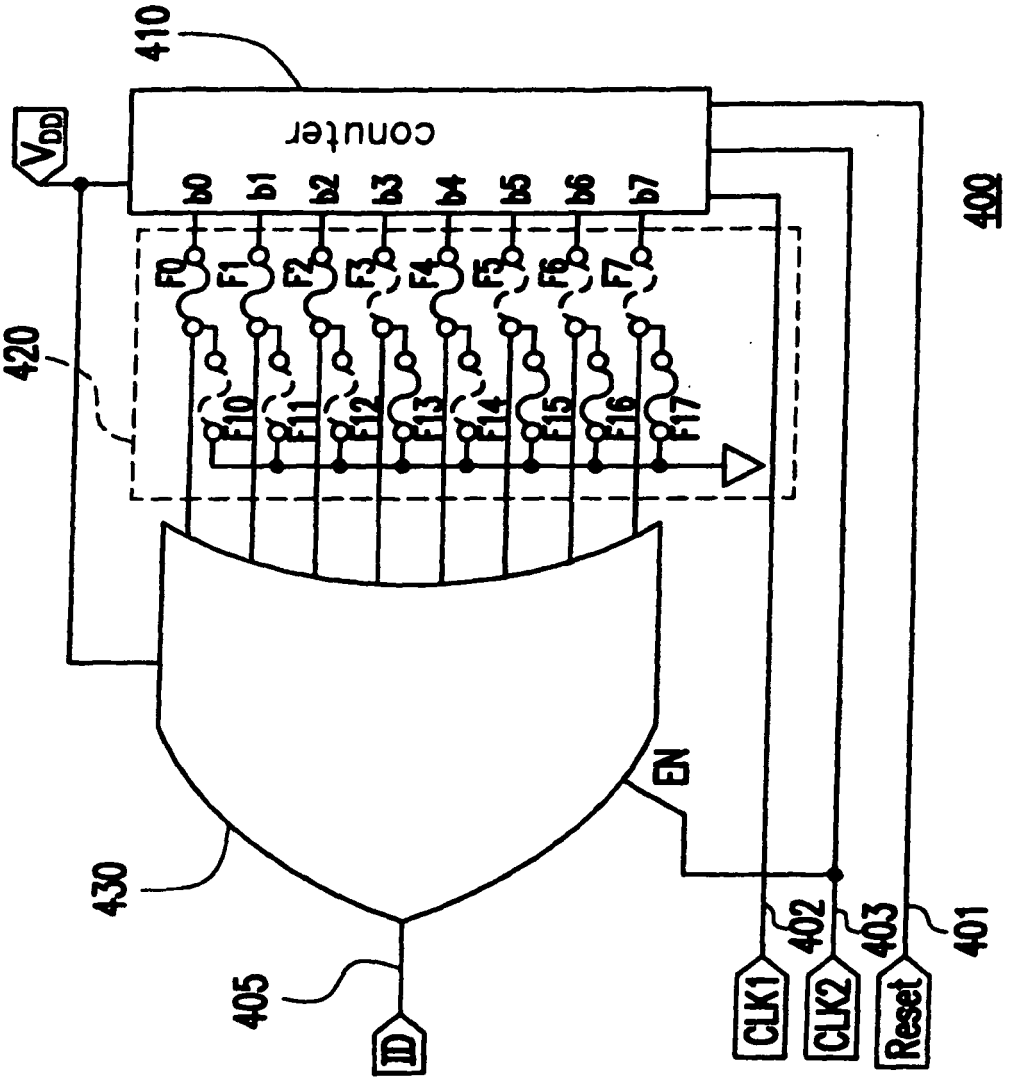

FIG. 4 (EXPLANATORY)

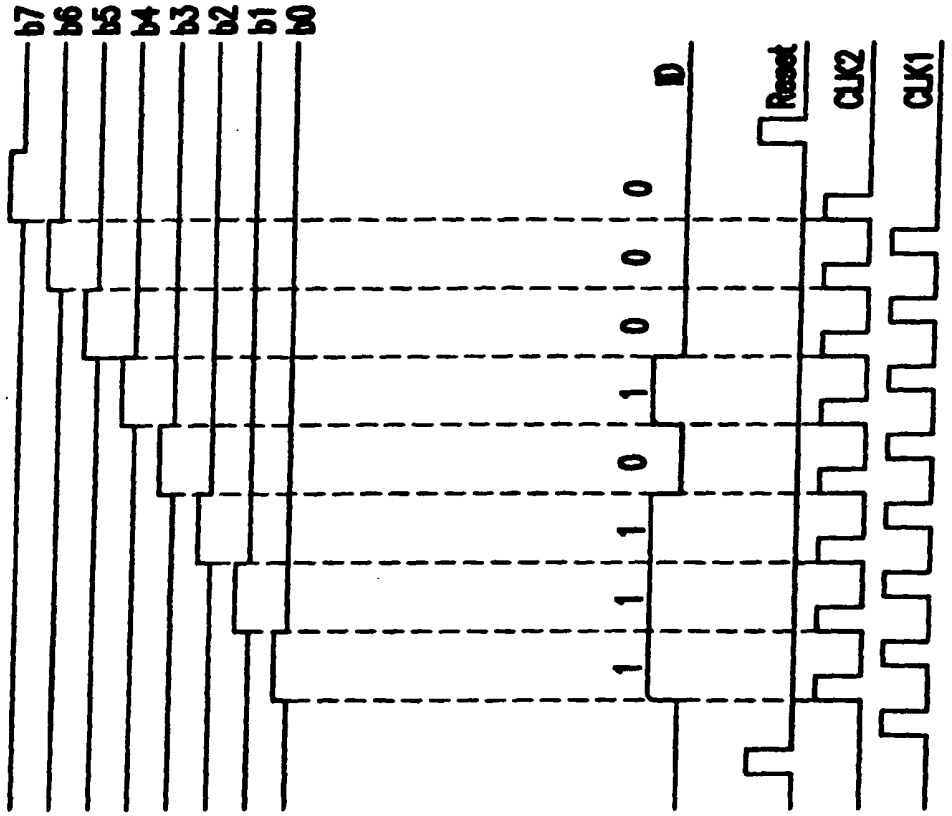

FIG. 5 (EXPLANATORY)

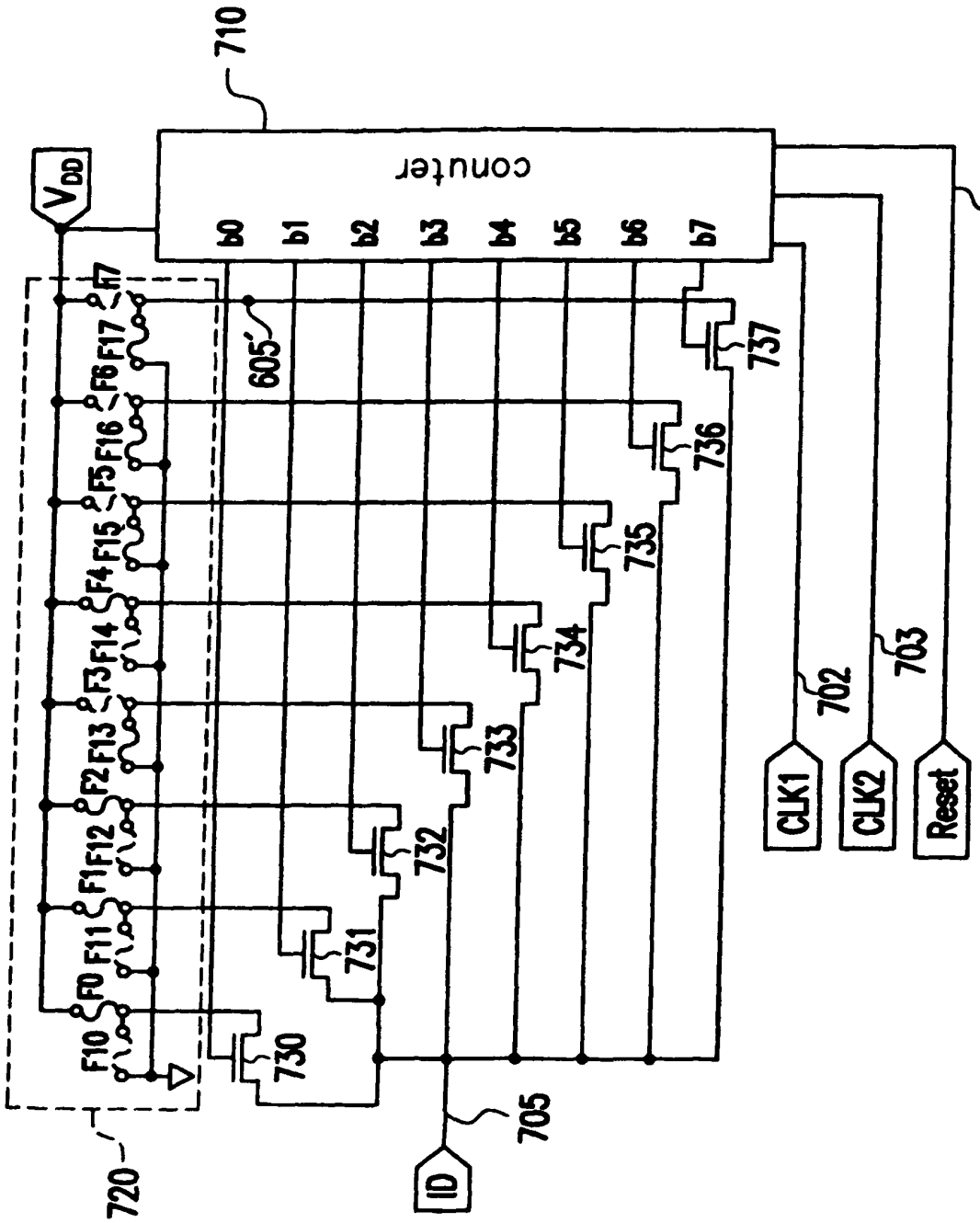

FIG. 6(EXPLANATORY)

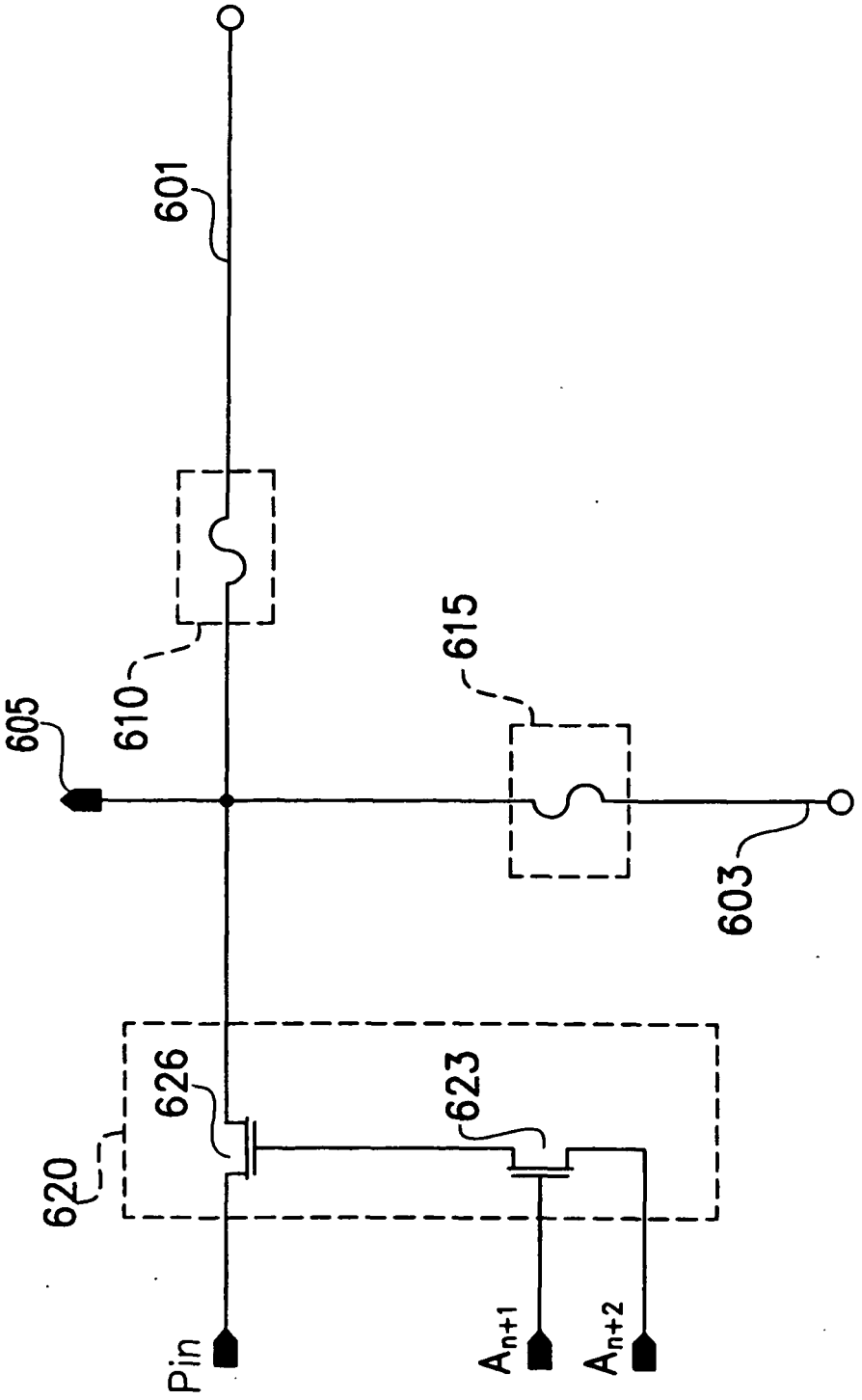

FIG. 7A

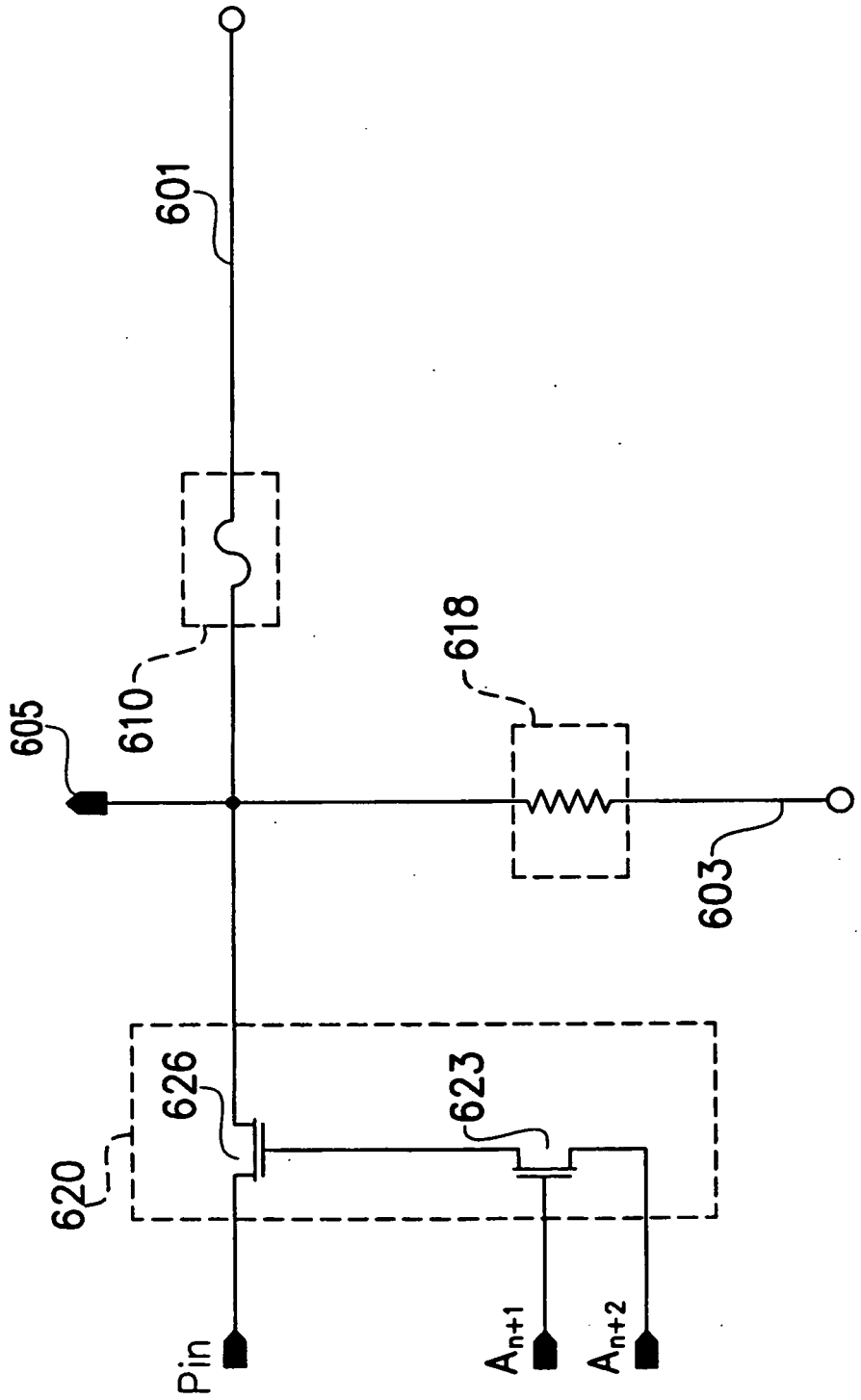

FIG. 7B

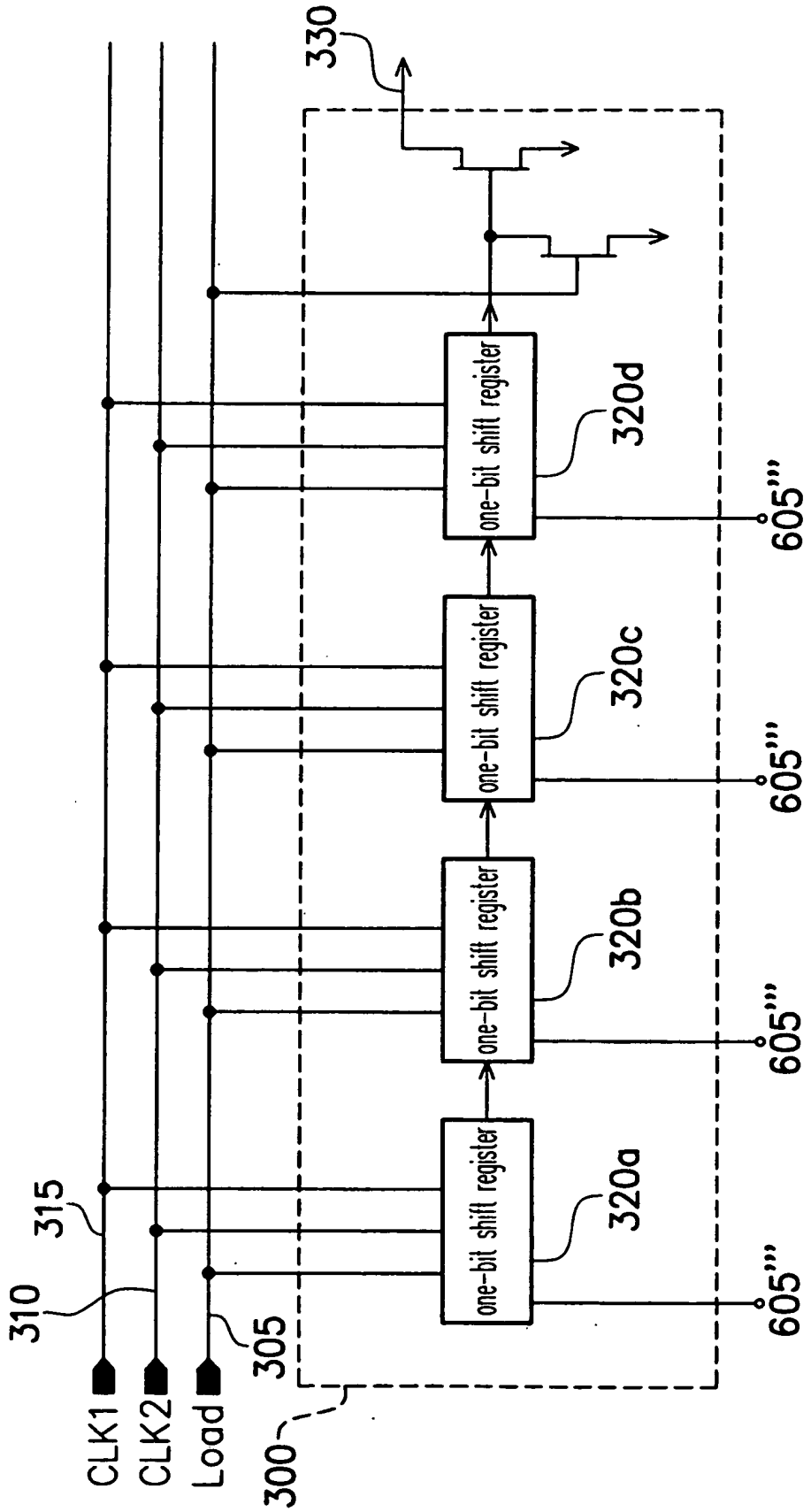
330
one-bit shift register
320d
one-bit shift register
320c
one-bit shift register
320b
one-bit shift register
320a
605'''
605'''
605'''
605'''
315
310
305
CLK1
CLK2
Load
300

FIG. 7C

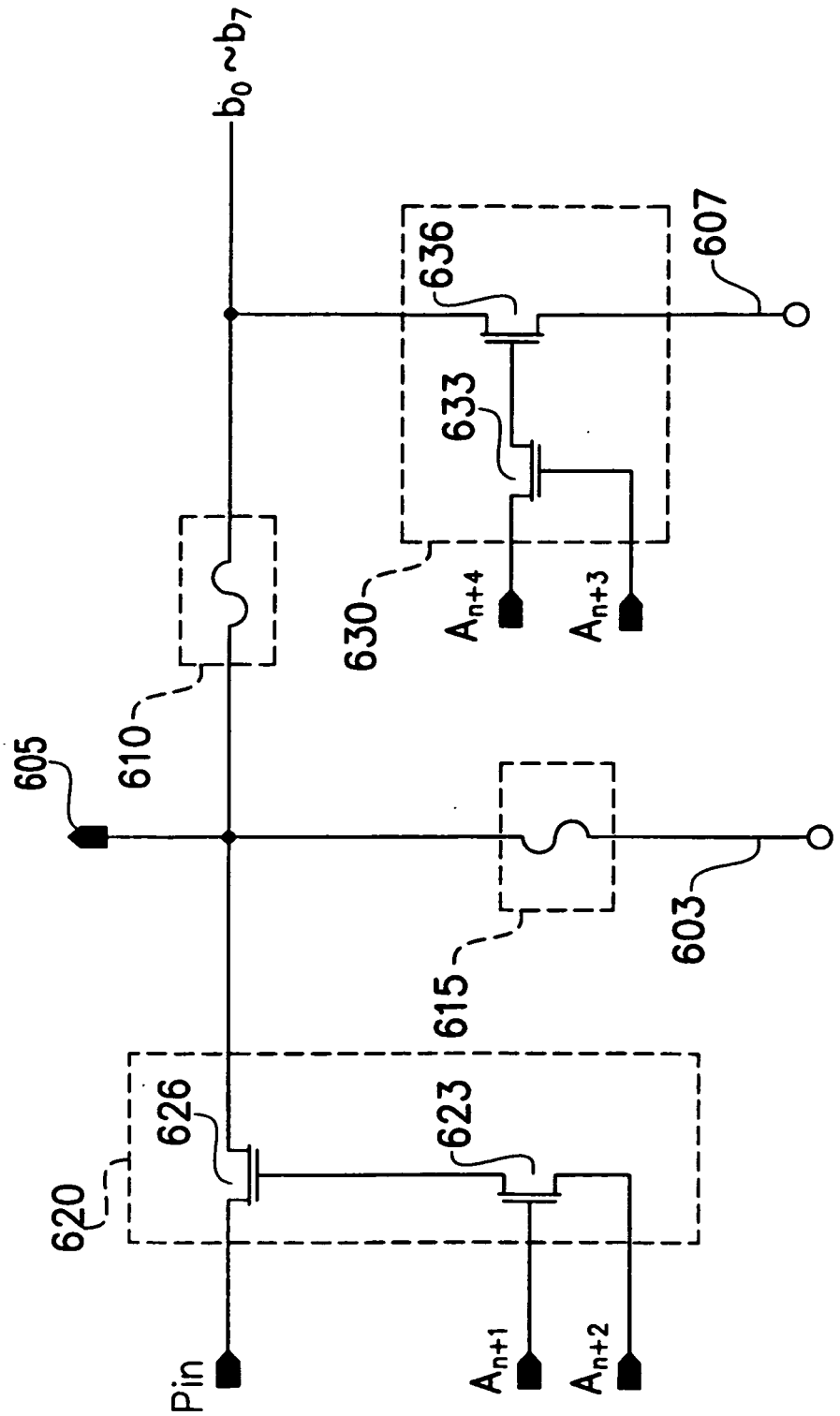
b0 ~b7
636
607
633
630
An+4
An+3
610
605
603
615
626
623
620
Pin
An+1
An+2

FIG. 8A

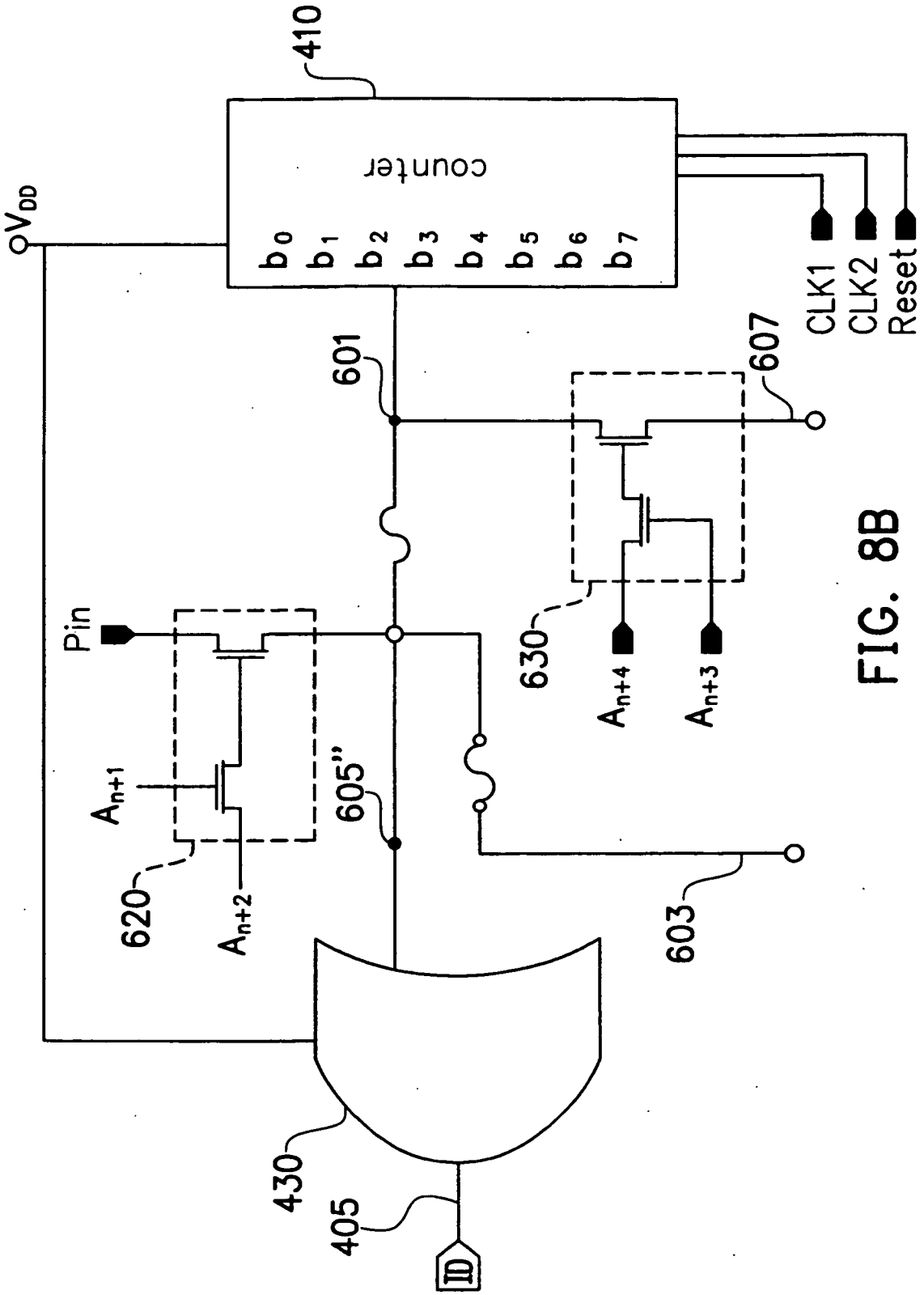
410
counter
V_{DD}
b_0 b_1 b_2 b_3 b_4 b_5 b_6 b_7
CLK1
CLK2
Reset
601
607
Pin
630
A_{n+4}
A_{n+3}
A_{n+1}
605"
620
A_{n+2}
603
430
405
ID

FIG. 8B

REFERENCES CITED IN THE DESCRIPTION

This list of references cited by the applicant is for the reader's convenience only. It does not form part of the European patent document. Even though great care has been taken in compiling the references, errors or omissions cannot be excluded and the EPO disclaims all liability in this regard.

Patent documents cited in the description

- US 6325483 B **[0003] [0003]**
- US 5363134 B **[0023]**
- EP 0571093 A **[0023]**
- US 5940095 A **[0024]**
- EP 0765762 A **[0024]**
- EP 03250724 A **[0033]**