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- **Divakaruni, Rama,**
IBM United Kingdom Ltd.
Winchester,
Hampshire SO21 2JN (GB)
- **Jammy, Rajarao,**
IBM United Kingdom Ltd.
Winchester,
Hampshire SO21 2JN (GB)

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(71) Applicants:
• **International Business Machines Corporation**
Armonk, NY 10504 (US)
• **Infineon Technologies AG**
81669 München (DE)

(74) Representative: **Burt, Roger James**
IBM United Kingdom Limited
Intellectual Property Department
Hursley Park
Winchester
Hampshire SO21 2JN (GB)

(72) Inventors:
• **Beintner, Jochen,**
IBM United Kingdom Ltd.
Winchester,
Hampshire SO21 2JN (GB)

(54) **Nitrided STI liner oxide for reduced corner device impact on vertical device performance**

(57) A method of fabricating an integrated circuit device comprises etching a trench in a substrate and forming a dynamic random access memory (DRAM) cell having a storage capacitor at a lower end and an overlying vertical metal oxide semiconductor field effect transistor (MOSFET) comprising a gate conductor and a boron-doped channel. The method includes forming trenches adjacent the DRAM cell and a silicon-oxy-nitride isolation liner on either side of the DRAM cell, adjacent the gate conductor. Isolation regions are then formed in the trenches on either side of the DRAM cell. Thereafter, the DRAM cell, including the boron-containing channel region adjacent the gate conductor, is subjected to elevated temperatures by thermal processing, for example, forming a support device on the substrate adjacent the isolation regions. The nitride-containing isolation liner reduces segregation of the boron in the channel region, as compared to an essentially nitrogen-free oxide-containing isolation liner.

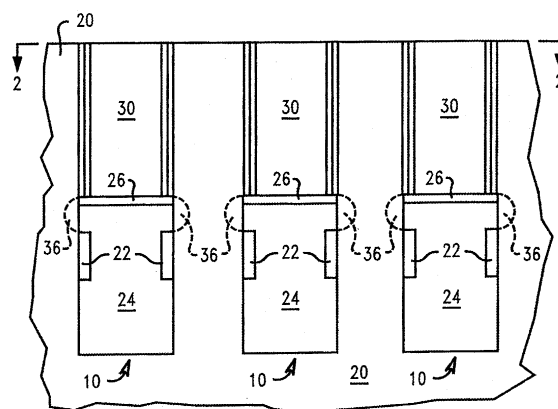


FIG. 1



EUROPEAN SEARCH REPORT

Application Number
EP 05 25 0031

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The present search report has been drawn up for all claims			
Place of search Munich		Date of completion of the search 25 August 2009	Examiner Neumann, Andreas
CATEGORY OF CITED DOCUMENTS X : particularly relevant if taken alone Y : particularly relevant if combined with another document of the same category A : technological background O : non-written disclosure P : intermediate document		T : theory or principle underlying the invention E : earlier patent document, but published on, or after the filing date D : document cited in the application L : document cited for other reasons & : member of the same patent family, corresponding document	

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**ANNEX TO THE EUROPEAN SEARCH REPORT
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