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(54) **DIGITAL SIGNAL PROCESSING DEVICE AND AUDIO SIGNAL REPRODUCTION DEVICE**

EINRICHTUNG ZUR DIGITALEN SIGNALVERARBEITUNG UND
AUDIOSIGNALWIEDERGABEEINRICHTUNG

DISPOSITIF DE TRAITEMENT DE SIGNAL NUMERIQUE ET DISPOSITIF DE REPRODUCTION DE
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(56) References cited:
JP-A- 5 022 952 **JP-A- 5 067 976**
JP-A- 5 145 423 **JP-A- 5 235 773**

- **SARAMAKI T ET AL: "Multiplierless realization of all pole digital filters" SIGNAL PROCESSING, 2002 6TH INTERNATIONAL CONFERENCE ON AUG. 26-30, 2002, PISCATAWAY, NJ, USA,IEEE, vol. 1, 26 August 2002 (2002-08-26), pages 1-4, XP010627909 ISBN: 0-7803-7488-6**
- **HENTSCHKE S ET AL: "A flexible repetitive CSD code filter processor unit in CMOS" ASIC CONFERENCE AND EXHIBIT, 1994. PROCEEDINGS., SEVENTH ANNUAL IEEE INTERNATIONAL ROCHESTER, NY, USA 19-23 SEPT. 1994, NEW YORK, NY, USA,IEEE, 19 September 1994 (1994-09-19), pages 261-264, XP010140477 ISBN: 0-7803-2020-4**
- **TATTERSALL G D ET AL: "Digital bandlimiting filters for PCM transmission systems" IEEE TRANSACTIONS ON COMMUNICATIONS USA, vol. COM-27, no. 1, January 1979 (1979-01), pages 240-246, XP002344683 ISSN: 0090-6778**
- **APFEL R J ET AL: "A SINGLE-CHIP FREQUENCY-SHIFT KEYED MODEM IMPLEMENTED USING DIGITAL SIGNAL PROCESSING" IEEE JOURNAL OF SOLID-STATE CIRCUITS, IEEE INC. NEW YORK, US, vol. SC-19, no. 6, December 1984 (1984-12), pages 869-877, XP000759228 ISSN: 0018-9200**

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EP 1 557 953 B1

- MAY M W ET AL: "A synchronous dual-output switching dc-dc converter using multibit noise-shaped switch control" SOLID-STATE CIRCUITS CONFERENCE, 2001. DIGEST OF TECHNICAL PAPERS. ISSCC. 2001 IEEE INTERNATIONAL FEB. 5-7, 2001, PISCATAWAY, NJ, USA, IEEE, 5 February 2001 (2001-02-05), pages 358-359, XP010536301 ISBN: 0-7803-6608-5

Description

Technical field

[0001] The present invention relates to a digital signal processing device in accordance with the precharacterizing part of claim 1. A digital signal processing device of that kind is known from SARAMAKI T ET AL.: "Multiplierless realization of all pole digital filters" SIGNAL PROCESSING, 2002 6TH INTERNATIONAL CONFERENCE ON AUG. 26-30, 2002, PISCATAWAY. NJ. USA. IEEE. vol. 1, 26 August 2002 (2002-08-26), pages 1-4. ISBN: 0-7803-7488-6. A digital signal processing device of that kind may be advantageously used in audio signal reproduction devices.

Background art

[0002] Audio signal reproduction devices that are used to reproduce an audio signal stored in a recording medium such as a CD or MD are classified into those adopting a multiple-bit PCM (pulse code modulation) system and those adopting a one-bit system. The one-bit system can reproduce a sound source with higher fidelity than the multiple-bit PCM system can.

[0003] A conventional one-bit audio signal reproduction device first encodes an audio signal, which is in the form of a multiple-bit digital signal, into a one-bit digital signal. It then digitally amplifies the one-bit digital signal, and then, by using a low-pass filter, converts the digitally amplified one-bit digital signal into a reproduced signal, which is in the form of an analog signal (for example, see Japanese Patent Application Laid-Open No. H10-322215).

[0004] Now, an example of the configuration of a PDM (pulse density modulation) signal generation circuit incorporated in a conventional one-bit audio signal reproduction device will be described with reference to Fig. 5.

[0005] The PDM signal generation circuit shown in Fig. 5 is composed of an input terminal IN, an output terminal OUT, multipliers 101 to 111, adders 112 to 119, a quantizer 120, and delay elements 121 to 128. The multiplication factors of the multipliers 101, 102, ..., and 111 are m_1 , m_2 , ..., and m_{11} , respectively.

[0006] The PDM signal generation circuit shown in Fig. 5 performs seventh-order delta-signal modulation on an audio signal, which is a multiple-bit digital signal, to produce a PDM signal, which is a one-bit digital signal. The PDM signal consists of pluses of fixed amplitude and fixed pulse width, and represents the level of a signal by varying the density, i.e., occurrence rate, of those pulses.

[0007] Moreover, to reproduce a sound source with fidelity, the PDM signal generation circuit shown in Fig. 5 processes data at a very high sampling frequency of 2.8 MHz or 5.6 MHz throughout, i.e., from the input terminal IN to the output terminal OUT.

[0008] When a one-bit digital signal is produced by delta-sigma modulation, quantization error components ex-

hibit a distribution shifted to a higher range. This is known as "noise shaping". Accordingly, the PDM signal generation circuit shown in Fig. 5 is used to reduce quantization noise in a frequency range of interest (for example, the audible frequency range), and thus functions as an IIR (infinite-duration impulse response) filter. This helps obtain a desired S/N ratio in the frequency range of interest and achieve wider-range coverage.

[0009] However, the PDM signal generation circuit shown in Fig. 5 operates at a very high sampling frequency (for example, 2.8 MHz, 5.6 MHz, or the like), and thus exerts an undesirable influence due to unnecessary electromagnetic radiation. This makes it essential to lay sufficient shielding against noise as by laying double shielding using a steel plate and a copper plate. As a result, in an audio signal reproduction device, the steel plate and other components for shielding occupy a considerable space and increase the weight of the audio signal reproduction device. This makes it unfeasible to reduce the size and weight of audio signal reproduction devices.

[0010] Moreover, the PDM signal generation circuit shown in Fig. 5 incorporates many multipliers and adders, and thus has a large circuit scale. The large circuit scale requires accordingly high power consumption. Furthermore, the PDM signal generation circuit shown in Fig. 5 is typically built as an analog circuit, and can only handle signal processing for a single channel. Accordingly, in stereophonic applications (involving left and right channels), it is necessary to use two of the PDM signal generation circuit shown in Fig. 5. As described above, the PDM signal generation circuit has a complicated circuit configuration and a large circuit scale, and is therefore difficult to mount on a conventional LSI. This makes it unfeasible to reduce the size and weight of audio signal reproduction devices.

[0011] Having the disadvantages described above, the PDM signal generation circuit shown in Fig. 5 is unsuitable particularly for use in portable audio signal reproduction devices, in which low power consumption, compactness and light weight, and low cost are eagerly sought, and are accordingly not adopted in such applications.

[0012] The document of SARAMAKI T ET AL. mentioned above describes in general a multiplierless implementation of an all-pole filter. That is a digital filter which replaces a multiplier unit by adding and shifting units.

[0013] HENTSCHE S ET AL.: "A flexible repetitive CSD code filter processor unit in CMOS" ASIC CONFERENCE AND EXHIBIT, 1994. PROCEEDINGS, SEVENTH ANNUAL IEEE INTERNATIONAL ROCHESTER, NY, USA 19-23 SEPT.1994. NEW YORK. NY, USA, IEEE. 19 September 1994 (1994-09=19); pages 261-264, XPO10140477 ISBN: 0-7803-2020-4 describes a multiplier-free second order sigma-delta modulator. Fig. 5 of the latter document depicts a filter processor with four filtering modules which can be switched into four operational modes as shown in Fig. 6 of this document.

Disclosure of the invention

[0014] It is an object of the present invention to provide a digital signal processing device that can be built with a smaller circuit scale.

[0015] To achieve the above object, the present invention provides a digital signal processing device comprising: adding means; first multiplying means for multiplying a signal by a predetermined multiplication value; delaying means for delaying an output signal of the adding means; and second multiplying means for multiplying an output signal of the delaying means by a predetermined multiplication value, wherein the adding means adds together an output signal of the first multiplying means, the output signal of the delaying means and an inverted output signal of the second multiplying means and wherein the digital processing device further includes controlling means for controlling the processing of the signal by repeating a plurality of times an operation of feeding the output of the adding means to the first multiplying means and to the delaying means.

[0016] The digital signal processing device is further provided with: storing means for storing the output signal of the adding means; totally adding means; and quantizing means. The digital processing device further includes controlling means for controlling the processing of the signal by repeating a plurality of times the operation of feeding the output of the adding means to the first multiplying means and to the delaying means. Here, the operations up to and including the addition operation performed by the adding means constitute one step. In the first step, an input signal from outside is multiplied by the predetermined multiplication value by the first multiplying means and is then fed to the adding means. In the second and following steps, the operation of feeding the output signal of the storing means to the first multiplying means and to the delaying means and the operation of making the adding means add together the output signal of the first multiplying means, the output signal of the delaying means, and the inverted output signal of the second multiplying means are performed in a plurality of steps. Then, in the last step, different values of the output signal of the adding means as stored in different steps in the storing means are totally added together by the totally adding means, then the output signal of the totally adding means is quantized by the quantizing means, and then the output signal of the quantizing means is fed to outside and is simultaneously fed back to the second multiplying means in the first step.

[0017] With this configuration, it is possible to perform a multiplication operation by using shared, small-circuit-scale shifters in combination with an adder, and thus without using large-circuit-scale multipliers as conventionally used. This helps greatly to reduce the power consumption, and also makes it possible to mount on an LSI the signal processing device that performs operations repeatedly as described above.

[0018] In a digital signal processing device according

to the present invention, it is preferable to use separate control signals to control whether or not the first multiplying means receives an input signal, whether or not the delaying means outputs a signal, and whether or not the second multiplying means outputs a signal. With this configuration, it is possible to keep inactive whichever means is not currently needed. This helps greatly reduce the power consumption.

[0019] In the digital signal processing device described above, the adding means may be adding-and-subtracting means that is also capable of performing subtraction, so that it at least either or both replaces the operation of making the first multiplying means multiply the signal by the predetermined multiplication value with a first operation of multiplying the signal with a predetermined multiplication factor by repeatedly performing calculation operations consisting of making the first multiplying means multiply the signal by a multiplication value equal to a predetermined multiple or the reciprocal thereof and then output the result to the adding-and-subtracting means, then making the adding-and-subtracting means add together or subtract from each other the output of the first multiplying means and the output of the delaying means, and then making the delaying means receive the output of the adding-and-subtracting means, and replaces the operation of making the second multiplying means multiply the signal by the predetermined multiplication value with a second operation of multiplying the signal with a predetermined multiplication factor by repeatedly performing calculation operations consisting of making the second multiplying means multiply the signal by a multiplication value equal to a predetermined multiple or the reciprocal thereof and then output the result to the adding-and-subtracting means, then making the adding-and-subtracting means add together or subtract from each other the output of the second multiplying means and the output of the delaying means, and then making the delaying means receive the output of the adding-and-subtracting means.

[0020] By making the adding-and-subtracting means add together or subtract from each other the output of the first or second multiplying means and the output of the delaying means, it is possible to reduce the number of times the operations need to be repeated to fewer than when only addition operations are performed between the output of the first or second multiplying means and the output of the delaying means. For example, in a case where the predetermined multiplication factor is 0.9375 and the multiplication value equal to the predetermined multiple or the reciprocal thereof is $1/16$, addition operations need to be repeated 15 times when only addition operations are used. By contrast, when a subtraction operation is performed with the multiplication value equal to the predetermined multiple or the reciprocal thereof set to 1 for the first time and to $1/16$ for the second time, operations need to be repeated only twice. Thus, even when the accuracy of the multiplication factor is increased, and thus it becomes necessary to process data

with a larger number of digits, it is possible to minimize the increase in the calculation clock frequency. Thus, it is possible to increase the accuracy of the multiplication factor while minimizing the power consumption.

[0021] Moreover, it is preferable that, every time the calculation operations are repeated, the predetermined multiple or the reciprocal thereof be set to a different value.

[0022] This helps reduce the number of repetition of operations. For example, in a case where the predetermined multiplication factor is 0.9375 and the multiplication value equal to the predetermined multiple or the reciprocal thereof is $1/16$, addition operations need to be repeated 15 times when only addition operations are used. By contrast, when the multiplication value equal to the predetermined multiple or the reciprocal thereof is switched from $1/2$ to $1/4$, then to $1/8$, and then to $1/16$ every time the operations are repeated, even if only addition operations are used, it is possible to make the predetermined multiplication factor equal to 0.9375 by repeating addition operations four times. In a case where the predetermined multiplication factor is 0.90625, if subtraction operations are performed with the multiplication value equal to the predetermined multiple or the reciprocal thereof set to 1 for the first time and to $1/32$ for the second and the following times, the operations need to be repeated four times to achieve the desired multiplication operation to make the predetermined multiplication factor equal to 0.90625 ($1 - 1/32 - 1/32 - 1/32$). By contrast, if the multiplication value equal to the predetermined multiple or the reciprocal thereof is switched from 1 to $1/16$ and then to $1/32$ every time the operations are repeated, operations need to be repeated only three times to achieve the desired multiplication operation to make the predetermined multiplication factor equal to 0.90625 ($1 - 1/16 - 1/32$).

[0023] Furthermore, it is preferable that, assuming that the predetermined multiplication factor is represented in two-bit notation using "0" and "1", when three or more consecutive digits have "1", the adding-and-subtracting means perform subtraction.

[0024] In this way, it is possible to permit the adding-and-subtracting means to perform a subtraction operation only when its doing so helps to reduce the number of repetition of operations to fewer than if it performs an addition operation.

[0025] It is further advantageous if the digital signal processing device performs a delta-sigma modulation on a PCM signal obtained by subjecting an audio signal to pulse code modulation. This helps greatly to reduce the power consumption.

[0026] Moreover, in the configuration described above, the digital signal processing means may alternately perform the delta-sigma modulation for the left-channel and right-channel signals of the audio signal. This permits the multiplying means, adding means, and quantizing means to be shared between the left and right channels. This helps further to reduce the circuit scale,

and thus leads to a further reduction of the power consumption.

[0027] Moreover, it may be advantageous to implement the digital processing device configured as described above in a portable audio signal reproduction device. This makes it possible to achieve low power consumption, compactness and light weight, and low cost in portable audio signal reproduction devices, in which low power consumption, compactness and light weight, and low cost are eagerly sought.

Brief description of drawings

[0028]

Fig. 1 is a diagram showing an example of the configuration of an MD reproduction device.

Fig. 2 is a diagram showing an example of the configuration of the seventh-order delta-sigma modulation circuit provided in the MD reproduction device of Fig. 1.

Fig. 3 is a diagram showing an example of the configuration of the PWM circuit provided in the MD reproduction device of Fig. 1.

Fig. 4 is a diagram showing the relationship between the clock signal of the 96-count counter, the count value of the 96-count counter, and the PWM signals.

Fig. 5 is a diagram showing an example of the configuration of the PDM signal generation circuit provided in a conventional one-bit audio signal reproduction device.

Fig. 6 is a diagram showing another example of the configuration of the seventh-order delta-sigma modulation circuit provided in the MD reproduction device of Fig. 1.

Best mode for carrying out the invention

[0029] Hereinafter, an embodiment of the present invention will be described with reference to the accompanying drawings. Here, a description will be given of an MD reproduction device as an example of a digital signal processing device according to the invention. Fig. 1 is a block diagram showing an example of the configuration of the MD reproduction device according to the invention.

[0030] An optical pickup device 2 extracts a signal from an MD 1, and feeds the signal to a decompression circuit 3. The decompression circuit 3 decompresses the signal (compressed music data) fed thereto. Thus, the signal outputted from the decompression circuit 3 is a PCM signal S1 having a sampling frequency of 44.1 kHz.

[0031] An oversampling circuit 4 converts the PCM signal outputted from the decompression circuit 3 into a 24-bit (multiple-bit) PCM signal S2 having a sampling frequency of 8fs. Here, $f_s = 44.1$ kHz.

[0032] A seventh-order delta-sigma demodulation circuit 5 performs delta-sigma modulation on the PCM sig-

nal S2 outputted from the oversampling circuit 4 to produce a left-channel six-bit PCM signal S3 and a right-channel six-bit PCM signal S4. The six-bit PCM signals S3 and S4 each have a sampling frequency of 8fs.

[0033] A PWM circuit 6 performs pulse width modulation on the left-channel six-bit PCM signal S3 outputted from the seventh-order delta-sigma demodulation circuit 5 to produce a left-channel one-bit PWM signal S5, and performs pulse width modulation on the right-channel six-bit PCM signal S4 outputted from the seventh-order delta-sigma demodulation circuit 5 to produce a right-channel one-bit PWM signal S6.

[0034] The left-channel one-bit PWM signal S5 outputted from the PWM circuit 6 is converted into an analog signal and amplified by a switching amplifier 7, then has high-frequency components eliminated therefrom by a low-pass filter (LPF) 8, and is reproduced as sound by a left-channel loudspeaker 9. The right-channel one-bit PWM signal S6 outputted from the PWM circuit 6 is converted into an analog signal and amplified by a switching amplifier 10, then has high-frequency components eliminated therefrom by a low-pass filter (LPF) 11, and is reproduced as sound by a right-channel loudspeaker 12.

[0035] In this embodiment, the decompression circuit 3, oversampling circuit 4, seventh-order delta-sigma demodulation circuit 5, and PWM circuit 6 are mounted on a single system LSI. It is, however, also possible to provide them separately.

[0036] The distinctive features of the invention lie in the seventh-order delta-sigma demodulation circuit 5 and the PWM circuit 6. Now, the configuration of these will be described in detail. First, a description will be given of the seventh-order delta-sigma demodulation circuit 5. Fig. 2 shows an example of the configuration of the seventh-order delta-sigma demodulation circuit 5.

[0037] The seventh-order delta-sigma modulation circuit is built as a digital signal processing device composed of an input terminal IN, an output terminal OUT, shifters 14 to 16, an adder 17, a quantizer 18, registers ds1_reg to ds7_reg, out_reg, ACC, and reg, and selectors 19 to 23.

[0038] The input terminal IN is connected to the "01" input terminal of the selector 21, and the output terminal of the selector 21 is connected to the input side of the shifter 14. The adder 17 receives the outputs of the shifters 14 and 15 on a non-inverting basis, and receives the output of the shifter 16 on an inverting basis. The output side of the adder 17 is connected to the input side of the register ACC. The output side of the register ACC is connected to the "10" input terminal of the selector 21 and to the input side of each of the registers ds1_reg to ds7_reg and out_reg.

[0039] The output side of the register ds1_reg is connected to the "000" input terminal of each of the selectors 19 and 20. The output side of the register ds2_reg is connected to the "001" input terminal of each of the selectors 19 and 20. The output side of the register ds3_reg is connected to the "010" input terminal of each of the

selectors 19 and 20. The output side of the register ds4_reg is connected to the "011" input terminal of each of the selectors 19 and 20. The output side of the register ds5_reg is connected to the "100" input terminal of each of the selectors 19 and 20. The output side of the register ds6_reg is connected to the "101" input terminal of each of the selectors 19 and 20. The output side of the register ds7_reg is connected to the "110" input terminal of each of the selectors 19 and 20. The output side of the register out_reg is connected to the input side of the quantizer 18, and the output side of the quantizer 18 is connected to the "111" input terminal of the selector 20 and to the input side of the register reg. The output side of the register reg is connected to the output terminal OUT.

[0040] The output terminal of the selector 19 is connected to the "1" input terminal of the selector 22, and the output terminal of the selector 22 is connected to the input side of the shifter 15. The output terminal of the selector 20 is connected to the "1" input terminal of the selector 23, and the output terminal of the selector 23 is connected to the input side of the shifter 16.

[0041] The shifters 14 to 16 are controlled by shifter control signals ctl1 to ctl3, respectively. The selector 19 is controlled by a selection signal regsel_1. The selector 20 is controlled by a selection signal regsel_2. The selector 21 is controlled by a selection signal asel. The selector 22 is controlled by a selection signal bsel. The selector 23 is controlled by a selection signal csel. The selectors 19 to 23 each select one of the input terminals thereof that corresponds to the state of the selection signal fed thereto, and output to the output terminal thereof the signal fed to the selected input terminal. The register ACC is controlled by an enable signal enable_acc. The register ds1_reg to ds7_reg are controlled by enable signals enable_1 to enable_7, respectively. The register out_reg is controlled by an enable signal enable_o. To each of the "00" input terminal of the selector 21, the "0" input terminal of the selector 22, and the "0" input terminal of the selector 23 is fed data consisting of a bit string of which all the bits are zero.

[0042] In this configuration, when a multiplication operation is performed, the selection signal asel for the selector 21, the selection signal bsel for the selector 22, and the selection signal csel for the selector 23 are switched to signals for a multiplication operation, so that the combined operation of the shifters 14, 15, and 16 and the adder 17 yields the result of the multiplication operation.

[0043] For example, the same result as that obtained in the PDM signal generation circuit shown in Fig. 5 as a result of the multiplier 101 performing a multiplication operation on a 358.8 kHz 24-bit PCM signal fed in via the input terminal IN can be obtained in the seventh-order delta-sigma modulation circuit shown in Fig. 2 in the following manner. When the multiplication factor m1 = 0.5, in the seventh-order delta-sigma modulation circuit shown in Fig. 2, the selection signal asel for the selector 21 is set to "01", and the output data dataa of the selector

21 received by the shifter 14 is shifted one bit rightward by the shifter 14. When the multiplication factor $m1 = 0.25$, in the seventh-order delta-sigma modulation circuit shown in Fig. 2, the selection signal *asel* for the selector 21 is set to "01", and the output data *dataa* of the selector 21 received by the shifter 14 is shifted two bits rightward by the shifter 14. Moreover, in either case, the selection signals *bsel* and *csel* are set to "0", so that the output value of the shifter 14 is stored in the register ACC.

[0044] Incidentally, better sound quality can be obtained by increasing the accuracy of the multiplication factor $m1$. This can be achieved by adding together, as necessary, differently shifted shifter values. For example, the multiplication factor $m1$ can be set to 0.9375 in the following manner. In this case, the seventh-order delta-sigma demodulation circuit 5 is given, instead of the circuit configuration shown in Fig. 2, a circuit configuration as shown in Fig. 6. In Fig. 6, such elements and signals as are found also in Fig. 2 are identified with the same reference numerals and symbols, and their detailed explanations will be omitted. In the seventh-order delta-sigma demodulation circuit shown in Fig. 6, the selector 22 used in the seventh-order delta-sigma demodulation circuit shown in Fig. 2 is replaced with a selector 22'. Correspondingly, the output side of the register ACC is connected to the "10" input terminal of the selector 22', the output terminal of the selector 19 is connected to the "00" input terminal of the selector 22', and the output terminal of the selector 22' is connected to the input side of the shifter 15. To the "01" input terminal of the selector 22' is fed data consisting of a bit string of which all the bits are zero. The selector 22' is controlled by the selection signal *bsel* so that the selector 22' selects one of the input terminals thereof that corresponds to the state of the selection signal and outputs to the output terminal thereof the signal fed to the selected input terminal. Here, depending on an external signal (not illustrated), the adder 17 can receive the output of the shifter 14 not only on a non-inverting basis but also on an inverting basis.

[0045] First, in the seventh-order delta-sigma modulation circuit shown in Fig. 6, the selection signal *asel* for the selector 21 is set to "01", and the output data *dataa* of the selector 21 received by the shifter 14 is shifted one bit rightward by the shifter 14. Moreover, the selection signal *bsel* is set to "01", and the selection signal *csel* is set to "0", so that the output value of the shifter 14 is stored in the register ACC.

[0046] Then, the selection signal *asel* for the selector 21 is set to "01", and the output data *dataa* of the selector 21 received by the shifter 14 is shifted two bits rightward by the shifter 14. Moreover, the selection signal *bsel* is set to "10", and the selection signal *csel* is set to "0", so that the sum of the output values of the shifters 14 and 15 is stored in the register ACC. At this time point, the multiplication factor $m1$ is equal to 0.75 ($= 1/2 + 1/4$).

[0047] Furthermore, the selection signal *asel* for the selector 21 is set to "01", and the output data *dataa* of the selector 21 received by the shifter 14 is shifted three

bits rightward by the shifter 14. Moreover, the selection signal *bsel* is set to "10", and the selection signal *csel* is set to "0", so that the sum of the output values of the shifters 14 and 15 is stored in the register ACC. At this time point, the multiplication factor $m1$ is equal to 0.875 ($= 1/2 + 1/4 + 1/8$).

[0048] Furthermore, the selection signal *asel* for the selector 21 is set to "01", and the output data *dataa* of the selector 21 received by the shifter 14 is shifted fourth bits rightward by the shifter 14. Moreover, the selection signal *bsel* is set to "10", and the selection signal *csel* is set to "0", so that the sum of the output values of the shifters 14 and 15 is stored in the register ACC. At this time point, the multiplication factor $m1$ is equal to 0.9375 ($= 1/2 + 1/4 + 1/8 + 1/16$).

[0049] By shifting the signal a plurality of times with the shifter 14 in this way, it is possible to increase the accuracy of the multiplication factor. The procedure described above (hereinafter referred to also as the first procedure) requires four addition operations to make the multiplication factor $m1$ equal to 0.9375. With the seventh-order delta-sigma demodulation circuit 5 shown in Fig. 6, it is possible to increase the accuracy of the multiplication factor also through the following procedure (hereinafter referred to also as the second procedure).

[0050] Consider a case where, as in the example described above, the multiplication factor $m1$ is made equal to 0.9375. In the seventh-order delta-sigma demodulation circuit shown in Fig. 6, first, the selection signal *asel* for the selector 21 is set to "01", but, here, the output data *dataa* of the selector 21 received by the shifter 14 is not shifted. Then, the selection signal *bsel* is set to "01" and the selection signal *csel* is set to "0", so that the output value of the shifter 14 is stored in the register ACC.

[0051] Now, the adder 17 is so switched that it receives the output of the shifter 14 not on a non-inverting basis but on an inverting basis. Then, the selection signal *asel* for the selector 21 is set to "01", and the output data *dataa* of the selector 21 received by the shifter 14 is shifted four bits rightward by the shifter 14. Moreover, the selection signal *bsel* is set to "10", and the selection signal *csel* is set to "0". As a result, the sum of the output of the shifter 15 and the output of the shifter 14, here inverted so as to be subtracted from the output of the shifter 15, is stored in the register ACC. At this time point, the multiplication factor $m1$ is already equal to 0.9375 ($1 - 1/16$). This procedure requires only two addition or subtraction operations, and thus requires fewer operations than when the necessary calculations are performed only as addition operations. With this procedure, even when the accuracy of the multiplication factor is increased, and thus it becomes necessary to process data with a larger number of digits, it is possible to minimize the increase in the calculation clock frequency. Thus, it is possible to increase the accuracy of the multiplication factor while minimizing the power consumption.

[0052] For maximum effect, whether to make the seventh-order delta-sigma demodulation circuit 5 shown in

Fig. 6 perform the first or second procedure is determined in the following manner. If a given fixed factor, when represented in binary notation and unfolded as a sequence of addition operations, includes three or more consecutive digits having "1", the second procedure is adopted. In the example described above where the multiplication factor m1 is made equal to 0.9375, the factor can be represented as $m1 = 0.1111 = (1/2) + (1/4) + (1/8) + (1/16)$ in binary notation, and this, when a subtraction operation is used, can be processed as $m1 = 0.1111 = (1) - (1/16)$.

[0053] The value obtained by multiplying the input signal stored in the register ACC by the multiplication factor m1 is then stored in the registers ds1_reg to ds7_reg and out_reg, which correspond respectively to the delay elements 121 to 128 of different orders in Fig. 5. The registers ds1_reg to ds7_reg and out_reg are each 24-bit wide.

[0054] When the selection signal asel for the selector 21 is "10", the output of the register ACC (which is equal to the register value of the register ds1_reg) is used as the output of the selector 21. This output of the selector 21 is shifted by the shifter 14 so as to be multiplied by a value corresponding to a multiplication factor m2, and is then fed to the adder 17 as one non-inverting input thereto. When the selection signal bsel is "1" and in addition the selection signal regsel_1 is "001", the previous register value of the register ds2_reg is used as the output of the selector 22. This output of the selector 22 is, without being shifted for multiplication by the shifter 15, fed to the adder 17 as the other non-inverting input thereto. When the selection signal csel is "1" and in addition the selection signal regsel_2 is "010", the previous register value of the register ds3_reg is used as the output of the selector 23. This output of the selector 23 is shifted by the shifter 16 so as to be multiplied by a value corresponding to a multiplication factor m8, and is then fed to the adder 17 as the inverting input thereto. In this case, the adder 17 operates in an equivalent manner to the adder 113 provided in the PDM signal generating circuit in Fig. 5.

[0055] By varying the selection signals for the selectors 19 to 23 and the control signals for the shifters 14 to 16, it is possible to make the adder 17 operate in an equivalent manner to any of the adders 114 to 118 provided in the PDM signal generating circuit in Fig. 5.

[0056] In this way, the operations that need to be performed to obtain data of each order can be performed with a single clock pulse. Thus, in an nth-order noise shaper (delta-sigma modulation circuit), the data of all the orders can be obtained with n clock pulses at the minimum.

[0057] The seventh-order delta-sigma modulation circuit shown in Fig. 2 or 6 does not require the multipliers 101 to 111 provided in the PDM signal generating circuit in Fig. 5. This helps reduce the circuit scale. Moreover, it is easy to increase the number of orders of delta-sigma modulation. This makes it possible to obtain excellent

noise characteristics. Furthermore, it is possible to permit the input signal to have a very low sampling frequency.

[0058] Advisably, the frequency of the main clock is calculated from the total number of operation steps, and an address counter is created that is needed in a ROM (not illustrated) provided in the seventh-order delta-sigma modulation circuit shown in Fig. 2 or 6.

[0059] In a case where 24 steps are needed for each of the left and right channels during a period of 8fs, it is necessary to use a clock having a frequency of $8fs \times (24 \text{ steps} \times 2 \text{ channels}) = 384 \text{ fs}$ (16.8688 MHz). Thus, the individual registers receive this clock or a signal having a phase deviated therefrom. A 24-count counter (not illustrated) is provided in the seventh-order delta-sigma modulation circuit shown in Fig. 2 or 6, and the count value of this 24-count counter is used as the address in the above-mentioned ROM. In this ROM are stored the enable signals enable_1 to enable_7, enable_o, and enable_q for the registers, the selection signals asel, bsel, csel, regsel_1, and regsel_2 for the selectors, and the control signals ctl1 to ctl3 for controlling the number of digits by which the shifters shift the data fed thereto. The values of these signals as actually outputted with every clock pulse are varied from one clock pulse to another. The shifters 14 to 16, adder 17, and quantizer 18 are used alternately for the left and right channels (for example, when the 8fs signal is "1", for the left channel and, when it is "0", for the right channel). This helps greatly reduce the circuit scale. It should be noted that, with respect to the registers ds1_reg to ds7_reg, out_reg, and reg and the output terminal OUT, there are provided two sets of them separately, one for the left channel and the other for the right channel.

[0060] The data stored as the register values of the registers ds1_reg, ds2_reg, ds3_reg, ds4_reg, ds5_reg, ds6_reg, to ds7_reg, and out_reg (each 24-bit wide, and for each of the left and right channels) in the seventh-order delta-sigma modulation circuit shown in Fig. 2 or 6 corresponds respectively to ds1, ds2, ds3, ds4, ds5, ds6, ds7, and out in the PDM signal generation circuit in Fig. 5.

[0061] There exist enable signals one for each of the registers ds1_reg to ds7_reg and out_reg, which thus each become active only once during a period of 8fs to store data. That is, these registers do not operate every 384fs (= 16.8688 MHz), and thus exert no effect on the power consumption.

[0062] As described above, a multiplication operation can be achieved by the combined operation of the shifters 14 to 16 and the adder 17. The multiplication factor is set according to the ultimately desired characteristics. The 24-bit data ultimately stored in the register out_reg is divided into 47 sections by the quantizer 18, and is thereby replaced with six-bit data (in the embodiment under discussion, each section being one of the 47 values in total, namely "000000" to "101110"). In this way, the PCM signal fed in via the input terminal IN is subjected to delta-sigma modulation, and is thereby converted into a PCM signal with a smaller number of bits. This PCM signal

with a smaller number of bits is then, by way of the register reg, fed out via the output terminal OUT.

[0063] Next, a description will be given of the PWM circuit 6. Fig. 3 shows an example of the configuration of the PWM circuit 6. The PWM circuit 6 shown in Fig. 3 is composed of input terminals 24 and 27, comparators 25 and 28, output terminals 26 and 29, and a 96-count counter 30.

[0064] Via the input terminal 24 is fed in the left-channel six-bit PCM signal S3 outputted from the seventh-order delta-sigma demodulation circuit shown in Fig. 2 or 6. The comparator 25 compares the left-channel six-bit PCM signal S3 fed in via the input terminal 24 with the count value of the 96-count counter 30 to produce the left-channel PWM signal S5, and then feeds this to the output terminal 26. On the other hand, via the input terminal 27 is fed in the right-channel six-bit PCM signal S4 outputted from the seventh-order delta-sigma demodulation circuit shown in Fig. 2 or 6. The comparator 28 compares the right-channel six-bit PCM signal S4 fed in via the input terminal 27 with the count value of the 96-count counter 30 to produce the right-channel PWM signal S6, and then feeds this to the output terminal 29. The 96-count counter 30 counts 96 values during a period of 8fs.

[0065] The left-channel PWM signal S5 produced by the comparator 25 toggles to a high level when the decimal value corresponding to the left-channel six-bit PCM signal S3 becomes equal to the count value of the 96-count counter 30, and toggles to a low level when the sum of the decimal value corresponding to the left-channel six-bit PCM signal S3 and the count value of the 96-count counter 30 becomes equal to 95. On the other hand, the right-channel PWM signal S6 produced by the comparator 28 toggles to a high level when the decimal value corresponding to the right-channel six-bit PCM signal S4 becomes equal to the count value of the 96-count counter 30, and toggles to a low level when the sum of the decimal value corresponding to the right-channel six-bit PCM signal S4 and the count value of the 96-count counter 30 becomes equal to 95. The purpose of the comparators 25 and 28 operating in this way is to permit the left-channel and right-channel PWM signals S5 and S6 to always toggle twice each during a period of 8fs without being fixed at a high or low level. Fig. 4 shows the relationship here between the clock signal CK of the 96-count counter 30, the count value of the 96-count counter 30, and the PWM signals.

[0066] The left-channel and right-channel PWM signals S5 and S6 are pulse signals of fixed amplitude and fixed pulse occurrence rate, and represent signal levels by varying the pulse width along the time axis. Thus, the left-channel and right-channel PWM signals S5 and S6 are each one-bit wide in the amplitude direction, but have multiple values in the time axis direction. As shown in Fig. 4, data conversion of 47 values into different patterns within one period of 8fs (= 352.8 kHz) is achieved by varying, from one value to the next, the width of the high

level period by 768fs (= 33.8688 MHz) symmetrically, i.e., on each of the left and right sides of the pulse.

[0067] In this embodiment, a seventh-order delta-sigma modulation circuit is used as the delta-sigma modulation circuit. It is, however, also possible to use a delta-sigma modulation circuit of any other order.

Industrial applicability

[0068] Digital signal processing devices according to the present invention find wide application in various devices, such as audio appliances, that process digital signals.

Claims

1. A digital signal processing device comprising:

adding means (17);
first multiplying means (14, 21) adapted for multiplying a signal by a predetermined multiplication value;
delaying means (ds1_reg.... ds7_reg. 15, 19, 22) adapted for delaying an output signal of the adding means; and
second multiplying means (16, 20, 23) adapted for multiplying an output signal of the delaying means by a predetermined multiplication value, the adding means (17) being adapted to add together an output signal of the first multiplying means (14, 21), the output signal of the delaying means (ds1_reg. ... ds7_reg, 15, 19, 22) and an inverted output signal of the second multiplying means (16, 20, 23) **characterized in that** the digital processing device further includes controlling means for controlling the processing of the signal by repeating a plurality of times an operation of feeding the output of the adding means (17) to the first multiplying means (14, 21) and to the delaying means (ds1_reg, ... ds7_reg. 15, 19, 22).

2. The digital signal processing device of claim 1, further comprising:

storing means (ACC) for storing the output signal of the adding means (17);
totally adding means (out-reg), and
quantizing means (18),
the controlling means being adapted to control the operations up to and including an addition operation performed by the adding means (17) as constituting one step,

wherein the controlling means controls:

in a first step the first multiplying means (14, 21)

- to multiply an input signal from outside by the predetermined multiplication value to feed the multiple to the adding means (17);
 in second and following steps the storing means (ACC) to feed its output signal to the first multiplying means (14, 21), and to the delaying means (ds1_reg. ... ds7_reg. 15, 19, 22) and the adding means (17) to add in a plurality of steps together the output signal of the first multiplying means (14, 21), the output signal of the delaying means (ds1_reg, ... ds7 reg, 15, 19, 22) and the inverted output signal of the second multiplying means (15, 20, 23), and
 in a last step the totally adding means (out_reg) to totally add together different values of the output signal of the adding means (17) as stored in different steps in the storing means (ACC), then the quantizing means (Q) to quantize an output signal of the totally adding means (out_reg) and then to feed the output signal of the quantizing means (Q) to outside and simultaneously back to the second multiplying means (16, 20, 23) for carrying out the first step.
3. The digital processing device of claim 2, wherein said controlling means is comprising:
- first controlling means for controlling which step the delaying means (ds1_reg, ... ds7_reg. 15, 19, 22) outputs a signal of.
4. The digital processing device of one of claims 2 and 3, wherein said controlling means is further comprising:
- second controlling means for controlling which step the second multiplying means (16, 20, 23) outputs a signal of.
5. The digital processing device of one of claims 1 to 3, wherein said controlling means is further comprising:
- third controlling means for controlling whether the first multiplying means (14, 21) receives the input signal from outside, receives the output signal of the adding means (17), or receives no signal.
6. The digital processing device of one of claims 1 to 3, wherein said controlling means is further comprising:
- fourth controlling means for controlling whether or not the delaying means (ds1_reg, ... ds7_reg, 15, 19, 22) outputs a signal.
7. The digital processing device of one of claims 1 to 3, wherein said controlling means is further comprising:
- fifth controlling means for controlling whether or not the multiplying means (16, 20, 23) outputs a signal.
8. The digital signal processing device of claim 1, wherein the adding means (17) is adding-and-subtracting means that is also capable of performing subtraction, and the controlling means is controlling the processing of multiplying the signal with a predetermined multiplication factor by repeatedly performing calculation operations consisting of making the first multiplying means multiply the signal by a multiplication value equal to a predetermined multiple or a reciprocal thereof and then output a result to the adding-and-subtracting means, then making the adding-and-subtracting means add together or subtract from each other the output of the first multiplying means and the output of the delaying means, and then making the delaying means receive an output of the adding-and-subtracting means, and/or
 an output signal of the delaying means with a predetermined multiplication factor by repeatedly performing calculation operations consisting of making the second multiplying means multiply the output signal by a multiplication value equal to a predetermined multiple or a reciprocal thereof and then output a result to the adding-and-subtracting means, then making the adding-and-subtracting means add together or subtract from each other the output of the second multiplying means and the output of the delaying means, and then making the delaying means receive an output of the adding-and-subtracting means.
9. The digital signal processing device of claim 8, wherein the controlling means sets every time the calculation operations are repeated, the predetermined multiple or the reciprocal thereof to a different value.
10. The digital signal processing device of one claims 8 and 9, wherein, assuming that the predetermined multiplication factor is represented in two-bit notation using "0" and "1", when three or more consecutive digits have "1", the controlling means controls the adding-and-subtracting means to perform subtraction.

11. The digital signal processing device of one of the claims 1 to 10, wherein it performs a delta-sigma modulation on a PCM signal obtained by subjecting an audio signal to pulse code modulation. 5
12. The digital signal processing device of claim 11, wherein it performs the delta-sigma modulation alternately for left-channel and right-channel signals of the audio signal. 10
13. The digital signal processing device of one of claims 11 or 12, wherein it is implemented in a portable audio signal reproduction device. 15

Patentansprüche

1. Einrichtung zur digitalen Signalverarbeitung, umfassend: 20
- eine Addierereinrichtung (17); 25
- eine erste Multipliziereinrichtung (14, 21), die sich zur Multiplikation eines Signals mit einem vorgegebenen Multiplikationswert eignet; 30
- eine Verzögerungseinrichtung (ds1_reg, ... ds7_reg, 15, 19, 22), die sich zur Verzögerung eines Ausgangssignals der Addiereinrichtung eignet; und 35
- eine zweite Multipliziereinrichtung (16, 20, 23), die sich zur Multiplikation eines Ausgangssignals der Verzögerungseinrichtung mit einem vorgegebenen Multiplikationswert eignet, 40
- wobei die Addiereinrichtung (17) sich zur Addition eines Ausgangssignals der ersten Multipliziereinrichtung (14, 21), des Ausgangssignals der Verzögerungseinrichtung (ds1_reg, ... ds7_reg, 15, 19, 22) und eines invertierten Ausgangssignals der zweiten Multipliziereinrichtung (16, 20, 23) eignet, **dadurch gekennzeichnet, dass** 45
- die Einrichtung zur digitalen Verarbeitung zudem eine Steuereinrichtung aufweist zum Steuern der Verarbeitung des Signals durch mehrfaches Wiederholen des Einspeisens der Ausgabe der Addiereinrichtung (17) in die erste Multipliziereinrichtung (14, 21) und in die Verzögerungseinrichtung (ds1_reg, ... ds7_reg, 15, 19, 22). 50
2. Einrichtung zur digitalen Signalverarbeitung nach Anspruch 1, zusätzlich umfassend: 55
- eine Speichereinrichtung (ACC) zum Speichern des Ausgangssignals der Addiereinrichtung (17);

eine Gesamtaddiereinrichtung (out-reg), und eine Quantisiereinrichtung (18), wobei sich die Steuereinrichtung zur Steuerung der Vorgänge bis und einschließlich eines von der Addiereinrichtung (17) durchgeführten Addiervorgangs als ein Schritt eignet, wobei die Steuereinrichtung steuert:

in einem ersten Schritt, die erste Multipliziereinrichtung (14, 21) zur Multiplikation eines Ausgangssignals von außerhalb mit dem vorgegebenen Multiplikationswert zur Einspeisung des Multiplikators in die Addiereinrichtung (17);

in einem zweiten und nachfolgenden Schritten, die Speichereinrichtung (ACC) zur Einspeisung deren Ausgangssignal in die erste Multipliziereinrichtung (14, 21), und in die Verzögerungseinrichtung (ds1_reg, ... ds7_reg, 15, 19, 22), und die Addiereinrichtung (17) zur Addition, in einer Mehrzahl von Schritten, des Ausgangssignals der ersten Multipliziereinrichtung (14, 21), des Ausgangssignals der Verzögerungseinrichtung (ds1_reg, ... ds7_reg, 15, 19, 22) und des invertierten Ausgangssignals der zweiten Multipliziereinrichtung (15, 20, 23), und

in einem letzten Schritt, die Gesamtaddiereinrichtung (out_reg) zur Gesamtaddition verschiedener Werte des Ausgangssignals der Addiereinrichtung (17), die in verschiedenen Schritten in der Speichereinrichtung (ACC) gespeichert wurden, dann die Quantisiereinrichtung (Q) zur Quantisierung eines Ausgangssignals der Gesamtaddiereinrichtung (out_reg) und dann zur Einspeisung des Ausgangssignals der Quantisiereinrichtung (Q) nach außerhalb und gleichzeitig zurück in die zweite Multipliziereinrichtung (16, 20, 23) zum Durchführen des ersten Schritts.

3. Einrichtung zur digitalen Verarbeitung nach Anspruch 2, wobei die Steuereinrichtung aufweist:
- eine erste Steuereinrichtung zum Steuern, in welchem Schritt die Verzögerungseinrichtung (ds1_reg, ...ds7_reg, 15, 19, 22) ein Signal ausgibt.
4. Einrichtung zur digitalen Signalverarbeitung nach einem der Ansprüche 2 und 3, wobei die Steuereinrichtung zudem aufweist:
- eine zweite Steuereinrichtung zum Steuern, in welchem Schritt die zweite Multipliziereinrichtung (16, 20, 23) ein Signal ausgibt.

5. Einrichtung zur digitalen Signalverarbeitung nach einem der Ansprüche 1 bis 3, wobei die Steuereinrichtung zudem aufweist:

eine dritte Steuereinrichtung zum Steuern, ob die erste Multipliziereinrichtung (14, 21) das Eingangssignal von außerhalb empfängt, das Ausgangssignal der Addiereinrichtung (17) empfängt, oder kein Signal empfängt.

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6. Einrichtung zur digitalen Signalverarbeitung nach einem der Ansprüche 1 bis 3, wobei die Steuereinrichtung zudem aufweist:

eine vierte Steuereinrichtung zum Steuern, ob die Verzögerungseinrichtung (ds1_reg, ... ds7_reg, 15, 19, 22) ein Signal ausgibt oder nicht.

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7. Einrichtung zur digitalen Signalverarbeitung nach einem der Ansprüche 1 bis 3, wobei die Steuereinrichtung zudem aufweist:

eine fünfte Steuereinrichtung zum Steuern, ob die Multipliziereinrichtung (16, 20, 23) ein Signal ausgibt oder nicht.

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8. Einrichtung zur digitalen Signalverarbeitung nach Anspruch 1,

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wobei die Addiereinrichtung (17) eine Addier- und-Subtrahier-Einrichtung ist, die ebenso eine Subtraktion durchführen kann, und die Steuereinrichtung die Verarbeitung des Multiplizierens des Signals mit einem vorgegebenen Multiplikationsfaktor durch wiederholtes Durchführen von Berechnungsvorgängen steuert, die darin bestehen, dass die erste Multipliziereinrichtung das Signal mit einem Multiplikationswert entsprechend einem vorgegebenen Multiplikator oder dessen Reziprokwert multipliziert und dann ein Ergebnis zur Addier-und-Subtrahier-Einrichtung ausgibt, die Addier-und-Subtrahier-Einrichtung dann veranlasst wird, die Ausgabe der ersten Multipliziereinrichtung und die Ausgabe der Verzögerungseinrichtung zusammenzuaddieren oder voneinander zu subtrahieren und dann die Verzögerungseinrichtung veranlasst wird, eine Ausgabe der Addier-und-Subtrahier-Einrichtung zu empfangen, und/oder eines Ausgangssignals der Verzögerungseinrichtung mit einem vorgegebenen Multiplikationsfaktor steuert durch wiederholtes Durchführen von Berechnungsvorgängen bestehend aus einem Veranlassen der zweiten Multipliziereinrichtung zur Multiplikation des Ausgangssignals mit einem Multiplikationswert entsprechend einem vorgegebenen Multiplikator oder dessen

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Reziprokwert und Ausgeben eines Ergebnisses an die Addier-und-Subtrahier-Einrichtung. Veranlassen der Addier-und-Subtrahier-Einrichtung dazu, die Ausgabe der zweiten Multipliziereinrichtung und die Ausgabe der Verzögerungseinrichtung zusammenzuaddieren oder voneinander zu subtrahieren, und Veranlassen der Verzögerungseinrichtung dazu, eine Ausgabe der Addier-und-Subtrahier-Einrichtung zu empfangen.

9. Einrichtung zur digitalen Signalverarbeitung nach Anspruch 8.

wobei die Steuereinrichtung bei jeder Wiederholung der Berechnungsvorgänge den vorgegebenen Multiplikator oder dessen Reziprokwert auf einen verschiedenen Wert einstellt.

10. Einrichtung zur digitalen Signalverarbeitung nach einem der Ansprüche 8 und 9,

wobei, unter Annahme, dass der vorgegebene Multiplikationsfaktor in zwei-Bit Notierung unter Verwendung von "0" und "1" dargestellt ist, und drei oder mehr aufeinander folgende Ziffern einer "1" entsprechen, die Steuereinrichtung die Addier-und-Subtrahier-Einrichtung zur Durchführung einer Subtraktion steuert.

11. Einrichtung zur digitalen Signalverarbeitung nach einem der Ansprüche 1 bis 10, wobei diese eine Delta-Sigma-Modulation bezüglich eines empfangenen PCM Signals durchführt, in dem ein Audiosignal einer Pulsmodulation unterzogen wird.

12. Einrichtung zur digitalen Signalverarbeitung nach Anspruch 11,

wobei diese die Delta-Sigma-Modulation aufeinanderfolgend für Linkskanal- und Rechtskanal-Signale des Audiosignals durchführt.

13. Einrichtung zur digitalen Signalverarbeitung nach einem der Ansprüche 11 oder 12,

wobei diese in eine tragbare Audiosignalwiedergabevorrichtung implementiert ist.

Revendications

1. Dispositif de traitement de signal numérique comprenant:

des moyens additionneurs (17);
des premiers moyens multiplicateurs (14, 21) adaptés pour multiplier un signal par une valeur

- de multiplication prédéterminée;
des moyens retardateurs (ds1_reg,... ds7_reg, 15, 19, 22) adaptés pour retarder un signal de sortie des moyens additionneurs; et
des seconds moyens multiplicateurs (16, 20, 23) adaptés pour multiplier un signal de sortie des moyens retardateurs par une valeur de multiplication prédéterminée,
les moyens additionneurs (17) étant adaptés pour additionner les uns aux autres un signal de sortie des premiers moyens multiplicateur (14, 21), le signal de sortie des moyens retardateurs (ds1_reg,... ds7_reg, 15, 19, 22) et un signal de sortie inversé des seconds moyens multiplicateurs (16, 20, 23), **caractérisé en ce que**
le dispositif de traitement numérique comprend également des moyens de commande pour commander le traitement du signal en répétant plusieurs fois une opération de fourniture de la sortie des moyens additionneurs (17) aux premiers moyens multiplicateurs (14, 21) et aux moyens retardateurs (ds1_reg,... ds7_reg, 15, 19, 22).
2. Dispositif de traitement de signal numérique selon la revendication 1, comprenant également:
- des moyens de stockage (ACC) pour stocker le signal de sortie des moyens additionneurs (17);
des moyens totalisateurs (out_reg); et
des moyens quantificateurs (18),
les moyens de commande étant adaptés pour commander les opérations allant jusqu'à et y compris une opération d'addition exécutée par les moyens additionneurs (17), pour former une seule étape,
les moyens de commande commandant:
- au cours d'une première étape, les premiers moyens multiplicateurs (14, 21) pour qu'ils multiplient un signal d'entrée provenant de l'extérieur par la valeur de multiplication prédéterminée afin de fournir le multiple aux moyens additionneurs (17);
au cours d'une deuxième étape et d'étapes suivantes, les moyens de stockage (ACC) pour qu'ils fournissent leur signal de sortie aux premiers moyens multiplicateurs (14, 21) et aux moyens retardateurs (ds1_reg,... ds7_reg, 15, 19, 22), et les moyens additionneurs (17) pour qu'ils additionnent les uns aux autres en plusieurs étapes le signal de sortie des premiers moyens multiplicateurs (14, 21), le signal de sortie des moyens retardateurs (ds1_reg, ... ds7 reg, 15, 19, 22) et le signal de sortie inversé des seconds moyens multiplicateurs (16, 20, 23); et
- au cours d'une dernière étape, les moyens totalisateurs (out_reg) pour qu'ils totalisent les uns avec les autres différentes valeurs du signal de sortie des moyens additionneurs (17) stocké au cours de différentes étapes dans les moyens de stockage (ACC), puis les moyens quantificateurs (Q) pour qu'ils quantifient un signal de sortie des moyens totalisateurs (out_reg) et qu'ils fournissent ensuite leur signal de sortie à l'extérieur en le renvoyant simultanément aux seconds moyens multiplicateurs (16, 20, 23) pour l'exécution de la première étape.
3. Dispositif de traitement numérique selon la revendication 2, dans lequel lesdits moyens de commande se composent de:
- premiers moyens de commande destinés à déterminer à quelle étape appartient un signal délivré par les moyens retardateurs (ds1_reg,... ds7_reg, 15, 19, 22).
4. Dispositif de traitement numérique selon la revendication 2 ou 3, dans lequel lesdits moyens de commande se composent également de :
- deuxièmes moyens de commande destinés à déterminer à quelle étape appartient un signal délivré par les seconds moyens multiplicateurs (16, 20, 23).
5. Dispositif de traitement numérique selon l'une quelconque des revendications 1 à 3, dans lequel lesdits moyens de commande se composent aussi de:
- troisièmes moyens de commande destinés à déterminer si les premiers moyens multiplicateurs (14, 21) reçoivent le signal d'entrée de l'extérieur, le signal de sortie des moyens additionneurs (17) ou aucun signal.
6. Dispositif de traitement numérique selon l'une quelconque des revendications 1 à 3, dans lequel lesdits moyens de commande se composent en outre de:
- quatrièmes moyens de commande destinés à déterminer si les moyens retardateurs (ds1_reg, ... ds7_reg, 15, 19, 22) délivrent ou non un signal.
7. Dispositif de traitement numérique selon l'une quelconque des revendications 1 à 3, dans lequel lesdits moyens de commande se composent également de:
- cinquièmes moyens de commande destinés à déterminer les moyens multiplicateurs (16, 20,

- 23) délivrent ou non un signal.
8. Dispositif de traitement de signal numérique selon la revendication 1,
- dans lequel les moyens additionneurs (17) sont des moyens additionneurs et soustracteurs qui sont également capables d'exécuter une soustraction, et les moyens de commande commandent le traitement de multiplication du signal par un facteur de multiplication prédéterminé par l'exécution répétée d'opérations de calcul consistant à faire en sorte que les premiers moyens multiplicateurs multiplient le signal par une valeur de multiplication égale à un multiple prédéterminé ou à l'inverse de celui-ci et délivrent ensuite un résultat aux moyens additionneurs et soustracteurs, puis que les moyens additionneurs et soustracteurs additionnent l'une à l'autre ou soustraient l'un de l'autre la sortie des premiers moyens multiplicateurs et la sortie des moyens retardateurs, et ensuite que les moyens retardateurs reçoivent une sortie des moyens additionneurs et soustracteurs, et/ou un signal de sortie des moyens retardateurs par un facteur de multiplication prédéterminé par l'exécution répétée d'opérations de calcul consistant à faire en sorte que les seconds moyens multiplicateurs multiplient le signal de sortie par une valeur de multiplication égale à un multiple prédéterminé ou à l'inverse de celui-ci et délivrent ensuite un résultat aux moyens additionneurs et soustracteurs, puis que les moyens additionneurs et soustracteurs additionnent l'une à l'autre ou soustraient l'une de l'autre la sortie des seconds moyens multiplicateurs et la sortie des moyens retardateurs, et ensuite que les moyens retardateurs reçoivent une sortie des moyens additionneurs et soustracteurs.
9. Dispositif de traitement de signal numérique selon la revendication 8,
- dans lequel les moyens de commande fixent, à chaque fois que les opérations de calcul sont répétées, le multiple prédéterminé ou l'inverse de celui-ci à une valeur différente.
10. Dispositif de traitement de signal numérique selon la revendication 8 ou 9,
- dans lequel, en supposant que le facteur de multiplication prédéterminé soit représenté sous la forme d'une notation à deux bits à l'aide de "0" et "1", lorsqu'au moins trois chiffres consécutifs comportent un "1", les moyens de commande commandent les moyens additionneurs et soustracteurs pour qu'ils exécutent une soustraction.
11. Dispositif de traitement de signal numérique selon l'une quelconque des revendications 1 à 10, qui exécute une modulation delta sigma sur un signal PCM obtenu en soumettant un signal audio à une modulation par impulsions codées.
12. Dispositif de traitement de signal numérique selon la revendication 11, qui exécute la modulation delta sigma alternativement pour des signaux de canal gauche et de canal droit du signal audio.
13. Dispositif de traitement de signal numérique selon la revendication 11 ou 12, qui est mis en oeuvre dans un dispositif de reproduction de signal audio portable.

FIG. 1

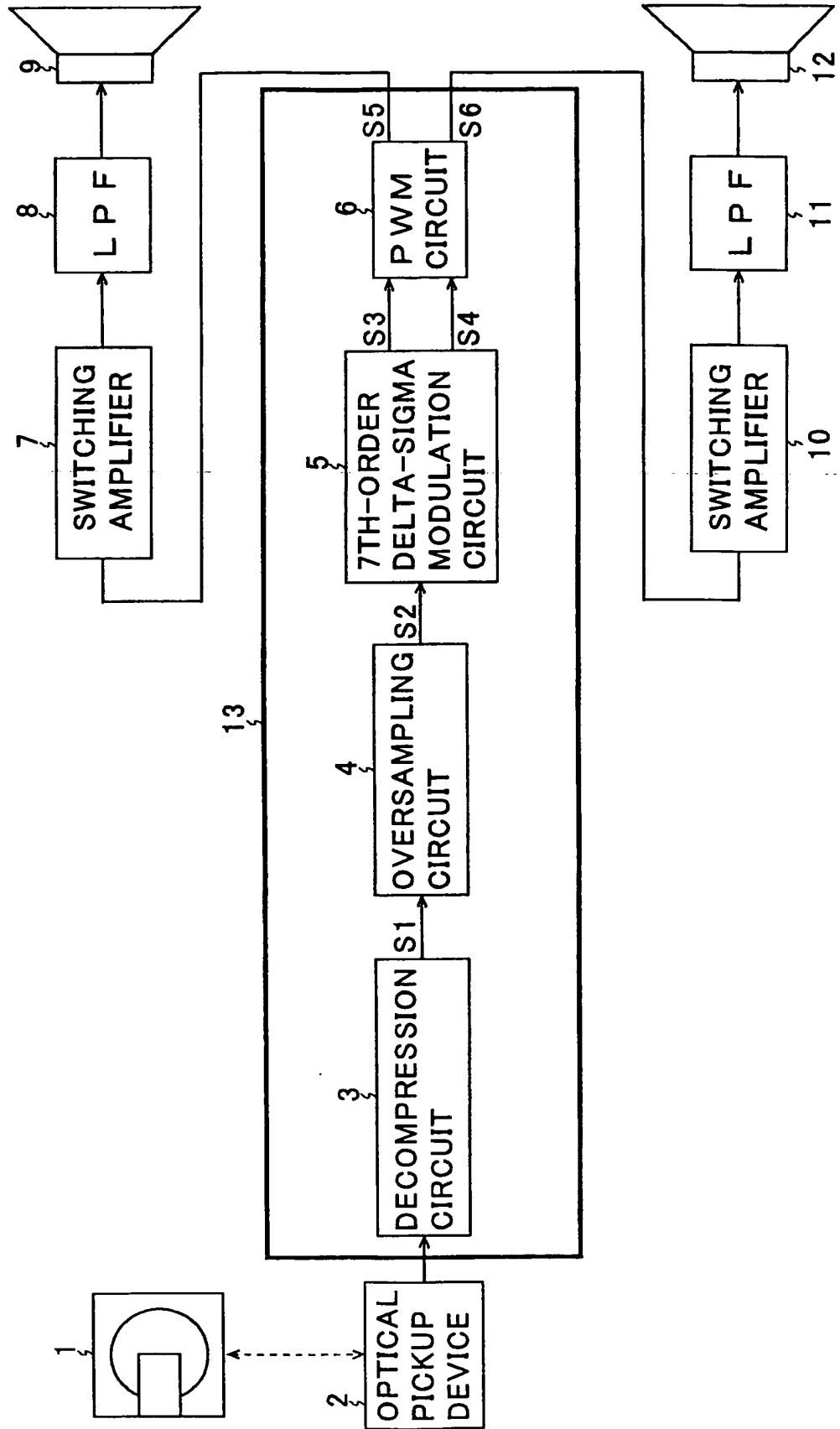


FIG. 2

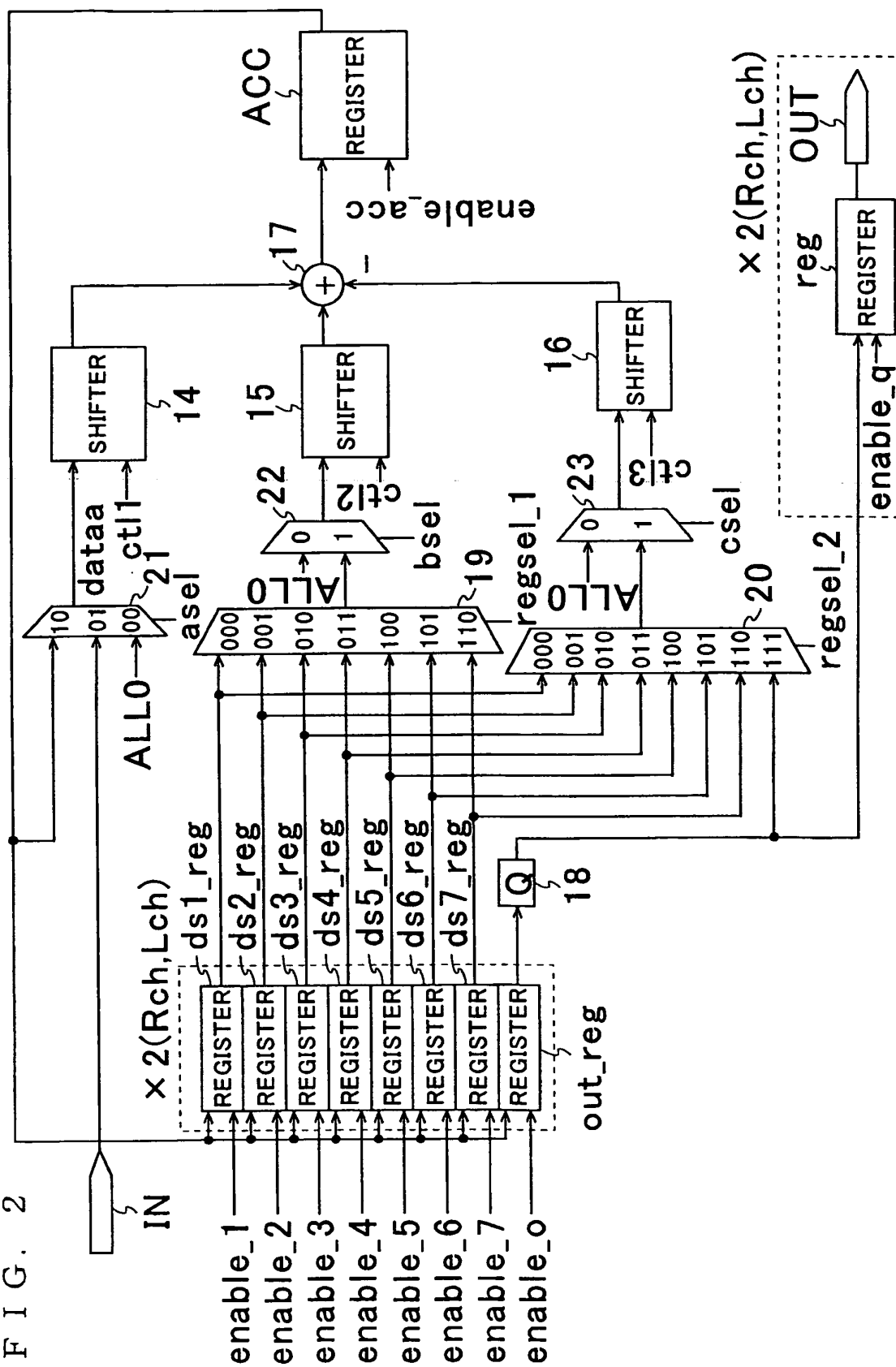


FIG. 3

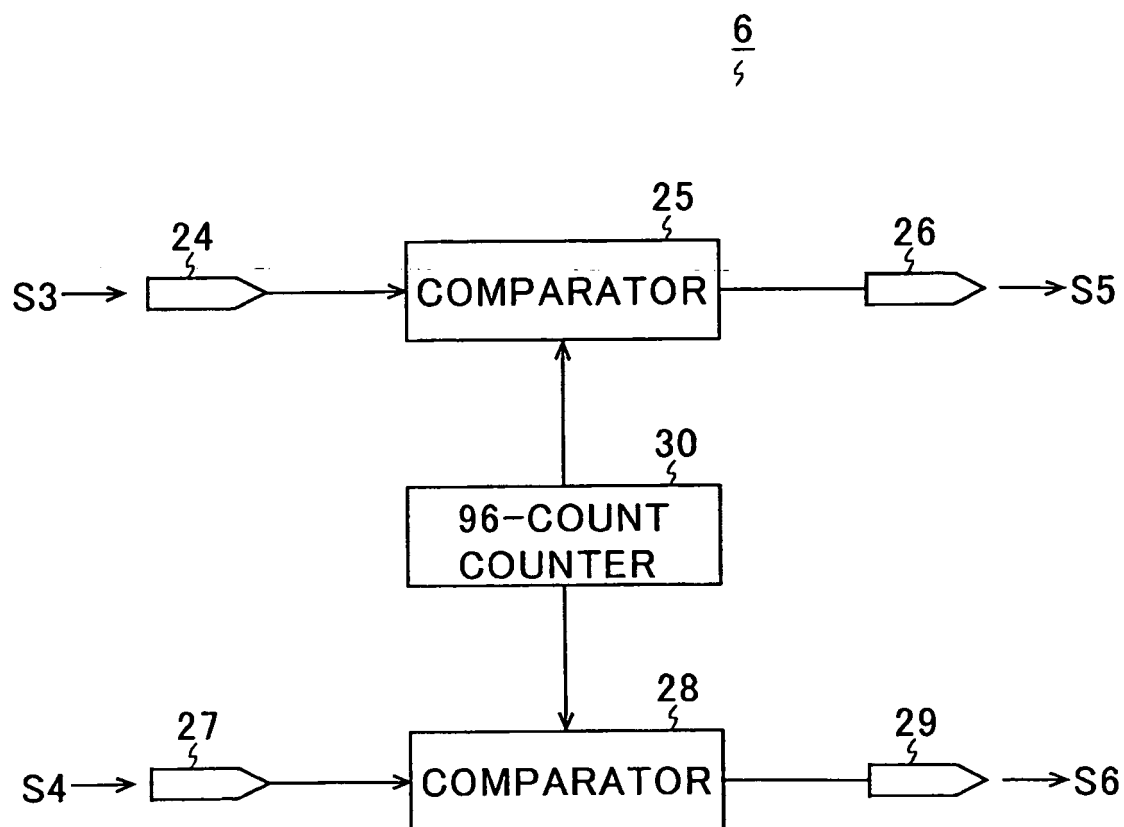


FIG. 4

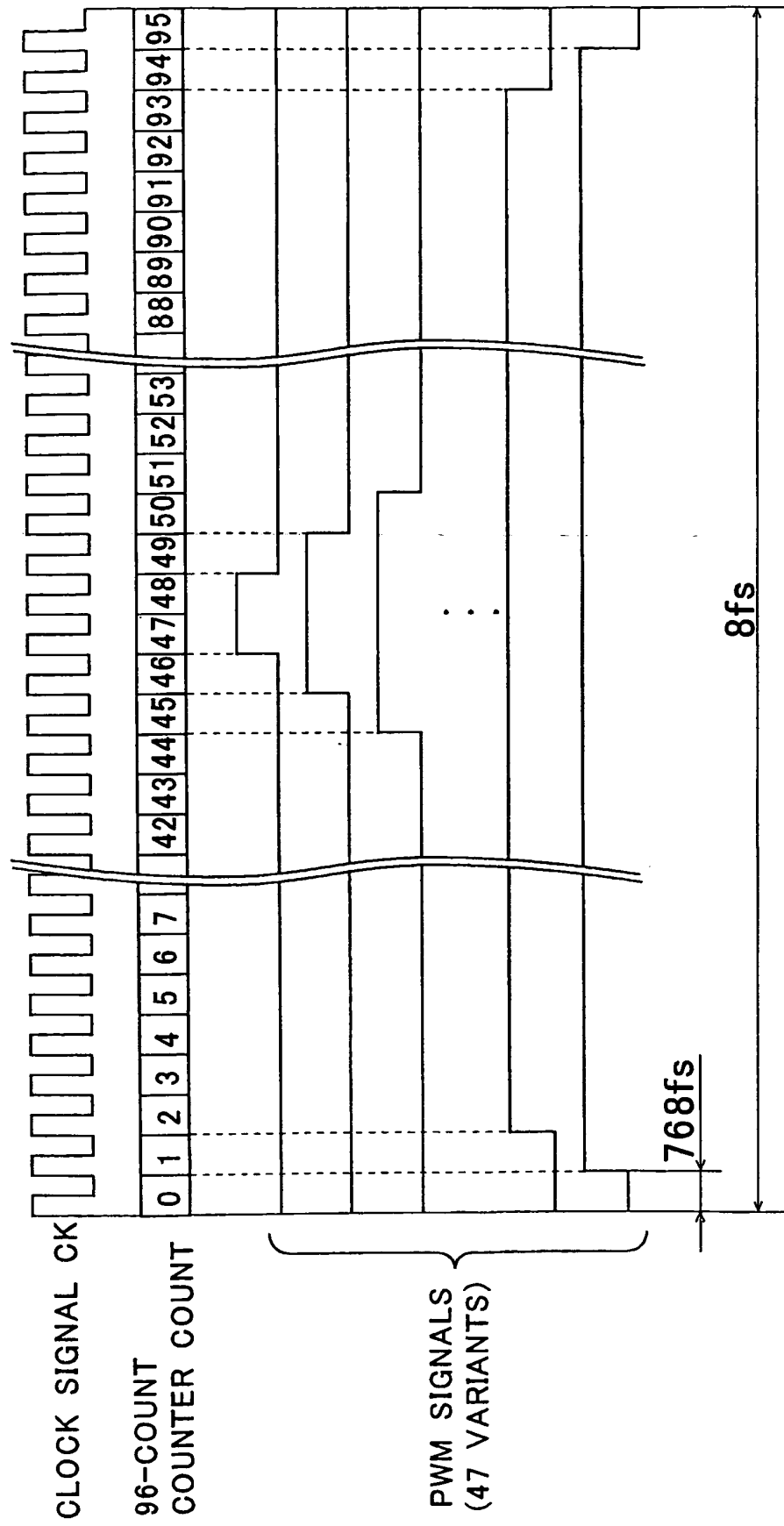


FIG. 5

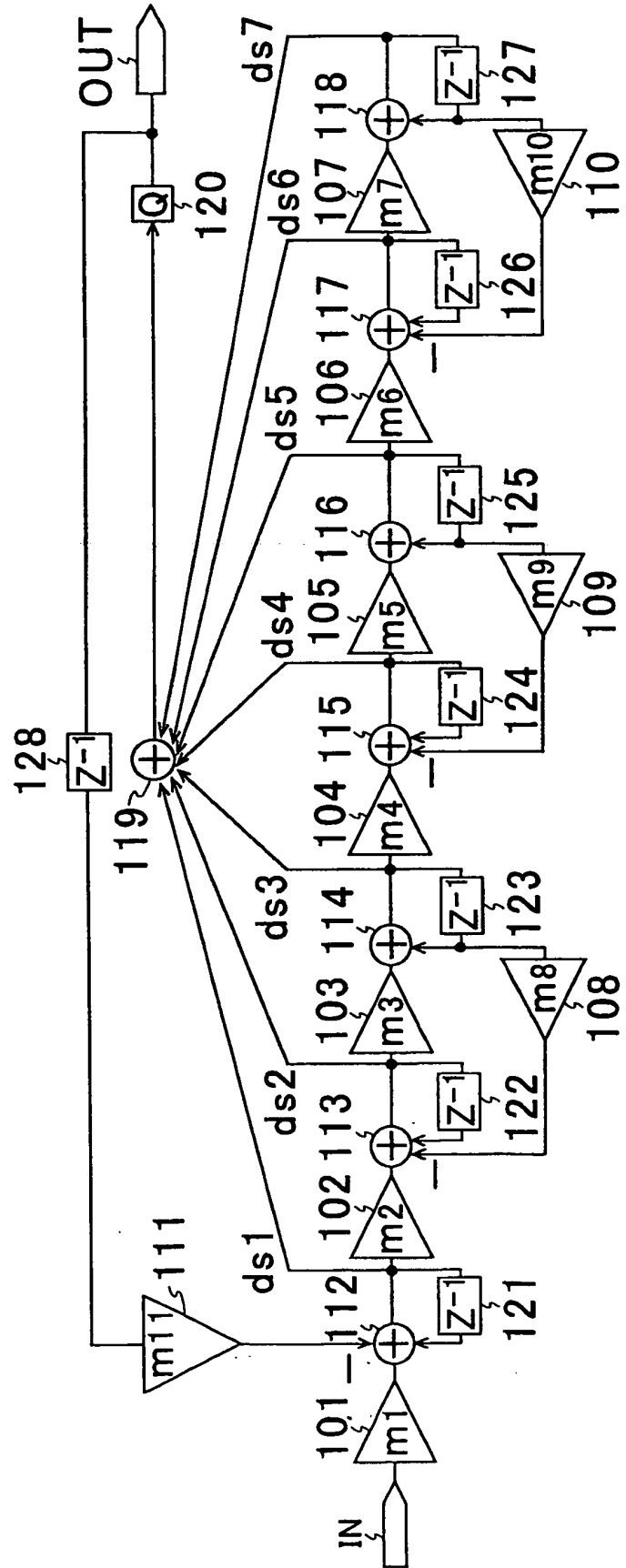
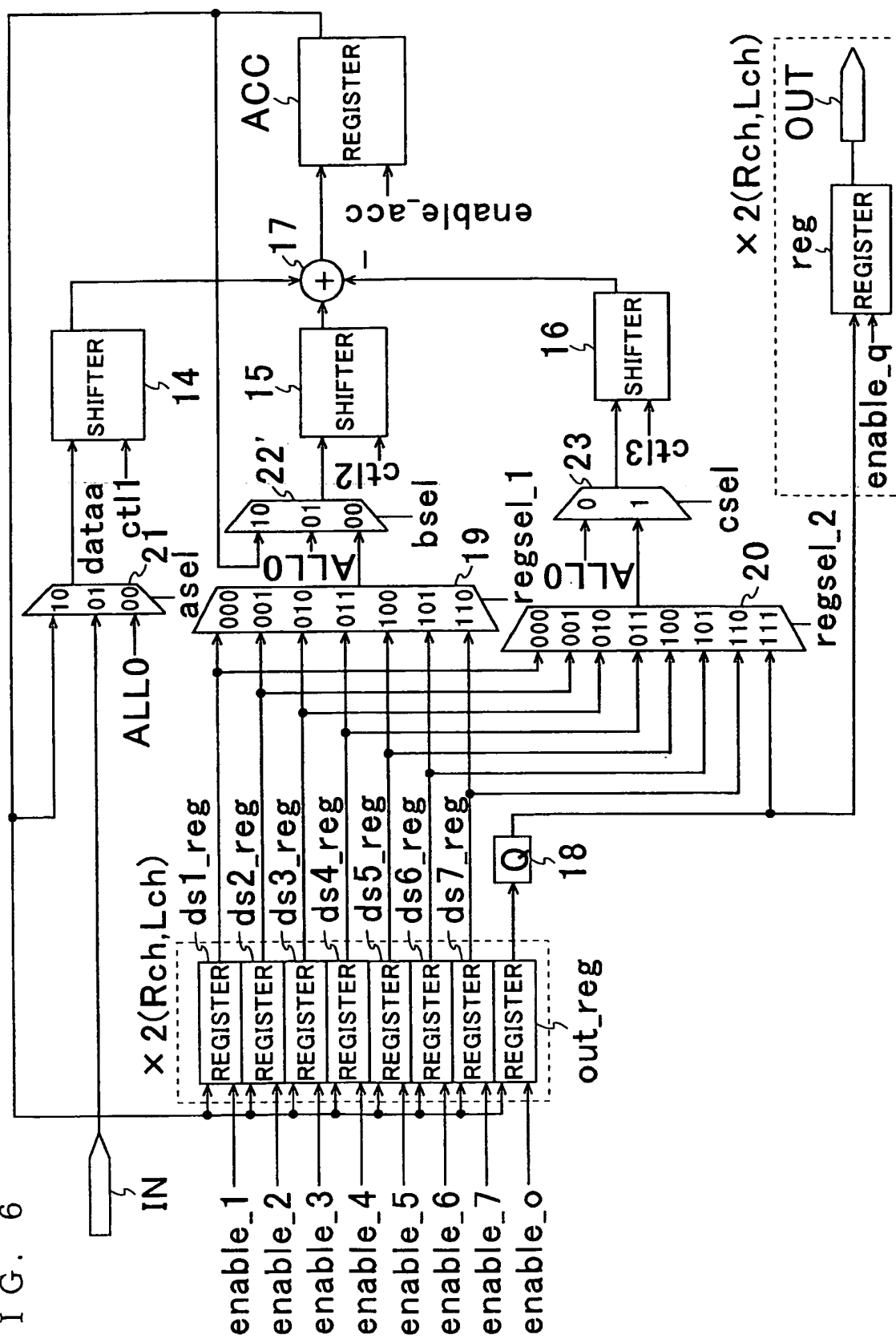


FIG. 6



REFERENCES CITED IN THE DESCRIPTION

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Patent documents cited in the description

- JP H10322215 A [0003]

Non-patent literature cited in the description

- Multiplierless realization of all pole digital filters. **SARAMAKI T et al.** SIGNAL PROCESSING, 2002 6TH INTERNATIONAL CONFERENCE ON AUG. 26-30, 2002, PISCATAWAY. NJ. USA. IEEE. 26 August 2002, vol. 1, 1-4 [0001]
- A flexible repetitive CSD code filter processor unit in CMOS. **HENTSCHE S et al.** SIC CONFERENCE AND EXHIBIT, 1994. PROCEEDINGS, SEVENTH ANNUAL IEEE INTERNATIONAL ROCHESTER, NY, USA 19-23 SEPT.1994. NEW YORK. NY, USA, IEEE. 19 September 1994, 261-264 [0013]