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(54) **Ferroelectric memory**

Ferroelektrischer Speicher

Mémoire ferroelectrique

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(56) References cited:
EP-A- 0 721 190
EP-A- 1 304 701
EP-A- 1 306 851
US-A1- 2003 026 123

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Description

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application is based upon and claims the benefit of priority from the prior Japanese, Patent Application No. 2004 159032, filed on May 28, 2004, and published with the number JP 2005 339 704.

BACKGROUND OF THE INVENTION

[Field of the Invention]

[0002] The present invention relates to a ferroelectric memory, and particularly to a ferroelectric memory according to the upper clause of claim 1. Such a memory is know from EP-A-1 304 701.

[Description of the Related Art]

[0003] The ferroelectric capacitors have a nonvolatile feature as well as a high-speed data reading and writing feature. Therefore, the ferroelectric capacitors are put into practical use as ferroelectric memories (FeRAMs) by taking advantage of these features. The ferroelectric memories can exercise the nonvolatile feature at a high speed and with low power consumption in the same manner as SRAMs do, so that the forroelectric memories are utilized for LSIs for IC cards and tag chips, and are widely used in the market.

[0004] The readout of the potential of a cell of the ferroelectric memory is determined depending on the capacitance ratio of the cell to a bit line, as in DRAMs. When the capacitance is small, the memory area is decreased and the capacitance of the bit line lowers, so that the voltage applied to the ferroelectric capacitor of the cell lowers. Therefore, the charge supplied from the ferroelectric capacitor to the bit line reduces, and thereby the readout margin of a sense amplifier reduces. On the contrary, a devisal is conceivable in which a load is applied to the bit line to thereby prevent the reduction of voltage applied to the ferroelectric capacitor of the cell.

[0005] Further, since the capacitance to be added to the bit line is required to correspond to that of the ferroelectric capacitor of the cell, it is presumable that a great amount of gate capacitance or source-drain capacitance, or a ferroelectric capacitor or the like be utilized. However, the gate capacitance and the source-drain capacitance have a problem of increasing area, and the ferroelectric capacitor has a problem of insufficient accuracy in fluctuation.

[0006] Further, the ferroelectric memories are disclosed in Japanese Patent Application Laid-Open No. 2001-319472 (Patent Document 1) and Japanese Patent Application Laid-Open No. 2004-13951 (Patent Document 2).

SUMMARY OF THE INVENTION

[0007] It is an object of the present invention to provide a ferroelectric memory capable of generating stable bit-line potential without regard to the capacitance value of a bit line.

[0008] This object and other objects are solved by the features of the independent claim. Preferred embodiments of the invention are described by the features of the dependent claims.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009]

Fig. 1 is a circuit diagram showing a configuration example of a ferroelectric memory according to a first embodiment of the present invention;
Fig. 2 is a circuit diagram showing a configuration example of a ferroelectric memory according to a second embodiment of the present invention;
Fig. 3 is a timing chart for illustrating an operation of the ferroelectric memory in Fig. 2;
Fig. 4 is a circuit diagram showing a configuration example of a ferroelectric memory according to a third embodiment of the present invention;
Fig. 5 is a timing chart for illustrating an operation of the ferroelectric memory in Fig. 4;
Fig. 6 is a circuit diagram showing a configuration example of a ferroelectric memory;
Fig. 7 is a graphic chart showing a hysteresis curve of a ferroelectric capacitor;
Fig. 8 is a timing chart for illustrating an operation of a ferroelectric memory; and
Figs. 9A to 9D are views showing hysteresis characteristics of a ferroelectric capacitor.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0010] Fig. 6 is a circuit diagram showing a configuration example of a ferroelectric memory. An n-channel MOS (metal-oxide semiconductor) field effect transistor (FET) 103 is connected to a word line WL with a gate thereof, to a bit line "bl" with a drain thereof, and to a plate line PL with a source thereof via a ferroelectric capacitor C1. Hereinafter, the MOSFET is simply referred to as a "transistor". An n-channel transistor 104 is connected to the word line WL with a gate thereof, to a complementary bit line "/bl" with a drain thereof, and to the plate line PL with a source thereof via a ferroelectric capacitor C0 (zero). Between the bit line "bl" and ground potential (reference potential), there exists parasitic capacitance CBL, and between the complementary bit line "/bl" and the ground potential (reference potential), there exists parasitic capacitance /CBL. A sense amplifier 101 is connected to the bit line "bl" and the complementary bit line "/bl". This configuration forms one memory cell. The transistors 103, 104 serve as switching elements.

[0011] The ferroelectric capacitors C0, C1 store data that complement each other. Specifically, the ferroelectric capacitor C1 stores data "1" while the ferroelectric capacitor C0 stores data "0 (zero)", and the ferroelectric capacitor C1 stores the data "0" while the ferroelectric capacitor C0 stores the data "1". The bit line "bl" and the complementary bit line "/bl" can input and output data with respect to the ferroelectric capacitor C1 and the ferroelectric capacitor C0, respectively. The transistor 103 selectively connects the ferroelectric capacitor C1 and the bit line "bl" in accordance with electrical potential of the word line WL. The transistor 104 selectively connects the ferroelectric capacitor C0 and the complementary bit line "/bl" in accordance with the electrical potential of the word line WL. The sense amplifier 101 amplifies a potential difference between the bit line "bl" and the complementary bit line "/bl".

[0012] Fig. 7 is a graphic chart showing a hysteresis curve of the ferroelectric capacitors C0, C1. The horizontal axis indicates the voltage v of the ferroelectric capacitor, and the vertical axis indicates a polarization Q. For instance, when the plate line PL is at 0 (zero) V, two states 702, 703 are possible to exist. For instance, the state 702 indicates the data "0" and the state 703 indicates the data "1". Description will be given on the assumption that the ferroelectric capacitor C1 be in the state 703 and the ferroelectric capacitor C0 be in the state 702, as an example.

[0013] When the plate line PL is applied a potential VP. the ferroelectric capacitor C1 comes into a state P11. Specifically, a series connection between the ferroelectric capacitor C1 and the bit-line parasitic capacitance CBL is applied the potential VP. The voltage of the ferroelectric capacitor C1 is VC, and the voltage of the bit line "bl" comes to V11. These voltages are determined by the capacitance ratio of the ferroelectric capacitor C1 to the bit-line parasitic capacitance CBL. The total of the voltages VC and V11 becomes the voltage VP. A straight line 701 indicates the ratio of voltage corresponding to the bit-line parasitic capacitance CBL to charge. A cross-point P11 of the straight line 701 and the hysteresis curve is the voltage VC of the ferroelectric capacitor C1.

[0014] Meanwhile, when the plate line PL is applied the potential VP, the ferroelectric capacitor C0 comes into a state P10. Specifically, a series connection between the ferroelectric capacitor C0 and the complementary bit-line parasitic capacitance /CBL is applied the potential VP. The voltage of the ferroelectric capacitor C0 is VbC, and the voltage of the complementary bit line "/bl" comes to V10. These voltages are determined by the capacitance ratio of the ferroelectric capacitor C0 and the complementary bit-line parasitic capacitance /CBL. The total of the voltages VbC and V10 becomes the voltage VP. A straight line 700 indicates the ratio of voltage corresponding to the complementary bit-line parasitic capacitance /CBL to charge. A cross-point P10 of the straight line 700 and the hysteresis curve is the voltage VbC of the ferroelectric capacitor C0.

[0015] At this time, the potential of the bit line "bl" is V11, and the potential of the complementary bit line "/bl" is V10. Then, the potential difference therebetween is V11 - V10 = VBL. The sense amplifier 101 amplifies this potential difference VBL. Accordingly, as the potential difference VBL increases, the margin of the sense amplifier increases, so that the data with higher reliability can be obtained.

[0016] Fig. 8 is a timing chart for illustrating an operation of a ferroelectric memory. When the potential of the word line WL is at low level, the transistors 103, 104 are OFF. The bit line "bl" is disconnected from the ferroelectric capacitor C1 to thereby have a voltage of 0V. The complementary bit line "/bl" is disconnected from the ferroelectric capacitor C0 to thereby have a voltage of 0V.

[0017] Subsequently, when the potential of the word line WL comes to high level, the transistors 103, 104 are turned ON. The bit line "bl" is connected to the ferroelectric capacitor C1, and the complementary bit line "/bl" is connected to ferroelectric capacitor C0. When the potential of the plate line PL is OV, the potentials of the bit line "bl" and the complementary bit line "/bl" are 0V.

[0018] Subsequently, the plate line PL is brought into high level (for example to VP). Then, the bit line "bl" comes to have the potential V11, and the complementary bit line "/bl" comes to have the potential V10. The potential difference between the bit line "bl" and the complementary bit line "/bl" is VBL.

[0019] Subsequently, when the sense amplifier 101 is activated, the potential difference between the bit line "bl" and the complementary bit line "/bl" is amplified. Specifically, the bit line "bl" comes to high level (power source potential) and the complementary bit line "/bl" comes to low level (0V). In accordance with the potentials of the bit line "bl" and the complementary bit line "/bl", a readout data can be outputted to outside.

[0020] After that, the plate line PL is brought into low level, the sense amplifier 101 is inactivated, and the word line WL is brought into low level.

[0021] Fig. 9D shows the potential V11 of the bit line "bl" and the potential V10 of the complementary bit line "/bl" both shown in Fig. 7. As described above, the potential difference between the bit line "bl" and the complementary bit line "/bl" is VBL, which is preferably larger. The potential difference VBL varies depending on the size of the parasitic capacitance CBL of the bit line "bl" and the parasitic capacitance /CBL of the complementary bit line "/bl". Incidentally, the parasitic capacitances CBL and /CBL are substantially the same, and the ferroelectric capacitors C1 and C0 are substantially the same. It is disadvantageous for the parasitic capacitances CBL and /CBL to be excessively large as well as excessively small, since both cause the potential difference VBL to lower. This will be described with reference to Figs. 9A to 9C.

[0022] Fig. 9A is a graphic chart showing hysteresis curves of the ferroelectric capacitors C1, C0. First, a case, in which the plate line PL is brought into high level, and the bit line "bl" comes into a state P21 and the complementary bit line "/bl" comes into a state P20, will be described. In this case, the potential of the bit line "bl" comes to V21 and the potential of the complementary bit line "/bl" comes to V20. As shown in Fig. 9B, the potential difference VBL between the potential V21 of the bit line "bl" and the potential V20 of the complementary bit line "/bl" becomes smaller than that of the case in Fig. 9D.

[0023] Subsequently, a case, in which the plate line PL is brought into high level, and the bit line "bl" comes into a state P31 and the complementary bit line "/bl" comes into a state P30, will be described. In this case, the potential of the bit line "bl" comes to V31 and the potential of the complementary bit line "/bl" comes to V30. As shown in Fig. 9C, the potential difference VBL between the potential v31 of the bit line "bl" and the potential V30 of the complementary bit line "/bl" becomes smaller than that of the case in Fig. 9D.

[0024] As described above, when the parasitic capacitances CBL, /CBL are excessively small or excessively large, the potential difference VBL becomes small, as shown in Figs. 9B and 9C. When the parasitic capacitances CBL, /CBL have appropriate values, the potential difference VBL becomes large as shown in Fig. 9D. In other words, when the plate line PL is brought into high level, if the polarization Q of the ferroelectric capacitor C1 and the ferroelectric capacitor C0 is excessively small or excessively large, the potential difference VBL becomes small, as shown in Figs. 9B and 9C. When the plate line PL is brought into high level, if the polarization Q of the ferroelectric capacitors C1, C0 comes to an appropriate value, the potential difference VBL becomes large, as shown in Fig. 9D. Still, in other words, as shown in Figs. 9B and 9C. when the plate line PL is brought into high level, if the potentials of the bit line "bl" and the complementary bit line "/bl" are excessively small or excessively large, the potential difference VBL becomes small. As shown in Fig. 9D, when the plate line PL is brought into high level, if the potentials of the bit line "bl" and the complementary bit line "/bl" come to appropriate values, the potential difference VBL becomes large.

-First Embodiment-

[0025] Fig. 1 is a circuit diagram showing a configuration example of a ferroelectric memory according to a first embodiment of the present invention. The ferroelectric memory in Fig. 1 is configured to have a current source 110 in addition to the ferroelectric memory in Fig. 6, having the same configuration as of the ferroelectric memory in Fig. 6 except the current source 110. Even though the description of the parasitic capacitances CBL, /CBL will be omitted for the ferroelectric memory in Fig. 1, practically, the parasitic capacitances CBL, /CBL exist in the same manner as in the case of Fig. 6. Also, the parasitic capacitances CBL, /CBL exist in ferroelectric memories in Fig. 2 and Fig. 4, which will be described later.

[0026] The current source 110 is a control circuit that is connected to the bit line "bl" and the complementary bit line "/bl" so as to lower the potentials of the bit line "bl" and the complementary bit line "/bl" when the word line WL and the plate line PL is at high level. More specifically, the current source 110 lowers such potentials of the bit line "bl" and the complementary bit line "/bl" as V21, V20 shown in Fig. 9B to such appropriate potentials as V11 and V10 shown in Fig. 9D. When the potentials of the bit line "bl" and the complementary bit line "/bl" are excessively large as shown in Fig. 9B, it is possible to increase the potential difference VBL to larger as shown in Fig. 9D, by lowering the potentials of the bit line "bl" and the complementary bit line "/bl" using the current source 110.

-Second Embodiment-

[0027] Fig. 2 is a circuit diagram showing a configuration example of a ferroelectric memory according to a second embodiment of the present invention, in which the ferroelectric memory is embodied in more concrete form than that of the first embodiment. The second embodiment is basically the same as the first embodiment, and the description below will be given for differences. In the present embodiment, a reference circuit 200 is additionally provided and the current source 110 is embodied in more concrete form. The current source 110 includes n-channel transistors Q00, Q01, Q10, Q11 and switching elements 203, 204.

[0028] The ferroelectric memory includes a number of memory cells, allowing a number of data to be stored. A single memory cell includes the two transistors 103, 104 and the two ferroelectric capacitors C1, C0. The single reference circuit 200 is provided for a number of memory cells.

[0029] The reference circuit 200 includes the transistors 103, 104, the ferroelectric capacitors C1, C0, a bit line RBL, a complementary bit line /RBL, and the sense amplifier 101 in the same manner as in the memory cell. Although the bit line RBL and the complementary bit line /RBL have the same configurations as of the bit line "bl" and the complementary bit line "/bl" and have parasitic capacitances CBL, /CBL, different reference numbers are used for the purpose of distinguishing them. In the reference circuit 200 and the memory cell, the gates of the transistors 103, 104 are connected to the same word line WL, and also the plate line PL is used in common. However, in the reference circuit 200, the ferroelectric capacitor C1 stores fixed data "1" and the ferroelectric capacitor C0 stores fixed data "0 (zero)". The ferroelectric capacitor C0 and the ferroelectric capacitor C1 store fixed data complementing each other.

[0030] As for an n-channel transistor QR1, the gate and the drain are connected to each other and the source is connected to the ground potential (reference potential) via a switching element 201. The mutual connection point of the gate and the drain is connected to the reference bit line RBL. As for an n-channel transistor QR0 (zero), the gate and the drain are connected to each other and the source is connected to the ground potential via a switching element 202. The mutual connection point of the gate and the drain is connected to the complementary reference bit line /RBL.

[0031] Subsequently, the configuration of the current source 110 will be described. As for the n-channel transistor Q11, the gate is connected to the reference bit line "RBL", the drain is connected to the bit line "bl", and the source is connected to the ground potential via the switching element 203. As for the n-channel transistor Q10, the gate is connected to the complementary reference bit line /RBL, the drain is connected to the bit line "bl", and the source is connected to the ground potential via the switching elements 203. The transistor Q10 and the transistor Q11 are connected in parallel to each other.

[0032] As for the n-channel transistor Q01, the gate is connected to the reference bit line RBL, the drain is connected to the complementary bit line "/bl", and the source is connected to the ground potential via the switching elements 204. As for the n-channel transistor Q00, the gate is connected to the complementary reference bit line /RBL, the drain is connected to the complementary bit line "/bl", the source is connected to the ground potential via the switching elements 204. The transistor Q01 and the transistor Q00 are connected in parallel to each other. The transistors QR1, Q11, and Q01 configure a current mirror circuit and the same current flows therein. The transistors QR0, Q10, Q00 configure a current mirror circuit and the same current flows therein.

[0033] The reference circuit 200 is a circuit to cause the same current as of the actual memory cell to flow with the help of the current mirror circuit. The currents flowing in the transistors QR1, QR0 are represented by Ir1 and Ir0, and the currents flowing in the transistors Q11, Q10, Q01, Q00 are represented by I11, I10, I01, I00, respectively. Then, the relation can be expressed by the following equation.

$$Ir1 + Ir0 = I11 + I10 = I01 + I00$$

[0034] As a result, since the same charge amounts are pulled out from the bit line "bl" and the complementary bit line "/bl" to thereby lower the potentials of the bit line "bl" and the complementary bit line "/bl", so that the potential difference VBL increases as shown in Fig. 9D.

[0035] Fig. 3 is a timing chart for illustrating an operation of the ferroelectric memory in Fig. 2. Before a time "t1" the word line WL and the plate line PL are at low level. When the word line WL is at low level, the transistors 103, 104 are turned OFF, and the reference bit line RBL, the complementary reference bit line /RBL, the bit line "bl", and the complementary bit line "/bl" come to 0V. The sense amplifier (SA) 101 is in an inactive state. The switching elements 201 to 204 are turned OFF (disconnected).

[0036] Subsequently, at the time "t1", when the word line WL comes into high level, the transistors 103, 104 are turned ON. The reference bit line RBL is connected to the ferroelectric capacitor C1, the complementary reference bit line /RBL is connected to the ferroelectric capacitor C0, the bit line "bl" is connected to the ferroelectric capacitor C1, and the complementary bit line "/bl" is connected to the ferroelectric capacitor C0. Since the plate line PL is at 0V, the bit lines RBL, /RBL, "bl", "/bl" are at 0V.

[0037] Subsequently, between the time "t1" and a time "t2", the switching elements 201 to 204 are turned ON (connected).

[0038] Subsequently, at the time "t2", the plate line PL is brought into high level (for example to VP). The reference bit line RBL increases toward the potential V21, whereas it falls in due time to a threshold voltage Vth of the transistor QR1 affected by the transistor QR1. Similarly, the complementary reference bit line /RBL increases toward the potential V21, whereas it falls in due time to the threshold voltage Vth of the transistor QR0 affected by the transistor QR0.

[0039] To the gates of the transistors Q11, Q01, the potentials Vth of the reference bit line RBL are supplied. To the

gates of the transistors Q10, Q00, the potentials Vth of the complementary reference bit line /RBL are supplied. The transistors Q11, Q10, Q01, Q00 serve as the current source.

[0040] The bit line "bl" increases toward the potential V21, whereas the transistors Q11 and Q10 pull out charge from the bit line "bl", so that the potential lowers to the appropriate value. This appropriate value is a potential larger than 0V. Similarly, the complementary bit line "/bl" increases toward the potential V20, whereas the transistors Q01 and Q00 pull out charge from the complementary bit line "/bl", so that the potential lowers to the appropriate value. This appropriate value is a potential smaller than the potential of the bit line "bl". The potential difference VBL between the bit line "bl" and the complementary bit line "/bl" becomes a larger appropriate value. After that, the switching elements 201 to 204 are tuned OFF.

[0041] Subsequently, at a time "t3", when the sense amplifier (SA) 101 is activated, the potential difference VBL between the bit line "bl" and the complementary bit line "/bl" is amplified. Specifically, the bit line "bl" comes to high level (power source potential) and the complementary bit line "/bl" comes to low level (0V). In accordance with the potentials of the bit line "bl" and the complementary bit line "/bl", readout data can be outputted to outside.

[0042] After that, the plate line PL is brought into low level, the sense amplifier (SA) 101 is inactivated, and the word line WL is brought into low level.

[0043] As described above, even in the case where the potentials of the bit line "bl" and the complementary bit line "/bl" are excessively large as in Fig. 9B, it is possible to lower the potentials of the bit line "bl" and the complementary bit line "/bl" to the appropriate values as in Fig. 9D by pulling out charges from the bit line "bl" and the complementary bit line "/bl" using the current source 110, so that the potential difference VBL can be increased. A large potential difference VBL allows correct data to be outputted to outside. Note that, when the potentials of the bit line "bl" and the complementary bit line "/bl" are appropriate from the beginning, no charge is pulled out by the current source 110, allowing normal operation.

[0044] According to the present embodiment, even if the bit lines "bl", "/bl" have small parasitic capacitances, the bit lines "bl", "/bl" require no capacitance to be added, so that area increase and fluctuation in the potential difference VBL can be prevented. Without regard to the parasitic capacitances of the bit lines "bl", "/bl", it is possible to increase the potential difference VBL that is read out from the ferroelectric capacitors C1, C0 to the bit lines "bl", "/bl" in accordance with the data stored in the ferroelectric capacitors C1, C0. On the back of this, the readout data can be improved in reliability. Specifically, when the bit lines "bl", "/bl" have small capacitances, stable bit-line potentials can be obtained without the need to add new capacitance.

-Third Embodiment-

[0045] Fig. 4 is a circuit diagram showing a configuration example of a ferroelectric memory according to a third embodiment of the present invention, in which the ferroelectric memory is embodied in more concrete form than that of the first embodiment. The third embodiment is basically the same as the second embodiment, and the description below will be given for differences.

[0046] According to the present embodiment, the transistor 104, the ferroelectric capacitor C0, the complementary reference bit line /RBL, the sense amplifier 101, the transistor QR0, and the switching element 202 of the second embodiment (Fig. 2) are removed from the reference circuit 200. Further, according to the present embodiment, the transistors Q10, Q00 of the second embodiment (Fig. 2) are removed from the current source 110.

[0047] That is, the reference circuit 200 includes a single transistor 103 and a single ferroelectric capacitor C1, which always generate fixed data "1" as a memory cell. The potential of the reference bit line RBL generated in the reference circuit 200 is supplied to the gates of the transistors Q11, Q01 connected to the actual memory cell.

[0048] Fig. 5 is a timing chart for illustrating an operation of the ferroelectric memory in Fig. 4. The description is the same as of Fig. 3 up to the time "t2".

[0049] When the plate line PL is brought into high level (for example to VP) at the time "t2", the reference bit line RBL increases toward the potential V21, whereas falls in due time to the threshold voltage Vth of the transistor QR1 affected by the transistor QR1. The potential Vth of the reference bit line RBL is supplied to the gates of the transistors Q11, Q01.

[0050] The bit line "bl" increases toward the potential V21, whereas the potential falls to the appropriate value, since the transistor Q11 pulls out charge from the bit line "bl". Similarly, the complementary bit line "/bl" increases toward the potential V20, whereas the potential falls to the appropriate value, since the transistor Q01 pulls out charge from the complementary bit line "/bl". The potential difference VBL between the bit line "bl" and the complementary bit line "/bl" becomes a large appropriate value. Subsequent description is the same as of Fig. 3.

[0051] As has been described above, according to the first to third embodiments, without regard to the capacitances of the bit lines "bl", "/bl", it is possible to increase the potentials of the bit lines "bl", "/bl" to appropriate values, so that the potential difference VBL can be increased to larger. A large potential difference VBL allows correct data to be outputted to outside. Even when the bit lines "bl", "/bl" have small capacitances, the bit lines "bl", "/bl" require no capacitance to be added, so that area increase and fluctuation in the potential difference VBL can be prevented.

[0052] In should be noted that any of the above-described embodiments are merely concrete examples to implement the present invention, and it is to be understood that the technical scope of the present invention will not be construed restrictive by these embodiments. In other words, the present invention can be realized in various forms without departing from the technological spirit and the main features thereof.

[0053] It is possible to increase the potential difference that is read out from the ferroelectric capacitor to the bit line in accordance with the data stored in the ferroelectric capacitor, without regard to the capacitance value of the bit line. Backed by this, the readout data can be improved in reliability. In other words, when the bit line has small capacitance, it is possible to obtain stable bit line potential without the need to add new capacitance.

[0054] The present embodiments are to be considered in all respects as illustrative and no restrictive, and all changes which come within the meaning and range of equivalency of the claims are therefore intended to be embraced therein. The invention may be embodied in other specific forms without departing from the essential characteristics thereof as set art in the independent claim.

Claims

1. A ferroelectric memory comprising:

ferroelectric capacitors (C0, C1) to store data that complement each other;
a bit line (bl) inputting and outputting data with respect to a first one (C1) of said ferroelectric capacitors;
a complementary bit line (/bl) inputting and outputting data with respect to a second one (C0) of said ferroelectric capacitors;
a first switching element (103) selectively connecting said first ferroelectric capacitor (C1) and said bit line (bl);
a second switching element (104) selectively connecting said second ferroelectric capacitor (C0) and said complementary bit line (/bl);
a control circuit (110) including a first field effect transistor (Q11) to be connected to said bit line (bl) and a reference potential, and to lower potential of said bit line (bl) when said bit line (bl) is connected to said first ferroelectric capacitor (C1); and
a second field effect transistor (QR1) to be connected to a reference bit line (RBL) and the reference potential, wherein said first field effect transistor (Q11) and said second field effect transistor (QR1) configure a current mirror circuit,
characterized by
a reference ferroelectric capacitor (C1) to store fixed data, wherein the reference bit line (RBL) inputs and outputs data with respect to said reference ferroelectric capacitor (C1); and
a reference switching element (103) selectively connecting said reference ferroelectric capacitor (C1) and said reference bit line (RBL); and in that
the gate and the drain of the second field effect transistor (QR1) are connected to each other so that the current flow of the reference bit line (RBL) controls the current flow of the bit line (bl) and the complementary bit line (/bl), and
the reference potential is a ground potential.

2. The ferroelectric memory according to claim 1, further comprising:

a complementary ferroelectric capacitor to store complementary data with respect to the data stored in the ferroelectric capacitor;
a complementary bit line to input and output data with respect to said complementary ferroelectric capacitor; and
a second switching element selectively connecting said complementary ferroelectric capacitor and the complementary bit line,
wherein said control circuit lowers the potentials of said bit line and said complementary bit line when said bit line is connected to said ferroelectric capacitor and said complementary bit line is connected to said complementary ferroelectric capacitor.

3. The ferroelectric memory according to claim 2, further comprising a sense amplifier to amplify a potential difference between said bit line and said complementary bit line.

4. The ferroelectric memory according to claim 3,
wherein said control circuit includes said first field effect transistor to be connected to said bit line and the reference potential and a third field effect transistor to be connected to said complementary bit line and the reference potential.

5. The ferroelectric memory according to claim 4, further comprising:

a complementary reference ferroelectric capacitor to store complementary fixed data with respect to the fixed data stored by the reference ferroelectric capacitor;
a complementary reference bit line to input and output data with respect to said complementary reference ferroelectric capacitor;
a complementary reference switching element selectively connecting said complementary reference ferroelectric capacitor and said complementary reference bit line;
a fourth field effect transistor to be connected to said complementary reference bit line and the reference potential;
a fifth field effect transistor to be connected in parallel to said first field effect transistor; and
a sixth field effect transistor to be connected in parallel to said third field effect transistor,
wherein said first field effect transistor, said second field effect transistor, and said third field effect transistor configure a current mirror circuit, and said fourth field effect transistor, said fifth field effect transistor, and said sixth field effect transistor configure a current mirror circuit.

6. The ferroelectric memory according to claim 1,
wherein said control circuit lowers the potential of said bit line to a first potential being larger than 0V.

7. The ferroelectric memory according to claim 1,
wherein a gate and a drain of said second field effect transistor are connected to each other and a mutual connection point thereof is connected to a gate of said first field effect transistor.

8. The ferroelectric memory according to claim 4,
wherein a gate and a drain of said second field effect transistor are connected to each other and a mutual connection point thereof is connected to a gate of said first field effect transistor.

9. The ferroelectric memory according to claim 1, further comprising:

a second switching element to connect or disconnect said bit line and the reference potential via said first field effect transistor; and
a third switching element to connect or disconnect said reference bit line and the reference potential via said second field effect transistor.

10. The ferroelectric memory according to claim 4, further comprising:

a third switching element to connect or disconnect said bit line and the reference potential via said first field effect transistor;
a fourth switching element to connect or disconnect said reference bit line and the reference potential via said second field effect transistor; and
a fifth switching element to connect or disconnect said complementary bit line and the reference potential via said third field effect transistor.

11. The ferroelectric memory according to claim 5,
wherein a gate and a drain of said second field effect transistor are connected to each other and a mutual connection point thereof is connected to gates of said first field effect transistor and said third field effect transistor, and
wherein a gate and a drain of said fourth field effect transistor are connected to each other and a mutual connection point thereof is connected to gates of said fifth field effect transistor and said sixth field effect transistor.

12. The ferroelectric memory according to claim 5, further comprising:

a third switching element to connect or disconnect said bit line and the reference potential via said first field effect transistor and said fifth field effect transistor;
a fourth switching element to connect or disconnect said complementary bit line and the reference potential via said third field effect transistor and said sixth field effect transistor;
a fifth switching element to connect or disconnect said reference bit line and the reference potential via said second field effect transistor; and
a sixth switching element to connect or disconnect said complementary reference bit line and the reference potential via said fourth field effect transistor.

13. The ferroelectric memory according to claim 5, further comprising a sense amplifier to amplify a potential difference between said reference bit line and said complementary reference bit line.

14. The ferroelectric memory according to claim 12, further comprising a sense amplifier to amplify a potential difference between said reference bit line and said complementary reference bit line.

Patentansprüche

1. Ferroelektrischer Speicher mit:

ferroelektrischen Kondensatoren (C0, C1), um Daten zu speichern, die einander komplementieren;
einer Bitleitung (bl), die Daten bezüglich eines ersten (C1) der ferroelektrischen Kondensatoren eingibt und ausgibt;
einer komplementären Bitleitung (/bl), die Daten bezüglich eines zweiten (C0) der ferroelektrischen Kondensatoren eingibt und ausgibt;
einem ersten Schaltelement (103), das den ersten ferroelektrischen Kondensator (C1) und die Bitleitung (bl) selektiv verbindet;
einem zweiten Schaltelement (104), das den zweiten ferroelektrischen Kondensator (C0) und die komplementäre Bitleitung (/bl) selektiv verbindet;
einer Steuerschaltung (110), die einen ersten Feldeffekttransistor (Q11) enthält, um mit der Bitleitung (bl) und einem Referenzpotential verbunden zu werden und um das Potential der Bitleitung (bl) zu verringern, wenn die Bitleitung (bl) mit dem ersten ferroelektrischen Kondensator (C1) verbunden ist; und
einem zweiten Feldeffekttransistor (QR1), um mit einer Referenzbitleitung (RBL) und dem Referenzpotential verbunden zu werden,
bei dem der erste Feldeffekttransistor (Q11) und der zweite Feldeffekttransistor (QR1) eine Stromspiegelschaltung konfigurieren,
gekennzeichnet durch
einen ferroelektrischen Referenzkondensator (C1), um feste Daten zu speichern, bei dem die Referenzbitleitung (RBL) Daten bezüglich des ferroelektrischen Referenzkondensators (C1) eingibt und ausgibt; und
ein Referenzschaltelement (103), das den ferroelektrischen Referenzkondensator (C1) und die Referenzbitleitung (RBL) selektiv verbindet; und **dadurch, dass**
das Gate und der Drain des zweiten Feldeffekttransistors (QR1) miteinander verbunden sind, so dass der Stromfluss der Referenzbitleitung (RBL) den Stromfluss der Bitleitung (bl) und der komplementären Bitleitung (/bl) steuert, und
das Referenzpotential ein Erdpotential ist.

2. Ferroelektrischer Speicher nach Anspruch 1, ferner mit:

einem komplementären ferroelektrischen Kondensator, um komplementäre Daten bezüglich der in dem ferroelektrischen Kondensator gespeicherten Daten zu speichern;
einer komplementären Bitleitung, um Daten bezüglich des komplementären ferroelektrischen Kondensators einzugeben und auszugeben; und
einem zweiten Schaltelement, das den komplementären ferroelektrischen Kondensator und die komplementäre Bitleitung selektiv verbindet,
bei dem die Steuerschaltung die Potentiale der Bitleitung und der komplementären Bitleitung verringert, wenn die Bitleitung mit dem ferroelektrischen Kondensator verbunden ist und die komplementäre Bitleitung mit dem komplementären ferroelektrischen Kondensator verbunden ist.

3. Ferroelektrischer Speicher nach Anspruch: 2,
ferner mit einem Leseverstärker, um eine Potentialdifferenz zwischen der Bitleitung und der komplementären Bitleitung zu verstärken.

4. Ferroelektrischer Speicher nach Anspruch 3,
bei dem die Steuerschaltung den ersten Feldeffekttransistor enthält, um mit der Bitleitung und dem Referenzpotential verbunden zu werden, und einen dritten Feldeffekttransistor, um mit der komplementären Bitleitung und dem Referenzpotential verbunden zu werden.

5. Ferroelektrischer Speicher nach Anspruch 4, ferner mit:

einem komplementären ferroelektrischen Referenzkondensator, um komplementäre feste Daten bezüglich der durch den ferroelektrischen Referenzkondensator gespeicherten festen Daten zu speichern;
einer komplementären Referenzbitleitung, um Daten bezüglich des komplementären ferroelektrischen Referenzkondensators einzugeben und auszugeben;
einem komplementären Referenzschaltelement, das den komplementären ferroelektrischen Referenzkondensator und die komplementäre Referenzbitleitung selektiv verbindet;
einem vierten Feldeffekttransistor, um mit der komplementären Referenzbitleitung und dem Referenzpotential verbunden zu werden;
einem fünften Feldeffekttransistor, um mit dem ersten Feldeffekttransistor parallel verbunden zu werden; und
einem sechsten Feldeffekttransistor, um mit dem dritten Feldeffekttransistor parallel verbunden zu werden,
bei dem der erste Feldeffekttransistor, der zweite Feldeffekttransistor und der dritte Feldeffekttransistor eine Stromspiegelschaltung konfigurieren und der vierte Feldeffekttransistor, der fünfte Feldeffekttransistor und der sechste Feldeffekttransistor eine Stromspiegelschaltung konfigurieren.

6. Ferroelektrischer Speicher nach Anspruch 1, bei dem die Steuerschaltung das Potential der Bitleitung auf ein erstes Potential verringert, das größter als 0 V ist.

7. Ferroelektrischer Speicher nach Anspruch 1, bei dem ein Gate und ein Drain des zweiten Feldeffekttransistors miteinander verbunden sind und ein gemeinsamer Verbindungspunkt derselben mit einem Gate des ersten Feldeffekttransistors verbunden ist.

8. Ferroelektrischer Speicher nach Anspruch 4, bei dem ein Gate und ein Drain des zweiten Feldeffekttransistors miteinander verbunden sind und ein gemeinsamer Verbindungspunkt derselben mit einem Gate des ersten Feldeffekttransistors verbunden ist.

9. Ferroelektrischer Speicher nach Anspruch 1, ferner mit:

einem zweiten Schaltelement, um die Bitleitung und das Referenzpotential über den ersten Feldeffekttransistor zu verbinden oder zu trennen; und
einem dritten Schaltelement, um die Referenzbitleitung und das Referenzpotential über den zweiten Feldeffekttransistor zu verbinden oder zu trennen.

10. Ferroelektrischer Speicher nach Anspruch 4, ferner mit:

einem dritten Schaltelement, um die Bitleitung und das Referenzpotential über den ersten Feldeffekttransistor zu verbinden oder zu trennen;
einem vierten Schaltelement, um die Referenzbitleitung und das Referenzpotential über den zweiten Feldeffekttransistor zu verbinden oder zu trennen; und
einem fünften Schaltelement, um die komplementäre Bitleitung und das Referenzpotential über den dritten Feldeffekttransistor zu verbinden oder zu trennen.

11. Ferroelektrischer Speicher nach Anspruch 5, bei dem ein Gate und ein Drain des zweiten Feldeffekttransistors miteinander verbunden sind und ein gemeinsamer Verbindungspunkt derselben mit Gates des ersten Feldeffekttransistors und des dritten Feldeffekttransistors verbunden ist und
bei dem ein Gate und ein Drain des vierten Feldeffekttransistors miteinander verbunden sind und ein gemeinsamer Verbindungspunkt derselben mit Gates des fünften Feldeffekttransistors und des sechsten Feldeffekttransistors verbunden ist.

12. Ferroelektrischer Speicher nach Anspruch 5, ferner mit:

einem dritten Schaltelement, um die Bitleitung und das Referenzpotential über den ersten Feldeffekttransistor

und den fünften Feldeffekttransistor zu verbinden oder zu trennen;
einem vierten Schaltelement, um die komplementäre Bitleitung und das Referenzpotential über den dritten Feldeffekttransistor und den sechsten Feldeffekttransistor zu verbinden oder zu trennen;
einem fünften Schaltelement, um die Referenzbitleitung und das Referenzpotential über den zweiten Feldeffekttransistor zu verbinden oder zu trennen; und
einem sechsten Schaltelement, um die komplementäre Referenzbitleitung und das Referenzpotential über den vierten Feldeffekttransistor zu verbinden oder zu trennen.

13. Ferroelektrischer Speicher nach Anspruch 5,
ferner mit einem Leseverstärker, um eine Potentialdifferenz zwischen der Referenzbitleitung und der komplementären Referenzbitleitung zu verstärken.

14. Ferroelektrischer Speicher nach Anspruch 12,
ferner mit einem Leseverstärker, um eine Potentialdifferenz zwischen der Referenzbitleitung und der komplementären Referenzbitleitung zu verstärken.

Revendications

1. Mémoire ferroélectrique comprenant :

des condensateurs ferroélectriques (C0, C1) pour mémoriser des données qui se complémentent l'une l'autre ;
une ligne de bit (bl) entrant et sortant une donnée en ce qui concerne un premier (C1) desdits condensateurs ferroélectriques ;
une ligne de bit complémentaire (/bl) entrant et sortant une donnée en ce qui concerne un second (C0) desdits condensateurs ferroélectriques ;
un premier élément (103) de commutation connectant sélectivement ledit premier condensateur ferroélectrique (C1) et ladite ligne de bit (bl) ;
un deuxième élément (104) de commutation connectant sélectivement ledit second condensateur ferroélectrique (C0) et ladite ligne de bit complémentaire (/bl) ;
un circuit (110) de commande incluant un premier transistor (Q11) à effet de champ destiné à être connecté à ladite ligne de bit (bl) et à un potentiel de référence, et à un potentiel plus bas de ladite ligne de bit (bl) lorsque ladite ligne de bit (bl) est connectée audit premier condensateur ferroélectrique (C1) ; et
un deuxième transistor (QR1) à effet de champ destiné à être connecté à une ligne de bit (RBL) de référence et au potentiel de référence,
dans laquelle ledit premier transistor (Q11) à effet de champ et ledit deuxième transistor (QR1) à effet de champ configurent un circuit miroir de courant,
caractérisée :

par un condensateur ferroélectrique (C1) de référence pour mémoriser une donnée fixe, la ligne de bit (RBL) de référence entrant et sortant une donnée en ce qui concerne ledit condensateur ferroélectrique (C1) de référence ; et
par un élément de commutation (103) de référence connectant sélectivement ledit condensateur ferroélectrique (C1) de référence et ladite ligne de bit (RBL) de référence ; et
en ce que la grille et le drain du deuxième transistor (QR1) à effet de champ sont connectés l'un à l'autre de sorte que le passage de courant dans la ligne de bit (RBL) de référence commande le passage de courant dans la ligne de bit (bl) et dans la ligne de bit complémentaire (/bl) ; et
en ce que le potentiel de référence est le potentiel de la masse.

2. Mémoire ferroélectrique selon la revendication 1, comprenant en outre :

un condensateur ferroélectrique complémentaire pour mémoriser une donnée complémentaire par rapport à la donnée mémorisée dans le condensateur ferroélectrique ;
une ligne de bit complémentaire pour entrer et sortir une donnée en ce qui concerne ledit condensateur ferroélectrique complémentaire ; et
un deuxième élément de commutation connectant sélectivement ledit condensateur ferroélectrique complémentaire et la ligne de bit complémentaire,
dans laquelle ledit circuit de commande abaisse les potentiels de ladite ligne de bit et de ladite ligne de bit

complémentaire lorsque ladite ligne de bit est connectée audit condensateur ferroélectrique et que ladite ligne de bit complémentaire est connectée audit condensateur ferroélectrique complémentaire.

3. Mémoire ferroélectrique selon la revendication 2, comprenant en outre un amplificateur de lecture pour amplifier une différence de potentiel entre ladite ligne de bit et ladite ligne de bit complémentaire.

4. Mémoire ferroélectrique selon la revendication 3, dans laquelle ledit circuit de commande inclut ledit premier transistor à effet de champ destiné à être connecté à ladite ligne de bit et au potentiel de référence et un troisième transistor à effet de champ destiné à être connecté à ladite ligne de bit complémentaire et au potentiel de référence.

5. Mémoire ferroélectrique selon la revendication 4, comprenant en outre :

un condensateur ferroélectrique de référence complémentaire pour mémoriser une donnée fixe complémentaire par rapport à la donnée fixe mémorisée dans le condensateur ferroélectrique de référence ;
une ligne de bit de référence complémentaire pour entrer et sortir une donnée en ce qui concerne ledit condensateur ferroélectrique de référence complémentaire ;
un élément de commutation de référence complémentaire connectant sélectivement ledit condensateur ferroélectrique de référence complémentaire et ladite ligne de bit de référence complémentaire ;
un quatrième transistor à effet de champ destiné à être connecté à ladite ligne de bit de référence complémentaire et au potentiel de référence ;
un cinquième transistor à effet de champ destiné à être connecté en parallèle audit premier transistor à effet de champ ; et
un sixième transistor à effet de champ destiné à être connecté en parallèle audit troisième transistor à effet de champ,
dans laquelle ledit premier transistor à effet de champ, ledit deuxième transistor à effet de champ et ledit troisième transistor à effet de champ configurent un circuit miroir de courant, et dans laquelle ledit quatrième transistor à effet de champ, ledit cinquième transistor à effet de champ et ledit sixième transistor à effet de champ configurent un circuit miroir de courant.

6. Mémoire ferroélectrique selon la revendication 1, dans laquelle ledit circuit de commande abaisse le potentiel de ladite ligne de bit jusqu'à un premier potentiel qui est plus grand que 0 V.

7. Mémoire ferroélectrique selon la revendication 1, dans laquelle la grille et le drain dudit deuxième transistor à effet de champ sont connectés l'un à l'autre et leur point de connexion mutuel est connecté à la grille dudit premier transistor à effet de champ.

8. Mémoire ferroélectrique selon la revendication 4, dans laquelle la grille et le drain dudit deuxième transistor à effet de champ sont connectés l'un à l'autre et leur point de connexion mutuel est connecté à la grille dudit premier transistor à effet de champ.

9. Mémoire ferroélectrique selon la revendication 1 comprenant en outre :

un deuxième élément de commutation pour connecter ou déconnecter ladite ligne de bit et le potentiel de référence via ledit premier transistor à effet de champ ; et
un troisième élément de commutation pour connecter ou déconnecter ladite ligne de bit de référence et le potentiel de référence via ledit deuxième transistor à effet de champ.

10. Mémoire ferroélectrique selon la revendication 4, comprenant en outre :

un troisième élément de commutation pour connecter ou déconnecter ladite ligne de bit et le potentiel de référence via ledit premier transistor à effet de champ ;
un quatrième élément de commutation pour connecter ou déconnecter ladite ligne de bit de référence et le potentiel de référence via ledit deuxième transistor à effet de champ ; et
un cinquième élément de commutation pour connecter ou déconnecter ladite ligne de bit complémentaire et le potentiel de référence via ledit troisième transistor à effet de champ.

11. Mémoire ferroélectrique selon la revendication 5,
dans laquelle la grille et le drain dudit deuxième transistor à effet de champ sont connectés l'un à l'autre et leur point

de connexion mutuel est connecté aux grilles dudit premier transistor à effet de champ et dudit troisième transistor à effet de champ ; et
dans laquelle la grille et le drain dudit quatrième transistor à effet de champ sont connectés l'un à l'autre et leur point de connexion mutuel est connecté aux grilles dudit cinquième transistor à effet de champ et dudit sixième transistor à effet de champ.

12. Mémoire ferroélectrique selon la revendication 5, comprenant en outre :

un troisième élément de commutation pour connecter ou déconnecter ladite ligne de bit et le potentiel de référence via ledit premier transistor à effet de champ et ledit cinquième transistor à effet de champ ;
un quatrième élément de commutation pour connecter ou déconnecter ladite ligne de bit complémentaire et le potentiel de référence via ledit troisième transistor à effet de champ et ledit sixième transistor à effet de champ ;
un cinquième élément de commutation pour connecter ou déconnecter ladite ligne de bit de référence et le potentiel de référence via ledit deuxième transistor à effet de champ ; et
un sixième élément de commutation pour connecter ou déconnecter ladite ligne de bit de référence complémentaire et le potentiel de référence via ledit quatrième transistor à effet de champ.

13. Mémoire ferroélectrique selon la revendication 5, comprenant en outre un amplificateur de lecture pour amplifier une différence de potentiel entre ladite ligne de bit de référence et ladite ligne de bit de référence complémentaire.

14. Mémoire ferroélectrique selon la revendication 12, comprenant en outre un amplificateur de lecture pour amplifier une différence de potentiel entre ladite ligne de bit de référence et ladite ligne de bit de référence complémentaire.

FIG. 1

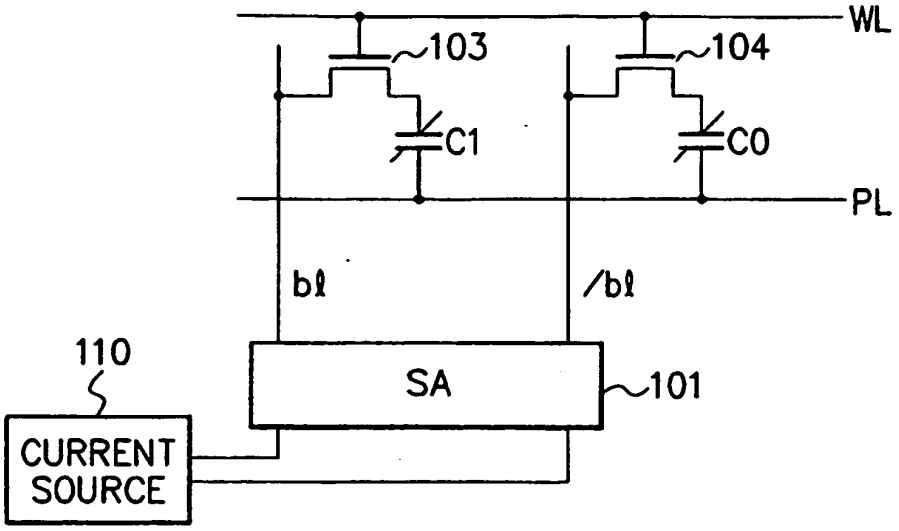
WL
103
104
C1
C0
PL
bl
/bl
110
SA
101
CURRENT SOURCE

FIG. 2

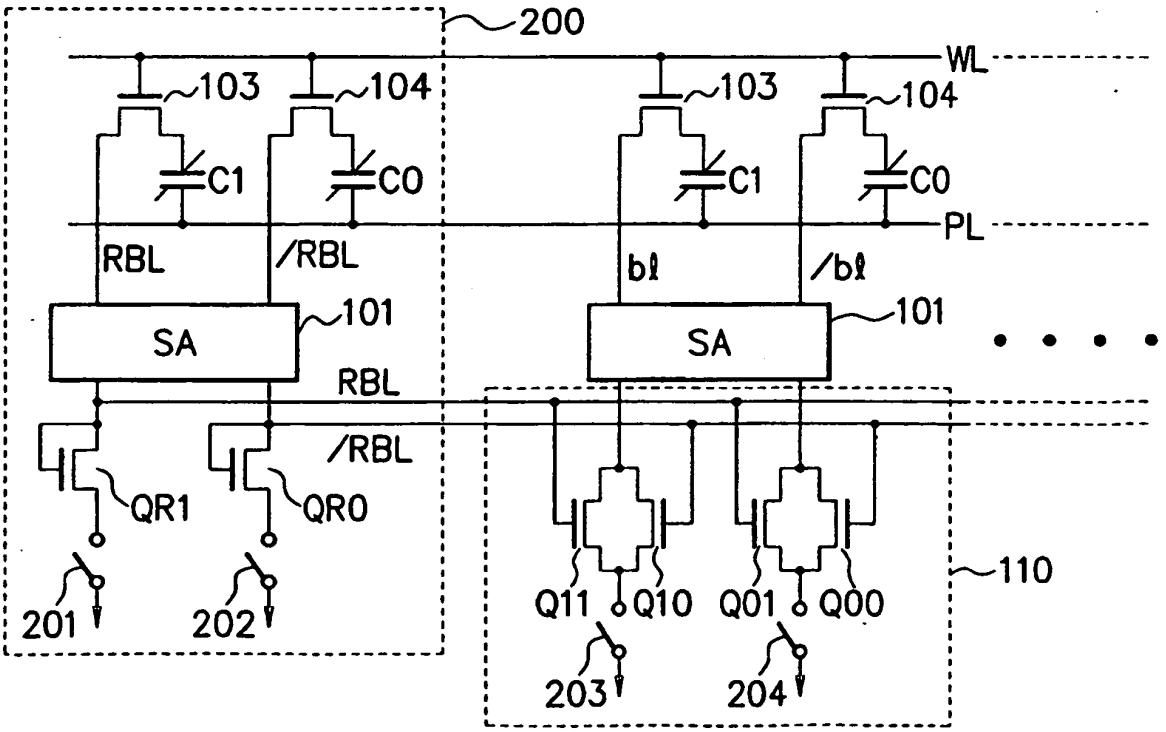
200
WL
103
104
C1
C0
PL
RBL
/RBL
bl
/bl
SA
101
RBL
/RBL
QR1
QR0
201
202
Q11
Q10
Q01
Q00
203
204
110

FIG. 3

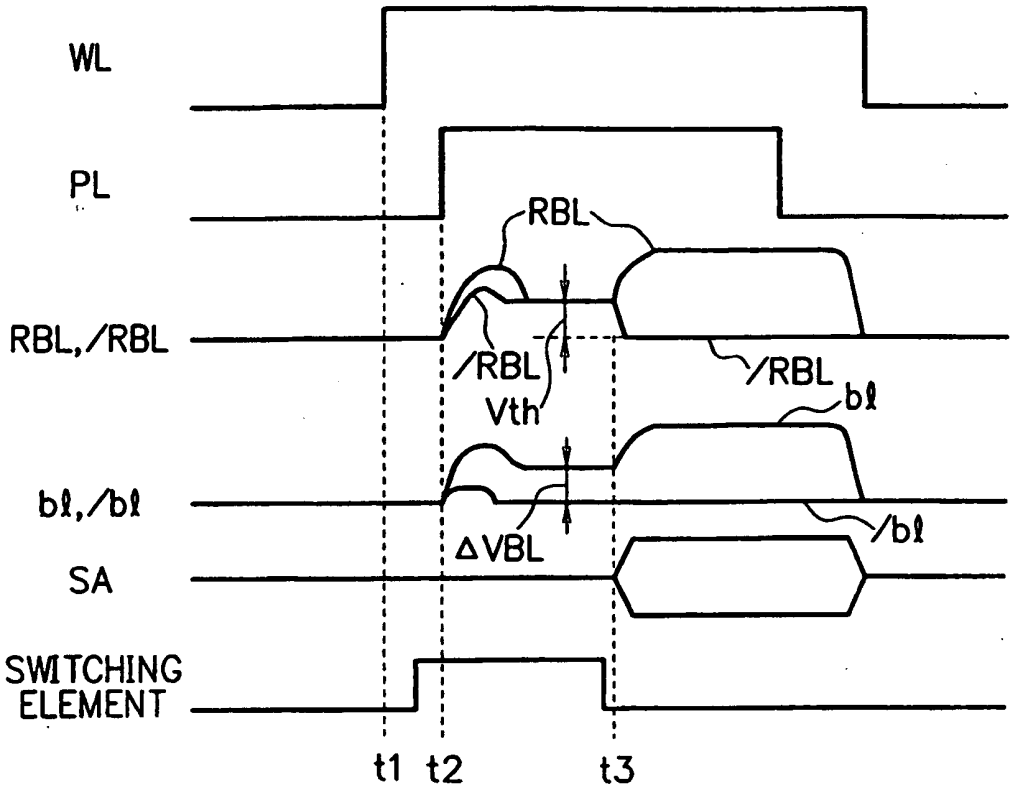
WL
PL
RBL
RBL,/RBL
/RBL
Vth
/RBL
bl
bl,/bl
/bl
ΔVBL
SA
SWITCHING ELEMENT
t1
t2
t3

FIG. 4

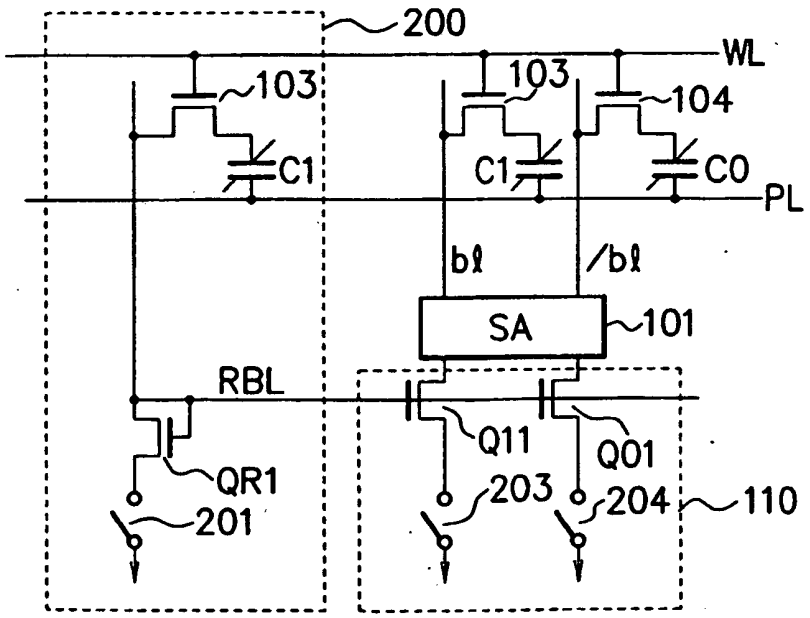
200
WL
103
103
104
C1
C1
C0
PL
bl
/bl
SA
101
RBL
Q11
Q01
QR1
203
204
110
201

FIG. 5

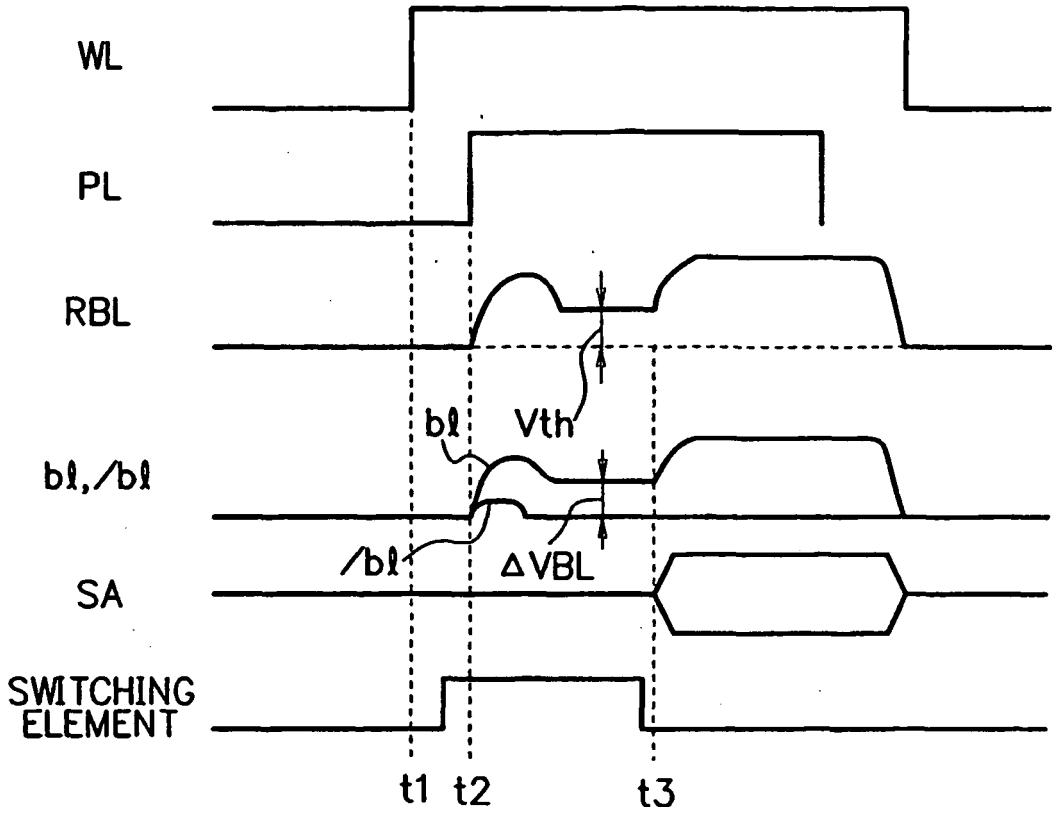
WL
PL
RBL
bl
Vth
bl,/bl
/bl
ΔVBL
SA
SWITCHING ELEMENT
t1
t2
t3

FIG. 6

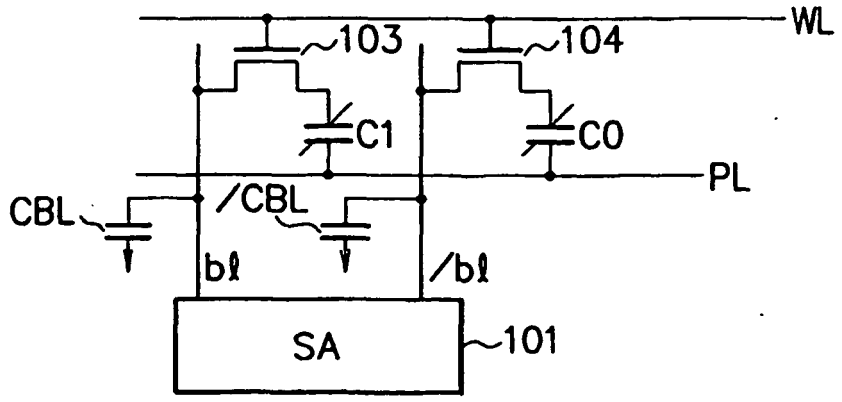
WL
103
104
C1
C0
PL
CBL
/CBL
bl
/bl
SA
101

FIG. 7

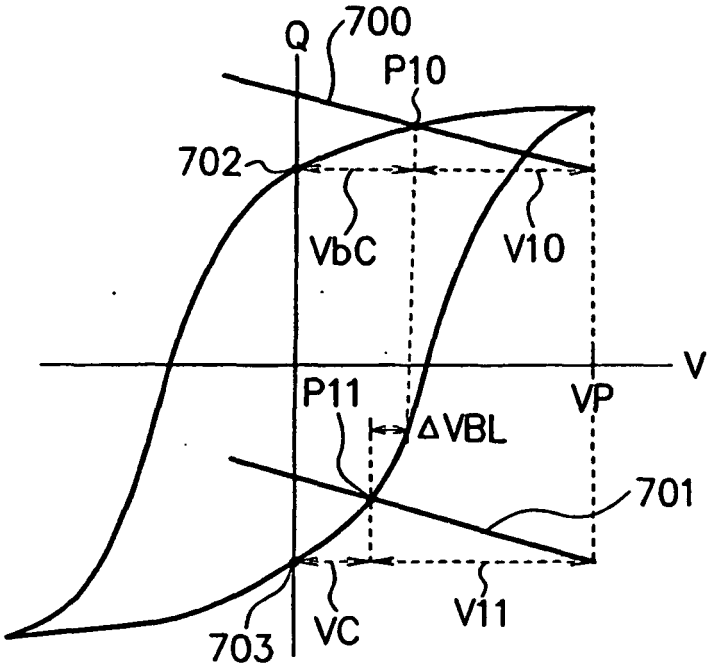

FIG. 8

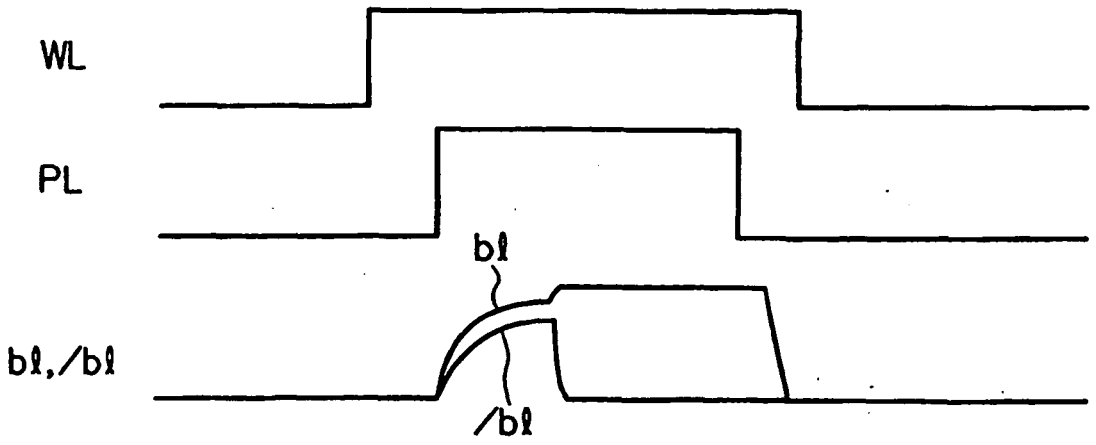

FIG. 9A

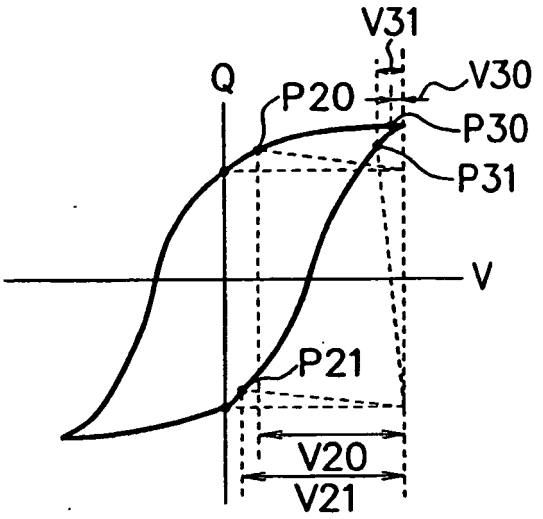

FIG. 9B

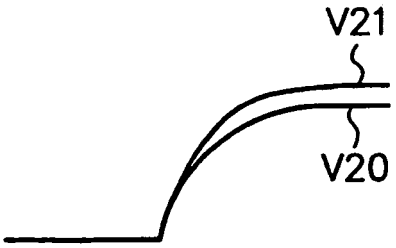

FIG. 9C

FIG. 9D

REFERENCES CITED IN THE DESCRIPTION

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Patent documents cited in the description

- JP 2004159032 A **[0001]**
- JP 2005339704 B **[0001]**
- EP 1304701 A **[0002]**
- JP 2001319472 A **[0006]**
- JP 2004013951 A **[0006]**