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(54) **Method and device used for simulating CRT impulse type image display**

(57) Disclosed is a method and a device for simulating CRT impulse type image display on a liquid crystal display (LCD) in order to improve the display quality of the hold type display and eliminate the after image and the phenomenon of image blurring.

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Description

BACKGROUND OF THE INVENTION

1. Field of the Invention

[0001] The present invention relates to a method and a device used for the simulating CRT impulse type image display, and more particularly, to a method and a device used for the simulating CRT impulse type image display with a liquid crystal display (LCD).

2. The Prior Arts

[0002] In recent years, the technology and device of liquid crystal display (LCD) have been very popular and widely used for the consumer electronic products, especially for video products, for example, television, computer, display, telephone handset, personal data assistant (PDA), and the like. The varieties of the products are enormous, so as to stimulate the tremendous rapid progress of the technology of liquid crystal display and its direction of development is in agreement with the requirement of the future trend of development of electronic products toward the features of light weight, thin thickness, short length, small size, low power consumption, and low heat dissipation, etc.

[0003] Presently, televisions and display devices made with the technology of liquid crystal display have been produced in large quantities, to replace the televisions and display devices made with the conventional CRT. However, in the liquid crystal display technology of the present days, there still exist drawbacks and limitations, which must be overcome and improved.

[0004] With regard to the image display of CRT, it utilizes the "impulse type" image display. It produces light emissions by means of irradiating a single electron beam on the pixels coated with fluorescence materials. However, as shown in curve (a) in Figure 1, the pixel only produces the emission of light in an instant of a minute portion of time in each frame period. Therefore, it seems almost no visual overlapping phenomenon will be noticed for the images displayed between the frames.

[0005] However, for the LCD image display, it utilizes the "hold type" image display due to the intrinsic property of the LCD material. It produces the image display through the optical response (namely, the gray level response) by means of applying driving voltages on the LCD material. Nevertheless, due to the limitation of the intrinsic property of the liquid crystal material, the image it displays occupies the predominant portion of time of that frame as shown in curve (c) in Figure 1. And for every time its image changes, its luminance (or brightness) also changes stepwise. Therefore, from the viewpoint of the spectators, he may feel the overlapping of the image of the new frame on that of the old frame, so as to cause the blurring of the image outlines and pro-

duce the phenomenon of the so-called "after-image".

[0006] When utilizing LCD display as the displaying device of personal computer, this after image phenomenon is not evident and usually will not be noticed, since the images it displays are static display for most of the time. However, when utilizing this LCD displaying device as television, the problem of slow LCD gray scale optical response will be more pronounced, since almost all the television programs utilize dynamic image displays. Therefore, the image displaying effectiveness of the conventional LCD television is evidently inferior to that of CRT television.

[0007] In order to eliminate the above-mentioned after image caused by the LCD display device slow optical response, and the resulting image outline blurring phenomenon, currently most LCD television manufacturers try to convert the "hold type" image display of the LCD displaying device into the simulated (or pseudo) impulse type LCD displaying device similar to that of the CRT displaying device, by means of a kind of the so-called "overdrive" technology, with its image only occupies a portion of the frame period according to the optical response as shown in curve (b) in Figure 1, namely, the image is not displayed during a portion of each frame period.

[0008] The kind of method utilized in this technology is a kind of "overdrive" method. It applies to the liquid crystal material the voltage (for example code 200) which is much higher than the originally set target voltage (for example code 120), so as to expedite and accelerate the response speed of the liquid crystal molecules, and accelerating them to reach the predetermined optical response value, and as such shortening the liquid crystal gray level response time to less than one frame period, as shown in curve (b) in Figure 1.

[0009] However, even the LCD display device made with this kind of over drive technology is able to shorten its gray level response time to less than and within one frame period, yet due to the intrinsic property of the liquid crystal, the generation of the optical response is slow so is its decline. Therefore, the image overlapping and the image outlines blurring phenomenon of the "after image" for the images displayed still can not be eliminated completely.

[0010] In order to completely eliminate the "after image", presently there are three methods adopted by the prior art, which are listed as follows:

[0011] (1) to write black data or black images into the frame in the remaining portion of that frame period after the original formal image is displayed;

[0012] (2) to shut off the backlight, for example, the blink light method as announced by Hitachi;

[0013] (3) the combination of the above methods (1) and (2), namely, both write in black image and shut off the backlight.

[0014] And in the following we will explain their respective drawbacks and limitations in detail.

[0015] First, referring to Figures 2A-2C, which indi-

cate the methods adopting by the prior art in simulating the CRT impulse type image display with LCD display device, the images displayed by the liquid crystal display of the prior art are composed of a series of frames 1, 2, 3, and 4. The method utilized is to insert the complete black frames 11, 12, and 13 between frames 1, 2; frames 2, 3; and frames 3, 4 so as to achieve the purpose of simulating CRT impulse type image display, and at the same time the backlight source at time points 14-20 corresponding to the time points of the above-mentioned frames are all in the illumination state.

[0016] Next, we are going to explain the second method of the prior art. Please refer to Figure 2B. At this time the images displayed by the LCD display consist of the sequentially displayed frames 1-7. The second method is performed by shutting off the backlight source at time points 22, 24, and 26 corresponding to the time points of frames 2, 4, and 6 and the backlight source at time points 21, 23, 25, and 27 corresponding to time points of frames 1, 3, 5, 7, and 9 are in the illumination state and in this manner, achieving the purpose of simulating CRT display impulse type image display with LCD display and eliminating the "after image".

[0017] And then next, we are going to explain the third method of the prior art. Please refer to Figure 2C, which indicates that the images displayed by the LCD display are composed of a series of sequentially displayed frames 1-4. The method is carried out by inserting the complete black frames 11, 12, and 13 between frames 1, 2; frames 2, 3; and frames 3, 4 respectively, and by putting the backlight source at time points 22, 24, and 26 corresponding to those of frames 11, 12, and 13 into the shut-off state, and by putting the backlight source at other time points corresponding to those of frames 1, 2, 3, and 4 into the illumination state. And that is to say, the third method achieves the effect of simulating CRT display impulse type image display with LCD display by inserting the complete black frames between frames 1, 2, 3, and 4, and at the same time utilizing this blink light mode of alternate illumination state and shut off state by means of shutting off the backlight source at the corresponding time points.

[0018] However, the three above-mentioned methods have their respective drawbacks and limitations.

[0019] First, the first method of inserting complete black frames between frames necessitates the addition of extra equipments, for example, frequency doubling device. Supposing that the original image displaying speed is 60 frames/min, then the application of this method necessitates the addition of the frequency doubling device to increase the image displaying speed to 120 frames/min, and wherein half of the number are used for inserting those black frames. Therefore, the utilization of this method would increase the cost of the equipment. Besides, the doubling of the image display frequency leads to the increase of electric-magnetic interference (EMI), and these are the drawbacks and limitations of the first method the prior art.

[0020] Next, the application of the second method also necessitates the addition of frequency doubling device, so as to achieve the equivalent number of display frames/unit time. Since half of the frames displayed in the unit time correspond to the backlight shut-off state and cannot be displayed as visible images. Therefore, the second method will increase the cost of the equipment, and it will also cause the increase of EMI. In addition, it requires the addition of extra equipment so as to make the backlight source blink, and therefore it further increases the cost of this method. And these are the drawbacks and limitations of the second method of the prior art.

[0021] And next, the third method of the prior art is the combination of the above two methods, namely, inserting the black frames and blinking the backlight modules. As such the drawbacks and limitations of the third method includes those of the above two methods. Therefore, it is not satisfying either.

[0022] In addition, in the above first and second methods, since the characteristics and speeds of optical response of different liquid crystal materials are different, the method of inserting black frames is not suitable for certain liquid crystal materials. Because for certain liquid crystal materials, their optical responses are fast from brightness to dark, and are slow from dark to brightness; but for other liquid crystal materials their optical responses are slow from brightness to dark, and are fast from dark to brightness. Therefore, the effectiveness of inserting black frames at equal time intervals in simulating CRT impulse type image display is not ideal and thus not satisfying, and in certain circumstances it is even not suitable for application. And it cannot achieve the purpose of simulating CRT display with LCD display, and it is not able to achieve the effectiveness of eliminating the "after image" either.

[0023] In view of the various above mentioned drawbacks and limitations of the prior art, the inventor of the present case dedicates all his talent, ingenuity, knowledge and experience in this field to the related research, development, experiment, and improvement, so as to bring about the realization of the present invention.

SUMMARY OF THE INVENTION

[0024] Therefore, the purpose of the present invention is to provide a device used for simulating CRT impulse type image display so as to overcome and improve the drawbacks and limitations of the related prior art. It neither utilizes the method of inserting black frames, nor does it utilize the method and design of blinking the backlights. Instead, it makes use of the method of providing the scanning black lines on the screen of the LCD display, to ensure achieving the purpose of simulating CRT impulse type image display, and to effectively eliminate the "after image" and phenomenon of image outline blurring, so as to significantly improve the quality of the displayed images of the LCD

display, and save the spending on the additional equipment.

[0025] In order to achieve the above mentioned purpose, the present invention provides a device to achieve simulating CRT display with LCD display, and its basic structure comprising:

[0026] A first input control line; a second input control line; a first input data line; a second input data line; a first capacitor; a second capacitor; a driving voltage output line; a first transistor, comprising a first gate connected to a first input control line, a first source connected to a first input data line, and a first drain connected to a driving voltage output line, a first capacitor and the drain of the second transistor; and a second transistor, comprising a second gate connected to a second input control line, a second source connected to a second input data line, and a second drain connected to a driving voltage output line, the drain of the first transistor and the second capacitor;

wherein the first capacitor and the second capacitor connected to ground respectively, and the driving voltage output line is used to output the said simulation driving voltage to the said pixels of LCD panel for displaying images; and it is characterized in that, the said first and second input control lines are connected to a gate driver, and the said first and second data lines are connected to a data driver respectively.

[0027] In the following we will explain in detail the embodiments and other variations of the device of the present invention used for simulating CRT impulse type image display.

[0028] The present invention also provides a method used for simulating CRT impulse type image display.

[0029] The various features and advantages of the present invention can be more thoroughly understood through the detailed description of the following embodiments with reference to the attached drawings, wherein similar reference numbers are used for similar elements.

BRIEF DESCRIPTION OF THE DRAWINGS

[0030] The related drawings in connection with the detailed description of the present invention to be made later are described briefly as follows, in which:

[0031] Figure 1 is the diagram of comparison of optical response curves of CRT image display, liquid crystal image display, and the simulated CRT impulse type image display;

[0032] Figures 2(a) to 2(c) indicate the methods of inserting black frames, black light blinking, and the combination of the two used by the prior art in simulating CRT display with LCD display;

[0033] Figure 3(a) is the schematic diagram indicating the pixel array formed by the cross points of a plurality of gate lines and data lines, and the driving circuit formed by a plurality of data driver and gate driver according to the first embodiment of the present invention;

[0034] Figure 3(b) indicates the simulation device according to the first embodiment of the present invention;

[0035] Figures 4(a) to 4(e) are the corresponding waveform diagrams of the control voltage pulse, driving voltage pulse, and the liquid crystal optical response curve generated by the simulation device according to the first embodiment of the present invention;

[0036] Figure 5(a) is the schematic diagram indicating the pixel array formed by the cross points of a plurality of gate lines and data lines, and the driving circuit formed by a plurality of data driver and gate driver according to the second embodiment of the present invention;

[0037] Figure 5(b) indicates the simulation device according to the second embodiment of the present invention;

[0038] Figures 6(a) to 6(g) are the corresponding waveform diagrams of the control voltage pulse, driving voltage pulse, and the liquid crystal optical response curve generated by the simulation device according to the second embodiment of the present invention;

[0039] Figure 7(a) is the schematic diagram indicating the pixel array formed by the cross points of a plurality of gate lines and data lines, and the driving circuit formed by a plurality of data driver and gate driver according to the third embodiment of the present invention;

[0040] Figure 7(b) indicates the simulation device according to the third embodiment of the present invention;

[0041] Figures 8(a) to 8(d) are the corresponding waveform diagrams of the control voltage pulse, driving voltage pulse, and the liquid crystal optical response curve generated by the simulation device according to the third embodiment of the present invention;

[0042] Figure 9(a) is the schematic diagram indicating the pixel array formed by the cross points of a plurality of gate lines and data lines, and the driving circuit formed by a plurality of data driver and gate driver according to the fourth embodiment of the present invention;

[0043] Figure 9(b) indicates the simulation device according to the fourth embodiment of the present invention;

[0044] Figures 10(a) to 10(d) are the corresponding waveform diagrams of the control voltage pulse, driving voltage pulse, and the liquid crystal optical response curve generated by the simulation device according to the fourth embodiment of the present invention;

[0045] Figure 11(a) is the schematic diagram indicating the pixel array formed by the cross points of a plurality of gate lines and data lines, and the driving circuit formed by a plurality of data driver and gate driver according to the fifth and sixth embodiments of the present invention;

[0046] Figure 11(b) indicates the simulation device according to the fifth and the sixth embodiments of the present invention;

[0047] Figures 12(a) to 12(e) are the corresponding waveform diagrams of the control voltage pulse, driving voltage pulse, and the liquid crystal optical response

curve generated by the simulation device according to the fifth embodiment of the present invention;

[0048] Figures 13(a) to 13(e) are the corresponding waveform diagrams of the control voltage pulse, driving voltage pulse, and the liquid crystal optical response curve generated by the simulation device according to the six embodiment of the present invention;

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

[0049] In the following the embodiments of the present invention will be described with reference to the attached drawings. And similar reference numbers represent similar elements.

[0050] In the following embodiments, the waveforms displayed are mainly used as instruments or tools to describe the voltage applied on the liquid crystal, and the characteristics and behaviors of the liquid crystal optical response. And the features and advantages of the present invention will be explained based on the above descriptions.

[0051] In Figures 4, 6, 8, 10, and 12 in the following five embodiments, the abscissa indicates time, and its units is millisecond (ms), with A1 to A6 as the sequentially progressing time points; and its ordinate indicates driving voltage, with "code" as its displaying unit. For the sake of convenient explanation, in the above-mentioned drawings, the time of the waveform progression on the abscissa can be divided into (N-1)th, Nth, (N+1)th, (N+2)th, and so on, equal frame time partitions as units of frame time. And the dotted lines in Figures 4(a), 6(a), 8(a), 10(a), and 12(a) indicate the optical response (namely, the gray level response) path characteristic curves for the liquid crystal molecules under the application of various different driving voltages. Usually, the optical response is the luminance displayed by the liquid crystal, and with nits (cd/m²) as its unit.

[0052] In the following descriptions the meanings of the symbols represented by the pulse of voltage in Figures 4(a) to 4(e), 6(a) to 6(g), 8(a) to 8(d), 10(a) to 10(d), and 12(a) to 12(e) can be better understood by referencing the circuit structure of Figures 3(b), 5(b), 7(b), 9(b), and 11(b). For example, the waveform shown in Figure 4(b) represents the pulse of control voltage applied on the gate of transistor Q of the simulation device in Figure 3(b); the waveform shown in Figure 4(c) represents the pulse of control voltage applied on the gate of transistor Q' of the simulation device in Figure 3(b); the waveform shown in Figure 4(d) represents the pulse of driving voltage applied on the source of transistor Q of the simulation device in Figure 3(b); the waveform shown in Figure 4(e) represents the pulse of driving voltage applied on the source of transistor Q' of the simulation device in Figure 3(b); V_{LC} represents the pulse of output driving voltage generated by the simulation device, and V_{COM} represents the reference voltage, The abscissa representing time is arranged below Figure 4

(e) for jointly used by Figures 4(a) to 4(e), and for being conveniently referenced and compared between Figures 4(a) to 4(e); and A1 to A6 represent the sequentially progressing points of time. And the similar details of the remaining Figures 6, 8, 10, and 12 can be explained similarly as above.

[0053] The CRT simulation method and device of the present invention will be explained in the following with the circuit diagram, the control voltage pulse waveform of the LCD display pixel unit, waveform of the driving voltage pulse, and the liquid crystal optical response characteristic curve of the respective five embodiments

Embodiment 1

[0054] In the following analysis, please refer to Figures 3(a), 3(b) and Figures 4(a) to 4(e) as we explain first embodiment of the present invention.

[0055] First, please refer to Figure 3(a), which indicates: the pixel array formed by the cross points of a plurality of gate lines and data lines, and the driving circuit formed by a plurality of data driver and gate driver according to the first embodiment of the present invention. And Figure 3(b) represents the simulation device according to the first embodiment.

Simulation Device

[0056] According to Figures 3(a) and 3(b) the simulation device comprises: a first input control line (G₁); a second input control line (G_{1'}); a first input data line (D₁); a second input data line (D_{1'}); a first capacitor (C_S); a second capacitor (C_{LS}); driving voltage output line; a first transistor(Q) comprising a first gate connected to the first input control line (G₁), a first source connected to the first input data line (D₁), and a first drain connected to the driving voltage output line and the first capacitor (C_S) and the drain of the second transistor(Q'); and a second transistor(Q') comprising a second gate connected to the second input control line (G_{1'}), a second source connected to the second input data line (D_{1'}), a second drain connected to the drain of the said first transistor and the second capacitor (C_{LC}) and driving voltage output line; wherein the said first capacitor and the said second capacitor are storage capacitor and liquid crystal equivalent capacitor respectively and are connected to ground, and the driving voltage output line is used to output the driving voltage used for simulation to the said pixels of the LCD panel so as to display images, and it is characterized in that, the said first and second input control lines are connected to a gate driver, and the said first and second input data lines are connected to a data driver respectively.

Simulation Method

[0057] The following is the simulation method used for the simulation device according to the first embodiment

of the present invention, comprising the following steps:
 (I) providing the first control signal (G_1) with periodic pulse waveforms to the first gate of the first transistor (Q) of the said circuit; (II) providing the second control signal (G_2) with periodic pulse waveforms to the second gate of the second transistor (Q') of the said circuit, wherein the second control signal (G_2) is the same as the first control signal (G_1) except the phase delay; (III) providing the first data signal (D_1) to the source of the first transistor (Q) of the said circuit, when activated by the said first control signal (G_1), the said circuit feeds the first data signal (D_1) to the said driving voltage output line; (IV) providing the second data signal (D_2) to the source of the second transistor (Q') of the said circuit, when activated by the said second control signal (G_2), the said circuit feeds the second data signal (D_2) to the said driving voltage output line; and (V) outputting the said output driving voltages generated by the above steps to the said pixels, so as to display images.

Waveform Analysis

[0058] In the following analysis, please refer to Figures 4(a) to 4(e) as we describe in detail the relations between the waveforms of the pulses of control voltages G_1 , G_2 , and the pulses of the driving voltages D_1 , D_2 , V_{LC} generated by the simulation device of Figures 3(a) and 3(b) according to the first embodiment of the present invention.

[0059] When the pulse of the control voltage of the simulation device is G_1 (Figure 4(b)), then the pulse of its corresponding driving voltage is D_1 (Figure 4(d)). When the pulse of the control voltage of the device is G_2 (Figure 4(c)), then the pulse of its corresponding driving voltage is D_2 (Figure 4(e)). And pulse of the actual combined output driving voltage generated by the simulation device of the present invention to the liquid crystal is V_{LC} (Figure 4(a)).

[0060] In the following discussion, the driving voltages V_1 , V_2 , V_3 can be considered as a kind of voltage value expressed in "code".

[0061] It must be re-emphasized here that the said driving voltage can reach its target voltage momentarily, however, the liquid crystal molecules have to take a certain period of response time to reach its optical response target position after being applied the driving voltages. This is due to the intrinsic property of the liquid crystal.

[0062] Since usually AC voltage is utilized as the voltage for driving the liquid crystal, therefore, this voltage indicates the phenomenon of alternating positive and negative phases during the control and driving process of the liquid crystal (namely, the waveforms of the pulses of driving voltages D_1 , D_2 ; and V_{LC} indicate the phenomenon of alternating positive and negative phases relative to the reference voltage V_{COM}).

[0063] These waveforms proceed sequentially and periodically from time points A1 to A6 repeatedly in the

following manner:

[0064] The value of driving voltage pulse D_1 in the (N-1)th frame before time point A1 is V_1 (code 0), and the value of the driving voltage pulse V_{LC} is V_1 (code 0) of negative polarity; at time point A1, the waveform enters the Nth frame, at this time the value of the driving voltage pulse D_1 increases to V_2 (code 32), and due to the activation of the control voltage pulse G_1 , therefore the value of driving voltage pulse V_{LC} generated by the simulation device also increases to V_2 (code 32) of positive polarity and remains so until time point A2; then the time proceeds to time point A2, at this time the value of driving voltage pulse D_1 is V_1 (code 0), and due to the activation of control voltage pulse G_1 , resulting in the value of driving voltage pulse V_{LC} to drop momentarily from V_2 (code 32) to V_1 (code 0) and is still of positive polarity, and this value is maintained until time point A3; then the time proceeds to time point A3 and enters the (N+1)th frame, at this time the value of the driving voltage pulse D_1 drops to V_3 (code 120) and is of negative polarity, and due to the activation of control voltage pulse G_1 , the value of the driving voltage pulse V_{LC} also momentarily drops to V_3 (code 120) of negative polarity, and it remains so until time point A4; then time proceeds to A4, at this time, the value of driving voltage pulse D_1 is still V_1 (code 0), and due to the activation of control voltage pulse G_1 , resulting in the value of the driving voltage pulse V_{LC} also increases to V_1 (code 0) and is still of negative polarity and it remains so until time point A5; then time proceeds to time point A5 and starts to enter the (N+2)th frame, at this time the value of the driving voltage pulse D_1 increases to V_3 (code 120), and due to the activation of the control voltage pulse G_1 , resulting in the value of the driving voltage pulse V_{LC} also increases momentarily to V_3 (code 120) of positive polarity, and it remains so until time point A6.

[0065] The variations of control voltage pulses G_1 , G_2 , and driving voltage pulses D_1 , D_2 , and V_{LC} at the various time points after time points A6 can easily be inferred based on the above descriptions.

[0066] The dotted line as shown in Fig 4(a) is the liquid crystal optical response characteristic curve produced while performing the simulation drive. When the output driving voltage of the simulation device between each time point is code 0 as shown in the figure, this means that the black line scanning is performed on the display screen during this period, and by doing so, it can achieve the same results as inserting black frames or shutting off the backlights, so as to achieve the purpose of simulating CRT display impulse type image display.

[0067] In addition, the n shown at pulse G_1 in the Nth frame as shown in Figure 4(c) indicates n pulses, which means that there exists the time difference of n scanning lines between the control voltage pulse G_1 and G_2 in the same frame, namely, from the standpoint of the pixel, another control driving pulse G_2 will be input, at only nG_1 pulses after the first G_1 pulse. And this interval of time represented by n can be properly adjusted by the

designer depending on the actual requirements such as the property of liquid crystal material etc., so as to ensure achieving the effectiveness of simulating CRT display impulse type image display. And this is the most important advantage of the present invention over prior art.

Embodiment 2

[0068] In the following analyses, please refer to Figures 5(a), 5(b) and Figures 6(a) to 6(g) as we explain second embodiment of the present invention.

[0069] First, please refer to Figure 5(a), which indicates: the pixel array formed by the cross points of a plurality of gate lines and data lines, and the driving circuit formed by a plurality of data driver and gate driver according to the second embodiment of the present invention. And Figure 5(b) represents the simulation device according to the second embodiment.

Simulation Device

[0070] According to Figures 5(a) and 5(b) the simulation device of the second embodiment comprises: a first input control line (G_1); a second input control line (G_1'); a first input data line (D_1); a second input data line (D_1'); a third input data line (D'); a fourth input data line (D); a fifth input data line (D_s); a first capacitor (C_S); a second capacitor (C_{LS}); a third transistor (Q_3); a fourth transistor (Q_4); driving voltage output line; a first transistor (Q) comprising a first gate connected to the first input control line (G_1), a first source connected to the input data line (D_1), and a first drain connected to the driving voltage output line and the first capacitor (C_S) and the drain of the second transistor (Q'); and a second transistor (Q') comprising a second gate connected to the second input control line (G_1'), a second source connected to the second input data line (D_1'), a second drain connected to the drain of the said first transistor and the second capacitor (C_{LC}) and driving voltage output line; wherein the said first capacitor and the said second capacitor are storage capacitor and liquid crystal equivalent capacitor respectively and are connected to ground, and the driving voltage output line is used to output the driving voltage used for simulation to the said pixels of the LCD panel so as to display images, and it is characterized in that the said first and second input control lines are connected to a gate driver, and the said first and second input data lines are connected to the drains of two another switching transistors (Q_3 , Q_4) connected in parallel, the sources of the said two switching transistors connected in parallel are connected to a data driver, with its gate connected to the third and fourth input data lines (D' , D); and the time difference between the periodic pulse waveforms of the said first and second control signals (G_1 , G_1') is the time difference across n scanning lines generated by n pulses, and which can be adjusted.

Simulation Method

[0071] The following is the simulation method used for the simulation device according to the second embodiment of the present invention, comprising the following steps: (I) providing the first control signal (G_1) with periodic pulse waveforms to the first gate of the first transistor (Q) of the said circuit; (II) providing the second control signal (G_1') with periodic pulse waveforms to the second gate of the second transistor (Q') of the said circuit wherein the second control signal (G_1') is the same as the first control signal (G_1) except the phase delay; (III) providing the fifth data signal (D_s) to the sources of the third transistor (Q_3) and fourth transistor (Q_4) connected in parallel; (IV) providing the third data signal (D') to the gate of the third transistor (Q_3); (V) providing the voltage pulse generated by the drain of the third transistor to the source of the first transistor (Q_1) as the first data signal (D_1), when the said first transistor (Q_1) is activated by the first control signal (G_1), the first data signal (D_1) is fed by the said circuit to the driving voltage output line; (VI) providing the fourth data signal (D) to the gate of the fourth transistor (Q_4); (VII) providing the voltage pulse generated by the drain of the fourth transistor to the source of the second transistor (Q') as the second data signal (D_1'), when the said second transistor (Q') is activated by the second control signal (G_1'), the second data signal (D_1') is fed by the said circuit to the driving voltage output line; and (VIII) outputting the said output driving voltage generated by the above steps to the said pixels so as to display images.

Waveform Analysis

[0072] In the following analysis, please refer to Figures 6(a) to 6(g) as we describe in detail the relations between the waveforms of the pulses of control voltages G_1 , G_1' and the pulses of the driving voltages D_1 , D_1' , V_{LC} generated by the simulation device of Figures 5(a) and 5(b) according to the second embodiment of the present invention.

[0073] Since usually AC voltage is utilized as the voltage for driving the liquid crystal, therefore, this voltage indicates the phenomenon of alternating positive and negative phases during the control and driving process of the liquid crystal (namely, the waveforms of the pulses of driving voltages D_1 , D_1' , and V_{LC} indicate the phenomenon of alternating positive and negative phases relative to the reference voltage V_{COM}).

[0074] These waveforms proceed sequentially and periodically from time points A1 to A6 repeatedly in the following manner.

[0075] The value of driving voltage pulse D_1' in the ($N-1$)th frame before time point A1 is V_1' (code 0), and the value of the driving voltage pulse V_{LC} is V_1' (code 0) of negative polarity; at time point A1, the waveform enters the N th frame, at this time the value of the driving voltage pulse D_1 increases to V_2 (code 32), and due to the ac-

tivation of the control voltage pulse G_1 , therefore the value of driving voltage pulse V_{LC} generated by the simulation device also increases to V_2 (code 32) of positive polarity and remains so until time point A2; then the time proceeds to time point A2, at this time the value of driving voltage pulse D_1 is V_1 (code 0), and due to the activation of control voltage pulse G_1 , resulting in the value of driving voltage pulse V_{LC} to drop momentarily from V_2 (code 32) to V_1 (code 0) and is still of positive polarity, and this value is maintained until time point A3; then the time proceeds to time point A3 and enters the (N+1)th frame, at this time the value of the driving voltage pulse D_1 drops to V_3 (code 120) and is of negative polarity, and due to the activation of control voltage pulse G_1 , the value of the driving voltage pulse V_{LC} also momentarily drops to V_3 (code 120) of negative polarity, and it remains so until time point A4; then time proceeds to A4, at this time, the value of driving voltage pulse D_1 is still V_1 (code 0), and due to the activation of control voltage pulse G_1 , resulting in the value of the driving voltage pulse V_{LC} also increases to V_1 (code 0) and is still of negative polarity and it remains so until time point A5; then time proceeds to time point A5 and starts to enter the (N+2)th frame, at this time the value of the driving voltage pulse D_1 increases to V_3 (code 120), and due to the activation of the control voltage pulse G_1 , resulting in the value of the driving voltage pulse V_{LC} also increases momentarily to V_3 (code 120) of positive polarity, and it remains so until time point A6.

[0076] The variations of control voltage pulses G_1 , G_1' , and driving voltage pulses D_1 , D_1' , and V_{LC} at the various time points after time points A6 can easily be inferred based on the above descriptions.

[0077] Figures 6(d) and 6(e) indicate the waveforms of the voltage pulses of the third and fourth data signals of Figure 5(a).

[0078] The dotted line as shown in Fig 6(a) is the liquid crystal optical response characteristic curve produced while performing the simulation drive. When the output driving voltage of the simulation device between each time point is code 0 as shown in the figure, this means that the black line scanning is performed on the display screen during this period, and by doing so, it can achieve the same results as inserting black frames or shutting off the backlights, so as to achieve the purpose of simulating CRT display impulse type image display.

[0079] In addition, the n shown at pulse G_1 in the Nth frame as shown in Figure 6(c) indicates n pulses, which means that there exists the time difference of n scanning lines between the control voltage pulse G_1 and G_1' in the same frame, namely, from the standpoint of the pixel, another control driving pulse G_1 will be input, at only nG_1 pulses after the first G_1 pulse. And this interval of time represented by n can be properly adjusted by the designer depending on the actual requirements such as the property of liquid crystal material etc., so as to ensure achieving the effectiveness of simulating CRT display impulse type image display. And this is the most

important advantage of the present invention over prior art.

[0080] For the sake of easy and convenient explanation and understanding, the waveform of the driving voltage pulse V_{LC} output by the simulation device of the present Embodiment as shown above is the same as that of Embodiment 1, so as to avoid it being too complicated to understand in the process of explanation. However, the waveform can be designed to have various variations according to the actual requirements of the LCD display.

Embodiment 3

[0081] In the following analyses, please refer to Figures 7(a), 7(b) and Figures 8(a) to 8(d) as we explain third embodiment of the present invention.

[0082] First, please refer to Figure 7(a), which indicates: the pixel array formed by the cross points of a plurality of gate lines and data lines, and the driving circuit formed by a plurality of data driver and gate driver according to the third embodiment of the present invention. And Figure 7(b) represents the simulation device according to the third embodiment.

Simulation Device

[0083] According to Figures 7(a) and 7(b) the simulation device comprises: a first input control line (G_1); a second input control line (G_1'); a first input data line (D_1); a first capacitor (C_S); a second capacitor (C_{LS}); driving voltage output line; a first transistor (Q) comprising a first gate connected to the first input control line (G_1), a first source connected to the first input data line (D_1), and a first drain connected to the driving voltage output line and the first capacitor (C_S) and the second drain of the second transistor (Q'); and a second transistor (Q') comprising a second gate connected to the second input control line (G_1'), a second source connected to ground, a second drain connected to the drain of the said first transistor and the second capacitor (C_{LS}) and driving voltage output line; wherein the said first capacitor and the said second capacitor are storage capacitor and liquid crystal equivalent capacitor respectively and are connected to ground, and the driving voltage output line is used to output the driving voltage used for simulation to the said pixels of the LCD panel so as to display images, and it is characterized in that the said first and second input control lines are connected to a gate driver, and the said first input data line is connected to a data driver; and the time difference between the waveforms of the periodic pulses of the first and second control signals is the time difference across n scanning lines generated by n pulses, and which can be adjusted.

Simulation Method

[0084] The following is the simulation method used for

the simulation device according to the third embodiment of the present invention, comprising the following steps: (I) providing the first control signal (G_1) with periodic pulse waveforms to the first gate of the first transistor (Q) of the said circuit; (II) providing the second control signal (G_1') with periodic pulse waveforms to the second gate of the second transistor (Q') of the said circuit, wherein the second control signal (G_1') is the same as the first control signal (G_1) except the phase delay; (III) providing the first data signal (D_1) to the source of the first transistor (Q) of the said circuit, when activated by the said first control signal (G_1), the said circuit feeds the first data signal (D_1) to the said driving voltage output line; (IV) when activated by the second control signal (G_1'), the ground potential voltage (code 0) is fed by the said circuit to the driving voltage output line; and (V) outputting the said output driving voltages generated by the above steps to the said pixels so as to display images.

Waveform Analysis

[0085] In the following analysis, please refer to Figures 8(a) to 8(d), as we describe in detail the relations between the waveforms of the pulses of control voltages G_1 , G_1' , and the pulses of the driving voltages D_1 , D_1' , V_{LC} generated by the simulation device of Figures 7(a) and 7(b) according to the third embodiment of the present invention.

[0086] Since usually AC voltage is utilized as the voltage for driving the liquid crystal, this voltage indicates the phenomenon of alternating positive and negative phases during the control and driving process of the liquid crystal (namely, the waveforms of the pulses of driving voltages D_1 , D_1' , and V_{LC} indicate the phenomenon of alternating positive and negative phases relative to the reference voltage V_{COM}).

[0087] These waveforms proceed sequentially and periodically from time points A1 to A6 repeatedly in the following manner.

[0088] The value of driving voltage pulse D_1 in the (N-1)th frame before time point A1 is V_2 (code 32), and the value of the driving voltage pulse V_{LC} is V_{com} (since the source of the second transistor is connected to V_{com}); at time point A1, the waveform enters the Nth frame, at this time the value of the driving voltage pulse D_1 increases to V_2 (code 32), and due to the activation of the control voltage pulse G_1 , therefore the value of driving voltage pulse V_{LC} generated by the simulation device also increases to V_2 (code 32) of positive polarity and it remains so until time point A2; then the time proceeds to time point A2, at this time the value of driving voltage pulse D_1 is still V_2 (code 32), and due to the activation of control voltage pulse G_1' (since the source of the second transistor is connected to V_{com}), resulting in the value of driving voltage pulse V_{LC} to drop momentarily from V_2 (code 32) to V_1 (code 0) and is still of positive polarity, and this value is maintained until time point A3; then the time proceeds to time point A3 and enters the (N+1)th

frame, at this time the value of the driving voltage pulse D_1 drops to V_3 (code 120) and is of negative polarity, and due to the activation of control voltage pulse G_1 , the value of the driving voltage pulse V_{LC} also momentarily drops to V_3 (code 120) of negative polarity, and it remains so until time point A4; then time proceeds to time point A4, at this time, the value of driving voltage pulse D_1 is still V_3 (code 120) of negative polarity, and due to the activation of control voltage pulse G_1' (since the source of the second transistor is connected to V_{com}), resulting in the value of the driving voltage pulse V_{LC} also increases to V_{com} (code 0) and is still of negative polarity and it remains so until time point A5; then time proceeds to time point A5 and starts to enter the (N+2)th frame, at this time the value of the driving voltage pulse D_1 increases to V_3 (code 120), and due to the activation of the control voltage pulse G_1 , resulting in the value of the driving voltage pulse V_{LC} also increases momentarily to V_3 (code 120) of positive polarity, and it remains so until time point A6.

[0089] The variations of control voltage pulses G_1 , G_1' , and driving voltage pulses D_1 , D_1' , and V_{LC} at the various time points after time points A6 can easily be inferred based on the above descriptions.

[0090] The dotted line as shown in Figure 8(a) is the liquid crystal optical response characteristic curve produced while performing the simulation drive. When the output driving voltage V_{LC} of the simulation device between each time point is V_{com} as shown in the figure, this means that the black line scanning is performed on the display screen during this period, and by doing so, it can achieve the same results as inserting black frames or shutting off the backlights, so as to achieve the purpose of simulating CRT display impulse type image display.

[0091] In addition, the n shown at pulse G_1' in the Nth frame as shown in Figure 8(c) indicates n pulses, which means that there exists the time difference of n scanning lines between the control voltage pulse G_1 and G_1' in the same frame, namely, from the standpoint of the pixel, another control driving pulse G_1' will be input, at only nG_1 pulses after the first G_1 pulse. And this interval of time represented by n can be properly adjusted by the designer depending on the actual requirements such as the property of liquid crystal material etc., so as to ensure achieving the effectiveness of simulating CRT display impulse type image display. And this is the most important advantage of the present invention over prior art.

[0092] For the sake of easy and convenient explanation and understanding, the waveform of the driving voltage pulse V_{LC} output by the simulation device of the present Embodiment as shown above is the same as that of Embodiment 1, so as to avoid it being too complicated to understand in the process of explanation. However, the waveform can be designed to have various variations according to the actual requirements of the LCD display.

Embodiment 4

[0093] In the following analyses, please refer to Figures 9(a), 9(b) and Figures 10(a) to 10(d) as we explain fourth embodiment of the present invention.

[0094] First, please refer to Figure 9(a), which indicates: the pixel array formed by the cross points of a plurality of gate lines and data lines, and the driving circuit formed by a plurality of data driver and gate driver according to the fourth embodiment of the present invention. And Figure 9(b) represents the simulation device according to the fourth embodiment.

Simulation Device

[0095] According to Figures 9(a) and 9(b), the simulation device of the fourth Embodiment comprises: a first input controlline (G_1); a second input control line (G_m); a first input data line (D_1); a first capacitor (C_S); a second capacitor (C_{LS}); a driving voltage output line; and a first transistor (Q) comprising: a gate connected to the first input control line (G_1) or the second input control line (G_m), a source connected to the input data line (D_1), and a drain connected to the driving voltage output line and two capacitors (C_S , C_{LS}) connected in parallel; and wherein the said first capacitor and second capacitor are connected to ground, and the driving voltage output line is used to output the driving voltage used for simulation to the said pixels of the LCD panel so as to display images, and it is characterized in that the said input data line is connected to a data driver, the said input control line is connected to the gate driver, the said gate driver contains: an output enable (OE) input line and a start pulse horizontal (STH) input line and receives the related signals via the said input lines, so as to generate the synchronous control voltage pulses G_1 , G_m of the said input control lines, and supply them to the gate of the said transistor via the first and second input control lines, and to generate the driving voltage pulse V_{LC} through its control, and then be able to generate two synchronous scanning lines separated by m scanning lines on the display screen simultaneously, so as to display images.

Simulation Method

[0096] The following is the simulation method used for the simulation device according to the fourth embodiment of the present invention, comprising the following steps: (I) providing the data signal (D_1) with periodic pulse waveform to the source of the said first transistor (Q1); (II) providing control signals OE and STH to the gate driver, so as to generate the synchronous control signals G_1 , G_m and providing them to the gate of the said transistor (Q1) via the first and second input control lines; (III) when activated by the said synchronous control signals G_1 , G_m , the said circuit feeds the said data signal to the said driving voltage output line; and (IV)

outputting the said output driving voltage generated by the above steps to the said pixels so as to display images.

5 Waveform analysis

[0097] In the following, please refer to Figures 10(a) to 10(d), as we describe in detail the relations between the waveforms of the pulses of control voltages G_1 , G_m and the pulses of the driving voltages D_1 , V_{LC} generated by the simulation device of Figures 9(a) and 9(b) according to the fourth embodiment of the present invention.

[0098] Since usually AC voltage is utilized as the driving voltage for driving the liquid crystal, this voltage indicates the phenomenon of alternating positive and negative phases during the control and driving process of the liquid crystal (namely, the waveforms of the pulses of driving voltages D_1 and V_{LC} indicate the phenomenon of alternating positive and negative phases relative to the reference voltage V_{COM}).

[0099] These waveforms proceed sequentially and periodically from time points A1 to A6 repeatedly in the following manner.

[0100] The value of driving voltage pulse D_1 in the (N-1)th frame before time point A1 is V_1 (code 0), and the value of the driving voltage pulse V_{LC} is V_1 (code 0) of negative polarity; at time point A1, the waveform enters the Nth frame, at this time the value of the driving voltage pulse D_1 increases to V_2 (code 32), and due to the activation of the control voltage G_1 , therefore the driving voltage pulse V_{LC} generated by the simulation device also increases to V_2 (code 32) of positive polarity and remains so until time point A2; then the time proceeds to time point A2, at this time the value of driving voltage pulse D_1 is V_1 (code 0), and due to the activation of control voltage pulse G_1 , resulting in the value of driving voltage pulse V_{LC} to drop momentarily from V_2 (code 32) to V_1 (code 0) and is still of positive polarity, and this value is maintained until time point A3; then the time proceeds to time point A3 and enters the (N+1)th frame, at this time the value of the driving voltage pulse D_1 drops to V_3 (code 120) and is of negative polarity, and due to the activation of control voltage pulse G_1 , the value of the driving voltage pulse V_{LC} also momentarily drops to V_3 (code 120) of negative polarity, and it remains so until time point A4; then time proceeds to A4, at this time, the value of driving voltage pulse D_1 is still V_1 (code 0), and due to the activation of control voltage pulse G_1 , resulting in the value of the driving voltage pulse V_{LC} also increases to V_1 (code 0) and is still of negative polarity until time point A5; then time proceeds to time point A5 and starts to enter the (N+2)th frame, at this time the value of the driving voltage pulse D_1 increases to V_3 (code 120), and due to the activation of the control voltage pulse G_1 , resulting in the value of the driving voltage pulse V_{LC} also increases momentarily to V_3 (code 120) of positive polarity, and it remains so until time point A6.

[0101] The variations of control voltage pulses G_1 , G_1 , and driving voltage pulses D_1 , and V_{LC} at the various time points after time points A6 can easily be inferred based on the above descriptions.

[0102] The dotted line as shown in Figure 10 (a) is the liquid crystal display optical response characteristic curve produced while performing the simulation drive. When the output driving voltage V_{LC} of the simulation device between each time point is code 0 as shown in the figure, this means that the black line scanning is performed on the display screen during this period, and by doing so, it can achieve the same results as inserting black frames or shutting off the backlights, so as to achieve the purpose of simulating CRT display impulse type image display.

[0103] The symbol Hsync in Figure 10(c) indicates that the control voltage pulses G_1 and G_m are synchronous signals.

[0104] Therefore, according to the design of the present Embodiment, G_m and G_1 are synchronous control voltage pulses. The scanning line generated by the G_m control and the scanning line generated by G_1 control are separated on the screen by $m-1$ scanning lines, and these two scanning lines execute scanning on the display screen in a synchronous manner. And the relations between the waveforms of control voltage pulse G_m and driving voltage pulse D_1 , V_{LC} are the same as those between the waveforms of control voltage pulse G_1 and driving voltage pulse D_1 , V_{LC} (namely, the description above regarding Figures 10(a) to 10(d)), therefore, it will not be repeated here.

[0105] For the sake of easy and convenient explanation and understanding, the waveform of the driving voltage pulse V_{LC} output by the simulation device of the present Embodiment as shown above is the same as that of Embodiment 1, so as to avoid it being too complicated to understand in the process of explanation. However, the waveform can be designed to have various variations according to the actual requirements of the LCD display.

[0106] For the sake of easy and convenient explanation and understanding, the waveform of the driving voltage pulse V_{LC} output by the simulation device of the present Embodiment as shown above is the same as that of Embodiment 1, so as to avoid it being too complicated to understand in the process of explanation. However, the waveform can be designed to have various variations according to the actual requirements of the LCD display.

[0107] It must be particularly emphasized here that regardless of the positive or negative polarity of the liquid crystal driving voltage pulse V_{LC} , as long as it can attain the predetermined target level, then it is able to achieve the purpose and effectiveness of accelerated driving of the optical response of liquid crystal and simulating the CRT image display.

[0108] In addition, according to the design features of the present invention, the separation of m scanning lines

between two subsequent control voltage pulses G_1 (Figure 10(b)) and G_m (Figure 10(c)) in the same frame (for example the N th frame) can be adjusted depending on the actual effectiveness desired to be achieved and the design requirements. And this is the important invention and feature of the present case, and it is not disclosed in all the related prior art.

Embodiment 5

[0109] In the following, please refer to Figures 11(a), 11(b) and Figures 12(a) to 12(e) as we explain the fifth embodiment of the present invention. And Figures 11(a) and 11(b) are used to describe the fifth Embodiment and the subsequent sixth Embodiment of the present invention, its purpose is to indicate that: different image display effects can be achieved on the display screen by utilizing different control methods with the same device, and this characteristic will be discussed as follows.

[0110] First, please refer to Figure 11(a), which indicates: the pixel array formed by the cross points of a plurality of gate lines and data lines, and the driving circuit formed by a plurality of data driver and gate driver according to the fifth embodiment of the present invention. And Figure 11(b) represents the simulation device according to the fifth embodiment.

Simulation Device

[0111] According to Figures 11(a) and 11(b), the simulation device of the fifth Embodiment comprises: a first input control line (G_1); a second input control line (G_{m+1}); a third input control line (G_{2m+1}); a first input data line (D_1); a first capacitor (C_S); a second capacitor (C_{LS}); and a driving voltage output line; and a first transistor(Q) comprising a gate connected to the first input control line (G_1) or the second input control line (G_{m+1}) or the third input control line (G_{2m+1}); a source connected to the first input data line (D_1), and a drain connected to the driving voltage output line and two capacitors (C_S , C_{LS}) connected in parallel; and wherein the said first capacitor and second capacitor are the storage capacitor and liquid crystal equivalent capacitor respectively and connected to ground, and the driving voltage output line is used to output the driving voltage used for simulation to the said pixels of the LCD panel so as to display images, and it is characterized in that, the said input data line is connected to a data driver, the said input control line is connected to the gate driver, the said gate driver contains: the first, the second, and the third output enable (OE) input lines and the first, the second, and the third start pulse horizontal (STH) input lines, and receives the related signals via the said input lines, the said output enable (OE) signals input by the said gate drivers are so controlled that the two sets of synchronous control voltage pulses generated at the output of the said gate drivers are selected from the following three sets of control voltage pulses: (1) (G_1 , G_m), (2) (G_{m+1} , G_{2m}), (3)

(G_{2m+1} , G_{3m}); and these two sets of control voltage pulses (1, 3), or (1, 2), or (2, 3) are selected from the said three sets of control voltage pulses and then arranged and combined, such that they are provided to the gate of the said transistors through the corresponding first, or second, or third input control line in a cyclic alternating manner, and the driving voltage pulse VLC generated through the control of the gate can be used to drive the pixels to simultaneously generate two synchronous scanning lines separated by $2m$ scanning lines on the display screen in a cyclic alternating manner, so as to display images.

Simulation Method

[0112] The following is the simulation method used for the simulation device according to the fifth embodiment of the present invention, comprising the following steps: (I) providing the data signal (D1) with periodic pulse waveform to the source of the said first transistor (Q1); (II) providing the OE and STH control signals to the first, second, and third output enable (OE) input lines and start pulse horizontal (STH) input lines of the said gate driver, and receiving the related signals via the said input lines, the said output enable (OE) signals input by the said gate drivers are so controlled that the two sets of synchronous control voltage pulses generated at the output of the said gate drivers are selected from the following three sets of control voltage pulses: (1) (G_1 , G_m), (2) (G_{m+1} , G_{2m}), (3) (G_{2m+1} , G_{3m}); and these two sets of control voltage pulses (1,3), or (1, 2), or (2, 3) are selected from the said three sets of control voltage pulses and then arranged and combined, such that they are provided to the gate of the said transistors (Q1) through the corresponding first, second, or third input control lines in a cyclic alternating manner and it is characterized in that when activated by the said two sets of synchronous control signals (1, 3), or (1, 2), or (2, 3), the said circuit feeds the said data signal to the said driving voltage output line; and (III) outputting the said output driving voltage generated by the above steps to the said pixels, so as to simultaneously generate two synchronous scanning lines separated by $2m$ scanning lines on the display screen in a cyclic alternating manner, so as to display images.

Waveform analysis

[0113] In the following analysis, please refer to Figures 12(a) to 12(e) as we describe in detail the relations between the waveforms of the pulses of control voltages (G_1 , G_m), (G_{m+1} , G_{2m}), (G_{2m+1} , G_{3m}) and the pulses of the driving voltages D_1 , V_{LC} generated by the simulation device of Figures 11(a) and 11(b) according to the fifth embodiment of the present invention.

[0114] Since usually AC voltage is utilized as the driving voltage for driving the liquid crystal, therefore, this voltage indicates the phenomenon of alternating posi-

tive and negative phases during the control and driving process of the liquid crystal (namely, the waveforms of the pulses of driving voltages D_1 , V_{LC} indicate the phenomenon of alternating positive and negative phases relative to the reference voltage V_{COM}).

[0115] These waveforms proceed sequentially and periodically from time points A1 to A6 repeatedly in the following manner:

[0116] The value of driving voltage pulse D_1 in the (N-1)th frame before time point A1 is V_1 , (code 0), and the value of the driving voltage pulse V_{LC} is V_1 , (code 0) of negative polarity; at time point A1, the waveform enters the Nth frame, at this time the value of the driving voltage pulse D_1 increases to V_2 (code 32), and due to the activation of the control voltage G_1 , therefore the value of output driving voltage pulse V_{LC} generated by the simulation device also increases to V_2 (code 32) of positive polarity and it remains so until time point A2; then the time proceeds to time point A2, at this time the value of driving voltage pulse D_1 is V_1 (code 0), and due to the activation of control voltage pulse G_1 , resulting in the value of driving voltage pulse V_{LC} to drop momentarily from V_2 (code 32) to V_1 (code 0) and is still of positive polarity, and this value is maintained until time point A3; then the time proceeds to time point A3 and enters the (N+1)th frame, at this time the value of the driving voltage pulse D_1 drops to V_3 , (code 120), and due to the activation of control voltage pulse G_1 , the value of the driving voltage pulse V_{LC} also momentarily drops to V_3 , (code 120) of negative polarity, and it remains so until time point A4; then time proceeds to A4, at this time, the value of driving voltage pulse D_1 is still V_1 , (code 0), and due to the activation of control voltage pulse G_1 , resulting in the value of the driving voltage pulse V_{LC} also increases to V_1 , (code 0) and is still of negative polarity until time point A5; then time proceeds to time point A5 and starts to enter the (N+2)th frame, at this time the value of the driving voltage pulse D_1 increases to V_3 (code 120), and due to the activation of the control voltage pulse G_1 , resulting in the value of the driving voltage pulse V_{LC} also increases momentarily to V_3 (code 120) of positive polarity, and it remains so until time point A6.

[0117] The variations of control voltage pulses G_{m+1} , G_{2m+1} and driving voltage pulses D_1 , and V_{LC} at the various time points after time points A6 can easily be inferred based on the above descriptions.

[0118] The dotted line as shown in Figure 12(a) is the liquid crystal display optical response characteristic curve produced while performing the simulation drive. When the output driving voltage V_{LC} of the simulation device between each time point is code 0 as shown in the figure, this means that the black line scanning is performed on the display screen during this period, and by doing so, it can achieve the same results as inserting black frames or shutting off the backlights, so as to achieve the purpose of simulating CRT display impulse type image display.

[0119] For the sake of easy and convenient explana-

tion and understanding, the waveform of the driving voltage pulse V_{LC} output by the simulation device of the present Embodiment as shown above is the same as that of Embodiment 6, so as to avoid it being too complicated to understand in the process of explanation. However, the waveform can be designed to have various variations according to the actual requirements of the LCD display.

[0120] In summary, the purpose of the present invention is to generate two synchronous scanning lines on the display screen as shown in Figures 12 (b), 12(c) and 12(d). G_1 , G_{m+1} , G_{2m+1} are synchronous control voltage pulses, and two sets of scanning lines are generated on the display screen by the driving voltage pulses generated through the control of the said control voltage pulses, and are performed synchronous scanning separated by 2m scanning lines so as to display images.

Embodiment 6

[0121] In the following analyses, please refer to Figures 11(a), 11(b) and Figures 13(a) to 13(e) as we explain sixth embodiment of the present invention. And Figures 11(a) and 11(b) are used to describe the sixth Embodiment and the preceding fifth Embodiment of the present invention, its purpose is to indicate that: different image display effects can be achieved on the display screen by utilizing different control methods with the same device, and this characteristic will be discussed as follows.

[0122] First, please refer to Figure 11(a), which indicates: the pixel array formed by the cross points of a plurality of gate lines and data lines, and the driving circuit formed by a plurality of data driver and gate driver according to the sixth embodiment of the present invention. And Figure 11(b) represents the simulation device according to the sixth embodiment.

Simulation Device

[0123] According to Figures 11(a) and 11(b), the simulation device of the sixth Embodiment comprises: a first input control line (G_1); a second input control line (G_{m+1}); a third input control line (G_{2m+1}); a first input data line (D_1); a first capacitor (C_S); a second capacitor (C_{LS}); a driving voltage output line; and a first transistor (Q) comprising a gate connected to the first input control line (G_1) or the second input control line (G_{m+1}) or the third input control line (G_{2m+1}); a source connected to the first input data line (D_1), and a drain connected to the driving voltage output line and two capacitors (C_S , C_{LS}) connected in parallel; wherein the said first capacitor and second capacitor are the storage capacitor and liquid crystal equivalent capacitor respectively and connected to ground, and the driving voltage output line is used to output the driving voltage used for simulation to the said pixels of the LCD panel so as to display images, and it is characterized in that the said input data line is con-

nected to a data driver, the said input control line is connected to the gate driver, the said gate driver contains: the first, the second, and the third output enable (OE) input lines and the first, the second, and the third start pulse horizontal (STH) input lines, and receives the related signals via the said input lines, the said output enable (OE) signals input by the said gate drivers are so controlled that the three sets of synchronous control voltage pulses generated at the output of the said gate drivers are formed by and selected from the following three sets of control voltage pulses: (1) (G_1 , G_m), (2) (G_{m+1} , G_{2m}), (3) (G_{2m+1} , G_{3m}); and these three sets control voltage pulses (1, 2, 3) are provided to the gate of the said transistors (Q1) through the corresponding first, or second, and third input control lines, and it is characterized in that when activated by the said three sets of synchronous control signals (1, 2, 3) the said circuit feeds the said data signal to the said driving voltage output line; and the driving voltage pulse V_{LC} generated through the control of the gate can be used to drive the pixels to simultaneously generate three synchronous scanning lines separated by m scanning lines on the display screen, so as to display images.

Simulation Method

[0124] The following is the simulation method used for the simulation device according to the sixth embodiment of the present invention, comprising the following steps: (I) providing the data signal (D_1) with periodic pulse waveform to the source of the said first transistor (Q1); (II) providing the OE and STH control signals to the first, second, and third output enable (OE) input lines and start pulse horizontal (STH) input lines of the said gate driver, and receiving the related signals via the said input lines, the said output enable (OE) signals input by the said gate drivers are so controlled that the three sets of synchronous control voltage pulses generated at the output of the said gate drivers are selected from the following three sets of control voltage pulses: (1) (G_1 , G_m), (2) (G_{m+1} , G_{2m}), (3) (G_{2m+1} , G_{3m}); and these three sets of control voltage pulses (1,2,3) are provided to the gate of the said transistors (Q1) through the corresponding first, second and third input control lines, and it is characterized in that when activated by the said three sets of synchronous control signals (1, 2, 3), the said circuit feeds the said data signal to the said driving voltage output line; and (III) outputting the said output driving voltage generated by the above steps to the said pixels, so as to simultaneously generate three synchronous scanning lines separated by m scanning lines on the display screen in a cyclic alternating manner, so as to display images.

Waveform analysis

[0125] In the following analysis, please refer to Figures 13(a) to 13(e) as we describe in detail the relations

between the waveforms of the pulses of control voltages (G_1 , G_m), (G_{m+1} , G_{2m}), (G_{2m+1} , G_{3m}) and the pulses of the driving voltages D_1 , V_{LC} generated by the simulation device of Figures 11(a) and 11(b) according the sixth embodiment of the present invention.

[0126] Since usually AC voltage is utilized as the driving voltage for driving the liquid crystal, this voltage indicates the phenomenon of alternating positive and negative phases during the control and driving process of the liquid crystal (namely, the waveforms of the pulses of driving voltages D_1 , V_{LC} indicate the phenomenon of alternating positive and negative phases relative to the reference voltage V_{COM}).

[0127] These waveforms proceed sequentially and periodically from time points A1 to A6 repeatedly in the following manner:

[0128] The value of driving voltage pulse D_1 in the (N-1)th frame before time point A1 is V_1 , (code 0), and the value of the driving voltage pulse V_{LC} is V_1 , (code 0) of negative polarity; at time point A1, the waveform enters the Nth frame, at this time the value of the driving voltage pulse D_1 increases to V_2 (code 32), and due to the activation of the control voltage G_1 , therefore the value of output driving voltage pulse V_{LC} generated by the simulation device also increases to V_2 (code 32) of positive polarity and it remains so until time point A2; then the time proceeds to time point A2, at this time the value of driving voltage pulse D_1 is V_1 (code 0), and due to the activation of control voltage pulse G_1 , resulting in the value of driving voltage pulse V_{LC} to drop momentarily from V_2 (code 32) to V_1 (code 0) and is still of positive polarity, and this value is maintained until time point A3; then the time proceeds to time point A3 and enters the (N+1)th frame, at this time the value of the driving voltage pulse D_1 drops to V_3 , (code 120), and due to the activation of control voltage pulse G_1 , the value of the driving voltage pulse V_{LC} also momentarily drops to V_3 , (code 120) of negative polarity, and it remains so until time point A4; then time proceeds to A4, at this time, the value of driving voltage pulse D_1 is still V_1 , (code 0), and due to the activation of control voltage pulse G_1 , resulting in the value of the driving voltage pulse V_{LC} also increases to V_1 , (code 0) and is still of negative polarity until time point A5; then time proceeds to time point A5 and starts to enter the (N+2)th frame, at this time the value of the driving voltage pulse D_1 increases to V_3 (code 120), and due to the activation of the control voltage pulse G_1 , resulting in the value of the driving voltage pulse V_{LC} also increases momentarily to V_3 (code 120) of positive polarity, and it remains so until time point A6.

[0129] The variations of control voltage pulses G_{m+1} , G_{2m+1} and driving voltage pulses D_1 , and V_{LC} at the various time points after time points A6 can easily be inferred based on the above descriptions.

[0130] The dotted line as shown in Figure 13(a) is the liquid crystal display optical response characteristic curve produced while performing the simulation drive. When the output driving voltage V_{LC} of the simulation

device between each time point is code 0 as shown in the figure, this means that the black line scanning is performed on the display screen during this period, and by doing so, it can achieve the same results as inserting black frames or shutting off the backlights, so as to achieve the purpose of simulating CRT display impulse type image display.

[0131] In summary, the purpose of the present invention is to generate three synchronous scanning lines on the display screen as shown in Figures 13 (b), 13(c) and 13(d). G_1 , G_{m+1} , G_{2m+1} are synchronous control voltage pulses, and three sets of scanning lines are generated on the display screen by the driving voltage pulses generated through the control of the said control voltage pulses, and perform the synchronous line scanning on the screen separated by m scanning lines so as to display images.

[0132] Therefore, according to the design of the present invention, G_{m+1} and G_1 are synchronous control voltage pulses, and the scanning lines generated through the control of G_{m+1} and the scanning lines generated through the control of G_1 are separated by m scanning lines on the screen, and these two sets of scanning lines perform scanning on the screen in a synchronous manner, namely, start scanning on the screen from the first and the (m+1)th scanning lines respectively. The relations between the waveforms of the control voltage pulses G_{m+1} and the driving voltage pulses D_1 , V_{LC} are the same as those between waveforms of the control voltage pulse G_1 and the driving voltage pulses D_1 , V_{LC} (namely, as explained above with reference to Figures 13(a) to 13(e)), therefore, it will not be repeated here.

[0133] And at the same time, the corresponding driving voltage pulses generated by the control voltage pulses (G_{m+1} , G_{2m}), (G_{2m+1} , G_{2m}), and the resulting scanning lines generated on the screen, start scanning lines generated on the screen, start scanning from the (m+1)th, (2m+1)th scanning lines downward on the screen respectively in a synchronous manner (namely, the three sets of scanning lines generated on the display screen by the present embodiment, start scanning downward synchronously from the first, (m+1)th and (2m+1)th scanning lines in a repeated cyclic manner). And the relations between the waveforms of the respective control voltage pulses (G_{m+1} , G_{2m}), (G_{2m+1} , G_{3m}) and the driving voltage pulses D_1 , V_{LC} are the same as those between the waveforms of the respective control voltage pulses (G_1 , G_m) and driving voltage pulse D_1 , V_{LC} (namely, as explained above with reference to Figures 13(a) to 13(e)). Therefore, it will not repeated here.

[0134] For the sake of easy and convenient explanation and understanding, the waveform of the driving voltage pulse V_{LC} output by the simulation device of the present Embodiment as shown above is the same as that of Embodiment 1, so as to avoid it being too complicated to understand in the process of explanation. However, the waveform can be designed to have vari-

ous variations according to the actual requirements of the LCD display.

[0135] As it is known from the detailed description of the above six embodiments of the present invention that, the method and device of the present invention are characterized in that, the scanning black lines as described above can also achieve the similar effects of writing black frames, blinking backlights, or the combination of this two methods of the prior art, so as to simulate the CRT impulse type image display with LCD display, and apparently it is superior to the prior art for the following reasons:

[0136] (1) The present invention can save the extra cost and expense of the additional frequency doubling device or the backlight blinking equipment as required by the prior art;

[0137] (2) The present invention can avoid the electric magnetic interference induced by the additional equipment;

[0138] (3) The especially important feature of the present invention is, the interval between two input control voltage pulses G1 and G1' within the duration of the same frame can be adjusted depending on the actual requirements, so as to make the duration of the liquid crystal optical gray level response and the black line scanning (especially the black line scanning) adjustable in the duration of the same frame. Therefore, the designer of the LCD display is able to adjust the duration of the black line scanning depending on the time required by the optical response characteristic of different liquid crystal material, and the present invention can not only provide adequate design flexibility, but can also eliminate thoroughly the phenomenon of images superposition and outlines blurring created by the "after image" of the prior art, so as to optimize the quality of the images displayed. Therefore, the present invention can indeed achieve the purpose and the effectiveness of simulating the CRT impulse type image display with LCD display. The description above indicates all the features of the present invention superior to those of the prior art.

[0139] Summing up the above, the method and device utilized by the present invention in simulating the CRT impulse type image display can indeed overcome and improve the drawbacks and limitations of the similar liquid crystal display of the prior art, it can save the extra cost and expense of the additional equipment and significantly improve its functions. Therefore, the method and device used by the present invention in simulating the CRT impulse type image display is indeed superior to those of the prior art. The present invention does have the value of utilization in the industry, and it does contain novelty and inventive steps, and it is in conformity with the patent requirements.

[0140] The description mentioned above only relates to the preferred Embodiments of the present invention, and it is intended to be illustrative rather than restrictive to the contents of the claims and the present invention;

and various changes and modifications can be made by the people familiar with this technology without departing from the scope of the present invention and the appended claims.

Claims

1. A device used for simulating CRT impulse type image display, comprising:

a first input control line;
a second input control line;
a first input data line;
a second input data line;
a first capacitor;
a second capacitor;
a driving voltage output line;
a first transistor, comprising: a first gate connected to the first input control line, a first source connected to the first input data line, and a first drain connected to the driving voltage output line and the first capacitor and the drain of the second transistor; and
a second transistor, comprising: a second gate connected to the second input control line, a second source connected to the second input data line, a second drain connected to the drain of the said first transistor and the second capacitor and driving voltage output line;

wherein the said first capacitor and the said second capacitor are storage capacitor and liquid crystal equivalent capacitor respectively and are connected to ground, and the driving voltage output line is used to output the driving voltage used for simulation to the said pixels of the LCD panel so as to display images;

and **characterized in that** the said first and second input control lines are connected to a gate driver, and the said first and second input data lines are connected to a data driver respectively.

2. A method used for simulating CRT impulse type image display, comprising the following steps:

(1) providing a circuit comprising a first input control line, a second input control line, a first input data line, a second input data line, a first transistor, a second transistor, a first capacitor, a second capacitor, and a driving voltage output line;
(2) providing the first control signal with periodic pulse waveforms to the first gate of the first transistor of the said circuit;
(3) providing the second control signal with periodic pulse waveforms to the second gate of the second transistor of the said circuit;

- (4) the second control signal is the same as the first control signal except the phase delay;
- (5) providing the first data signal to the source of the first transistor of the said circuit, when activated by the said first control signal, the said circuit feeds the first data signal to the said driving voltage output line;
- (6) providing the second data signal to the source of the second transistor of the said circuit, when activated by the said second control signal, the said circuit feeds the second data signal to the said driving voltage output line; and
- (7) outputting the said output driving voltages generated by the above steps to the said pixels, so as to display images.
3. The method as claimed in Claim 2, wherein since AC voltage is used as the control voltage and driving voltage, these voltages indicate the phenomenon of alternating positive and negative phases during their control and driving processes, and their waveforms proceed sequentially and periodically from time points A1 to A6 repeatedly in the following manner.
- (a) the value of driving voltage pulse D_1 in the (N-1)th frame before time point A1 is V_1 , and the value of the driving voltage pulse V_{LC} is V_1 of negative polarity;
- (b) at time point A1, the waveform enters the Nth frame, at this time the value of the driving voltage pulse D_1 increases to V_2 , and due to the activation of the control voltage pulse G_1 , therefore the value of driving voltage pulse V_{LC} generated by the simulation device also increases to V_2 of positive polarity and remains so until time point A2;
- (c) then the time proceeds to time point A2, at this time the value of driving voltage pulse D_1 is V_1 , and due to the activation of control voltage pulse G_1 , resulting in the value of driving voltage pulse V_{LC} to drop momentarily from V_2 to V_1 and is still of positive polarity, and this value is maintained until time point A3;
- (d) then the time proceeds to time point A3 and enters the (N+1)th frame, at this time the value of the driving voltage pulse D_1 drops to V_3 , and is of negative polarity, and due to the activation of control voltage pulse G_1 , the value of the driving voltage pulse V_{LC} also momentarily drops to V_3 of negative polarity, and it remains so until time point A4;
- (e) then time proceeds to A4, and at this time, the value of driving voltage pulse D_1 is still V_1 , and due to the activation of control voltage pulse G_1 , resulting in the value of the driving voltage pulse V_{LC} also increases to V_1 , and is still of negative polarity and it remains so until time point A5; and
- (f) then time proceeds to time point A5 and starts to enter the (N+2)th frame, at this time the value of the driving voltage pulse D_1 increases to V_3 , and due to the activation of the control voltage pulse G_1 , resulting in the value of the driving voltage pulse V_{LC} also increases momentarily to V_3 of positive polarity, and it remains so until time point A6.
4. The method as claimed in Claim 3, wherein when the output driving voltage V_{LC} of the simulation device between each time point is code 0, this means that the black line scanning is performed on the display screen during this period, and it can achieve the better results than inserting black frames or shutting off the backlights, so as to optimally realize the purpose of simulating CRT display impulse type image display with LCD display.
5. A device used for simulating CRT impulse type image display, comprising:
- a first input control line;
 - a second input control line;
 - a first input data line;
 - a second input data line;
 - a third input data line;
 - a fourth input data line;
 - a fifth input data line;
 - a first capacitor;
 - a second capacitor;
 - a third transistor;
 - a fourth transistor;
- driving voltage output line;
- a first transistor, comprising: a first gate connected to the first input control line, a first source connected to the input data line, and a first drain connected to the driving voltage output line and the first capacitor and the drain of the second transistor; and
- a second transistor, comprising: a second gate connected to the second input control line, a second source connected to the second input data line, a second drain connected to the drain of the said first transistor and the second capacitor and driving voltage output line;
- wherein the said first capacitor and the said second capacitor are storage capacitor and liquid crystal equivalent capacitor respectively and are connected to ground, and the driving voltage output line is used to output the driving voltage used for simulation to the said pixels of the LCD panel so as to display images,

characterized in that the said first and second input control lines are connected to a gate driver, and the said first and second input data lines are connected to the drains of two another switching transistors connected in parallel, the sources of the said two switching transistors connected in parallel are connected to a data driver, with its gate connected to the third and fourth input data lines, and the time difference between the periodic pulse waveforms of the said first and second control signals is the time difference across n scanning lines generated by n pulses, and which can be adjusted.

6. A method used for simulating CRT impulse type image display, comprising the following steps:

- (1) providing a circuit, comprising a first input control line, a second input control line, a first input data line, a second input data line, a third input data line, a fourth input data line, a fifth input data line, a first transistor, a second transistor, a third transistor, a fourth transistor, a first capacitor, a second capacitor, and a driving voltage output line;
- (2) providing the first control signal with periodic pulse waveforms to the first gate of the first transistor of the said circuit;
- (3) providing the second control signal with periodic pulse waveforms to the second gate of the second transistor of the said circuit;
- (4) the second control signal is the same as the first control signal except the phase delay;
- (5) providing the fifth data signal to the sources of the third transistor and fourth transistor connected in parallel;
- (6) providing the third data signal to the gate of the third transistor;
- (7) providing the voltage pulse generated by the drain of the third transistor to the source of the first transistor as the first data signal, when the said first transistor is activated by the first control signal, the first data signal is fed by the said circuit to the driving voltage output line;
- (8) providing the fourth data signal to the gate of the fourth transistor;
- (9) providing the voltage pulse generated by the drain of the fourth transistor to the source of the second transistor as the second data signal, when the said second transistor is activated by the second control signal, the second data signal is fed by the said circuit to the driving voltage output line; and
- (10) outputting the said output driving voltage generated by the above steps to the said pixels so as to display images.

7. The method as claimed in Claim 6, wherein since AC voltage is used as the control voltage and driv-

ing voltage, these voltages indicate the phenomenon of alternating positive and negative phases during their control and driving processes, and their waveforms proceed sequentially and periodically from time points A1 to A6 repeatedly in the following manner:

- (a) the value of driving voltage pulse D_1 in the (N-1)th frame before time point A1 is V_1 , and the value of the driving voltage pulse V_{LC} is V_1 of negative polarity;
- (b) at time point A1, the waveform enters the Nth frame, at this time the value of the driving voltage pulse D_1 increases to V_2 , and due to the activation of the control voltage pulse G_1 , therefore the value of driving voltage pulse V_{LC} generated by the simulation device also increases to V_2 of positive polarity and remains so until time point A2;
- (c) then the time proceeds to time point A2, at this time the value of driving voltage pulse D_1 is V_1 , and due to the activation of control voltage pulse G_1 , resulting in the value of driving voltage pulse V_{LC} to drop momentarily from V_2 to V_1 and is still of positive polarity, and this value is maintained until time point A3;
- (d) then the time proceeds to time point A3 and enters the (N+1)th frame, at this time the value of the driving voltage pulse D_1 drops to V_3 and is of negative polarity, and due to the activation of control voltage pulse G_1 , the value of the driving voltage pulse V_{LC} also momentarily drops to V_3 of negative polarity, and it remains so until time point A4;
- (e) then time proceeds to A4, at this time, the value of driving voltage pulse D_1 is still V_1 , and due to the activation of control voltage pulse G_1 , resulting in the value of the driving voltage pulse V_{LC} also increases to V_1 and is still of negative polarity and it remains so until time point A5; and
- (f) then time proceeds to time point A5 and starts to enter the (N+2)th frame, at this time the value of the driving voltage pulse D_1 increases to V_3 , and due to the activation of the control voltage pulse G_1 , resulting in the value of the driving voltage pulse V_{LC} also increases momentarily to V_3 of positive polarity, and it remains so until time point A6.

8. The method as claimed in Claim 7, wherein when the output driving voltage V_{LC} of the simulation device between each time point is code 0, this means that the black line scanning is performed on the display screen during this period, and it can achieve the better results than inserting black frames or shutting off the backlights, so as to optimally realize the purpose of simulating CRT display impulse type

image display with LCD display.

9. A device used for simulating CRT impulse type image display, comprising:

a first input control line;
 a second input control line;
 a first input data line;
 a first capacitor;
 a second capacitor;
 driving voltage output line;
 a first transistor, comprising: a first gate connected to the first input control line, a first source connected to the first input data line, and a first drain connected to the driving voltage output line and the first capacitor and the second drain of the second transistor; and
 a second transistor, comprising: a second gate connected to the second input control line, a second source connected to ground, a second drain connected to the drain of the said first transistor and the second capacitor and driving voltage output line;

wherein the said first capacitor and the said second capacitor are storage capacitor and liquid crystal equivalent capacitor respectively and are connected to ground, and the driving voltage output line is used to output the driving voltage used for simulation to the said pixels of the LCD panel so as to display images,

characterized in that the said first and second input control lines are connected to a gate driver, and the said first input data line is connected to a data driver; and the time difference between the waveforms of the periodic pulses of the first and second control signals is the time difference across n scanning lines generated by n pulses, and which can be adjusted.

10. A method used for simulating CRT impulse type image display, comprising the following steps:

(1) providing a circuit, comprising a first input control line, a second input control line, a first input data line, a first transistor, a second transistor, a first capacitor, a second capacitor, and a driving voltage output line;
 (2) providing the first control signal with periodic pulse waveforms to the first gate of the first transistor of the said circuit;
 (3) providing the second control signal with periodic pulse waveforms to the second gate of the second transistor of the said circuit, wherein the second control signal is the same as the first control signal except the phase delay;
 (4) providing the first data signal to the source of the first transistor of the said circuit, when

activated by the said first control signal, the said circuit feeds the first data signal to the said driving voltage output line;

(5) when activated by the second control signal, the ground potential voltage is fed by the said circuit to the driving voltage output line; and

(6) outputting the said output driving voltages generated by the above steps to the said pixels so as to display images.

11. The method as claimed in Claim 10, wherein since AC voltage is used as the control voltage and driving voltage, these voltages indicate the phenomenon of alternating positive and negative phases during their control and driving processes, and their waveforms proceed sequentially and periodically from time points A1 to A6 repeatedly in the following manner:

(a) the value of driving voltage pulse D_1 in the (N-1)th frame before time point A1 is V_2 , and the value of the driving voltage pulse V_{LC} is V_{com} (since the source of the second transistor is connected to V_{com});

(b) at time point A1, the waveform enters the Nth frame, at this time the value of the driving voltage pulse D_1 increases to V_2 , and due to the activation of the control voltage pulse G_1 , therefore the value of driving voltage pulse V_{LC} generated by the simulation device also increases to V_2 of positive polarity and it remains so until time point A2;

(c) then the time proceeds to time point A2, at this time the value of driving voltage pulse D_1 is still V_2 , and due to the activation of control voltage pulse G_1 (since the source of the second transistor is connected to V_{com}), resulting in the value of driving voltage pulse V_{LC} to drop momentarily from V_2 to V_1 and is still of positive polarity, and this value is maintained until time point A3;

(d) then the time proceeds to time point A3 and enters the (N+1)th frame, at this time the value of the driving voltage pulse D_1 drops to V_3 , and is of negative polarity, and due to the activation of control voltage pulse G_1 , the value of the driving voltage pulse V_{LC} also momentarily drops to V_3 , of negative polarity, and it remains so until time point A4;

(e) then time proceeds to time point A4, at this time, the value of driving voltage pulse D_1 is still V_3 , of negative polarity, and due to the activation of control voltage pulse G_1 (since the source of the second transistor is connected to V_{com}), resulting in the value of the driving voltage pulse V_{LC} also increases to V_{com} and is still of negative polarity and it remains so until time point A5; and

(f) then time proceeds to time point A5 and it starts to enter the (N+2)th frame, at this time the value of the driving voltage pulse D_1 increases to V_3 , and due to the activation of the control voltage pulse G_1 , resulting in the value of the driving voltage pulse V_{LC} also increases momentarily to V_3 of positive polarity, and it remains so until time point A6.

12. The method as claimed in Claim 11, wherein when the output driving voltage V_{LC} of the simulation device between each time point is code 0, this means that the black line scanning is performed on the display screen during this period, and it can achieve the better results than inserting black frames or shutting off the backlights, so as to optimally realize the purpose of simulating CRT display impulse type image display with LCD display.
13. A device used for simulating CRT impulse type image display, comprising:

a first input control line;
 a second input control line;
 a first input data line;
 a first capacitor;
 a second capacitor;
 a driving voltage output line;
 a first transistor, comprising: a gate connected to the first input control line or the second input control line, a source connected to the input data line, and a drain connected to the driving voltage output line and two capacitors connected in parallel; and

wherein the said first capacitor and second capacitor are connected to ground, and the driving voltage output line is used to output the driving voltage used for simulation to the said pixels of the LCD panel so as to display images,

characterized in that the said input data line is connected to a data driver, the said input control line is connected to the gate driver, the said gate driver contains: an output enable (OE) input line and a start pulse horizontal (STH) input line and receives the related signals via the said input lines, so as to generate the synchronous control voltage pulses G_1 , G_m of the said input control lines, and supply them to the gate of the said transistor via the first and second input control lines, and to generate the driving voltage pulse V_{LC} through its control, and then be able to generate two synchronous scanning lines separated by m scanning lines on the display screen simultaneously, so as to display images.

14. A method used for simulating CRT impulse type image display, comprising the following steps:

(1) providing a circuit, comprising a first input control line, a second input control line, a first input data line, a first transistor, a first capacitor, a second capacitor, and a driving voltage output line;
 (2) providing the data signal with periodic pulse waveform to the source of the said first transistor;
 (3) providing control signals OE and STH to the gate driver, so as to generate the synchronous control signals G_1 , G_m , and providing them to the gate of the said transistor via the first and second input control lines;
 (4) when activated by the said synchronous control signals G_1 , G_m , the said circuit feeds the said data signal to the said driving voltage output line; and
 (5) outputting the said output driving voltage generated by the above steps to the said pixels so as to display images.

15. The method as claimed in Claim 14, wherein since AC voltage is used as the control voltage and driving voltage, these voltages indicate the phenomenon of alternating positive and negative phases during their control and driving processes, and their waveforms proceed sequentially and periodically from time points A1 to A6 repeatedly in the following manner:

(a) the value of driving voltage pulse D_1 in the (N-1)th frame before time point A1 is V_1 , and the value of the driving voltage pulse V_{LC} is V_1 , of negative polarity;
 (b) at time point A1, the waveform enters the Nth frame, at this time the value of the driving voltage pulse D_1 increases to V_2 , and due to the activation of the control voltage G_1 , therefore the driving voltage pulse V_{LC} generated by the simulation device also increases to V_2 of positive polarity and remains so until time point A2;
 (c) then the time proceeds to time point A2, at this time the value of driving voltage pulse D_1 is V_1 , and due to the activation of control voltage pulse G_1 , resulting in the value of driving voltage pulse V_{LC} to drop momentarily from V_2 to V_1 and is still of positive polarity, and this value is maintained until time point A3;
 (d) then the time proceeds to time point A3 and enters the (N+1)th frame, at this time the value of the driving voltage pulse D_1 drops to V_3 , and is of negative polarity, and due to the activation of control voltage pulse G_1 , the value of the driving voltage pulse V_{LC} also momentarily drops to V_3 , of negative polarity, and it remains so until time point A4;
 (e) then time proceeds to A4, at this time, the

value of driving voltage pulse D_1 is still V_1 , and due to the activation of control voltage pulse G_1 , resulting in the value of the driving voltage pulse V_{LC} also increases to V_1 , and is still of negative polarity until time point A5; and
 (f) then time proceeds to time point A5 and starts to enter the (N+2)th frame, at this time the value of the driving voltage pulse D_1 increases to V_3 , and due to the activation of the control voltage pulse G_1 , resulting in the value of the driving voltage pulse V_{LC} also increases momentarily to V_3 of positive polarity, and it remains so until time point A6.

16. The method as claimed in Claim 15, wherein when the output driving voltage V_{LC} of the simulation device between each time point is code 0, this means that the black line scanning is performed on the display screen during this period, and it can achieve the better results than inserting black frames or shutting off the backlights, so as to optimally realize the purpose of simulating CRT display impulse type image display with LCD display.

17. A device used for simulating CRT impulse type image display, comprising:

a first input control line;
 a second input control line;
 a third input control line;
 a first input data line;
 a first capacitor;
 a second capacitor;
 a driving voltage output line; and
 a first transistor comprising: a gate connected to the first input control line or the second input control line or the third input control line; a source connected to the first input data line, and a drain connected to the driving voltage output line and two capacitors connected in parallel; and

wherein the said first capacitor and second capacitor are the storage capacitor and liquid crystal equivalent capacitor respectively and connected to ground, and the driving voltage output line is used to output the driving voltage used for simulation to the said pixels of the LCD panel so as to display images,

characterized in that the said input data line is connected to a data driver, the said input control line is connected to the gate driver, the said gate driver contains: the first, the second, and the third output enable (OE) input lines and the first, the second, and the third start pulse horizontal (STH) input lines, and receives the related signals via the said input lines, the said output enable (OE) signals input by the said gate drivers are so controlled that the two

sets of synchronous control voltage pulses generated at the output of the said gate drivers are selected from the following three sets of control voltage pulses: (1) (G_1 , G_m), (2) (G_{m+1} , G_{2m}), (3) (G_{2m+1} , G_{3m}); and these two sets of control voltage pulses (1, 3), or (1, 2), or (2, 3) are selected from the said three sets of control voltage pulses and then arranged and combined, such that they are provided to the gate of the said transistors through the corresponding first, or second, or third input control line in a cyclic alternating manner, and the driving voltage pulse V_{LC} generated through the control of the gate can be used to drive the pixels to simultaneously generate two synchronous scanning lines separated by $2m$ scanning lines on the display screen in a cyclic alternating manner, so as to display images.

18. A method used for simulating CRT impulse type image display, comprising the following steps:

(1) providing a circuit comprising: a first input control line, second input control line, a third input control line, a first input data line, a first transistor, a first capacitor, a second capacitor, and a driving voltage output line;
 (2) providing the data signal with periodic pulse waveform to the source of the said first transistor;
 (3) providing the OE and STH control signals to the first, second, and third output enable (OE) input lines and start pulse horizontal (STH) input lines of the said gate driver; and
 (4) receiving the related signals via the said input lines, the said output enable (OE) signals input by the said gate drivers are so controlled that the two sets of synchronous control voltage pulses generated at the output of the said gate drivers are selected from the following three sets of control voltage pulses: (1) (G_1 , G_m), (2) (G_{m+1} , G_{2m}), (3) (G_{2m+1} , G_{3m}); and these two sets of control voltage pulses (1, 3), or (1, 2), or (2, 3) are selected from the said three sets of control voltage pulses and then arranged and combined, such that they are provided to the gate of the said transistors through the corresponding first, second, or third input control lines in a cyclic alternating manner;

characterized in that when activated by the said two sets of synchronous control signals (1, 3), or (1, 2), or (2, 3), the said circuit feeds the said data signal to the said driving voltage output line; and outputting the said output driving voltage generated by the above steps to the said pixels, so as to simultaneously generate two synchronous scanning lines separated by $2m$ scanning lines on the display screen in a cyclic alternating manner, so as to display

play images.

19. The method as claimed in Claim 18, wherein since AC voltage is used as the control voltage and driving voltage, these voltages indicate the phenomenon of alternating positive and negative phases during their control and driving processes, and their waveforms proceed sequentially and periodically from time points A1 to A6 repeatedly in the following manner:

(a) the value of driving voltage pulse D_1 in the (N-1)th frame before time point A1 is V_1 , and the value of the driving voltage pulse V_{LC} is V_1 , of negative polarity;

(b) at time point A1, the waveform enters the Nth frame, at this time the value of the driving voltage pulse D_1 increases to V_2 , and due to the activation of the control voltage G_1 , therefore the value of output driving voltage pulse V_{LC} generated by the simulation device also increases to V_2 of positive polarity and it remains so until time point A2;

(c) then the time proceeds to time point A2, at this time the value of driving voltage pulse D_1 is V_1 , and due to the activation of control voltage pulse G_1 , resulting in the value of driving voltage pulse V_{LC} to drop momentarily from V_2 to V_1 and is still of positive polarity, and this value is maintained until time point A3;

(d) then the time proceeds to time point A3 and enters the (N+1)th frame, at this time the value of the driving voltage pulse D_1 drops to V_3 , and due to the activation of control voltage pulse G_1 , the value of the driving voltage pulse V_{LC} also momentarily drops to V_3 , of negative polarity, and it remains so until time point A4;

(e) then time proceeds to A4, at this time, the value of driving voltage pulse D_1 is still V_1 , and due to the activation of control voltage pulse G_1 , resulting in the value of the driving voltage pulse V_{LC} also increases to V_1 , and is still of negative polarity until time point A5; and

(f) then time proceeds to time point A5 and starts to enter the (N+2)th frame, at this time the value of the driving voltage pulse D_1 increases to V_3 , and due to the activation of the control voltage pulse G_1 , resulting in the value of the driving voltage pulse V_{LC} also increases momentarily to V_3 of positive polarity, and it remains so until time point A6.

20. The method as claimed in Claim 19, wherein when the output driving voltage V_{LC} of the simulation device between each time point is code 0, this means that the black line scanning is performed on the display screen during this period, and it can achieve the better results than inserting black frames or

shutting off the backlights, so as to optimally realize the purpose of simulating CRT display impulse type image display with LCD display.

21. A device used for simulating CRT impulse type image display, comprising:

a first input control line;
a second input control line;
a third input control line;
a first input data line;
a first capacitor;
a second capacitor;
a driving voltage output line; and
a first transistor comprising: a gate connected to the first input control line or the second input control line or the third input control line; a source connected to the first input data line, and a drain connected to the driving voltage output line and two capacitors connected in parallel; and

wherein the said first capacitor and second capacitor are the storage capacitor and liquid crystal equivalent capacitor respectively and connected to ground, and the driving voltage output line is used to output the driving voltage used for simulation to the said pixels of the LCD panel so as to display images;

characterized in that the said input data line is connected to a data driver, the said input control the said input data line is connected to a data driver, the said input control line is connected to the gate driver, the said gate driver contains: the first, the second, and the third output enable (OE) input lines and the first, the second, and the third start pulse horizontal (STH) input lines, and receives the related signals via the said input lines, the said output enable (OE) signals input by the said gate drivers are so controlled that the three sets of synchronous control voltage pulses generated at the output of the said gate drivers are formed by and selected from the following three sets of control voltage pulses: (1) (G_1 , G_m), (2) (G_{m+1} , G_{2m}), (3) (G_{2m+1} , G_{3m}); and these three sets control voltage pulses (1, 2, 3) are provided to the gate of the said transistors through the corresponding first, or second, and third input control lines; when activated by the said three sets of synchronous control signals (1, 2, 3) the said circuit feeds the said data signal to the said driving voltage output line; and the driving voltage pulse V_{LC} generated through the control of the gate can be used to drive the pixels to simultaneously generate three synchronous scanning lines separated by m scanning lines on the display screen, so as to display images.

22. A method used for simulating CRT impulse type im-

age display, comprising the following steps:

- (1) providing a circuit comprising: a first input control line, a second input control line, a third input control line, a first input data line, a first transistor, a first capacitor, a second capacitor, and a driving voltage output line; 5
- (2) providing the data signal with periodic pulse waveform to the source of the said first transistor; 10
- (3) providing the OE and STH control signals to the first, second, and third output enable (OE) input lines and start pulse horizontal (STH) input lines of the said gate driver, and
- (4) receiving the related signals via the said input lines, the said output enable (OE) signals input by the said gate drivers are so controlled that the three sets of synchronous control voltage pulses generated at the output of the said gate drivers are selected from the following three sets of control voltage pulses: (1) (G_1 , G_m), (2) (G_{m+1} , G_{2m}), (3) (G_{2m+1} , G_{3m}); and these three sets of control voltage pulses (1, 2, 3) are provided to the gate of the said transistors through the corresponding first, second and third input control lines, 25

characterized in that when activated by the said three sets of synchronous control signals (1,2,3), the said circuit feeds the said data signal to the said driving voltage output line; and outputting the said output driving voltage generated by the above steps to the said pixels, so as to simultaneously generate three synchronous scanning lines separated by m scanning lines on the display screen in a cyclic alternating manner, so as to display images. 30 35

23. The method as claimed in Claim 22, wherein since AC voltage is used as the control voltage and driving voltage, these voltages indicate the phenomenon of alternating positive and negative phases during their control and driving processes, and their waveforms proceed sequentially and periodically from time points A1 to A6 repeatedly in the following manner: 40 45

- (a) the value of driving voltage pulse D_1 in the (N-1)th frame before time point A1 is V_1 , and the value of the driving voltage pulse V_{LC} is V_1 , of negative polarity; 50
- (b) at time point A1, the waveform enters the Nth frame, at this time the value of the driving voltage pulse D_1 increases to V_2 , and due to the activation of the control voltage G_1 , therefore the value of output driving voltage pulse V_{LC} generated by the simulation device also increases to V_2 of positive polarity and it remains 55

so until time point A2;

(c) then the time proceeds to time point A2, at this time the value of driving voltage pulse D_1 is V_1 , and due to the activation of control voltage pulse G_1 , resulting in the value of driving voltage pulse V_{LC} to drop momentarily from V_2 to V_1 and is still of positive polarity, and this value is maintained until time point A3;

(d) then the time proceeds to time point A3 and enters the (N+1)th frame, at this time the value of the driving voltage pulse D_1 drops to V_3 , and due to the activation of control voltage pulse G_1 , the value of the driving voltage pulse V_{LC} also momentarily drops to V_3 , of negative polarity, and it remains so until time point A4;

(e) then time proceeds to A4, at this time, the value of driving voltage pulse D_1 is still V_1 , and due to the activation of control voltage pulse G_1 , resulting in the value of the driving voltage pulse V_{LC} also increases to V_1 , and is still of negative polarity until time point A5; and

(f) then time proceeds to time point A5 and starts to enter the (N+2)th frame, at this time the value of the driving voltage pulse D_1 increases to V_3 , and due to the activation of the control voltage pulse G_1 , resulting in the value of the driving voltage pulse V_{LC} also increases momentarily to V_3 of positive polarity, and it remains so until time point A6.

24. The method as claimed in Claim 23, wherein when the output driving voltage V_{LC} of the simulation device between each time point is code 0, this means that the black line scanning is performed on the display screen during this period, and it can achieve the better results than inserting black frames or shutting off the backlights, so as to optimally realize the purpose of simulating CRT display impulse type image display with LCD display.

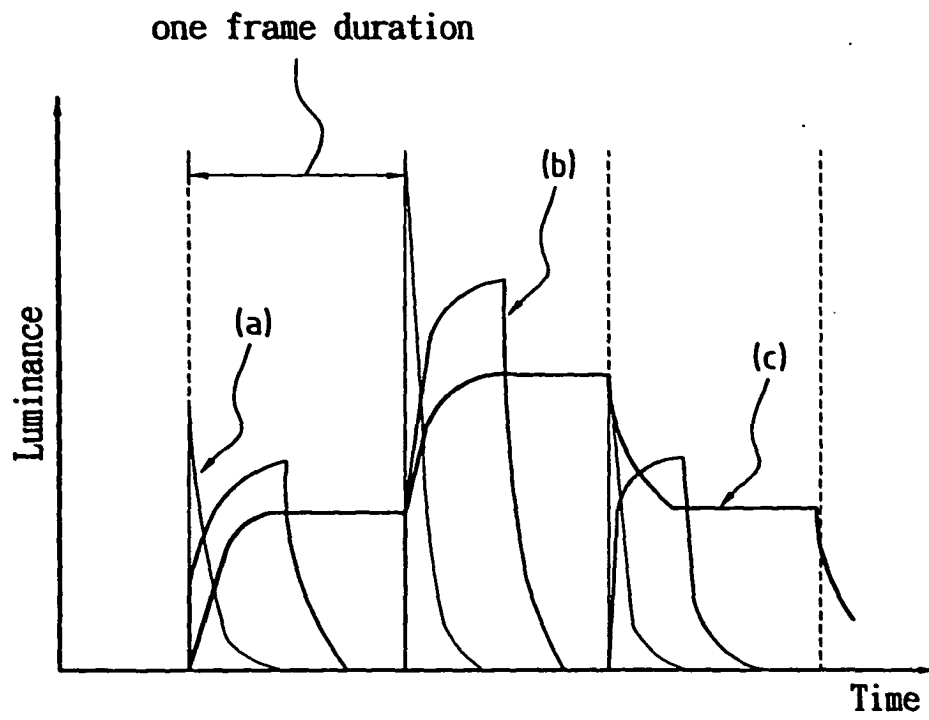


FIG. 1

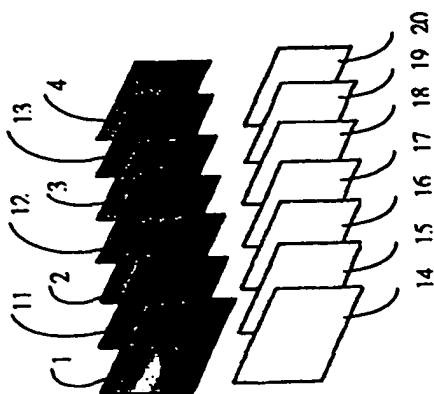


FIG. 2A

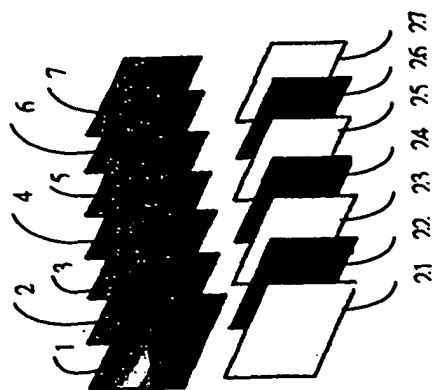


FIG. 2B

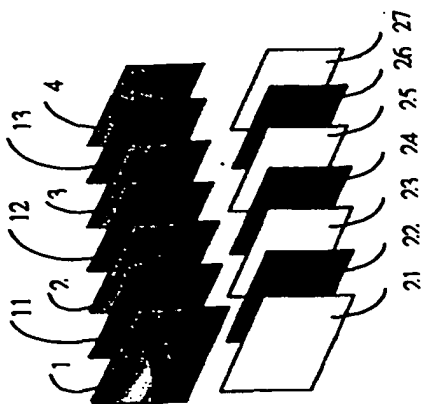
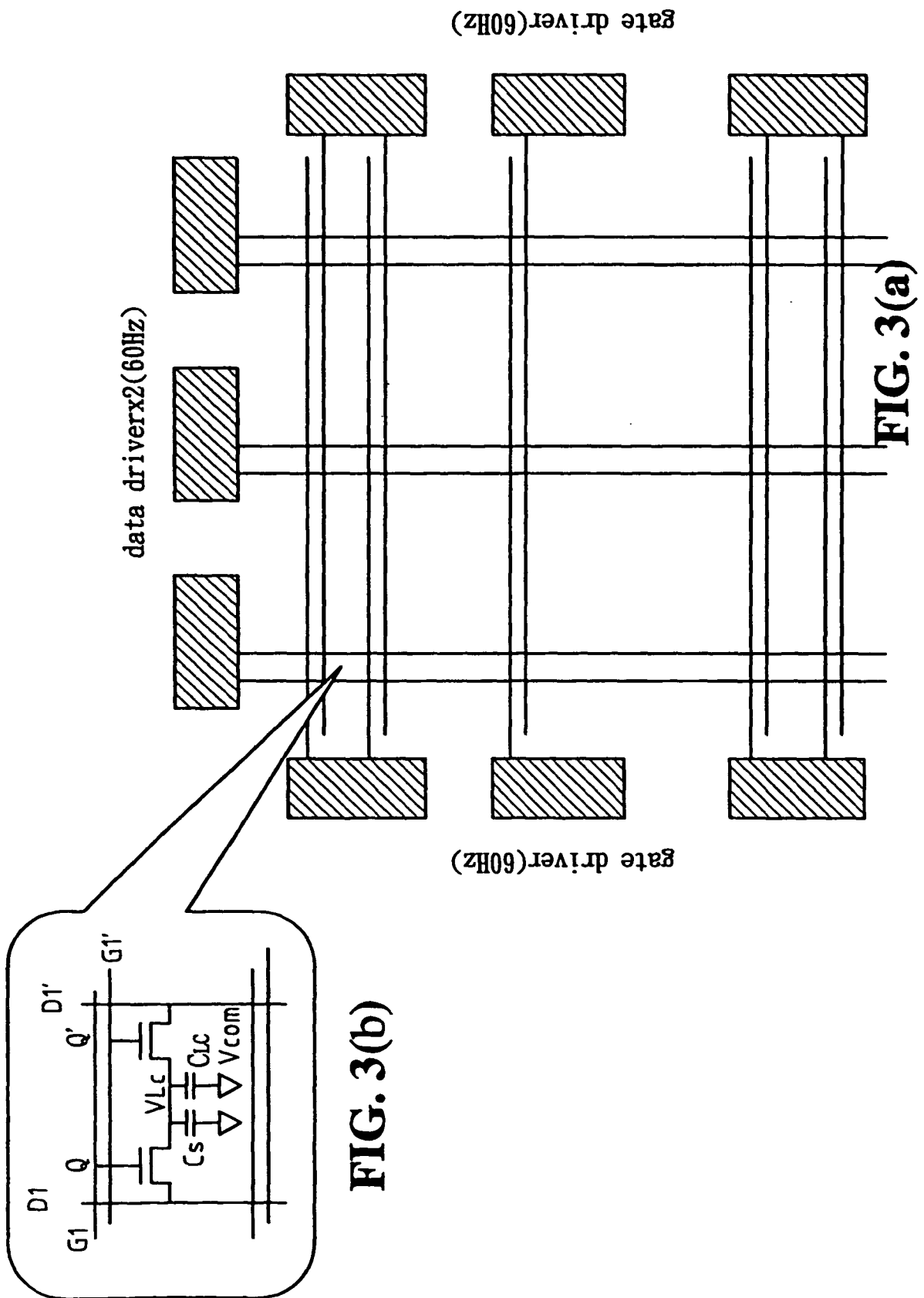
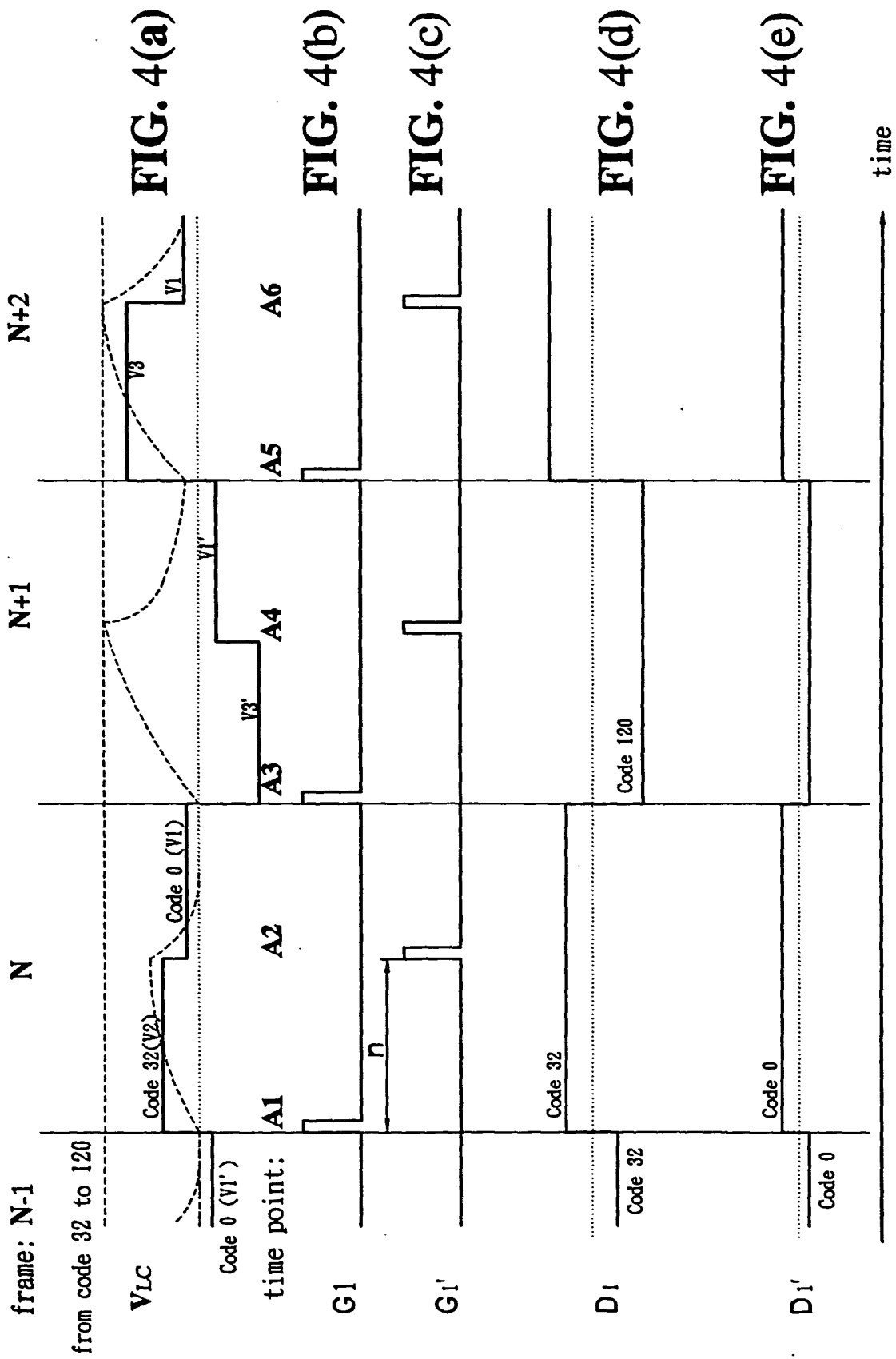
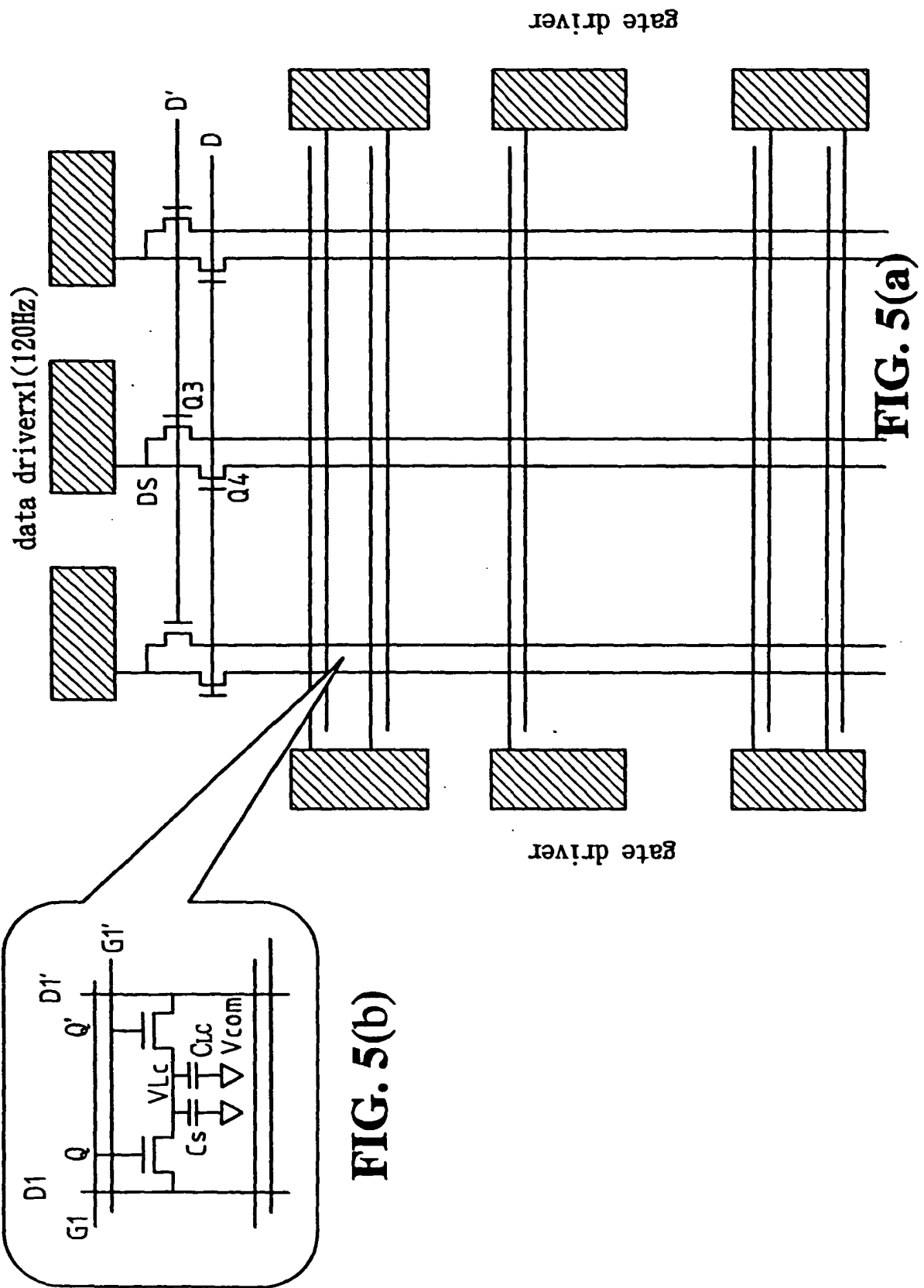
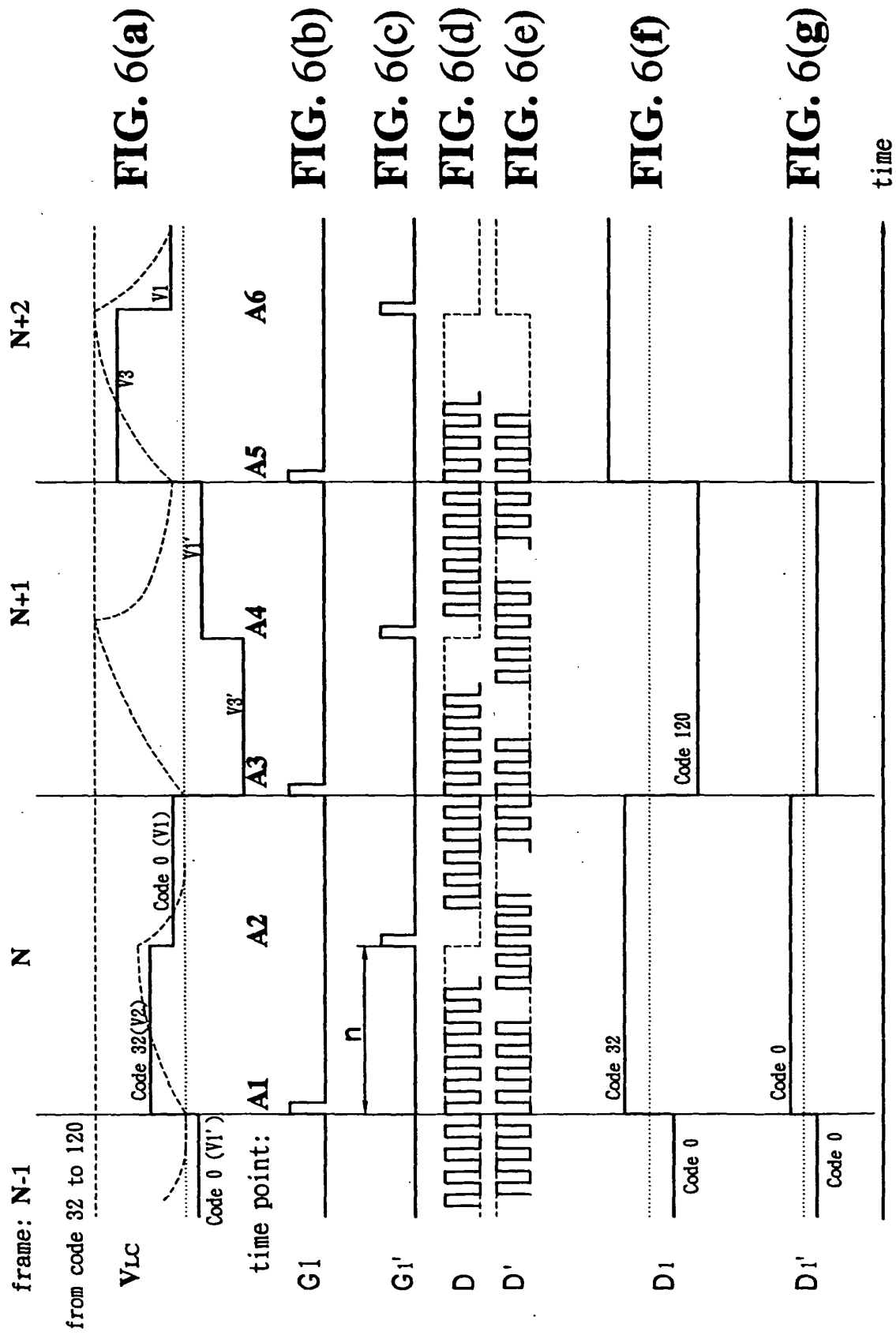


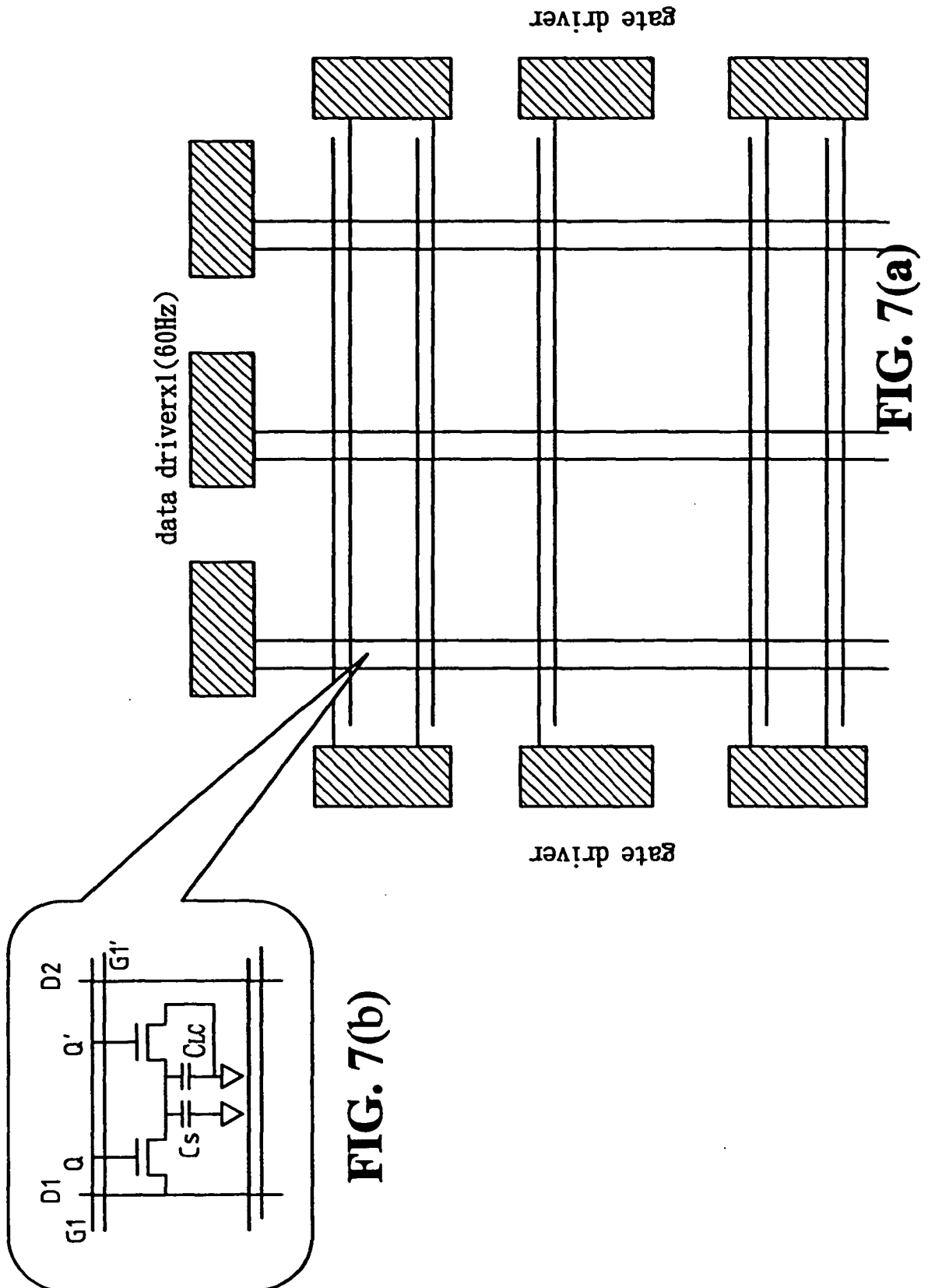
FIG. 2C

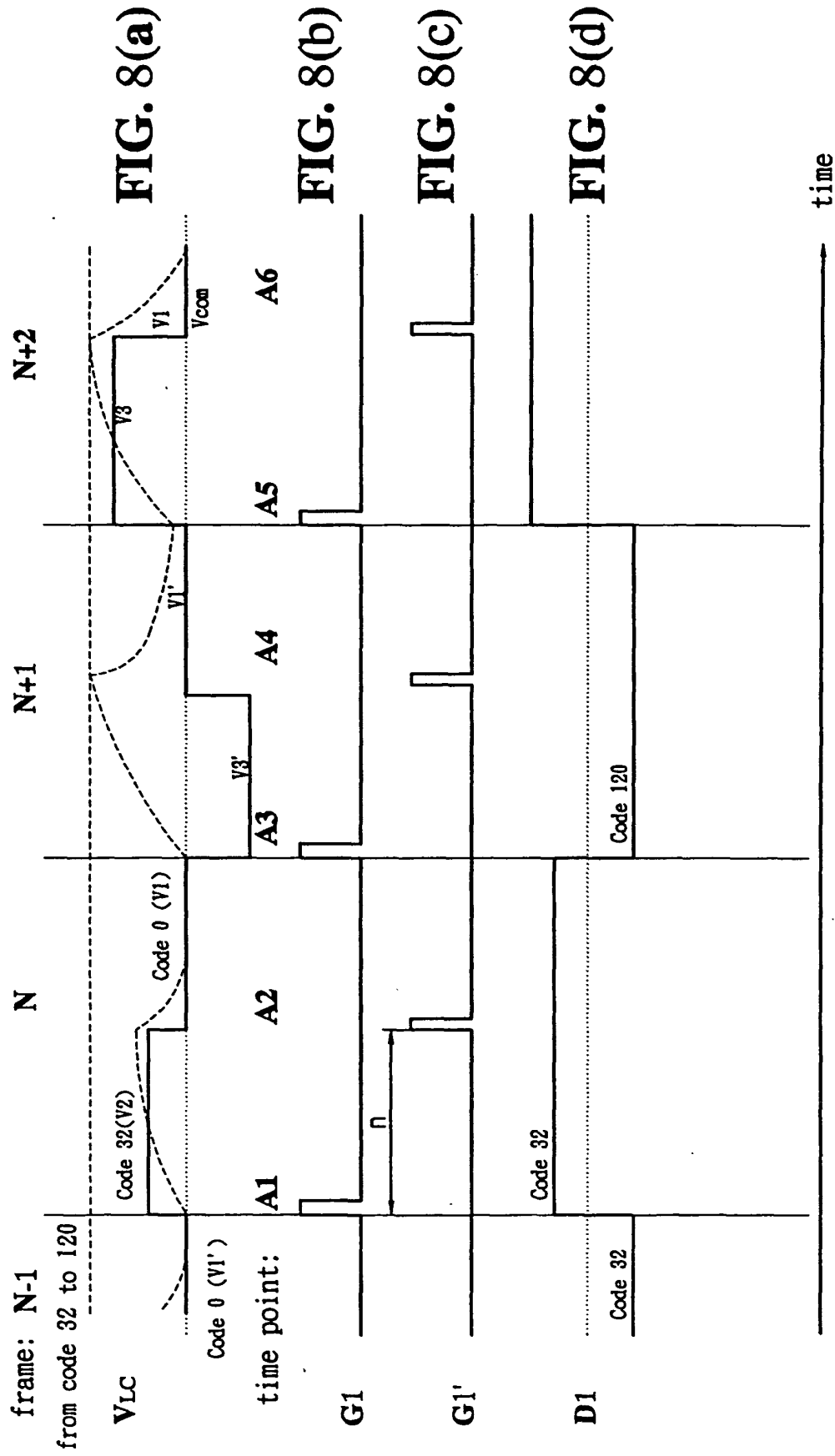


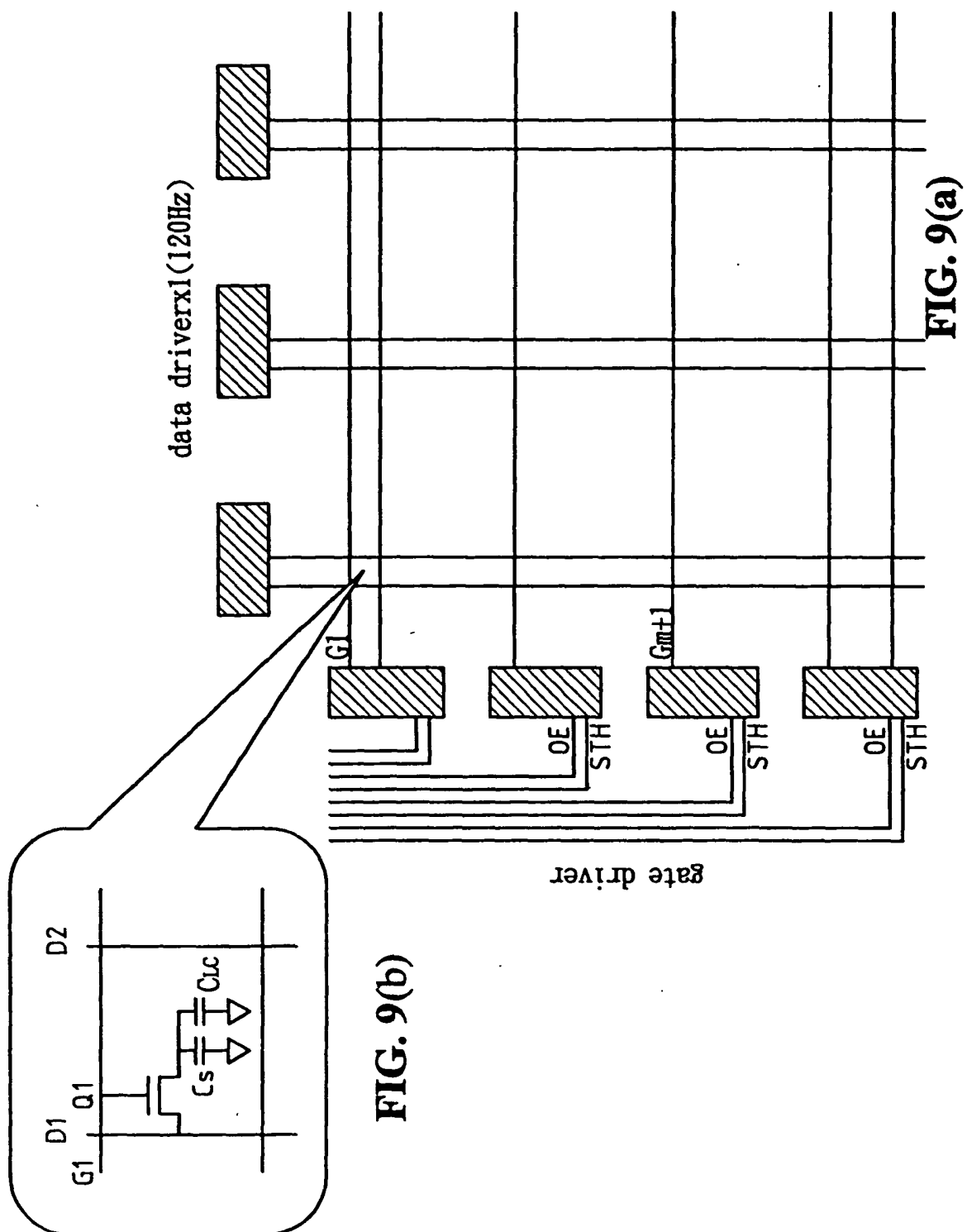


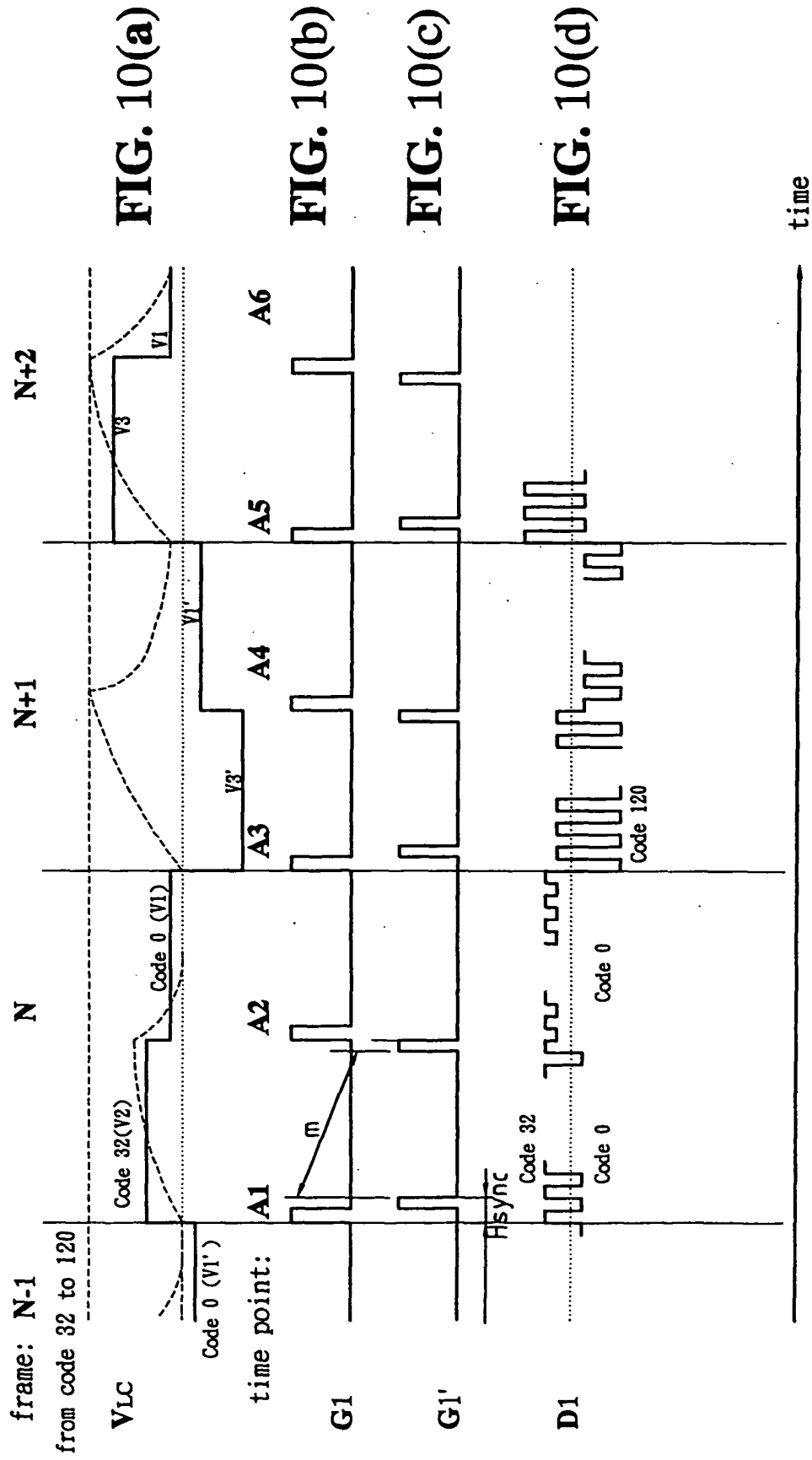












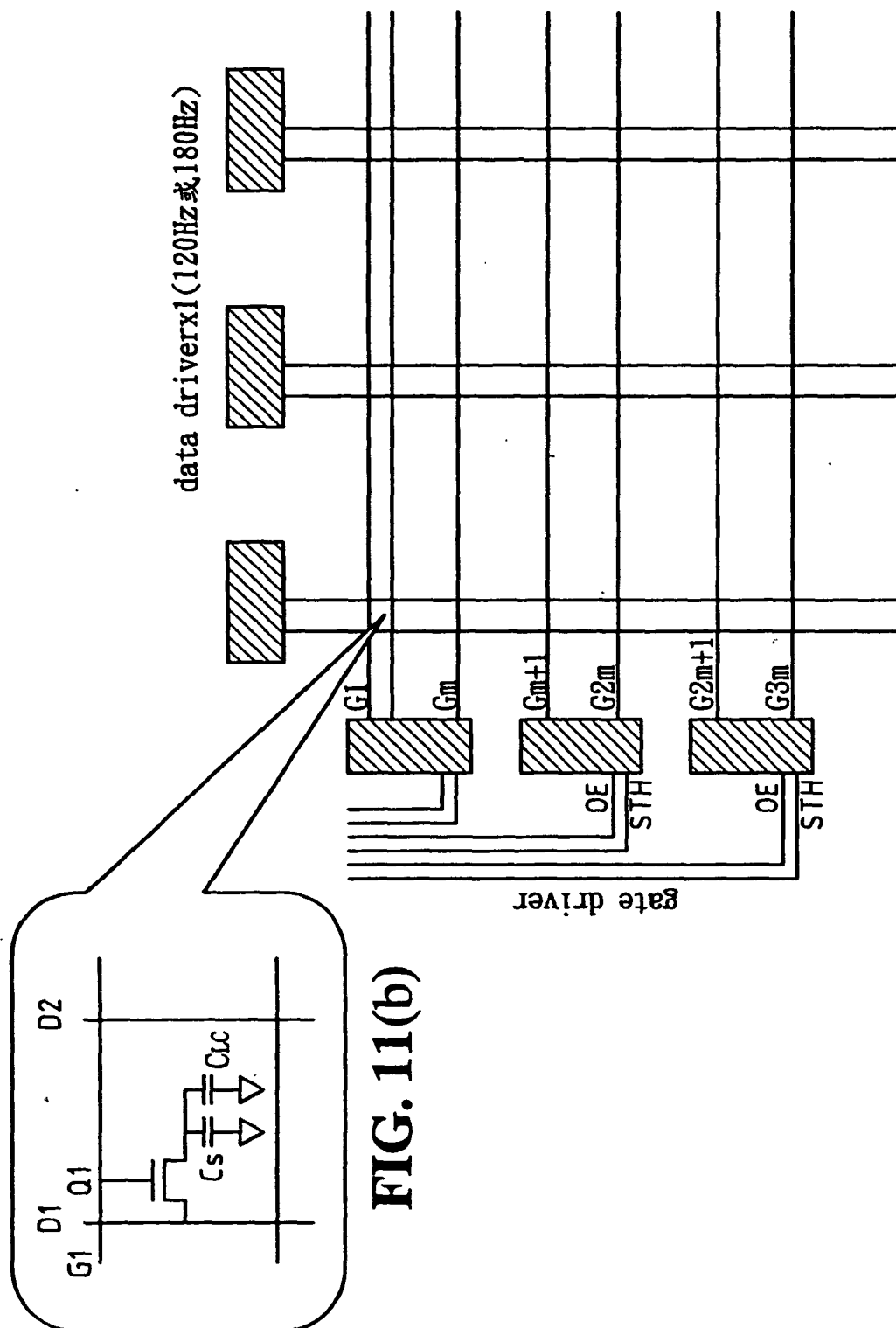
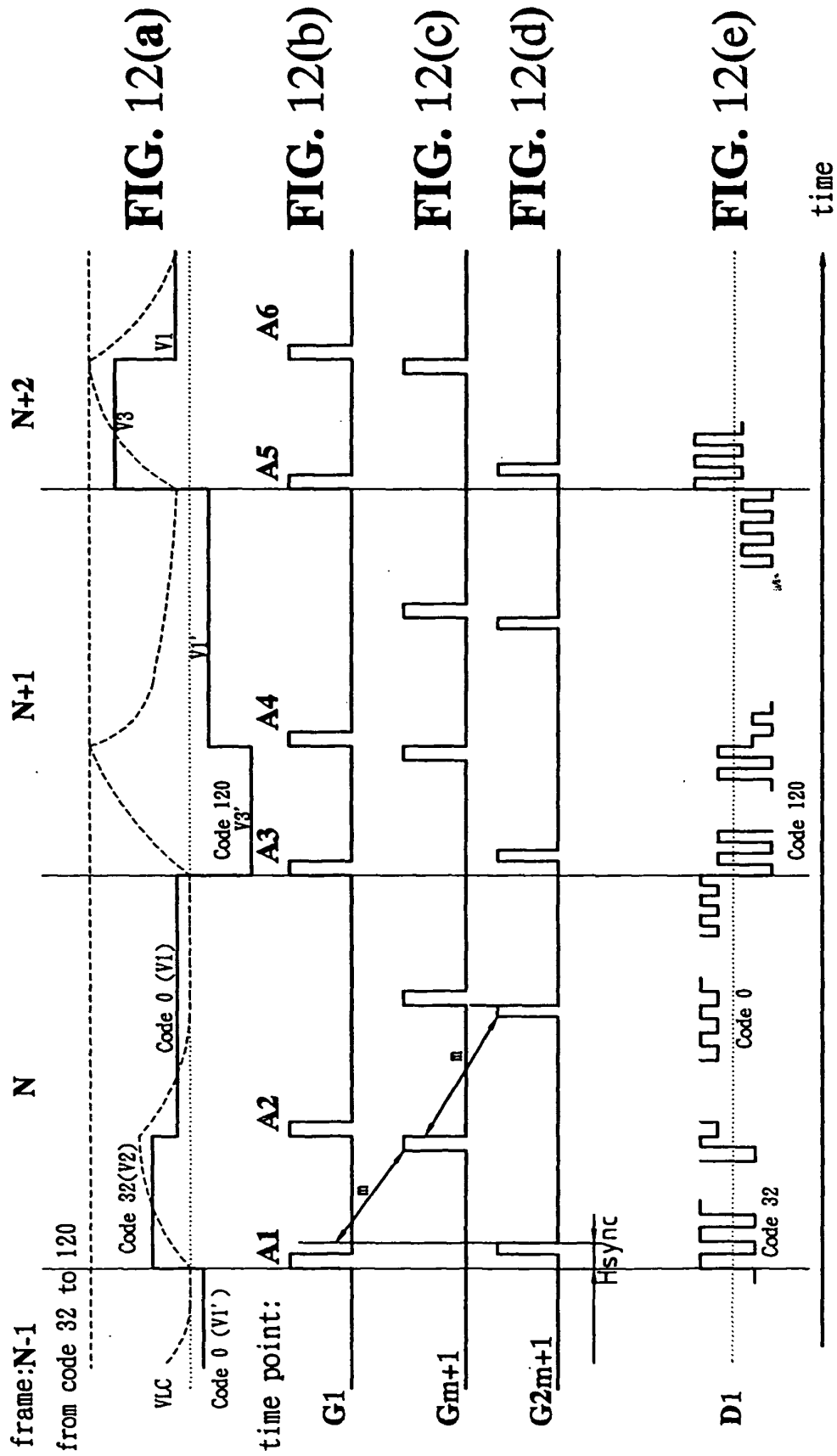
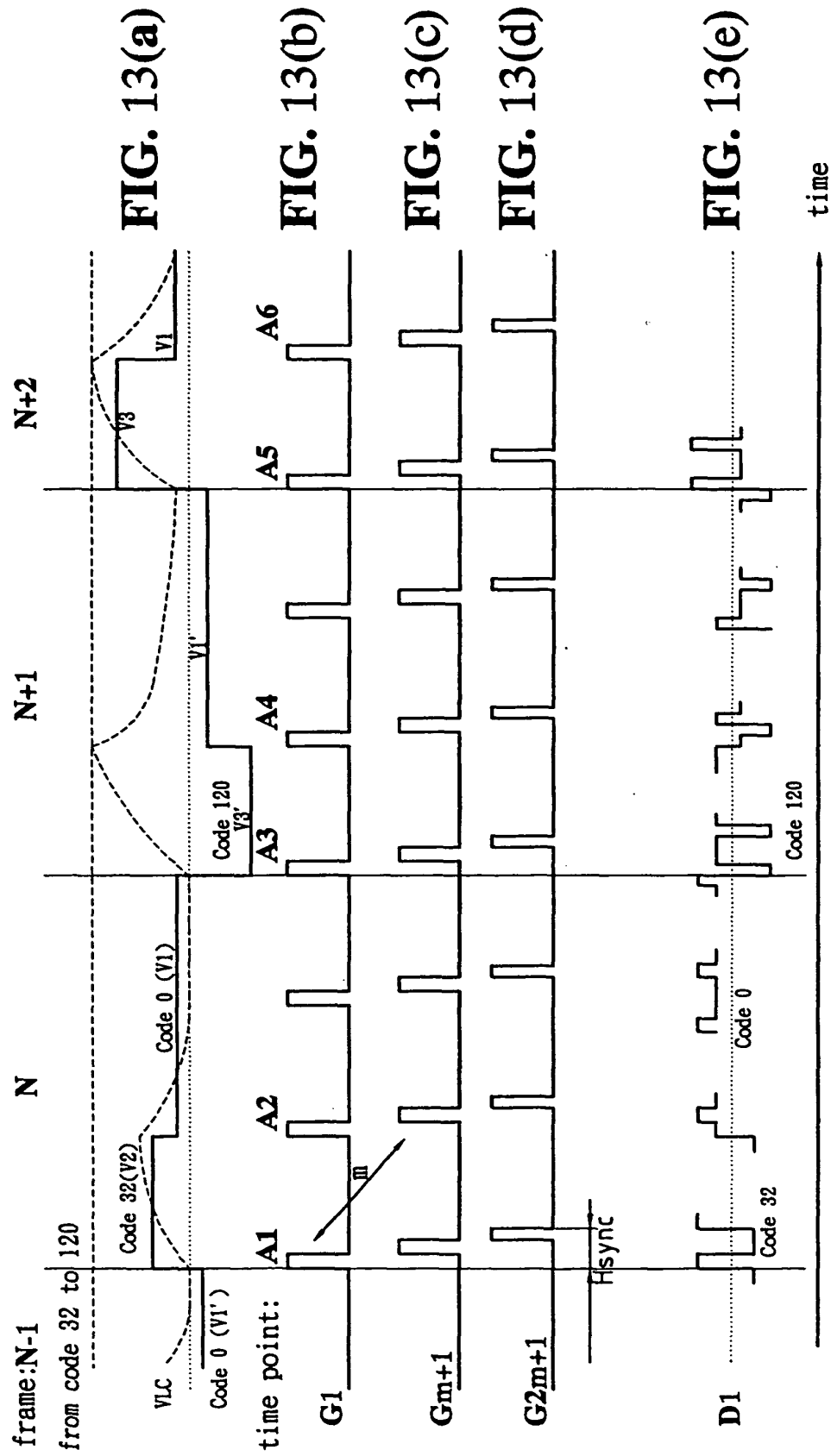


FIG. 11(a)

FIG. 11(b)







European Patent
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EUROPEAN SEARCH REPORT

Application Number
EP 04 01 3037

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The Hague		29 October 2004	Amian, D
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EPO FORM 1503 03.82 (P04C01)

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The members are as contained in the European Patent Office EDP file on
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29-10-2004

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