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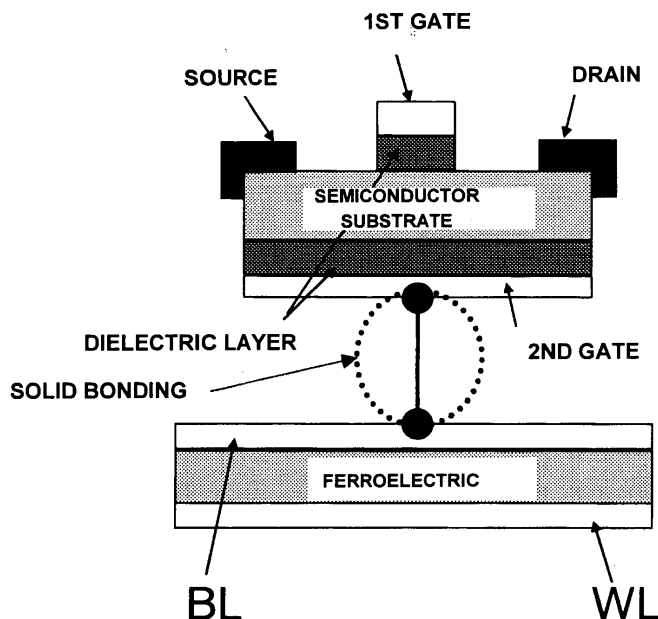
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(54) **Memory device and its manufacturing method**

(57) Disclosed is a memory device comprising: a semiconductor layer; a source formed in the semiconductor layer; a drain formed in the semiconductor layer, the drain being separated from the source; a gate dielectric layer formed on the semiconductor layer, the gate

dielectric layer being formed between the source and the drain; a first gate electrode formed on the gate dielectric layer; a dielectric layer formed below the semiconductor layer; a second gate electrode formed below the dielectric layer; and a ferroelectric capacitor electrically connected to the second gate electrode.

FIG. 6





European Patent
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EUROPEAN SEARCH REPORT

Application Number
EP 05 01 1305

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Place of search The Hague		Date of completion of the search 29 November 2006	Examiner Heising, Stephan
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**ANNEX TO THE EUROPEAN SEARCH REPORT
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