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(54) Active-matrix display device with reduced number of electrodes

(57) An active-matrix display device in which a plurality of pixel circuits (P11-Pnm) are arranged in a matrix and positioned at intersections of data lines (DL1-DLm) and scan lines (SL1-SLn) extending in respective directions perpendicular to each other, and one of the pixel circuits is selected by one of the scan lines to store data provided by one of the data lines, characterized in that two electrodes for providing a power-supply potential and a ground potential, respectively, are connected to a given one (Pk1) of the pixel circuits, and one of the two electrodes is one (SLk) of the scan lines.

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Description

BACKGROUND OF THE INVENTION

1. Field of the Invention

[0001] The present invention generally relates to display devices, and particularly relates to an active matrix display device.

2. Description of the Related Art

[0002] As flat panel displays, liquid crystal displays (LCDs) are widely used in many electrical devices. Now, LED (light emitting diode) displays are considered to be the technology that replaces the LCD technology as a next generation of the flat panel display. LED displays are brighter and thinner, and offer faster response time, lighter weight, and more power efficiency. There are two types of LED displays, i.e., an organic LED display (OLED) and an inorganic LED display.

[0003] The inorganic LED display uses an inorganic metal such as gallium arsenide, gallium nitride, etc., as a light emitting material, whereas the OLED display is based on an organic (i.e., carbon-based) material. Recently, the OLED has been attracting more attention despite the drawback of the lack of durability because it appears to promise vibrancy in color, lighter weight, flexible panels, cost advantage, etc.

[0004] An OLED is comprised of an organic light emitting material sandwiched between a metallic electrode and a transparent electrode. When a voltage is applied between the electrodes, positive holes and electrons are injected from the electrodes, and are recombined in the organic material to create electro luminescent light.

[0005] Like other flat panel displays such as LCDs, the OLED may be implemented as a passive matrix or an active matrix. In both a passive matrix and an active matrix, picture elements (pixels) are arranged in a matrix of columns and rows, at each intersection of which is provided an organic light emitting diode. In a passive matrix, an electrical signal is applied to a particular column while rows are scanned line by line, thereby illuminating a particular pixel at the intersection of the selected column and the selected row.

[0006] In an active matrix, each pixel is provided with a TFT (thin film transistor), which works as a switch and stores information as to an on/off state of each pixel (or how bright each pixel should shine). The information is conveyed through column lines while rows are scanned line by line, resulting in each pixel storing the information in the TFT. The OLED of each pixel shines all the time while a driving voltage is applied, thereby eliminating a need for an instantaneous, large electric current flow ing through an OLED as opposed to the necessity of such current in the passive matrix. This contributes to the increased durability of OLED materials.

[0007] In an active matrix, each pixel needs to have four electrodes, i.e., two power-supply electrodes (i.e., for providing a power-supply potential and a ground potential) that sandwich an organic light emitting material, a scan electrode for scanning each row, and a data electrode serving as a column line to provide data to be stored in each pixel. These electrodes extend in the row direction or the column direction throughout the active-matrix OLED panel.

[0008] In order to ensure proper transparency, these electrodes may need to be implemented by use of transparent electrodes such as ITO (Indium Tin Oxide). Such transparent electrodes have a drawback, however, in that conductivity is not as high as conventional metal electrodes. These transparent electrodes thus need to be wider and thicker, which may undermine the optical characteristics of OLED displays.

[0009] If the number of electrodes required for each pixel circuit is reduced, the transparent electrodes can be widened without compromising the optical characteristics of the display. With the reduced number of electrodes, also, metal electrodes made of Al, Cu, Ag, or the like may become usable without obstructing emitted light.

[0010] Accordingly, there is a need for an active-matrix display device with a reduced number of electrodes.

SUMMARY OF THE INVENTION

[0011] It is a general object of the present invention to provide an active-matrix display device that substantially obviates one or more problems caused by the limitations and disadvantages of the related art.

[0012] Features and advantages of the present invention will be presented in the description which follows, and in part will become apparent from the description and the accompanying drawings, or may be learned by practice of the invention according to the teachings provided in the description. Objects as well as other features and advantages of the present invention will be realized and attained by an active-matrix display device particularly pointed out in the specification in such full, clear, concise, and exact terms as to enable a person having ordinary skill in the art to practice the invention.

[0013] To achieve these and other advantages in accordance with the purpose of the invention, the invention provides an active-matrix display device in which a plurality of pixel circuits (P11-Pnm) are arranged in a matrix and positioned at intersections of data lines (DL1-DLm) and scan lines (SL1-SLn) extending in respective directions perpendicular to each other, and at least one (Pkl) of said pixel circuits is selected by one (SLk+1) of the scan lines to store data provided by one of the data lines, and is powered by two lines that provide a power-supply potential and a ground potential, respectively, characterized in that one of said two lines is another one (SLk) of the scan lines.

[0014] Preferably, any one (Pkl) of the pixel circuits may be selected by one (SLk+1) of the scan lines to

store data provided by one of the data lines, and is powered by two lines that provide a power-supply potential and a ground potential, respectively, one of said two lines being another one (SLk) of the scan lines.

[0015] In both cases above, the another one (SLk) of the scan lines that is used to provide either a power-supply potentail either a ground potential to said one (PK1) of the pixel circuits is used also to select another one P(k-1)1 of the pixel circuits.

[0016] In this manner, each of the scan lines has dual functions so as to serve both as a power-supply or ground electrode and as a scan electrode. This provision makes it possible to provide each pixel circuit with a power-supply potential, a ground potential, a scan electrode, and a data electrode, with only three types (or three networks) of lines laid out through the active-matrix structure.

BRIEF DESCRIPTION OF THE DRAWINGS

[0017] Other objects and further features of the present invention will be apparent from the following detailed description when read in conjunction with the accompanying drawings, in which:

Fig. 1 is a block diagram showing an example of the construction of an active-matrix display device according to the invention;
Fig. 2 is an expanded view of a display panel of Fig. 1;
Fig. 3 is a signal waveform diagram for explaining the operation of a pixel circuit of Fig. 2;
Fig. 4 is a circuit diagram showing an example of the logic construction of the pixel circuit;
Fig. 5 is a circuit diagram showing another example of the pixel circuit according to the invention;
Fig. 6 is a signal waveform diagram for explaining the brightness control of light emission in the pixel circuit of Fig. 5;
Fig. 7 is a signal waveform diagram showing a variation of signals on scan-power lines;
Fig. 8 is a circuit diagram showing an example of the construction of a pixel circuit that is specifically designed for the scan-power line signals of Fig. 7;
Fig. 9 is a signal waveform diagram showing another variation of signals on the scan-power lines;
Fig. 10 is a circuit diagram showing an example of the construction of a pixel circuit that is specifically designed for the scan-power line signals of Fig. 9;
Fig. 11 is a circuit diagram showing another example of the construction of a pixel circuit that is specifically designed for the scan-power line signals of Fig. 9;
Fig. 12 is a signal waveform diagram showing a case in which an end of each scan-pulse period is aligned with a start of a next scan-pulse period but data pulses on a given data line are shorter than corresponding scan-pulse periods;
Fig. 13 is a signal waveform diagram showing a variation of the signal of a scan-power line and the signal of a data line;
Fig. 14 is a circuit diagram showing an example of the construction of a pixel circuit that is used with the signal arrangement of Fig. 13;
Fig. 15 is an illustrative drawing showing a variation of the pixel circuit according to the invention;
Fig. 16 is a signal waveform diagram showing the operation of the pixel circuit of Fig. 15;
Fig. 17 is a circuit diagram showing an example of an actual implementation of the circuit of Fig. 15;
Fig. 18 is an illustrative drawing showing the construction of a pixel circuit and relevant electrodes according to a variation of the invention;
Fig. 19 is a signal waveform diagram for explaining the operation of the pixel circuit of Fig. 18; and
Fig. 20 is a circuit diagram showing an example of the pixel circuit according to the variation of the invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0018] In the following, embodiments of the present invention will be described with reference to the accompanying drawings.

[0019] Fig. 1 is a block diagram showing an example of the construction of an active-matrix display device according to the invention. An active-matrix display device 10 of Fig. 1 includes an image data extractor 11, a synchronizing signal converter 12, a synchronizing signal generator 13, a pixel circuit driving power unit 14, an image data memory 15, a data driver 16, a scan driver 17, a display panel 18, and switches SW1 and SW2. The display panel 18 includes pixel circuits P11 through Pnm, scan-power lines SL1 through SLn, and data lines DL1 through DLm. Here, "n" and "m" are integers, and represent the total number of scan lines (i.e., the number of rows) and the total number of data lines (i.e., the number of columns), respectively. For the sake of convenience of illustration, only P11, P12, and P21 are shown for the pixel circuits, only SL1 and SL2 for the scan-power lines, and only DL1 and DL2 for the data lines.

[0020] The image data extractor 11 and the synchronizing signal converter 12 receive image signals. The image data extractor 11 extracts image data from the received image signals. The synchronizing signal converter 12 extracts synchronizing signals such as a vertical synchronizing signal and a horizontal synchronizing signal from the received image signals.

[0021] If the switch SW1 couples the image data extractor 11 to the data driver 16, the image data extracted by the image data extractor 11 is supplied to the data driver 16. In this case, the switch SW2 couples the synchronizing signals generated by the synchronizing signal converter 12 to the data driver 16 and to the scan

driver 17. The data driver 16 operates in synchronization with the supplied synchronizing signals to provide pulses to the data lines DL1 through DLm in accordance with the image data supplied from the image data extractor 11. Concurrently with the operation of the data driver 16, the scan driver 17 operates in synchronization with the supplied synchronizing signals to scan and drive the scan-power lines SL1 through SLn. The drive power is supplied from the pixel circuit driving power unit 14.

[0022] The image data extracted by the image data extractor 11 is also supplied to the image data memory 15 for storage therein. The image data memory 15 may store a single image or a plurality of images. When the switch SW1 is switched to couple the image data memory 15 to the data driver 16, the switch SW2 is set such as to couple the synchronizing signal generator 13 to the image data memory 15, the data driver 16, and the scan driver 17. In this case, the image data stored in the image data memory 15 is read in synchronization with the synchronizing signals generated by the synchronizing signal generator 13 for provision to the data driver 16. The data driver 16 and the scan driver 17 operate based on the synchronizing signals generated by the synchronizing signal generator 13. This makes it possible to present an image or images stored in the image data memory 15 on the screen of the display panel 18. With this provision, an image shown on the screen may be paused, or a video segment may be repeated as a replay function.

[0023] Fig. 2 is an expanded view of the display panel 18. Fig. 2 illustrates a portion of the display panel 18 in which the pixel circuits Pk1, Pk(1+1), and P(k+1)1 are shown. Each pixel circuit includes a pixel control circuit 20 and an OLED (organic light emitting diode) 21. It should be noted that an active-matrix OLED display is shown as a non-limiting example in Fig. 2, and that the present invention is equally applicable to an inorganic LED display or even to a non-emission type display as long as an active matrix configuration is employed.

[0024] In the present invention shown in Fig. 2, only three types of lines, i.e., the scan-power lines, the data lines, and the ground line (illustrated as a ground node) are provided in the display panel 18. Each pixel circuit, however, is connected to four lines, i.e., a corresponding scan-power line, a next scan-power line, a corresponding data line, and a ground line.

[0025] In any conventional active-matrix structure, each pixel circuit still has four electrodes, i.e., two power-supply electrodes for providing a power-supply potential and a ground potential, a scan electrode, and a data electrode. But four types of lines are provided (instead of three in the invention) in the display panel, i.e., the scan-power lines, the data lines to provide data to be stored in each pixel, the power-supply lines and the ground line.

[0026] In the active-matrix structure of the invention as shown in Fig. 2, each pixel circuit is connected to the different lines of the panel using four electrodes as in the prior art, but only three types of lines (instead of four in the prior art) that extend through the active-matrix panel. This is made possible by connecting each pixel circuit to a corresponding scan-power line and also to a next scan-power line. That is, the pixel circuit Pkl, for example, is connected to the corresponding scan-power line SLk and also connected to the next scan-power line SLk+1. The scan-power line SLk serves as a power-supply line for providing a power-supply potential to this circuit Pkl, whereas the next scan-power line SLk+1 serves as a scan line for scanning the corresponding row to which this circuit Pkl belongs. Further, this scan-power line SLk+1 serving as a scan line for the pixel circuit Pkl serves as a power-supply line for the pixel circuit P(k+1)1 provided on the next row. This pixel circuit P(k+1)1 uses the scan-power line SLk+2 as a scan line.

[0027] In this manner, each of the scan-power lines has dual functions so as to serve both as a power-supply electrode and as a scan electrode. This provision makes it possible to provide each pixel circuit with a power-supply potential, a ground potential, a scan signal, and a data signal, with only three types of lines laid out through the active-matrix structure.

[0028] Fig. 3 is a signal waveform diagram for explaining the operation of the pixel circuit of Fig. 2. As shown in Fig. 3, a signal of each scan-power line is comprised of a scan-pulse period and a power period. In this example, the scan-pulse period corresponds to a low signal level, and the power period corresponds to a high signal level. The scan-pulse periods appear one after another in successive scan-power lines for the purpose of scanning successive rows.

[0029] The pixel circuit Pkl is driven during the power period of the scan-power line SLk. While the pixel circuit Pkl is driven, the next scan-power line SLk+1 enters into a scan-pulse period. In response to this scan-pulse period of the scan-power line SLk+1, the pixel circuit Pkl reads data on the data line DL1 for storage therein. In the example of Fig. 3, the data line DL1 has a data pulse that is LOW at the timing corresponding to the scan-pulse period of the scan-power line SLk+1. As a result, the pixel control circuit 20 outputs a HIGH-level signal for a duration corresponding to the power period of the scan-power line SLk, resulting in the OLED 21 emitting light during this time period.

[0030] Fig. 4 is a circuit diagram showing an example of the logic construction of the pixel circuit. Fig. 4 illustrates a circuit that is implemented by use of logic gates. While such a circuit provides a simple logic that is easy to understand, the circuit size may be prohibitively large for practical use.

[0031] The pixel circuit of Fig. 4 includes an AND gate 31, NOR gates 32 through 34, an NMOS transistor 35, and the OLED 21. The NOR gates 33 and 34 have their outputs coupled to each other's input, thereby forming a latch. One input of the AND gate 31 is a negative logic input, and is connected to the scan -power line SLk+1.

As the scan-power line SLk+1 changes to LOW during the scan-pulse period, data on the data line DL1 is input into the latch. If the data is LOW as shown in Fig. 3, the latch is set, so that the gate node of the NMOS transistor 35 becomes HIGH, resulting in an electric current running through the OLED 21. The OLED 21 thus emits light during the power period of the scan-power line SLk as shown in Fig. 3. If the data on the data line DL1 is HIGH, on the other hand, the latch is reset, so that the gate node of the NMOS transistor 35 becomes LOW, resulting in no electric current running through the OLED 21. The OLED 21 thus does not produce light during the power period of the scan-power line SLk.

[0032] As described above, while the circuit of Fig. 4 provides a simple logic that is easy to understand, the circuit size may be prohibitively large for practical use. Fig. 5 is a circuit diagram showing another example of a pixel circuit according to the invention. The circuit construction of Fig. 5 is simple and suitable for actual implementation.

[0033] The pixel circuit of Fig. 5 includes NMOS transistors 41 through 43, a capacitor 44, a resistor 45, and the OLED 21. The circuit construction of Fig. 5 achieves the same logic as that of Fig. 4, except that the data line DL1 is driven according to a positive logic in Fig. 5.

[0034] Signals on the scan-power lines are the same as those shown in Fig. 3. The HIGH-level period of the scan-power line SLk defines a power period during which the pixel circuit of Fig. 5 is driven. As the scan-power line SLk+1 changes to LOW during the scan-pulse period, the NMOS transistor 43 becomes nonconductive, thereby a positive voltage being applied to the gate of the NMOS transistor 41. The NMOS transistor 41 becomes conductive to pass data on the data line DL1 to the capacitor 44. The capacitor 44 serves as an information storage, and is charged according to the voltage level of the data line DL1. If the data is HIGH, the gate node of the NMOS transistor 42 becomes HIGH, resulting in an electric current running through the OLED 21. The OLED 21 thus emits light during the power period of the scan-power line SLk. If the data on the data line DL1 is LOW, on the other hand, the gate node of the NMOS transistor 42 becomes LOW, resulting in no electric current running through the OLED 21. The OLED 21 thus does not produce light during the power period of the scan-power line SLk.

[0035] In this manner, the simple circuit construction shown in Fig. 5 achieves the same logic as that of Fig. 4, except for the difference between a positive logic and a negative logic in respect of data values (the use of a negative logic may require a more complex circuit than that shown in Fig.5). The circuit of Fig. 5 is substantially simple, and is suitable as an actual circuit construction for practical use.

[0036] Further, in the circuit construction shown in Fig. 5, data stored in the capacitor 44 is not limited to binary values, but may have a data value that is continuous between "0" (LOW) and "1" (HIGH). Fig. 6 is a signal waveform diagram for explaining the brightness control of light emission in the pixel circuit of Fig. 5.

[0037] The HIGH-level period of the scan-power line SLk is a power period during which the pixel circuit of Fig. 5 is driven. As the scan-power line SLk+1 becomes LOW a first time, data D1 on the data line DL1 is read and stored in the capacitor 44, resulting in the OLED 21 shining with brightness responsive to D1. This level of brightness continues for the duration of the power period, and the OLED 21 is turned off at the end of the power period. As the scan-power line SLk+1 becomes LOW a second time with the start of the next power period, data D2 on the data line DL1 is read and stored in the capacitor 44, resulting in the OLED 21 shining with brightness responsive to D2. This level of brightness continues for the duration of the power period.

[0038] In this manner, the circuit of Fig. 5 can control the brightness of the OLED 21 according to data on the data line DL1. Alternatively, the brightness of the OLED 21 may be limited to binary levels (i.e., on/off), and gray-scale representation is achieved by use of a sub-field method which is typically used in plasma displays. In the sub-field method, one second is divided into a plurality of fields (e.g., 60 fields per second), and each field is further divided into a plurality of sub-fields (typically 8 sub-fields). These sub-fields are configured to have respective durations, ratios of which are typically 1:2:4:8:16:32:64:128 in the case of 8 sub-fields. An on/off state of a given pixel is controlled separately for each sub-field, so that this pixel may shine during one or more sub-fields for which it is directed to shine. With this provision, a total time length of light emission of this pixel in one field period can be controlled, and can be set to 255 different time lengths in the case of 8 sub-fields. Such different time lengths are perceived as different brightness levels by human vision, thereby achieving gray-scale representation by using only an on/off binary state of the OLED 21.

[0039] Fig. 7 is a signal waveform diagram showing a variation of signals on the scan-power lines. In Fig. 7, signals on the scan-power lines SLk through SLk+2 become LOW indicative of a scan-pulse period one after another in successive scan -power lines, with a gap G between adjacent scan-pulse periods.

[0040] The circuits of Fig. 4 and Fig. 5 properly work even in the case of scan-power line signals as shown in Fig. 7. If the shining of the OLED 21 is preferably suppressed during the gap period G, a circuit construction needs to be modified. Fig. 8 is a circuit diagram showing an example of the construction of a pixel circuit that is specifically designed for the scan-power line signals of Fig. 7. In Fig. 8, the same elements as those of Fig. 4 are referred to by the same numerals, and a description thereof will be omitted.

[0041] The pixel circuit of Fig. 8 differs from the pixel circuit of Fig. 4 in that a circuit block 50 is additionally provided. The circuit block 50 includes registers 51 and 52, a capacitor 53, and an NMOS transistor 54. As the

scan-power line SLk is changed from LOW to HIGH, an electric current flows through the register 51 to charge the capacitor 53. As electric charge in the capacitor 53 builds up, a potential rises at the gate node of the NMOS transistor 54. Sometime after the change from LOW to HIGH of the scan-power line SLk, the NMOS transistor 54 turns on, thereby changing the output of the circuit block 50 from HIGH to LOW, which allows the latch comprised of the NOR gates 33 and 34 to perform its latch operation.

[0042] With proper selection of resistance and capacitance, the circuit block 50 provides a proper delay that is equivalent to the length of the gap period G.

[0043] Fig. 9 is a signal waveform diagram showing another variation of signals on the scan-power lines. In Fig. 9, signals on the scan-power lines SLk through SLk+2 become LOW indicative of a scan-pulse period one after another in successive scan-power lines, with an overlap "O" between adjacent scan-pulse periods.

[0044] It should be noted that the scan-pulse periods of the scan-power lines should be accompanied by respective data signals on a given data line. Although the scan-pulse periods of adjacent scan-power lines are overlapping in Fig. 9, data signals cannot overlap on a given data line. As shown in Fig. 9. therefore, data pulses on the data line DL1 may only be valid during an early period within the respective scan-pulse periods. Because of this, the circuits of Fig. 4 and Fig. 5 may not properly work in the case of scan-power line signals as shown in Fig. 9.

[0045] Fig. 10 is a circuit diagram showing an example of the construction of a pixel circuit that is specifically designed for the scan -power line signals of Fig. 9. In Fig. 10, the same elements as those of Fig. 4 are referred to by the same numerals, and a description thereof will be omitted.

[0046] The pixel circuit of Fig. 10 differs from the pixel circuit of Fig. 4 in that a circuit block 60 is additionally provided. The circuit block 60 is a one-shot circuit, and includes a NAND gate 61, a capacitor 62, a resistor 63, and an inverter 64. In response to a change of the data line DL from HIGH to LOW, a potential at node A (i.e., input into the inverter 64) changes to HIGH, thereby supplying a LOW output signal to the AND gate 31 and the NOR gate 32. An electric current then flows through the register 63 to charge the capacitor 62. As electric charge in the capacitor 62 builds up, a potential drops at the node A. Sometime after the change from HIGH to LOW of the data line DL, the output of the inverter 64 changes from LOW to HIGH. With this provision, the circuit block 60 outputs a shortened data pulse, thereby ensuring a proper operation of the pixel circuit even when the scan-power signals have overlaps as shown in Fig. 9.

[0047] Fig. 11 is a circuit diagram showing another example of the construction of a pixel circuit that is specifically designed for the scan-power line signals of Fig. 9. In Fig. 11, the same elements as those of Fig. 5 are referred to by the same numerals, and a description thereof will be omitted.

[0048] The pixel circuit of Fig. 11 differs from the pixel circuit of Fig. 5 in that a circuit block 60A is additionally provided. The circuit block 60A is a one-shot circuit, and includes inverters 65 and 66, a capacitor 67, and a resistor 68. In response to a change of the scan-power line SLK+1 from HIGH to LOW, a potential at node B (i. e., input into the inverter 66) changes to HIGH, thereby supplying a LOW signal to the gate node of the NMOS transistor 43. An electric current then flows through the register 68 to charge the capacitor 67. As electric charge in the capacitor 67 builds up, a potential drops at the node B. Sometime after the change from HIGH to LOW of the scan-power line SLk+1, the output of the inverter 66 changes from LOW to HIGH. With this provision, the inverter 66 outputs a shortened data pulse, thereby ensuring a proper operation of the pixel circuit even when the scan-power signals have overlaps as shown in Fig. 9.

[0049] The one-shot circuit used in Fig. 10 and Fig. 11 may also be used even when an end of each scan-pulse period is aligned with a start of a next scan-pulse period. Fig. 12 is a signal waveform diagram showing a case in which an end of each scan-pulse period is aligned with a start of a next scan-pulse period but data pulses on a given data line are shorter than corresponding scan-pulse periods. In such a case, the one-shot circuit as described above may effectively be used to limit the time period during which the pixel circuit reads data on the data line.

[0050] Further, the circuit block used in Fig. 8 and the one-shot circuit used in Fig. 10 and Fig. 11 may be combined as such a need arises. For example, a data pulse (data signal) on a given data line may be shorter than a corresponding scan-pulse period, and successive scan-pulse periods in adjacent scan-power lines may be spaced apart with a gap as shown in Fig. 7. In such a case, the circuit block as used in Fig. 8 may additionally be provided to cope with the spaced-apart scan-pulse periods, and the one-shot circuit used in Fig. 10 and Fig. 11 may also be provided to cope with the shorter data pulse.

[0051] Fig. 13 is a signal waveform diagram showing a variation of the signal of a scan-power line and the signal of a data line. The signal of the scan-power line SLk in this case includes a scan-pulse period defined as a zero-potential period and a power period defined as a negative-potential period. Also, the signal of the data line is a positive logic in which "1" is represented by a higher potential (zero potential) and "0" is represented by a lower potential (negative potential).

[0052] Fig. 14 is a circuit diagram showing an example of the construction of a pixel circuit that is used with the signal arrangement of Fig. 13. The pixel circuit of Fig. 14 includes AND gates 71 and 72, NOR gates 73 and 74, an NMOS transistor 75, and the OLED 21. The NOR gates 73 and 74 have their outputs coupled to each other's input, thereby forming a latch. Logic on which

the operation of this circuit is based is substantially the same as that of Fig.4, and a description thereof will be omitted.

[0053] Fig. 15 is an illustrative drawing showing a variation of the pixel circuit according to the invention. In Fig. 15, a circuit block 80 is inserted into the output of the pixel control circuit 20, such that the output of the circuit block 80 is supplied to the OLED 21. The circuit block 80 includes a switch 81 and a capacitor 82. The switch 81 is closed while power is supplied to the pixel control circuit 20. If the pixel control circuit 20 has data stored therein indicative of the emission of light, thus, an electric current is supplied to the OLED 21 to turn it on. The switch 81 is opened when power is not supplied to the pixel control circuit 20. If the OLED 21 was on before the opening of the switch 81, the OLED 21 continues to be on for a while as an electric current is supplied from the capacitor 82 that is discharging.

[0054] Fig. 16 is a signal waveform diagram showing the operation of the pixel circuit of Fig. 15. As shown in Fig. 16, the OLED 21 continues emitting light even after power is turned off at timing T1. This is because the capacitor 82 illustrated in Fig. 15 supplies power to the OLED 21 while no power is supplied to the pixel control circuit 20 from the scan-power line SLk. With this provision, sudden turning off of the OLED 21 is avoided, and the emission of the OLED 21 slowly diminishes. This may contribute to better appearance of images to human eyes.

[0055] Fig. 17 is a circuit diagram showing an example of an actual implementation of the circuit of Fig. 15. The NOR gates 33 and 34 and the NMOS transistor 35 are the same as those shown in Fig. 4. The switch 81 is implemented by use of an NMOS transistor in this example. When the scan-power line SLk is HIGH to provide power, the NMOS transistor 81 becomes conductive to couple the OLED 21 to the power-supply voltage (assuming that the NMOS transistor 35 is conductive). As the scan-power line SLk is changed to LOW, the NMOS transistor 81 becomes nonconductive, resulting in the capacitor 82 providing power to the OLED 21.

[0056] In the embodiments described above, the scan-power lines are given dual functions, serving both as a scan line and as a power-supply line. Alternatively, a ground line may be given dual functions, serving both as a scan line and a ground line. Such a variation will be described in the following.

[0057] Fig. 18 is an illustrative drawing showing the construction of a pixel circuit and relevant electrodes according to a variation of the invention. Each pixel circuit includes a pixel control circuit 120 and an OLED (organic light emitting diode) 121.

[0058] In the variation of the invention shown in Fig. 18, only three types of lines, i.e., a scan-ground line (two of which are shown as SGk and SGk+1), a data line (one of which is shown as DL1), and a power-supply line (illustrated as a power-supply node V_{DD}) are provided in a display panel. Each pixel circuit, however, is connected to four lines, i.e., the corresponding scan-ground line SGk, the next scan-ground line SGk+1, the corresponding data line DL1, and the power-supply line V_{DD}.

[0059] In any conventional active-matrix structure, each pixel circuit needs to have four electrodes, i.e., two power-supply electrodes for providing a power-supply potential and a ground potential, a scan electrode for scanning each row, and a data electrode serving as a column line to provide data to be stored in each pixel. These four electrodes extend in the row direction or the column direction throughout the active-matrix panel.

[0060] In the active-matrix structure of the invention as shown in Fig. 18, each pixel circuit is connected to four electrodes, but only three types of lines extend through the active-matrix panel. This is made possible by connecting each pixel circuit to a corresponding scan-ground line and also to a next scan-ground line. That is, the pixel circuit of Fig. 18 is connected to the corresponding scan-ground line SGk and also connected to the next scan-ground line SGk+1. The scan-ground line SGk serves as a ground electrode for providing a ground potential, whereas the next scan-ground line SGk+1 serves as a scan electrode for scanning the corresponding row. Further, this scan-ground line SGk+1 serving as a scan electrode for the pixel circuit of Fig. 18 serves as a ground electrode for a pixel circuit provided on the next row. This pixel circuit on the next row uses a next scan-ground line SGk+2 as a scan electrode.

[0061] In this manner, each of the scan-ground lines has dual functions so as to serve both as a ground electrode and as a scan electrode. This provision makes it possible to provide each pixel circuit with a power-supply potential, a ground potential, a scan signal, and a data signal, with only three networks of lines laid out through the active-matrix structure.

[0062] Fig. 19 is a signal waveform diagram for explaining the operation of the pixel circuit of Fig. 18. The pixel circuit of Fig. 18 is driven during the ground-level period of the scan-ground line SGk. While the pixel circuit is driven, the next scan-ground line SGk+1 enters into a scan-pulse period that is defined by a HIGH signal level. In response to this scan-pulse period of the scan-ground line SGk+1, the pixel circuit reads data on the data line DL1 for storage therein. In the example of Fig. 19, the data line DL1 has a data pulse that is HIGH at the timing corresponding to the scan-pulse period of the scan-ground line SGk+1. As a result, the pixel control circuit 120 outputs a HIGH-level signal for a duration corresponding to the ground-level period of the scan-ground line SGk, resulting in the OLED 121 emitting light during this time period.

[0063] Fig. 20 is a circuit diagram showing an example of the pixel circuit according to the variation of the invention. The circuit construction of Fig. 20 is simple and suitable for actual implementation.

[0064] The pixel circuit of Fig. 20 includes NMOS transistors 131 and 132, a capacitor 133, and the OLED 21.

This pixel circuit is driven during a period in which the scan-ground line SGk is set to a ground level. As the scan-ground line SGk+1 changes to HIGH during the scan-pulse period, the NMOS transistor 131 becomes conductive, thereby passing data on the data line DL1 to the capacitor 133. The capacitor 133 serves as an information storage, and is charged according to the voltage level of the data line DL1. If the data is HIGH, the gate node of the NMOS transistor 132 becomes HIGH, resulting in an electric current running through the OLED 21. The OLED 21 thus emits light during the ground-level period of the scan-ground line SGk. If the data on the data line DL1 is LOW, on the other hand, the gate node of the NMOS transistor 132 becomes LOW, resulting in no electric current running through the OLED 21. The OLED 21 thus does not produce light during the ground-level period of the scan-ground line SGk.

[0065] In this manner, the simple circuit construction shown in Fig. 20 achieves the operation required of a pixel circuit, with only three types of lines laid out in the active-matrix configuration.

[0066] Further, the present invention is not limited to these embodiments, but various variations and modifications may be made without departing from the scope of the present invention.

Claims

1. An active-matrix display device in which a plurality of pixel circuits (P11-Pnm) are arranged in a matrix and positioned at intersections of data lines (DL1-DLm) and scan lines (SL1-SLn) extending in respective directions perpendicular to each other, and at least one (Pkl) of said pixel circuits is selected by one (SLk+1) of the scan lines to store data provided by one of the data lines, and is powered by two lines that provide a power-supply potential and a ground potential, respectively, **characterized in that** one of said two lines is another one (SLk) of the scan lines.

2. The active-matrix display device as claimed in claim 1, further **characterized in that** any one (Pkl) of the pixel circuits may be selected by one (SLk+1) of the scan lines to store data provided by one of the data lines, and is powered by two lines that provide a power-supply potential and a ground potential, respectively, one of said two lines being another one (SLk) of the scan lines.

3. The active-matrix display device as claimed in claim 1 or 2, further **characterized in that** said one (SLk) of the two lines is set to a first potential to provide one of the power-supply potential and the ground potential to said given one (Pkl) of the pixel circuits, and is set to a second potential to select another one (P(k-1)1) of the pixel circuits situated adjacent to said given one (Pkl) of the pixel circuits.

4. The active-matrix display device as claimed in claim 3, wherein that said given one of the pixel circuits includes a pixel control circuit (20, 120) and an optical device (21, 121), **characterized in that** said pixel control circuit is connected to a first one (SLk, SGk) of the scan lines, a second one (SLk+1, SGk+1) of the scan lines, and one (DL1) of the data lines, and is driven by the first potential of the first one (SLk, SGk) of the scan lines to store data provided by said one (DL1) of the data lines when the second one (SLk+1, SGk+1) of the scan lines is set to the second potential, said pixel control circuit (20, 120) controlling said optical device (21, 121) in response to the stored data.

5. The active-matrix display device as claimed in claim 4, **characterized in that** said optical device (21, 121) is a light emitting diode.

6. The active-matrix display device as claimed in claim 5, **characterized in that** said optical device (21, 121) is an organic light emitting diode.

7. The active-matrix display device as claimed in claim 4, **characterized in that** said pixel control circuit includes a one-shot circuit (60A) that produces a pulse in response to the second potential of the second one (SLk+1) of the scan lines, said pixel control circuit storing the data provided by said one (DL1) of the data lines in response to the produced pulse.

8. The active-matrix display device as claimed in claim 4, **characterized in that** said pixel control circuit includes a circuit (50) that delays the storing of the data provided by said one (DL1) of the data lines.

9. The active-matrix display device as claimed in claim 4, **characterized in that** a switch (81) and a capacitor (82) are provided between said pixel control circuit (20) and said optical device (21), such that the switch is closed to provide power to the capacitor and to the optical device from the first one (SLk) of the scan lines, and is opened to provide power from the capacitor to the optical device.

10. The active-matrix display device as claimed in claim 4, **characterized in that** the stored data indicates brightness of a corresponding pixel.

11. The active-matrix display device as claimed in claim 3, wherein a scan driver is provided for driving the scan lines, **characterized in that** said scan driver produces a pulse of the second potential in successive ones of the scan lines, such that said pulse on one of the scan lines is immediately followed by said pulse on an adjacent one of the scan lines without

a gap nor an overlap.

12. The active-matrix display device as claimed in claim 3, wherein a scan driver is provided for driving the scan lines, **characterized in that** said scan driver produces a pulse of the second potential in successive ones of the scan lines, such that said pulse on one of the scan lines is followed by said pulse on an adjacent one of the scan lines with either a gap or an overlap.

FIG.1

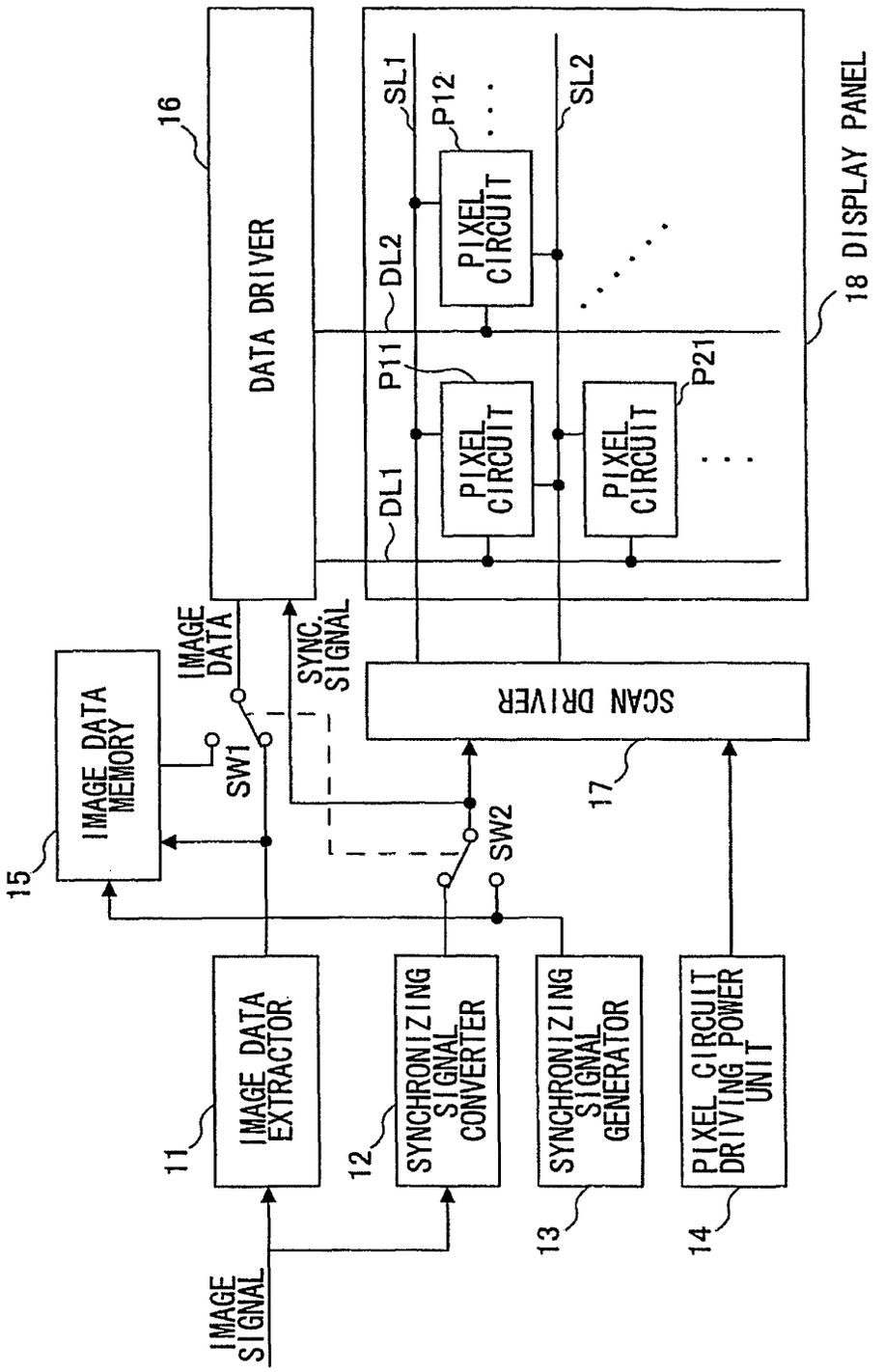

10
IMAGE SIGNAL
11
IMAGE DATA EXTRACTOR
12
SYNCHRONIZING SIGNAL CONVERTER
13
SYNCHRONIZING SIGNAL GENERATOR
14
PIXEL CIRCUIT DRIVING POWER UNIT
15
IMAGE DATA MEMORY
SW1
SW2
IMAGE DATA
SYNC. SIGNAL
16
DATA DRIVER
17
SCAN DRIVER
18 DISPLAY PANEL
DL1
DL2
SL1
SL2
P11
P12
P21
PIXEL CIRCUIT
PIXEL CIRCUIT

FIG.2

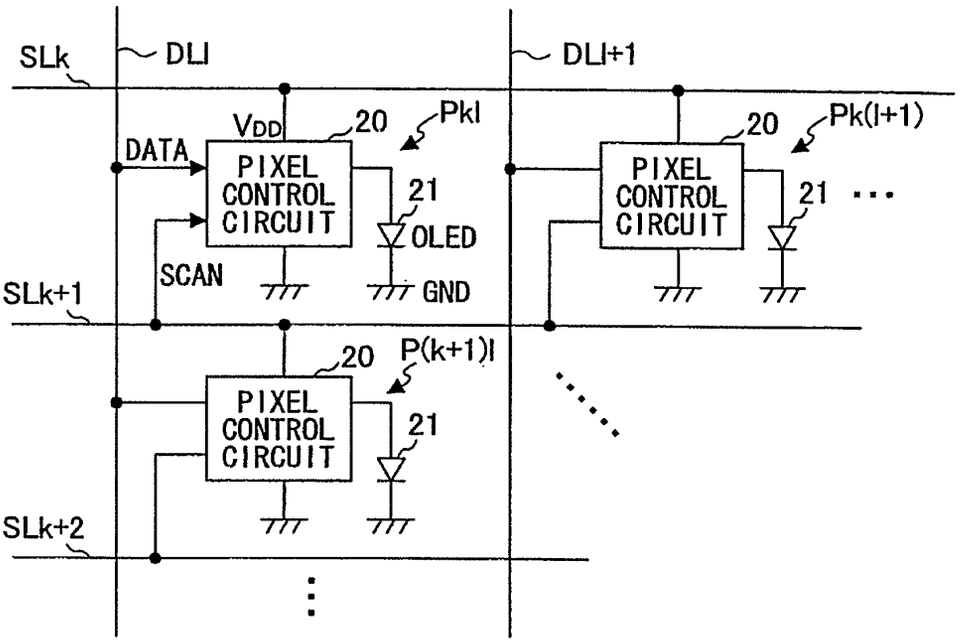

SLk
DLl
DLl+1
VDD
20
Pkl
DATA
PIXEL CONTROL CIRCUIT
21
OLED
SCAN
GND
SLk+1
Pk(l+1)
P(k+1)l
SLk+2

FIG.3

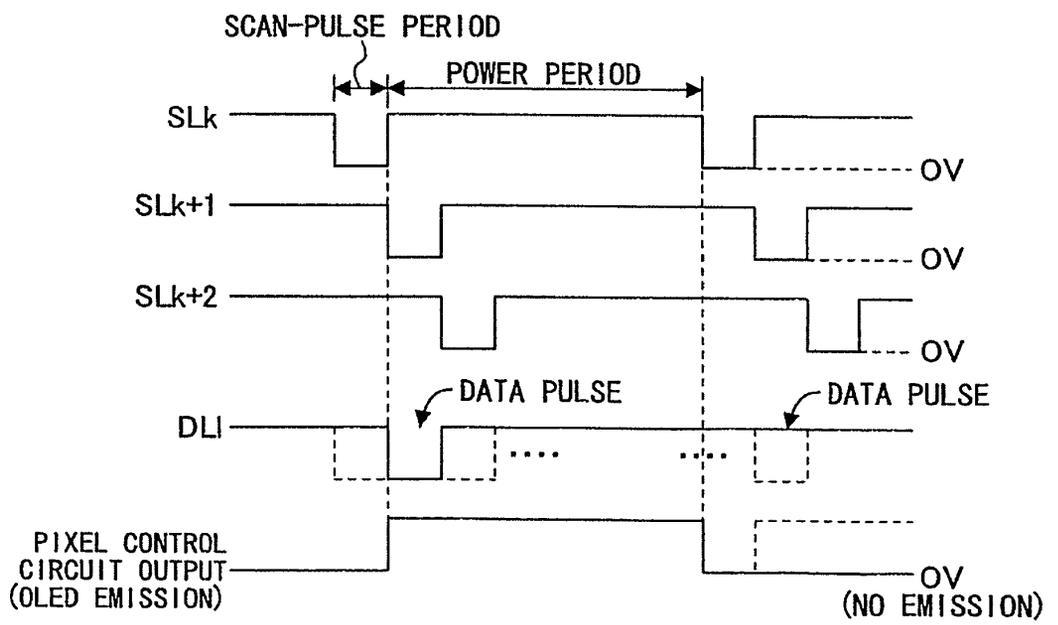

SCAN-PULSE PERIOD
POWER PERIOD
SLk
SLk+1
SLk+2
OV
DATA PULSE
DLl
PIXEL CONTROL CIRCUIT OUTPUT (OLED EMISSION)
(NO EMISSION)

FIG.4

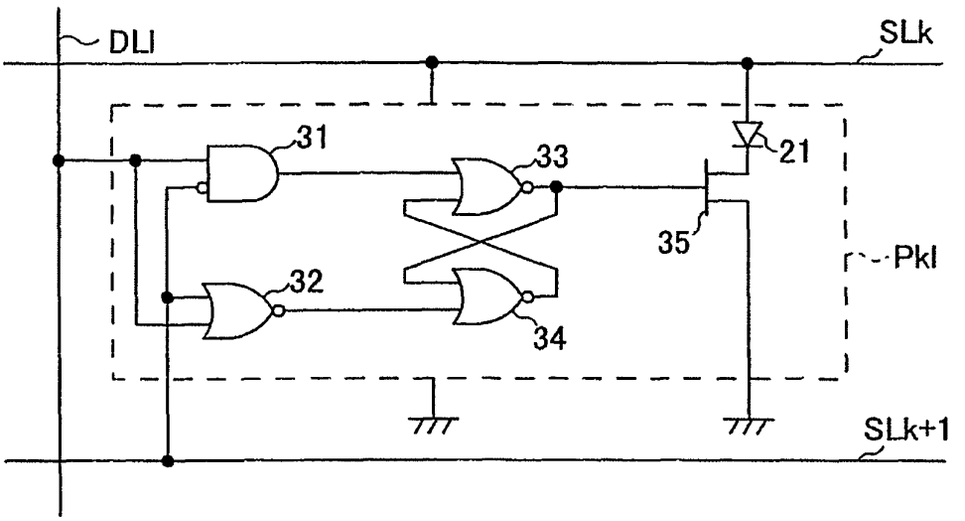


FIG.5

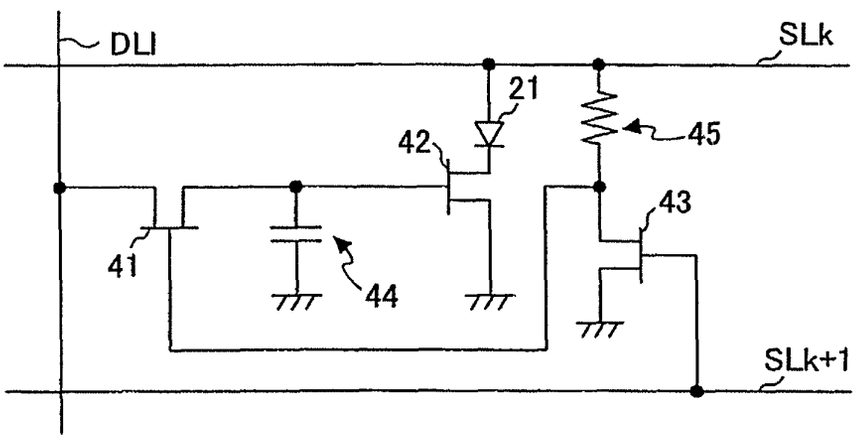


FIG.6

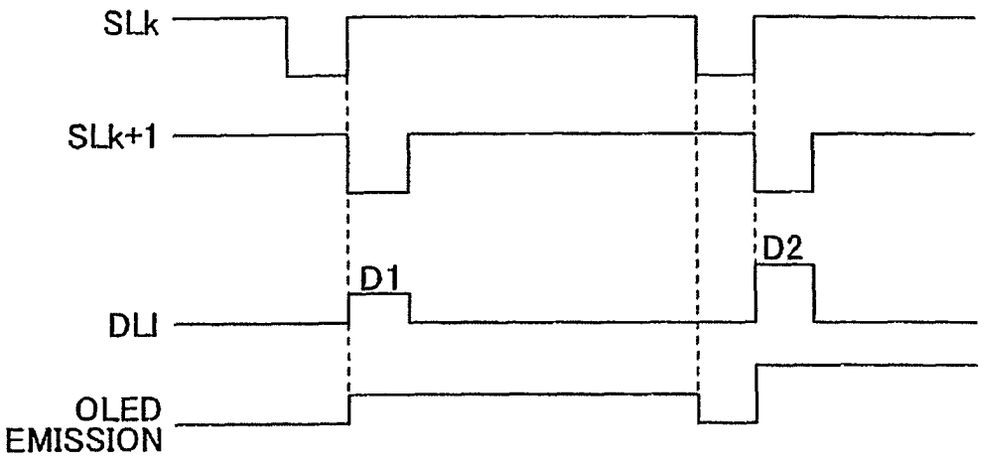


FIG.7

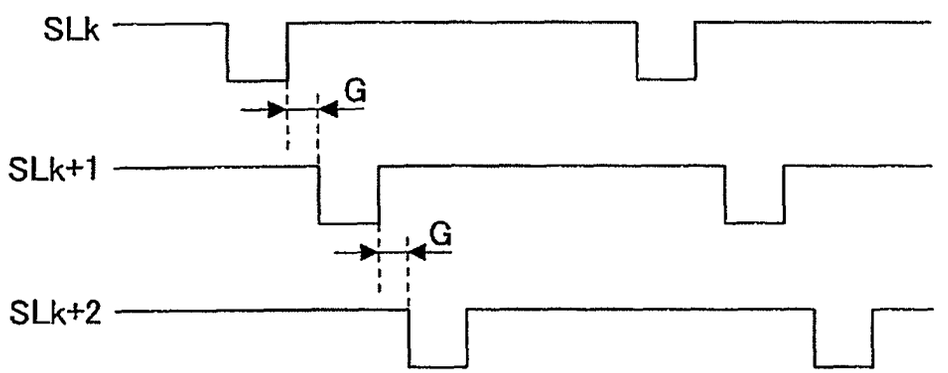


FIG.8

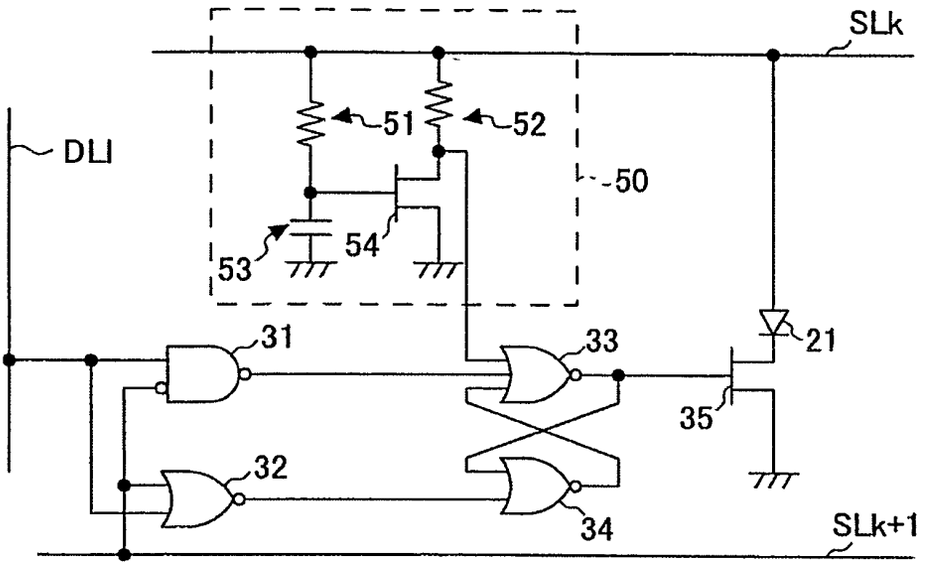


FIG.9

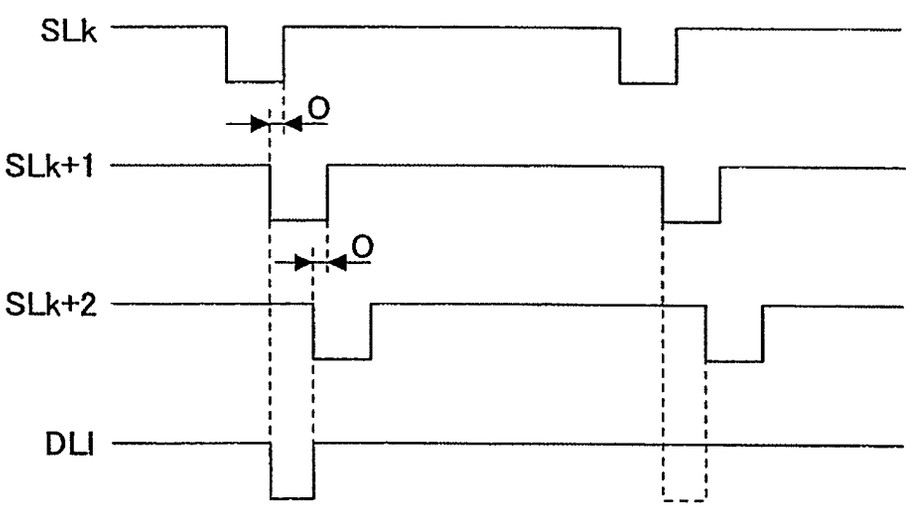


FIG.10

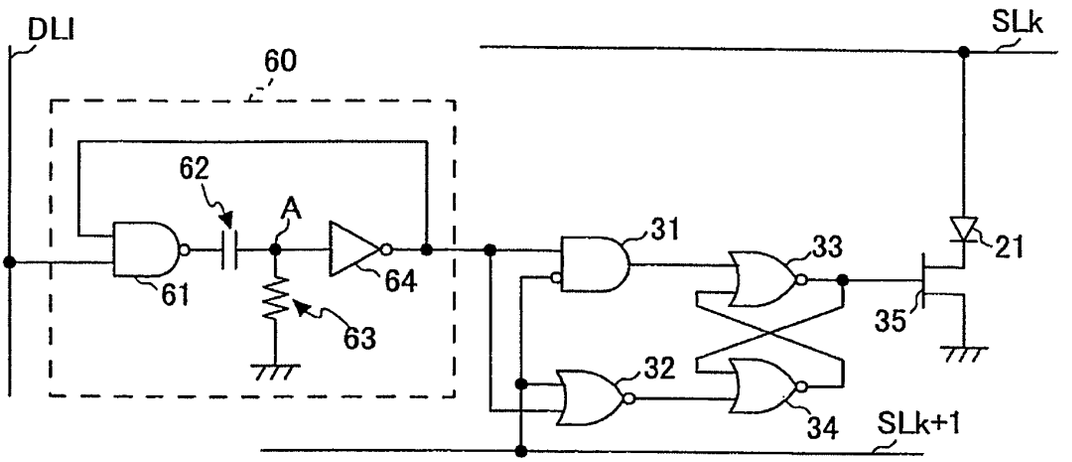

DLI
SLk
60
62
A
61
64
63
31
33
21
35
32
34
SLk+1

FIG.11

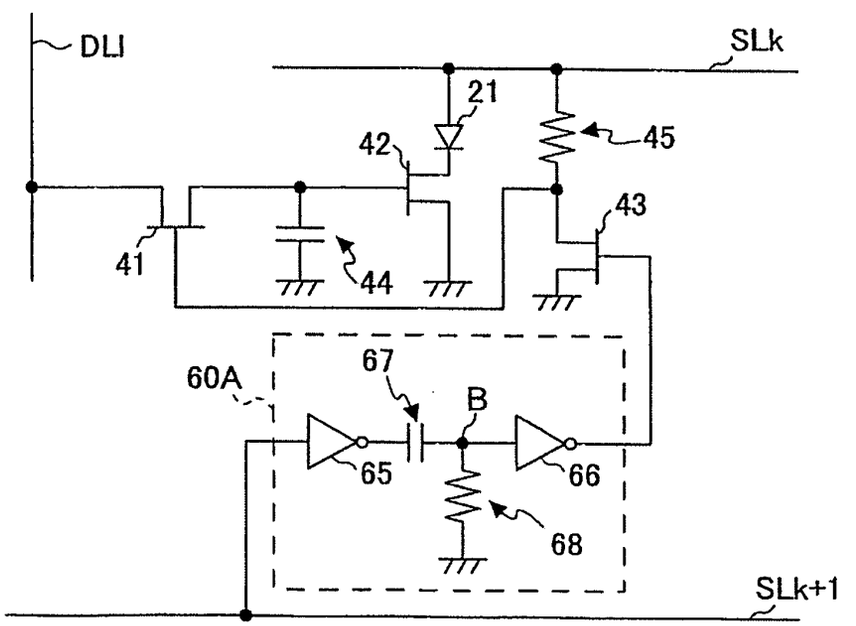

DLI
SLk
21
42
45
43
41
44
60A
67
B
65
66
68
SLk+1

FIG.12

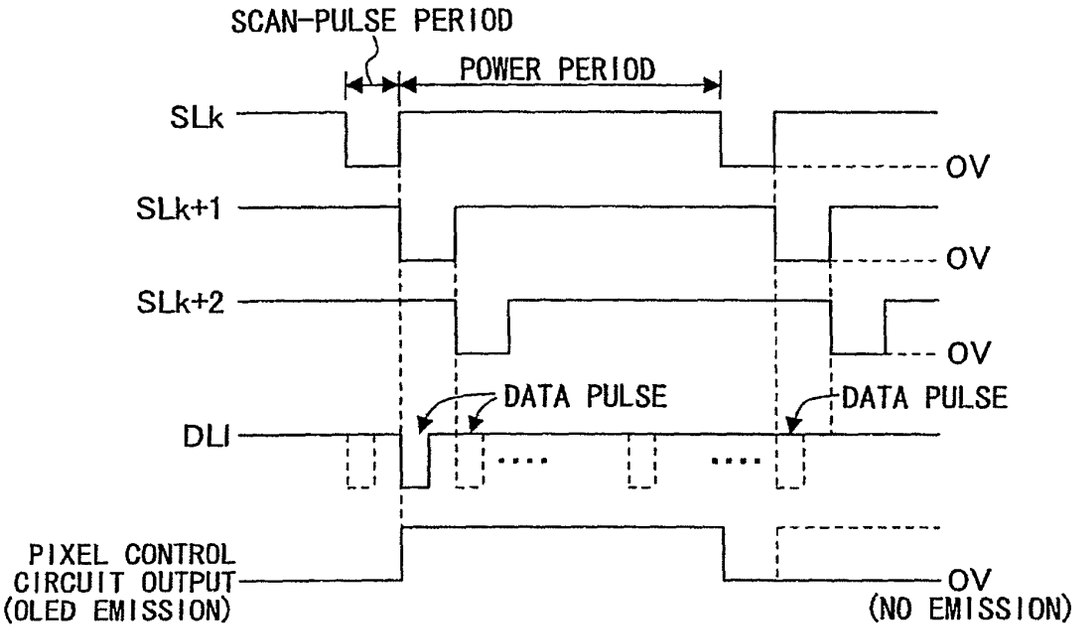

SCAN-PULSE PERIOD
POWER PERIOD
SLk
SLk+1
SLk+2
DLI
OV
OV
OV
DATA PULSE
DATA PULSE
PIXEL CONTROL CIRCUIT OUTPUT (OLED EMISSION)
OV (NO EMISSION)

FIG.13

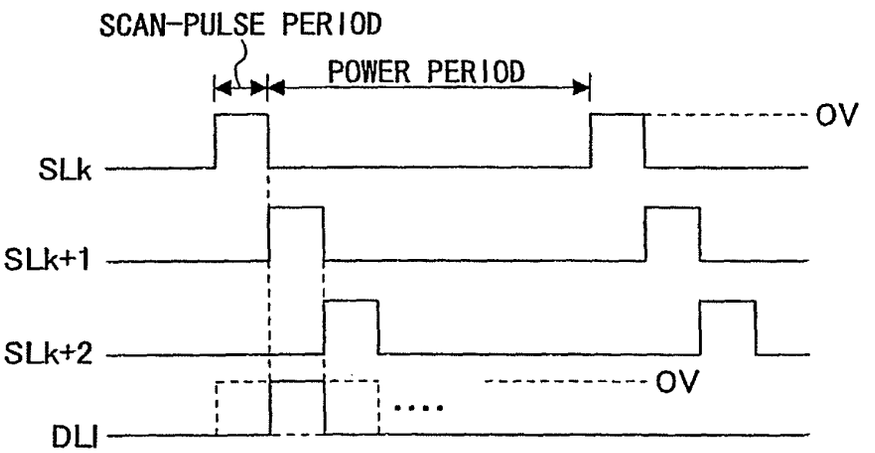

SCAN-PULSE PERIOD
POWER PERIOD
SLk
SLk+1
SLk+2
DLI
OV
OV

FIG.14

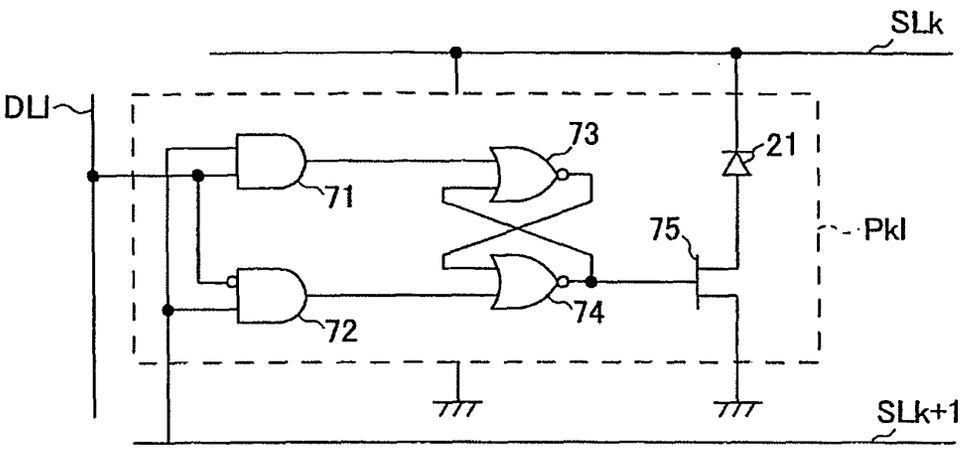

SLk
DLl
73
21
71
75
Pkl
74
72
SLk+1

FIG.15

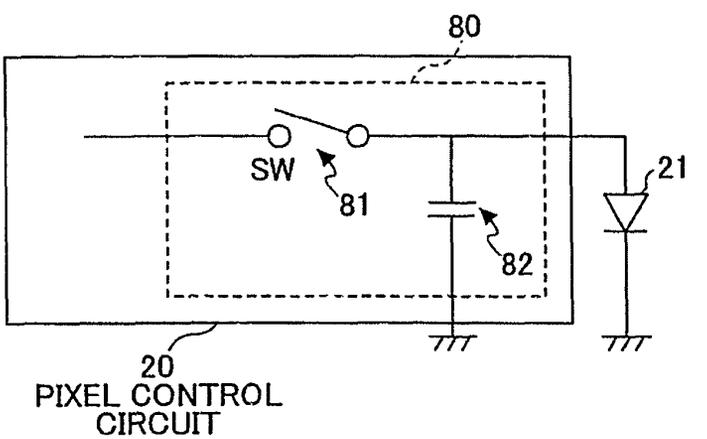

80
SW
81
21
82
20
PIXEL CONTROL
CIRCUIT

FIG.16

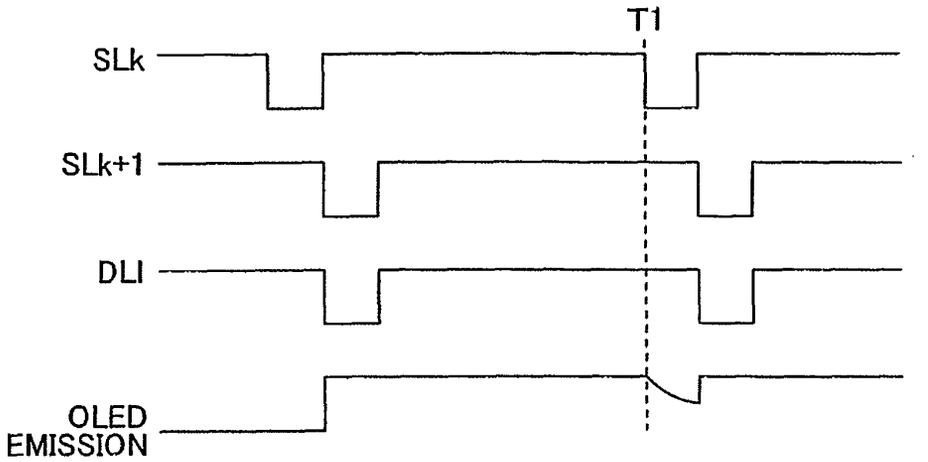


FIG.17

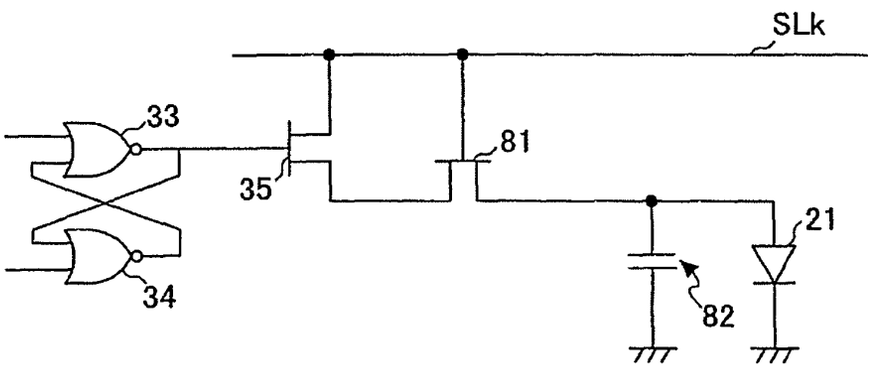


FIG.18

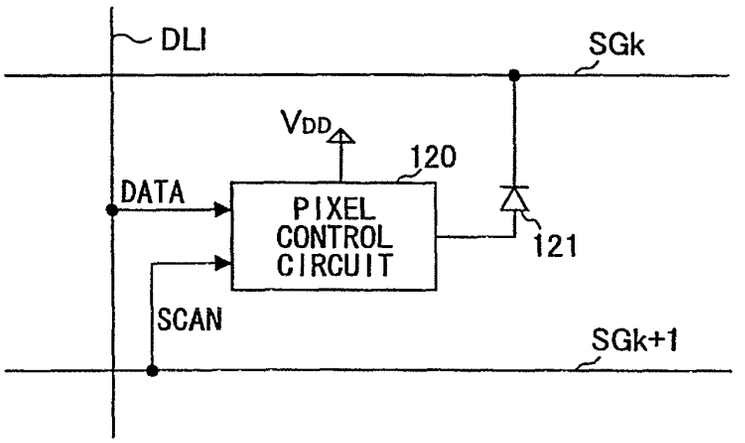

DLI
SGk
VDD
120
DATA
PIXEL
CONTROL
CIRCUIT
121
SCAN
SGk+1

FIG.19

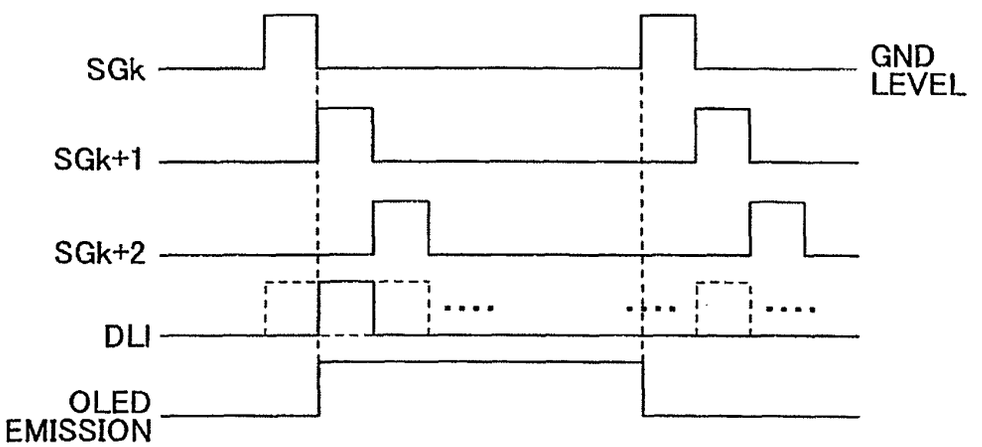
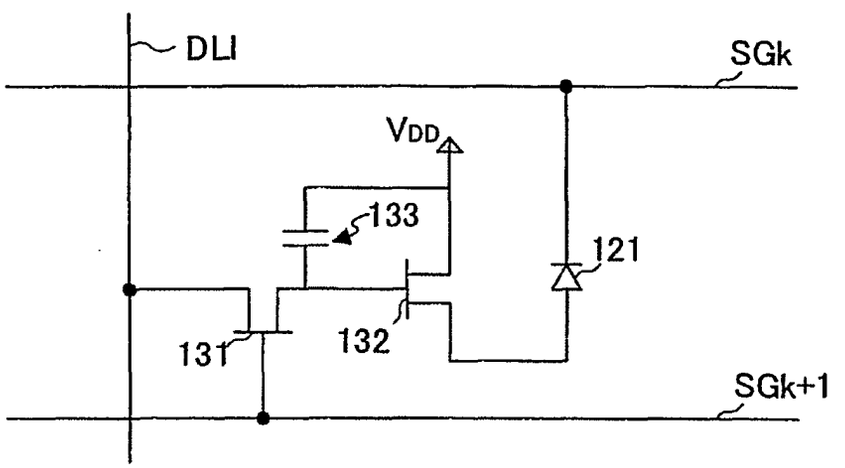

SGk
GND
LEVEL
SGk+1
SGk+2
DLI
OLED
EMISSION

FIG.20



European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 04 30 0319

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
X	EP 0 653 741 A (NIPPON ELECTRIC CO) 17 May 1995 (1995-05-17) * column 7, line 16 - line 52; figure 3 * * column 10, line 25 - line 48 *	1-12	G09G3/32 G09G3/20
X	US 6 380 689 B1 (OKUDA YOSHIYUKI) 30 April 2002 (2002-04-30) * column 9, line 44 - column 11, line 17; figures 12-14 *	1-12	
X	US 6 475 845 B2 (KIMURA HAJIME) 5 November 2002 (2002-11-05) * column 6, line 64 - column 7, line 24; figures 3,4 *	1-12	

TECHNICAL FIELDS SEARCHED (Int.Cl.7)

G09G

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
The Hague	8 December 2004	Amian, D

CATEGORY OF CITED DOCUMENTS

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3

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08-12-2004

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		US 2001026257 A1	04-10-2001

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