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(54) Spark gap apparatus and method for electrostatic discharge protection

Funkenstreckevorrichtung und Verfahren zum elektrostatischen Entladungsschutz

Dispositif éclateur et méthode de protection contre les décharges électrostatiques

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(56) References cited:
EP-A- 0 610 898
EP-A- 1 229 618
AU-B- 532 286
US-A- 5 915 757
US-B1- 6 241 537

- **GILMORE P ET AL: "A COMPONENTLASS, ELECTROSTATIC DISCHARGE TECHNIQUE" MOTOROLA TECHNICAL DEVELOPMENTS, MOTOROLA INC. SCHAUMBURG, ILLINOIS, US, vol. 20, 1 October 1993 (1993-10-01), page 135, XP000403852 ISSN: 0887-5286**

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Description

[0001] This disclosure generally relates to electrostatic discharge (ESD) protection devices, methods of manufacturing ESD protection devices, and electronic devices incorporating spark gap ESD protection devices.

[0002] Spark gaps are ESD protection devices that comprise two or more spaced apart electrodes having a breakdown voltage dependent on the electrode spacing and geometry. When a voltage across the gap spacing exceeds the breakdown voltage, an arc is created across the spark gap that causes the voltage across the spark gap to clamp to a clamp level.

[0003] This disclosure describes novel spark gap fabrication methods and novel spark gap devices. This disclosure also describes novel applications of conventional spark gap devices and novel applications of the novel spark gap devices described herein.

[0004] The document "A Componentless, Electrostatic Discharge Technique", P. Gilmore et al., Motorola Technical Developments, Motorola Inc., Schaumburg, Illinois, US, Vol. 20, 1 October 1993, page 135, discloses a configuration on a flexible or rigid printed circuit that provides a preferred path for the high energy of an electrostatic charge to discharge. As the charge builds up on a first circuit trace it is most likely to arc from the probe of the first circuit trace to the adjacent probe of a second circuit trace which could carry the charge to ground.

[0005] EP 1 229 618 A2 discloses a discharge gap apparatus. Here, a primary terminal including a primary discharge section for discharge and a secondary terminal including a secondary discharge section for discharge are arranged on a board at a distance from each other to satisfy an insulation standard. A floating-point terminal is provided between the primary terminal and the secondary terminal. A capacitor is connected between the floating-point terminal and the secondary terminal at a distance from the discharge sections. The interval at which the capacitor is connected is greater than the shortest distance between the secondary terminal and the floating-point terminal so as to satisfy the insulation standard.

[0006] US 5,915,757 discloses an electrostatic protective device which is highly effective in protecting relatively vulnerable devices such as IC's and LSI's from electrostatic damages, and a method for fabricating an electrostatic protective device which can simplify the structure as compared with the conventional devices sealed in a glass container, and can reduce the size and cost of the device. The chip type electrostatic protective device comprises an inner insulating layer made of organic resin material and provided with a plurality of holes for defining air gaps, a pair of outer insulating layers placed on both sides of the inner insulating layer, and circuit segments defining a discharge gap in each of the air gaps. Holes for interconnection are formed in the laminated assembly, and the interior of each of the holes is turned electroconductive. The assembly is then cut apart into individual chip type electrostatic protective devices by cutting through each of the holes for interconnection so as to define terminals for interconnection.

[0007] The invention relates to an apparatus according to the features of claim 1 and to a method of fabricating a spark gap on a substrate, according to the features of claim 5.

DRAWINGS

[0008]

Fig. 1 depicts a plurality of laser footprints in overlapping disposition on a conductor surface;
Fig. 2 is a flowchart for a method of fabricating a circumferential extension spark gap device;
Figs. 3 and 4 depict example embodiments of a circumferential extension spark gap device;
Fig. 5 depicts a plurality of laser footprints in both vertical and horizontal overlapping disposition on a conductor surface;
Fig. 6 is an example embodiment of a circumferential extension spark gap device formed by the laser footprint pattern of Fig. 5;
Fig. 7 depicts another embodiment of a circumferential extension spark gap device;
Fig. 8 depicts another embodiment of a spark gap device including a shunt capacitor;
Fig. 9 depicts a side view of a printed circuit board embodiment of the spark gap device of Fig. 8;
Fig. 10 depicts a side view of another printed circuit board embodiment of the spark gap device of Fig. 8;
Fig. 11 depicts a side view of a printed circuit board embodiment of the spark gap device of Fig. 8, according to the invention;
Fig. 12 depicts another embodiment of a circumferential extension spark gap device;
Figs. 13 and 14 depict side and top views of a spark gap device in a flex circuit;
Fig. 15 depicts example embodiments of spark gap devices integrated into surface mount components;
Fig. 16 depicts an example embodiment of a spark gap device in a surface mount capacitor;
Fig. 17 provides a plurality of circuit representations for various surface mount components having integrated spark gap devices;
Fig. 18 depicts a top view of a mobile communication device;
Fig. 19 depicts a spark gap device for providing ESD protection from a metal surface case component of the mobile communication device;
Figs. 20 and 21 depict side and bottom views of one embodiment of a spark gap device for providing ESD protection from a metal surface case component of the mobile communication device;
Figs. 22 and 23 depict side and bottom views of another embodiment of a spark gap device for providing ESD protection from a metal surface case compo-

nent of the mobile communication device;

Fig. 24 is an example printed circuit board (PCB) having integrated circumferential extension spark gap devices for providing ESD protection; and

Fig. 25 is an example subscriber identity module (SIM) card having integrated circumferential extension spark gap devices for providing ESD protection.

DETAILED DESCRIPTION

[0009] Fig. 1 depicts a plurality of laser footprints 10 in overlapping disposition on a conductor surface 12. The conductor surface 12 is typically a conductive trace material, such as copper, gold, or the like, that is deposited on a substrate material or integrated into a thin film interconnect layer. Conductive traces 13, 14, 15 and 16 are used to electrically connect electronic circuit elements or to define conductive electrical paths. For example, conductive trace 13 may be connected to signal processing circuitry and conductive trace 14 may be connected to an input pin on a Universal Serial Bus (USB) port, while conductive traces 15 and 16 may be connected to a reference ground.

[0010] The laser footprints 10 each have a diameter D within which the conductor surface 12 is etched away when a laser is activated. As the conductor surface 12 is ablated away in each footprint 10, a spark gap 20 is formed. The conductor surface 12 is removed by laser ablation, which results in overlapping arcuate voids 22 in the conductor surface 12 that coincide with the laser footprints 10. A plurality of remaining conductive circumferential extensions 24 define the overlapping arcuate voids 24. The distance G between the tips of the circumferential extensions 24 is the spark gap distance. Typically, the laser ablation will remove to a particular depth the substrate material on which conductive surface is deposited.

[0011] Fig. 2 is a flowchart 30 for a method of fabricating a circumferential extension spark gap device 20. In step 31, design data is input into a laser ablation device for conductor removal. The design data may comprise data used by a laser ablation device to selectively position and activate a laser used in steps 32 and 33. In step 32, laser footprints are overlapped on a conductor surface. The laser footprints may be overlapped simultaneously, such as when utilizing multiple lasers, or may be overlapped sequentially, such as when using a single laser and redirecting the laser beam relative to the conductor surface. The laser footprints may also be overlapped only in a horizontal direction as shown in Fig. 1, or may be overlapped in both a vertical and horizontal direction, as shown in Fig. 5.

[0012] In step 33, a void is laser ablated at each laser footprint. Laser ablation will remove the conductor surface within the laser footprint. After all of the voids in the conductor surface have been created, the resulting conductor surface is separated into two conductive regions separated by a circumferential extension spark gap 20.

[0013] In step 34, the laser-ablated spark gap is evaluated. The evaluation may comprise electrical testing, visual inspection, of a combination of both electrical testing and visual inspection.

[0014] Figs. 3 and 4 depict example embodiments of a circumferential extension spark gap device 20. Each spark gap 20 comprises a plurality of circumferential extensions 24 that define arcuate voids 22. The arcuate voids 22 in the conductive material separate a first conductor 36 and a second conductor 38. The circumferential extensions 24 on the first conductor 36 are in opposing disposition to the circumferential extensions 24 on the second conductor 38. Conductive traces 13 and 14 of the first conductor 36 are used to electrically connect electronic circuit elements or to define conductive electrical paths. Conductive traces 15 and 16 of the second conductor 38 are used to connect the second conductor to a reference potential, such as a ground.

[0015] The spark gap distance may be adjusted by adjusting the amount of overlap in the laser footprints. For example, the overlap amount of the laser footprints in Fig. 3 is less than the overlap amount of the laser footprints in Fig. 4. Accordingly, the spark gap distance G of Fig. 3 is less than the spark gap distance G' of Fig. 4. In one embodiment, the overlap amount of the laser footprints is adjusted to obtain a spark gap distance G of approximately 12 μm. In this embodiment, the laser footprints are horizontally overlapped as in Fig. 4, and thus the spark gap distance G is less than the diameter of the laser footprint.

[0016] In another embodiment, the laser footprints may be both vertically and horizontally overlapped to adjust the spark gap distance G. Fig. 5 depicts a plurality of laser footprints 22 in both vertical and horizontal overlapping disposition on a conductor surface. Fig. 6 is an example embodiment of a circumferential extension spark gap device 20 formed by the laser footprint pattern of Fig. 5. The circumferential extensions 24 define the arcuate voids 22 for each overlapping laser footprint. Thus, by vertically and horizontally overlapping the laser footprints, the spark gap distance G may be adjusted to a distance greater than the diameter of the laser beam footprint.

[0017] While only three void regions 22 are shown in Figs. 3 and 4, the spark gap 20 may comprise circumferential extensions defining tens, hundreds or even thousands of voids 22. Increasing the number of circumferential extensions tends to increase the durability of the spark gap to repeated use. Additionally, while the laser footprints 10 and/or resultant arcuate voids 22 are depicted as circular, the laser footprints 10 and/or resultant arcuate voids 22 may also comprise other arcuate shapes, depending on the particular laser device implemented.

[0018] Fig. 7 depicts another embodiment of a circumferential extension spark gap device 20. The spark gap device 20 of Fig. 7 is an embodiment that may be used in a printed circuit board (PCB) or a flex circuit. Conduc-

tive surfaces 46 and 48 are covered by solder masks 40 and 42, respectively. A spark gap 20 comprising a plurality of circumferential extensions 24 that define arcuate voids 22 separates the conductive surfaces 46 and 48. A keep-out zone 44 separates the spark gap 20 from adjacent pads. In one embodiment, the solder masks 40 and 42 lengths l_m, and the keep out zone 44 length l_k are 0.1mm, and the surface area of the spark gap device A is $0.5mm^2$.

[0019] Fig. 8 depicts another embodiment 50 of a spark gap device 20 including a shunt capacitor 54 that is connected in parallel with the spark gap device 20. An ESD sensitive device, such as digital processing circuitry, may be connected to a connection point 56. The connection point 58 defines ESD entry points, such as a signal line in a USB port. The connection point 62 defines ESD source, such as a person or an electrical device that may have a different potential than the potential of connection point 58. The ESD energy may be modeled as an energy discharge from a RLC circuit comprising a series connected resistor 64, capacitor 66, and inductor 68.

[0020] The shunt capacitor 54 provides additional shunt protection and voltage limiting. The voltage across the spark gap is approximated by the equation:

$$V_{SG} = V_{ESD}(C_{ESD}/(C_{SG} + C_{ESD}))$$

where

V_{ESD} is the voltage across the capacitor 66;
C_{ESD} is the capacitance of capacitor 66; and
C_{SG} is the capacitance of the capacitor 54.

[0021] In one embodiment, an optional resistor 60 may be connected in series with the parallel connected spark gap 20 and capacitor 54 to further limit the injection of ESD energy into the ESD sensitive device. Additionally, the resulting reactive network acts as a single-pole filter. In another embodiment, an optional inductor 61 may be connected in series with the parallel connected spark gap 20 and capacitor 54 to further limit the injection of ESD energy into the ESD sensitive device.

[0022] Fig. 9 depicts a side view of a printed circuit board 70 embodiment of the spark gap device 50 of Fig. 8. The printed circuit board 70 comprises a plurality of levels 71a-h. In particular, levels 71a, 71b, 71c, 71f, 71g and 71h comprises signal levels upon which conductive signal traces are deposited. Level 71d comprises a ground level upon which a conductive ground trace is deposited. Level 71e comprises a power level upon which a conductive power trace is deposited. The conductive signal traces of levels 71a, 71b, 71c, 71f, 71g and 71h are used to conduct electrical data signals. The ground trace of level 71d may be connected to a ground reference potential, such as a V_{ss} potential, and the conductive power trace of level 71e may connected to a power potential, such as a V_{cc} potential.

[0023] Conductive traces on each level 71a-h are depicted by their thickened side profiles 73 relative to surfaces 75 that represent the demarcation between printed circuit board levels. For example, the conductive trace 73a that is deposited on ground level 71d may comprise a ground trace or a ground plane. The conductive trace 73a is also connected to ground by vias 74a and 74b to provide access to the ground potential in other layers of the printed circuit board. Each ground via 74a and 74b comprises a conductive trace deposited on the interior surface of the via, or may comprise a conductive core filling the interior region of the via. The conductive trace 73b on power level 71f is not connected to the ground by vias 74a and 74b, as represented by the surface area 75 interposed between the conductive trace 73b and ground vias 74a and 74b. Likewise, the conductive trace 73e on signal level 71c is not connected to the ground by via 74a, as represented by the surface area 75 interposed between the conductive trace 73e and ground via 74a.

[0024] Conductive trace interconnections between levels 71 may also be established by conductive vias 72. Each conductive via 72 comprises a conductive trace deposited on the interior surface of the via, or may comprise a conductive core filling the interior region of the via. For example, in the cross section shown, conductive trace 73d is connected to conductive trace 73e through conductive vias 72a and 72b. Likewise, the conductive trace 73e is connected to conductive trace 73f through conductive vias 72e and 72d; conductive trace 73g is connected to ground via 74a by conductive via 72c; and conductive trace 73h is connected to ground via 74b through conductive via 72f.

[0025] A top signal layer 71a are a surface mount capacitor 54 and a ball grid array (BGA) mounted electrical device 69. Other mounting methods other than those shown may also be used. The electrical device 69 may comprise any electrical device having or requiring ESD protection, such as a discrete electrical component, an integrated circuit, and the like.

[0026] A circumferential spark gap 20, which comprises conductive traces 73f and 73g, is interposed between one terminal of the capacitor 54 and ground via 74a. The spark gap 20 is formed by the laser ablation process described above. The laser ablation typically removes a particular depth of the substrate material upon which the conductive material is deposited, as indicated in the slightly conical depression in the dielectric 76 beneath the spark gap 20.

[0027] Conductive trace 73g of the spark gap 20 is connected to the ground via 74a through conductive via 72c. The other conductive trace 73f of the spark gap 20 is connected to one terminal of the capacitor 54 through conductive vias 72d and 72e, and also to conductive trace 73e. The conductive trace 73e, in turn, is connected to the electronic device 69 through conductive vias 72a and 72b and conductive trace 73d. Additionally, the other end

of the capacitor 54 is connected to the ground via 74b through conductive trace 72f. Thus, the capacitor 54 and the spark gap 20 are interposed in parallel between the electrical device 69 and ground to provide spark gap ESD protection with a parallel shunt capacitance.

[0028] Fig. 10 depicts a side view of a second printed circuit board 70 embodiment of the spark gap device of Fig. 8. The printed circuit board 70 of Fig. 10 comprises signal levels 71i, 71j, 71n, 71o and 71p, ground levels 71k and 71l, and power level 71m. This embodiment is similar to the embodiment of Fig. 9, except that the circumferential spark gap is fabricated in a layer beneath the top layer 71i.

[0029] Fig. 11 depicts a side view of a printed circuit board 70 embodiment of the spark gap device of Fig. 8, according to the invention. The printed circuit board 70 of Fig. 11 comprises signal levels 71q, 71r, 71s, 71v, 71w and 71x, ground levels 71t and power level 71u. Signal level 71r further comprises a thin laminate 77 upon which one or more conductive traces may be deposited. The thin laminate 77 is used to form a spark gap 21. The laminate 77 includes a periphery 79 that defines an opening. The opening is placed over a space 78 in the dielectric 76 and extends over the periphery defined by the space 78. In the embodiment shown in Fig. 11, the geometry of the opening in the laminate 77 is such that the laminate 77 extends over the sides of the dielectric space 78.

[0030] A first side 80 of the opening comprises a conductive trace and is connected to a ground via 74d and a first terminal of the capacitor 54 through conductive via 721. A second side 81 of the opening likewise comprises a conductive trace and is connected to a conductive via 72m. The conductive via 72m is, in turn, connected to the other terminal of the capacitor 54 and the electronic device 69 by conductive trace 73n. Spark gap protection is thus provided by the gap formed by the conductive trace 73p on the second side 81 of the opening and the conductive ground trace 73a. Thus, the capacitor 54 and the spark gap 21 are interposed in parallel between the electrical device 69 and ground to provide spark gap ESD protection.

[0031] A shunt capacitor may also be fabricated directly in the printed circuit board 70. For example, in Fig. 11, the dielectric 76 interposed between the laminate 77 and the conductive ground trace 73a may be selected so that the dielectric 76 and the conductive traces 73a and 73p form a capacitor. Accordingly, a first terminal of the capacitor is connected to the electrical device 69 through the conductive via 72m and conductive trace 73n. The second terminal of the capacitor comprises the conductive ground trace 73a, and thus the capacitor 54 and the spark gap 21 are interposed in parallel between the electrical device 69 and ground to provide spark gap ESD protection.

[0032] Fig. 12 depicts another embodiment of a circumferential extension spark gap device 20. In this embodiment, conductor 90 and conductive traces 96 and 98 comprise a first signal path, and conductor 94 and conductive traces 104 and 106 comprise a second signal path. Conductive traces 100 and 102 are connected to a ground reference so that conductor 92 provides a spark gap ground reference. Each spark gap 20 is similar to the spark gaps described with respect to Figs. 1 - 6 above, and comprises a plurality of conductive circumferential extensions 24 that define voids 22 in the conductive surface.

[0033] Figs. 13 and 14 depict side and top views, respectively, of a spark gap device in a portion of a flex circuit 110. The flex circuit 110 comprises a flexible dielectric or insulating material 112. In one embodiment, the flexible material comprises a polyimide material. Other flexible materials may also be used, such as a liquid crystal polymer (LCP) material. In another embodiment, the dielectric 112 may be selected so that the dielectric constant and the conductive traces between which the dielectric is interposed form a capacitor.

[0034] Conductive traces 114, 116 and 118 are positioned near the top layer of the flex circuit 110. A bottom conductive trace comprises a conductive ground trace 120. The conductive trace 118 is connected to the conductive ground trace 120 through a conductive via 122. Conductive traces 114 and 116 may be connected to signal processing circuitry or data transmission, such as a semiconductor device or a input pin on a connector 124.

[0035] A first spark gap 20a is interposed between the conductive traces 116 and 118, and connected in parallel to a capacitor 54. The first spark gap 20a is laser ablated to a depth that does not exceed the depth of the dielectric 112. A second spark gap 20b is interposed between the conductive traces 114 and 118, and connected in parallel to a capacitor 54. The second spark gap 20 is laser ablated to a depth that extends through the flex circuit. The second spark gap 20b thus is also vertically disposed, providing alternate ESD protection via distance G that is defined by the thickness G of the dielectric or insulating material 112. Thus, the second spark gap 20b comprises the entire periphery of the conductor edges defining the arcuate voids 22. Capacitors 54 may be optionally connected in parallel with the spark gaps 20a and 20b to provide additional shunt capacitance protection.

[0036] Fig. 15 depicts example embodiments of spark gap devices integrated into surface mount components 130 and 150. Fig. 15(a) depicts a surface mount component 130 having a spark gap device comprising circumferential extensions 24 defining overlapping arcuate voids 22 as described with respect to Figs. 1-4 above. Fig. 15(b) depicts a surface mount component 150 having a spark gap 151 comprising angled extension. The spark gap 151 of Fig. 15(b) may be constructed by a chemical etching process, or by photolithography masking, or other fabrication methods.

[0037] Each of the surface mount components 130 and 150 also comprise solder masks 138 and 140 and solder tabs 142 and 144. The spark gap and solder masks 138 and 140 may be distributed on one surface of an insulator

136. The surface mount components 130 and 150 may also comprise a circuit element disposed between the solder tabs 142 and 144 so that the spark gap is connected to the solder tabs 142 and 144 in parallel with the circuit element. The spark gap thus provides bi-directional ESD protection to the electrical element and may further limit over-voltage spikes to a nondestructive level.

[0038] The circuit elements may comprise passive circuit components, such as a resistor, inductor or capacitor. Fig. 16 depicts an example embodiment of a spark gap device in a surface mount capacitor 150. The capacitor 150 comprises interlayered electrode plates 160, 161, 162 and 163 and an interposing dielectric 164. The electrode plates 160 and 161 are connected to the solder tab 144, and the electrode plates 162 and 163 are connected to the solder tab 142. A circumferential spark gap device 20 comprising circumferential extensions 24 that define arcuate voids 22 is connected to the solder tabs 142 and 144 in parallel with the electrode plates 160, 161, 162 and 163. Although the novel spark gap device 20 of Figs. 1-6 is implemented in the embodiment of Fig. 16, other spark gap devices comprising a different geometry may also be used, such as the angled spark gap device of Fig. 15(b).

[0039] Fig. 17 provides a plurality of circuit representations for various surface mount components having integrated spark gap devices. Figs. 17(a), (b) and (c) depict circuit representations for a surface mount capacitor, inductor, and resistor, respectively. The components of Figs. 17(a), (b) and (c) may facilitate a variety of implementations. For example, the resistor device of Fig. 17 (c) may be implemented as a protected resistor, or may alternatively be implemented as a spark gap having a high bypass resistance. Other two-terminal circuit elements may also be used, and other packing schemes may likewise be used. For example, a two-terminal, multipole filter may be protected by the parallel spark gap device of Fig. 15. Likewise, the parallel spark gap device may also be used to protect other packaging, such as dual in-line (DIP) or small-outline integrated circuit (SOIC) packaging, or be used in conjunction with an IC socket and module.

[0040] The capacitance of the spark gap device 20 may also be considered when fabricating the circuit element. For example, if the characteristic capacitance of a circumferential spark gap device 20 is 0.1 pF, and a surface mount component is to provide a capacitance of 10 pF, then the value of the actual capacitor to be connected in parallel with the spark gap device 20 may be adjusted accordingly so that the terminal capacitance is 10 pF.

[0041] Fig. 18 depicts a top view of a mobile communication device 200. The spark gap device of Figs. 1-4 may be implemented in the mobile communication device 200 to provide ESD protection to ESD-sensitive components. The mobile communication device 200 may have a data communication capability, a voice communication capability, or a combination of data and voice communication capability. The housing of the mobile communication device 200 may include a conductive surface, such as a metal bezel 210 having an interior edge 211. The interior edge 211 defines an opening for viewing a display assembly 202, such as a liquid crystal display (LCD). A keyboard 204, a speaker 206 and a microphone 208 are provided to facilitate voice and data communications.

[0042] The mobile device 200 is operable to communicate over a wireless network via a radio frequency link. The metal bezel 210 is an entry point for ESD energy. Typically, however, grounding the metal bezel 210 directly to ground will cause a high capacitive coupling to the mobile device 200 antenna and cause RF communication performance degradation. Accordingly, a spark gap device is implemented to provide ESD protection and minimize capacitive coupling, and reroutes the destructive ESD to a PCB ground.

[0043] Fig. 19 depicts a spark gap device 222 for providing ESD protection from a metal surface case component 210 of the mobile communication device 200. A spark gap device 222 provides ESD protection of an LCD assembly 202 by providing a spark gap from the metal bezel 210 to a ground potential on a PCB 220. The LCD assembly 202 may comprise a display window 212, a display gasket 213, an LCD module 214, a LCD driver chip 216, and an LCD I/O connector 218.

[0044] Figs. 20 and 21 depict side and bottom views of one embodiment of a spark gap device for providing ESD protection from a metal surface case component 210 of the mobile communication device 200. In this embodiment, the circumferential spark gap of Figs. 1-6 is used. An insulator 224 separates the spark gap device 222 from the metal bezel 210. A first conductor 230 is connected to the metal bezel 210, proximate to the interior edge 211. A second conductor 232 is connected to a reference ground potential. The first and second conductors 230 and 232 are separated by a spark gap 20 comprising circumferential extensions 24 that define a plurality of overlapping arcuate voids 24.

[0045] Figs. 22 and 23 depict side and bottom views of another embodiment of a spark gap device for providing ESD protection from the metal surface case component 210 of the mobile communication device 200. In this embodiment, a triangular shaped spark gap 223 is used. The triangular shaped spark gap 223 is separated from the interior edge 211 of the metal bezel 210 by a gap istance G. An insulator 224 is used to separate the conducting surface of the spark gap device 224 from the metal bezel 210. The other end of the spark gap device 224 is connected to a reference ground potential. In one embodiment, a poron strip is used to realize the spark gap device 224. In another embodiment, two conductors with triangle terminations are used to provide a triangular spark gap. This embodiment is similar to the embodiment of Figs. 18 and 19, except that the spark gap comprises a triangular geometry instead of the circumferential geometry.

[0046] The spark gap devices 20 described herein may be configured to protect other circuitry in the mobile com-

munication device 200. Fig. 24 is an example PCB 250 having integrated circumferential extension spark gap devices 240 for providing ESD protection. Each integrated circumferential spark gap device 240 comprises a first conductor 242 and a second conductor 244 separated by a spark gap 20 comprising a plurality of circumferential extensions 24 that define arcuate voids. The integrated circumferential spark gap devices 240 may be distributed to protect any ESD sensitive circuitry connected to an ESD entry point, such as battery contacts 252, I/O device jacks 254, SIM contacts 256, and/or keypad dome switches 258.

[0047] Keypad dome switches 258 comprise a conductive trace 260 and a conductive center pad 262. Each section of the conductive trace 260 defining a keypad area is connected to an integrated circumferential spark gap device 240. Likewise, each conductive center pad 262 is connected to an integrated circumferential spark gap device 240. In the embodiment shown, integrated circumferential spark gap devices 240 connected to the conductive center pad 262 are insulated from the conductive trace 260.

[0048] The integrated circumferential spark gap devices 240 may also protect removable electronic devices. Fig. 25 is an example subscriber identity module (SIM) card 270 having integrated circumferential extension spark gap devices 240 for providing ESD protection. The integrated circumferential spark gap devices 240 are interposed between a reference potential surface 272 and a power contact 274, a first data contact 276, a clock contact 278, a reset contact 280, and a second data contact.

[0049] The embodiments described herein are examples of structures, systems or methods having elements corresponding to the elements of the invention recited in the claims. This written description may enable those of ordinary skill in the art to make and use embodiments having alternative elements that likewise correspond to the elements of the invention recited in the claims. The intended scope of the invention thus includes other structures, systems or methods that do not differ from the literal language of the claims.

Claims

1. An apparatus for providing electrostatic discharge protection, comprising a spark gap device (21), the spark gap device (21) comprising:

   a substrate (76) defining first and second surfaces and a first opening (78) having a first inner periphery; and
   a first conductive surface (73a) disposed on the second surface of the substrate (76),

   characterized in that
   the spark gap device (21) further comprises

   a laminate (77) defining first and second surfaces and a second opening having a second inner periphery (79) and having a second conductive surface (73o, 73p) deposited on the first surface of the laminate, the first surface of the laminate being disposed on the first surface of the substrate so that the second inner periphery (79) of the second opening extends over the first opening (78) and beyond the first inner periphery.

2. The apparatus of claim 1, wherein the first conductive surface (73a) is further disposed to form a surface over the first opening (78).

3. The apparatus of claim 1 or 2, further comprising:

   a shunt capacitor (54) in parallel to the spark gap device (21).

4. The apparatus of claim 3, wherein
   the shunt capacitor is formed by the substrate (76) being a dielectric and the first (73a) and second (73o, p) conductive surfaces.

5. A method of fabricating a spark gap (21) according to claim 1, on a substrate (76) defining first and second surfaces, comprising:

   forming a first opening (78) defining a first inner periphery through a substrate (76);
   forming a second opening, having a smaller diameter than said first opening, defining a second inner periphery (79) through a laminate (77);
   depositing a first conductive surface (73o, 73p) on a first surface of the laminate (77);
   placing the first surface of the substrate in contact with a second conductive surface (73a); and
   placing the first surface of the laminate (77) on the second surface of the substrate (76); and
   positioning the laminate (77) so that second inner periphery (79) extends over the first opening (78) and beyond the first inner periphery.

6. The method of claim 5, wherein placing a first surface of the substrate (76) in contact with the second conductive surface (73a) comprises depositing the second conductive surface (73a) on the first surface of the laminate (77) so that the first surface of the substrate (76) defines a conductive periphery.

Patentansprüche

1. Vorrichtung zum Vorsehen eines elektrostatischen Entladungsschutzes, die eine Funkenstrecke (21) aufweist, wobei die Funkenstrecke (21) aufweist:

   ein Substrat (76), das erste und zweite Oberflä-

chen und eine erste Öffnung (78) mit einer ersten inneren Peripherie definiert; und
eine erste leitfähige Oberfläche (73a), die auf der zweiten Oberfläche des Substrats (76) angeordnet ist,
dadurch gekennzeichnet, dass
die Funkenstrecke (21) weiter aufweist
ein Laminat (77), das erste und zweite Oberflächen und eine zweite Öffnung mit einer zweiten inneren Peripherie (79) definiert und eine zweite leitfähige Oberfläche (73o, 73p) aufweist, die auf der ersten Oberfläche des Laminats aufgebracht ist, wobei die erste Oberfläche des Laminats auf der ersten Oberfläche des Substrats angeordnet ist, so dass sich die zweite innere Peripherie (79) der zweiten Öffnung über die erste Öffnung (78) und über die erste innere Peripherie hinaus erstreckt.

2. Vorrichtung gemäß Anspruch 1, wobei die erste leitfähige Oberfläche (73a) weiter angebracht ist, eine Oberfläche über die erste Öffnung (78) zu bilden.

3. Vorrichtung gemäß Anspruch 1 oder 2, die weiter aufweist:

einen Parallelkondensator (54) parallel zu der Funkenstrecke (21).

4. Vorrichtung gemäß Anspruch 3, wobei
der Parallelkondensator von dem Substrat (76), das dielektrisch ist, und der ersten (73a) und den zweiten (73o, p) leitfähigen Oberflächen gebildet wird.

5. Verfahren zur Herstellung einer Funkenstrecke (21) auf einem Substrat (76), das erste und zweite Oberflächen definiert, das aufweist:

Bilden einer ersten Öffnung (78), die eine erste innere Peripherie definiert, durch ein Substrat (76);
Bilden einer zweiten Öffnung, die eine zweite innere Peripherie (79) definiert, durch ein Laminat (77);
Aufbringen einer ersten leitfähigen Oberfläche (73o, 73p) auf eine erste Oberfläche des Laminats (77);
Platzieren der ersten Oberfläche des Substrats in Kontakt mit einer zweiten leitfähigen Oberfläche (73a); und
Platzieren der ersten Oberfläche des Laminats (77) auf die zweite Oberfläche des Substrats (76); und
Positionieren des Laminats (77), so dass sich die zweite innere Peripherie (79) über die erste Öffnung (78) und über die erste innere Peripherie hinaus erstreckt.

6. Verfahren gemäß Anspruch 5, wobei ein Platzieren einer ersten Oberfläche des Substrats (76) in Kontakt mit der zweiten leitfähigen Oberfläche (73a) aufweist ein Aufbringen der zweiten leitfähigen Oberfläche (73a) auf die erste Oberfläche des Laminats (77), so dass die erste Oberfläche des Substrats (76) eine leitfähige Peripherie definiert.

Revendications

1. Appareil pour fournir une protection contre les décharges électrostatiques, comprenant un éclateur (21), l'éclateur (21) comprenant :

un substrat (76) définissant une première et une seconde surfaces et une première ouverture (78) possédant une première périphérie interne ; et
une première surface conductrice (73a) placée sur la seconde surface du substrat (76),
caractérisé en ce que
l'éclateur (21) comprend en outre :

un stratifié (77) définissant une première et une seconde surfaces et une seconde ouverture possédant une seconde périphérie interne (79) et possédant une seconde surface conductrice (73o, 73p) déposée sur la première surface du stratifié, la première surface du stratifié étant placée sur la première surface du substrat de manière à ce que la seconde périphérie interne (79) de la seconde ouverture se prolonge sur la première ouverture (78) et au-delà de la première périphérie interne.

2. Appareil selon la revendication 1, dans lequel la première surface conductrice (73a) est en outre placée pour former une surface sur la première ouverture (78).

3. Appareil selon la revendication 1 ou 2, comprenant en outre :

un condensateur shunt (54) disposé parallèlement à l'éclateur (21).

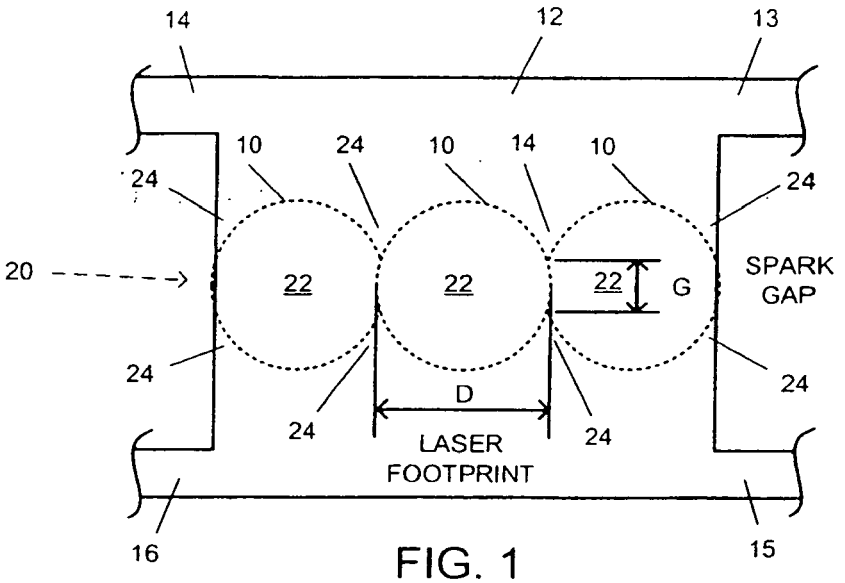
4. Appareil selon la revendication 3, dans lequel le condensateur shunt est formé par le substrat (76) qui est un diélectrique et la première (73a) et la seconde (73o, p) surfaces conductrices.

5. Procédé de fabrication d'un éclateur (21) sur un substrat (76) définissant une première et une seconde surfaces, comprenant :

la formation d'une première ouverture (78) dé-

finissant une première périphérie interne à travers un substrat (76) ;
la formation d'une seconde ouverture définissant une seconde périphérie interne (79) à travers un stratifié (77) ;
le dépôt d'une première surface conductrice (73o, 73p) sur une première surface du stratifié (77) ;
la mise en contact de la première surface du substrat avec une seconde surface conductrice (73a) ; et
le placement de la première surface du stratifié (77) sur la seconde surface du substrat (76) ; et le positionnement du stratifié (77) de manière à ce que la seconde périphérie interne (79) se prolonge sur la première ouverture (78) et au-delà de la première périphérie interne.

6. Procédé selon la revendication 5, dans lequel la mise en contact d'une première surface du substrat (76) avec la seconde surface conductrice (73a) comprend le dépôt de la seconde surface conductrice (73a) sur la première surface du stratifié (77) de manière à ce que la première surface du substrat (76) définisse une périphérie conductrice.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SPARK GAP
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D
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24
LASER FOOTPRINT
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FIG. 1

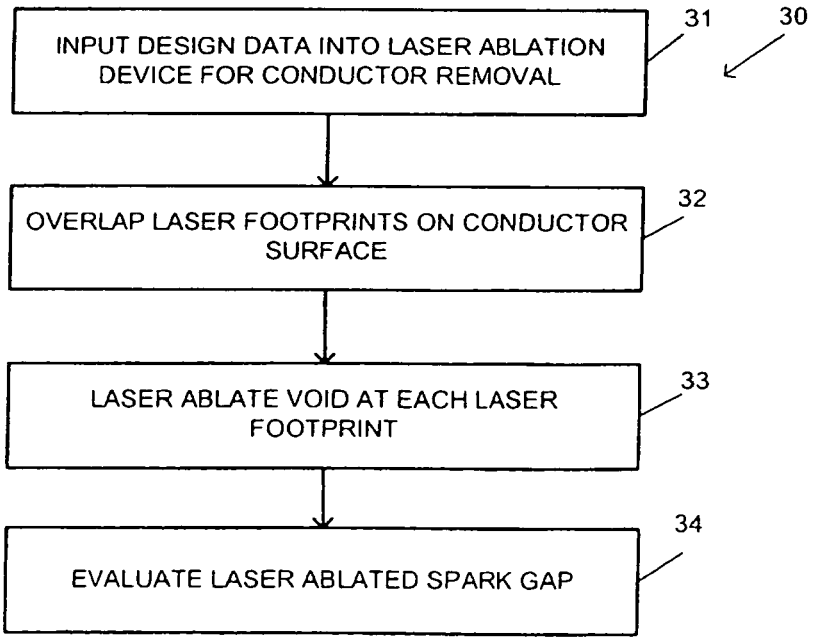
INPUT DESIGN DATA INTO LASER ABLATION DEVICE FOR CONDUCTOR REMOVAL
31
30
OVERLAP LASER FOOTPRINTS ON CONDUCTOR SURFACE
32
LASER ABLATE VOID AT EACH LASER FOOTPRINT
33
EVALUATE LASER ABLATED SPARK GAP
34

FIG. 2

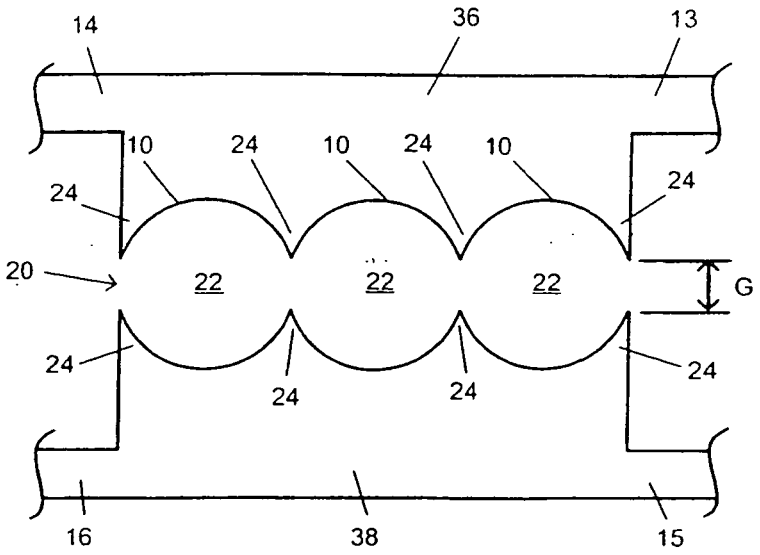
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FIG. 3

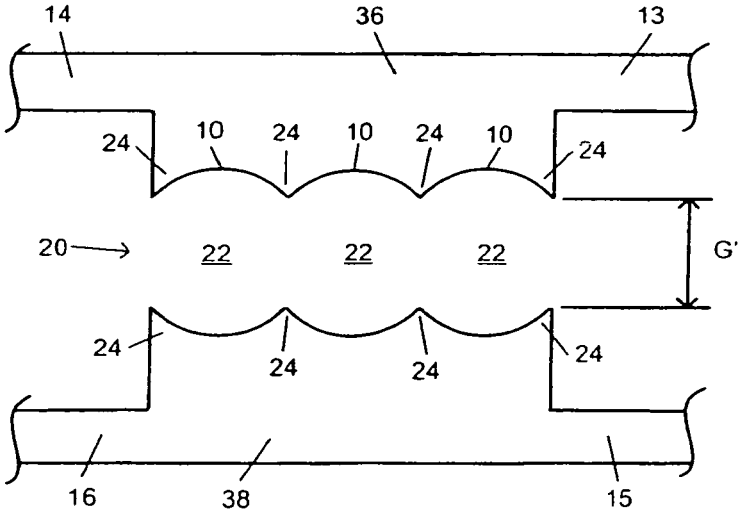
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FIG. 4

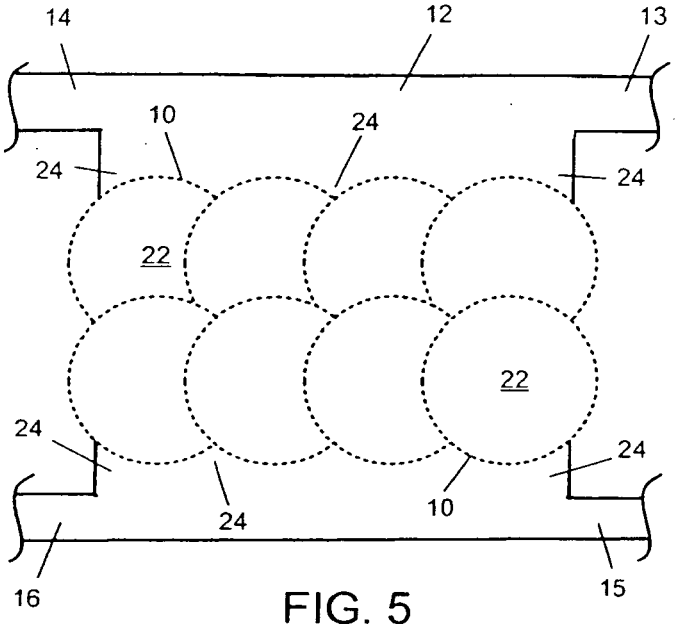
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FIG. 5

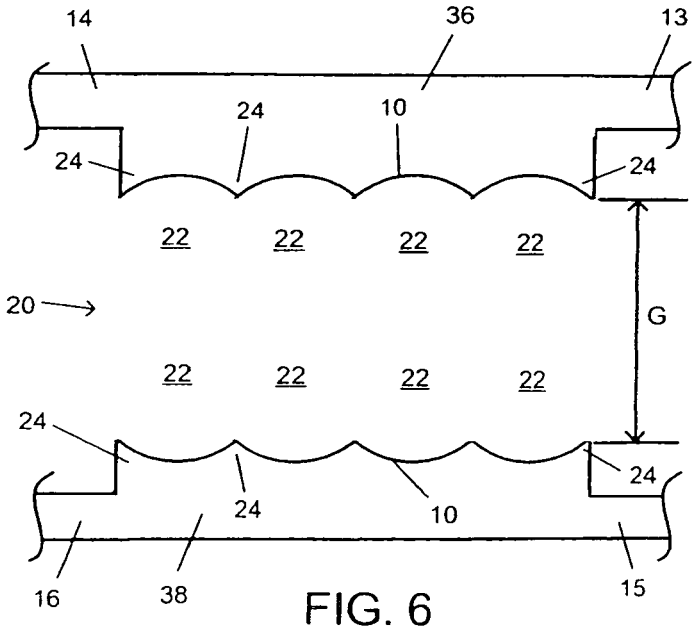
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FIG. 6

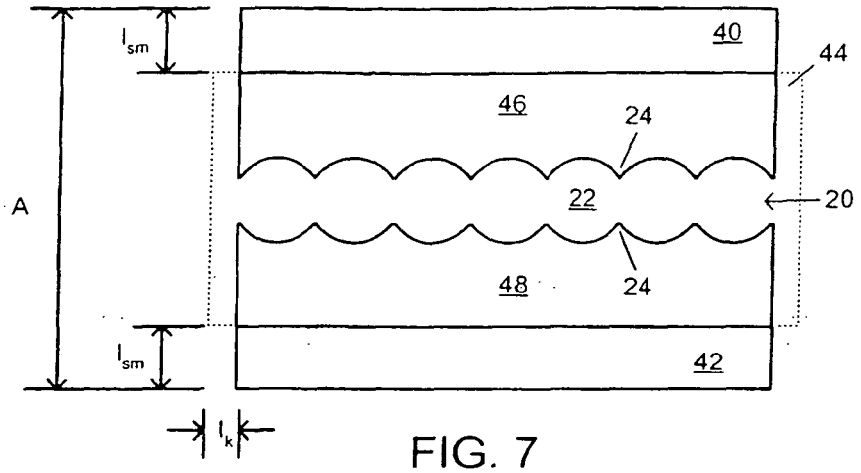


FIG. 7

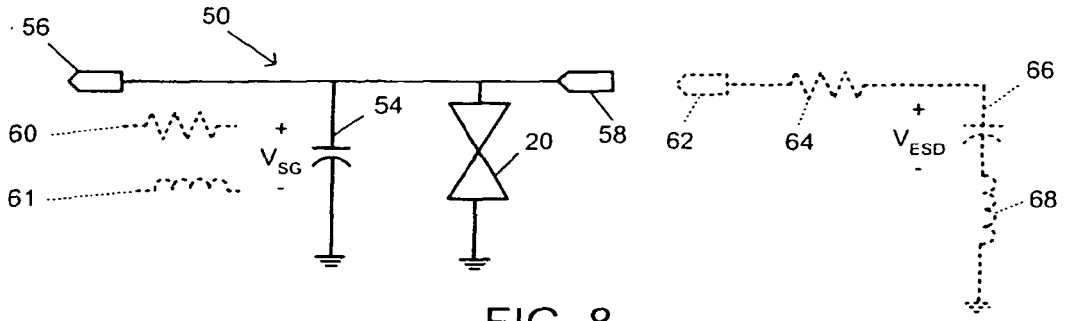


FIG. 8

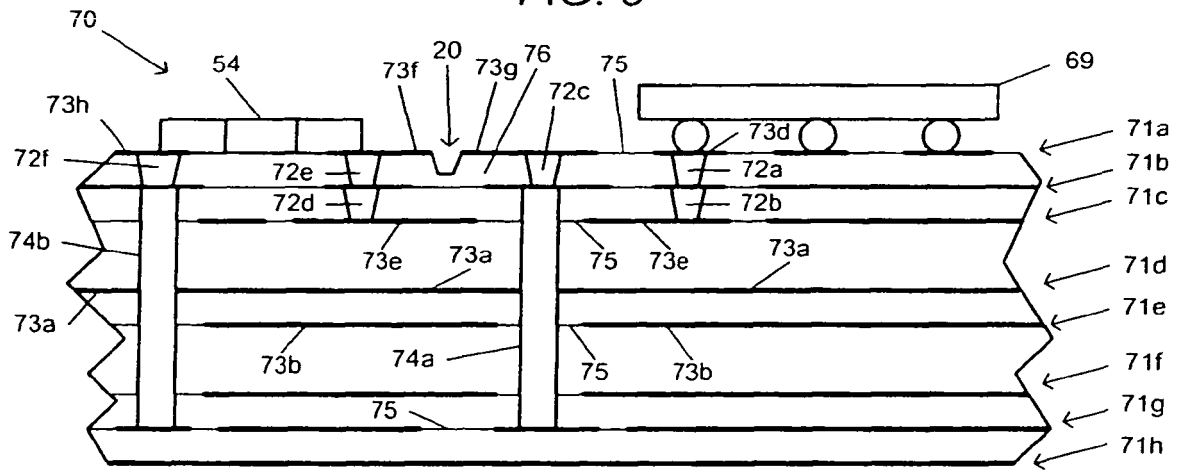
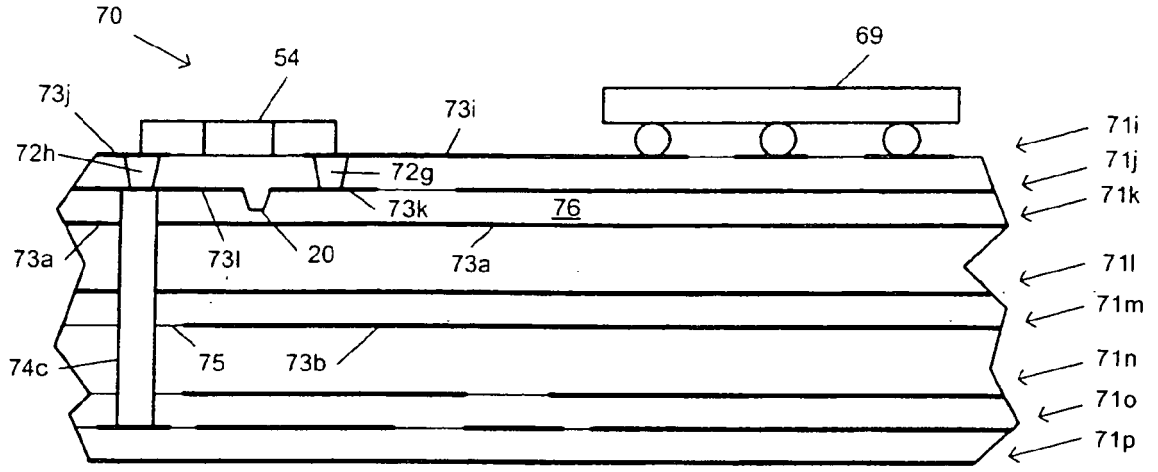


FIG. 9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71p

FIG. 10

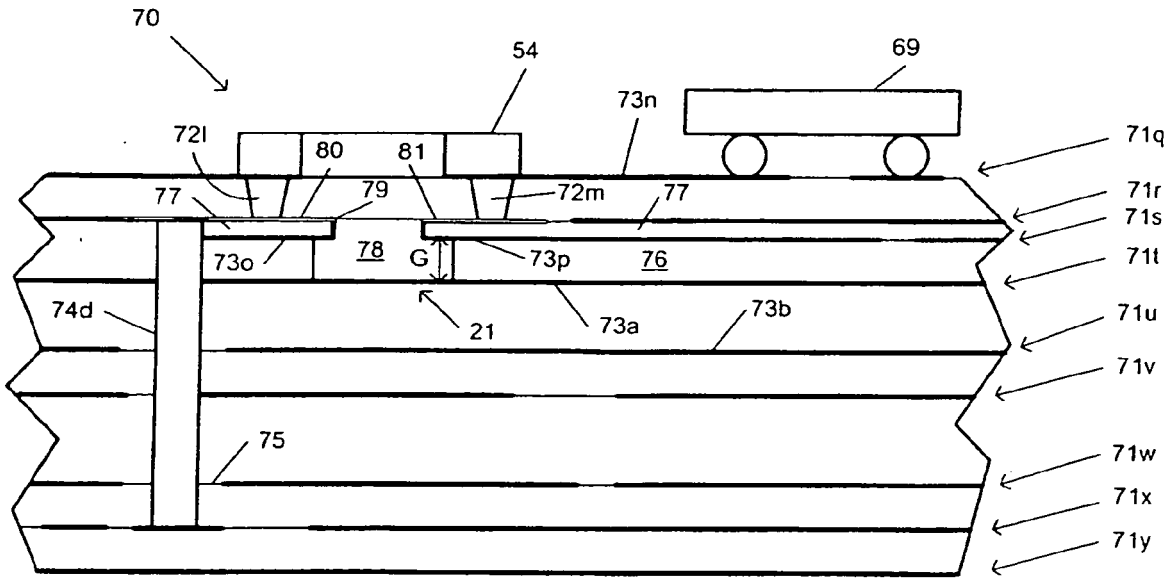
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FIG. 11

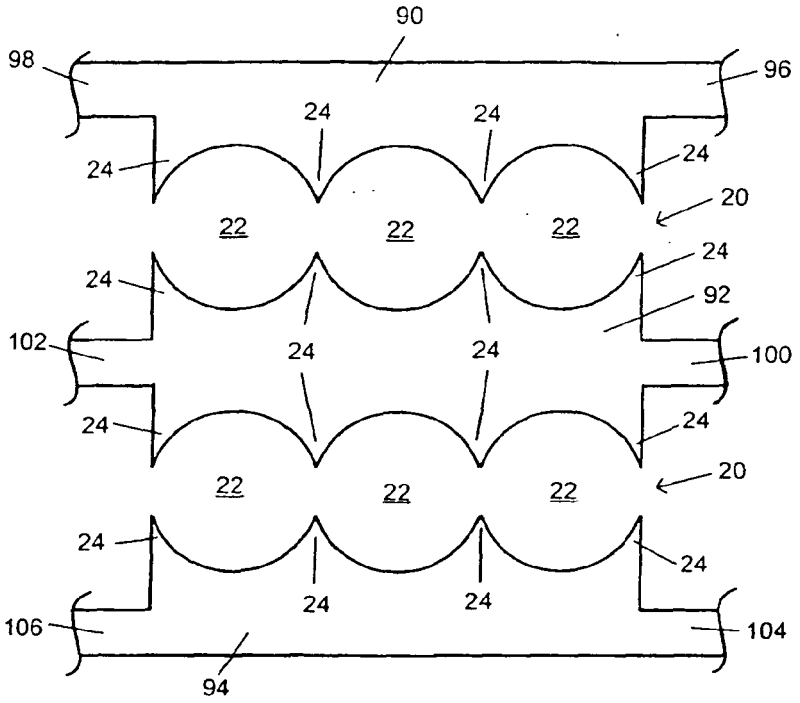
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FIG. 12

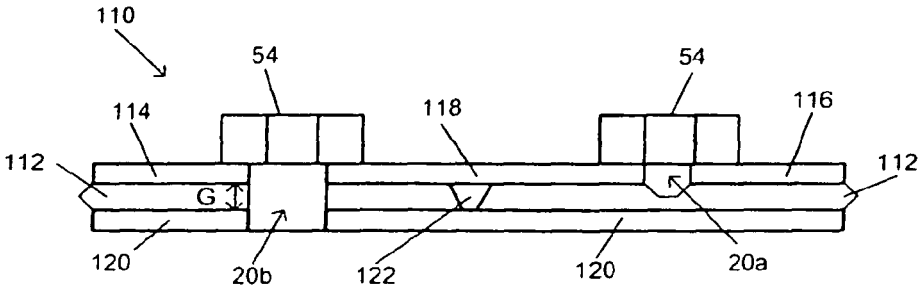
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FIG. 13

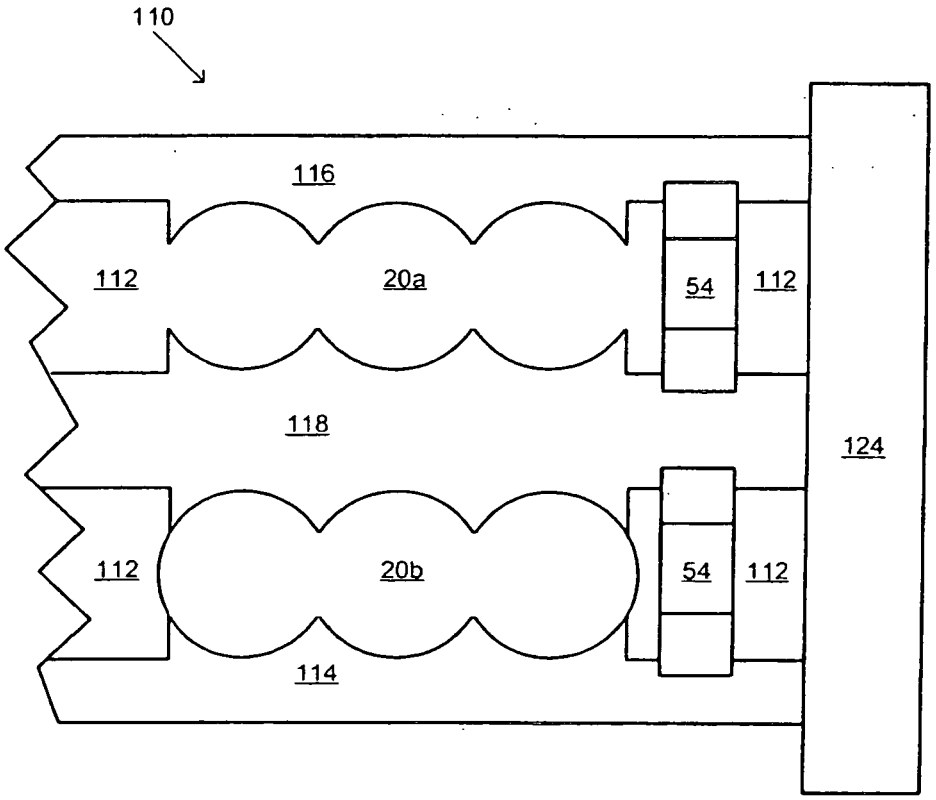

FIG. 14

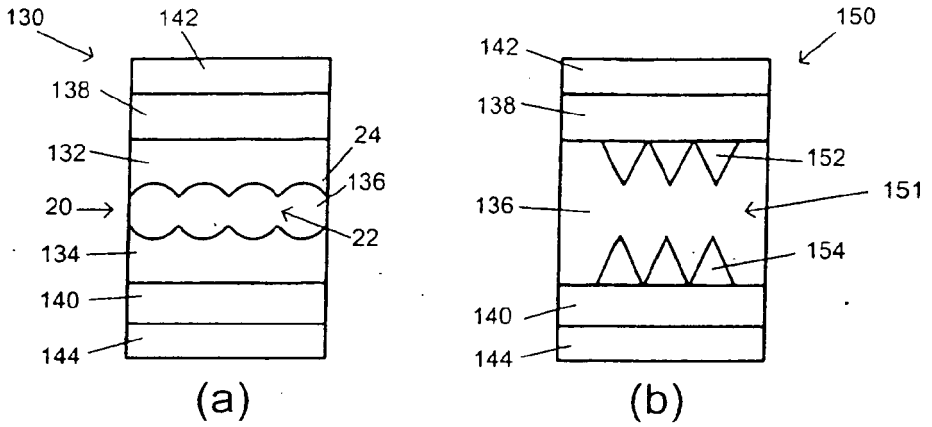

FIG. 15

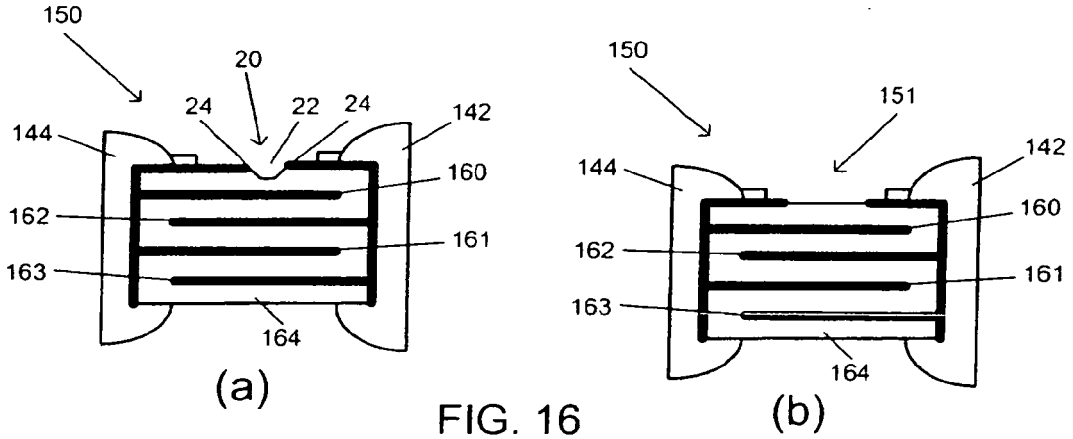

FIG. 16

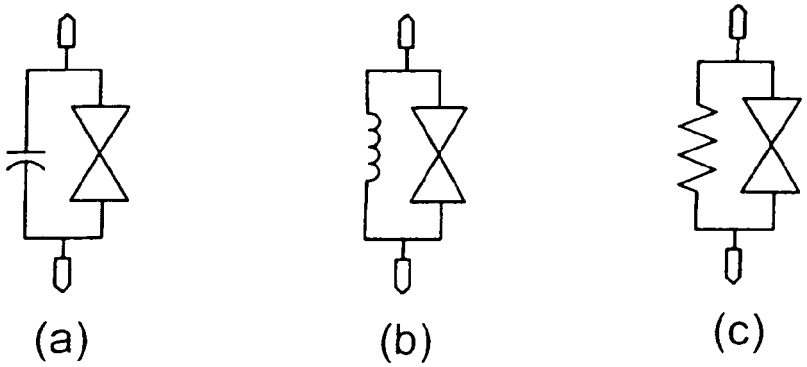

FIG. 17

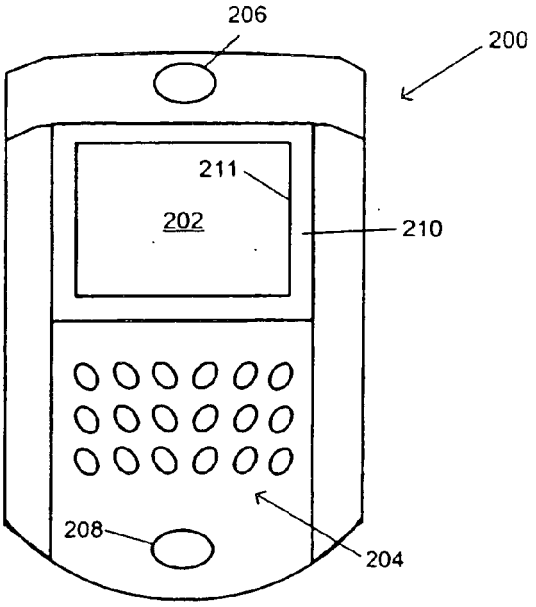
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FIG. 18

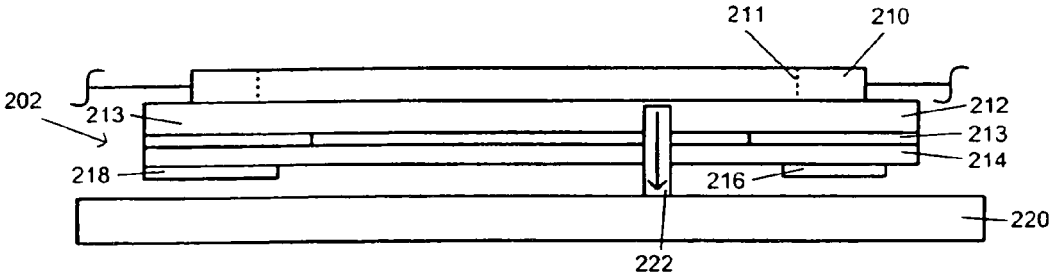
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FIG. 19

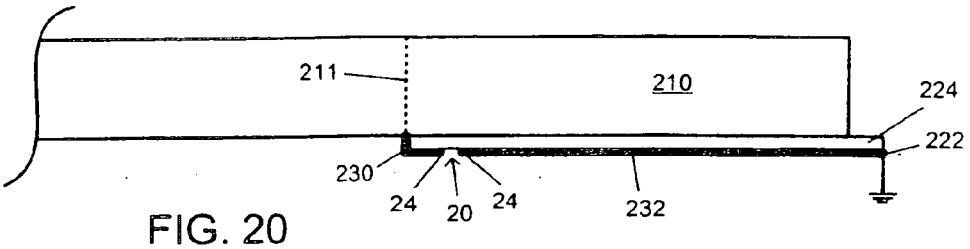

FIG. 20

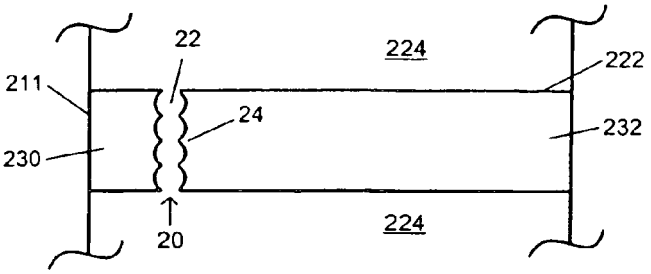

FIG. 21

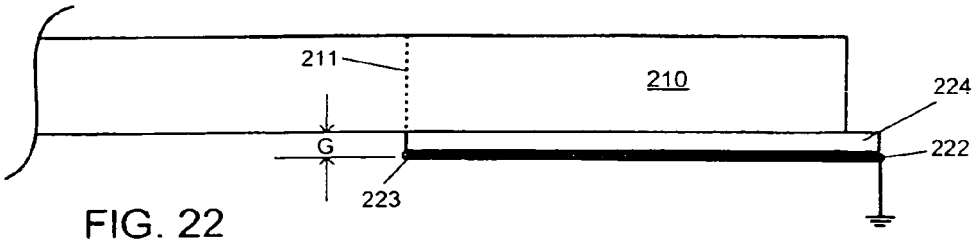

FIG. 22

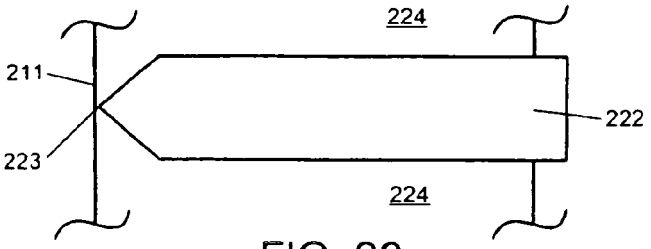

FIG. 23

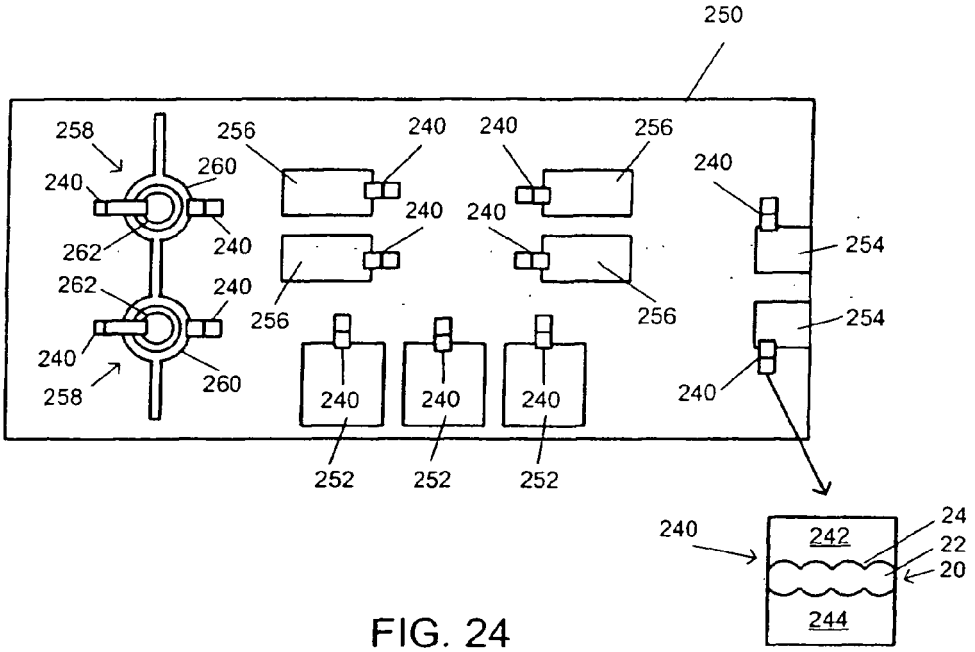
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FIG. 24

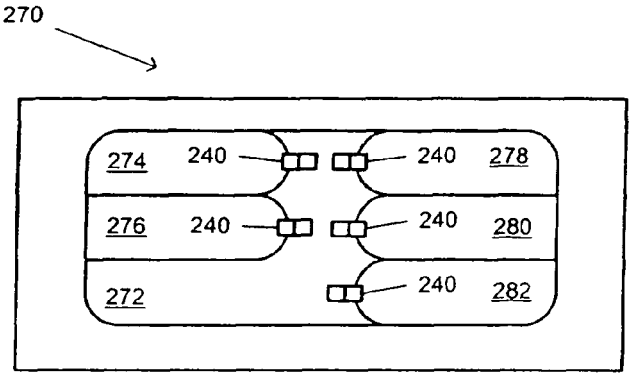
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FIG. 25

REFERENCES CITED IN THE DESCRIPTION

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Patent documents cited in the description

- EP 1229618 A2 **[0005]**
- US 5915757 A **[0006]**

Non-patent literature cited in the description

- A Componentless, Electrostatic Discharge Technique. **P. GILMORE et al.** Motorola Technical Developments. Motorola Inc, 01 October 1993, vol. 20, 135 **[0004]**