(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 1 630 657 A9

(12) **CORRECTED EUROPEAN PATENT APPLICATION**
Note: Bibliography reflects the latest situation

(15) Correction information:
Corrected version no 1 (W1 A1)
Corrections, see page(s) 1,7,8,10-14
INID code(s) 72

(48) Corrigendum issued on:
07.06.2006 Bulletin 2006/23

(43) Date of publication:
01.03.2006 Bulletin 2006/09

(21) Application number: **04425643.6**

(22) Date of filing: **30.08.2004**

(51) Int Cl.:
G06F 3/06 *(2006.01)*

(84) Designated Contracting States:
AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HU IE IT LI LU MC NL PL PT RO SE SI SK TR
Designated Extension States:
AL HR LT LV MK

(71) Applicant: **STMicroelectronics S.r.l.**
20041 Agrate Brianza (Milano) (IT)

(72) Inventors:
- **Ghezzi, Stefano**
  24048 Treviolo (IT)
- **Roveda, Marco**
  20086 Motta Visconti (IT)
- **Saltutti, Stefano**
  06023 Gualdo Tadino (IT)
- **Scarioni, Giorgio**
  20152 Milano (IT)

(74) Representative: **Cerbaro, Elena et al**
c/o Studio Torta S.r.l. Via Viotti, 9
10121 Torino (IT)

(54) **Embedded storage device with integrated data-management functions and storage system incorporating it**

(57) In a storage system (20) for an electronic device (27), a system controller (21) is connected to an embedded storage device (23) for supervising writing and reading operations in the embedded storage device; a data manager (36) based upon a microprocessor (38) is integrated in the embedded storage device (23) and provides a high-level abstraction of the physical organization of the embedded storage device (23) through the definition of an own logic map. The data manager (36) is implemented outside the controller (21). The controller (21) is formed in a first semiconductor material region, the embedded storage device (23) is formed in a second semiconductor material region distinct from the first semiconductor material region, and the data manager (36) is formed in a third semiconductor material region distinct from the first semiconductor material region.

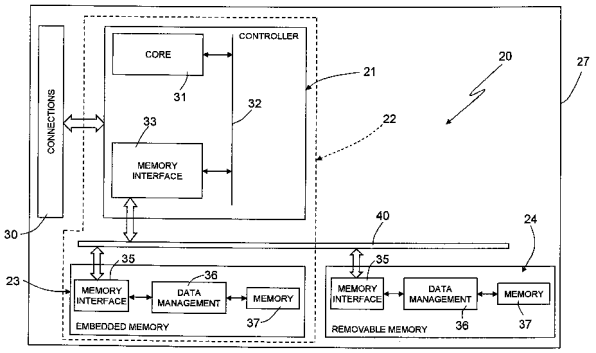

Fig.2

EP 1 630 657 A9

Description

[0001] The present invention relates to an embedded storage device with integrated data-management functions and to a storage system incorporating it.

[0002] As is known, many consumer electronic devices, such as, for example, cellphones, digital photocameras, readers of audio files in MP3 format, etc., are equipped with storage media operating as normal disk drives and storing the data as files.

[0003] As illustrated in Figure 1, a storage system 1 is basically made up of one or more embedded storage devices 3, one or more removable storage devices 4, and a controller 2 for controlling the storage system and operating as an interface and interpreter between the user and the various storage devices.

[0004] The fundamental difference between the embedded storage device 3 and the removable storage device 4 is represented by the fact that, whereas the former is basically constituted by a simple array of addressable memory cells, the latter has a more complex architecture and basically comprises an interface 8, an internal data manager 9, and a memory 10. For both of the storage devices, the memory is generally of a writeable and electrically erasable non-volatile type, in the majority of cases of a flash type. This type of memory, in fact, affords short access times, high storage capacity, low power consumption, and a great versatility of use, combined with contained costs.

[0005] The controller 2 is basically made up of a microprocessor 14 which supervises operation of the controller 2; an embedded memory interface 16; a removable memory interface 17; and a data manager 15, operatively connected to the embedded memory interface 16. The controller 2 further comprises a data bus 18, which is connected to the microprocessor 14, to the data manager 15, to the embedded memory interface 16, and to the removable memory interface 17, and enables transfer of data and control signals.

[0006] The main task of the data manager 15 is to define a logic map of the embedded storage device 3 and to determine its evolution in time, so as to allow the user to perform the desired functions irrespective of the knowledge of the structure and of the physical characteristics of the embedded storage device 3. In particular, in embedded flash storage devices, the data manager is known by the name of "Flash Translation Layer" (FTL) and supplies a high-level abstraction of the physical organization of the flash storage device, emulating the typical block structure of a disk drive, i.e., causing the flash storage device to appear from the outside as a vector of contiguous memory blocks. The FTL in particular enables rewriting of memory sectors (as occurs, for example, in hard disks), re-addressing the data towards other memory locations and marking as occupied the previously occupied sectors. When necessary, the FTL then frees part of the memory previously marked as invalid to enable writing of new data.

[0007] The storage system 1 illustrated in Figure 1 presents some disadvantages.

[0008] In particular, when a plurality of different embedded storage devices 3 is envisaged, the controller 2 must be provided with more specific embedded-memory interfaces 16, one for each embedded storage device 3, or else it must be provided with a single interface compatible with the different types of embedded memory 3. In the first case, the storage system 1 has the disadvantage of involving high production costs, because of the plurality of embedded-memory interfaces 16, whereas in the second case the single interface cannot be optimized as to performance for all the embedded storage devices 3, and moreover there always exists the risk that a new embedded storage device 3 will not be compatible with a pre-existing interface.

[0009] Furthermore, the storage system 1 comprises two data managers 9, 15, one in the removable storage device 4 and one in the controller 2. This can give rise to different levels of reliability of the data on account of the possible different management of the data in the embedded memory 3 as compared to the data management in the removable memory 4.

[0010] In addition, the presence of different memory interfaces in the controller 2 involves an additional workload for the microprocessor 14 of the controller 2, which must manage the accesses to the various storage devices in different ways, according to the type of interface, at the expense of the performance of the storage system 1.

[0011] Finally, in a storage system of the type illustrated in Figure 1, the controller 2 must necessarily be of a dedicated (or application-specific) type, which inevitably involves high costs.

[0012] The aim of the present invention is consequently to provide an embedded storage device and a storage system that overcomes the limits and problems highlighted with reference to the prior art.

[0013] The above aim is achieved by the present invention in so far as it relates to a storage system as defined in claim 1, and to a storage device as defined in claim 16.

[0014] For a better understanding of the present invention, some preferred embodiments are now described, purely by way of nonlimiting example, with reference to the attached drawings, wherein:

- Figure 1 shows a block diagram of a storage system of a known type;
- Figure 2 shows a block diagram of a storage system according to a first embodiment of the present invention;
- Figure 3 shows a schematic perspective view of a circuit embodiment of a part of the storage system of Figure 2;
- Figure 4 shows a block diagram of a detail of the system of Figure 2;
- Figure 5 shows a block diagram of a storage system

according to a second embodiment of the present invention;

- Figure 6 shows a block diagram of a storage system according to a third embodiment of the present invention;
- Figure 7 shows a block diagram of a storage system according to a fourth embodiment of the present invention;
- Figure 8 shows a block diagram of a storage system according to a fifth embodiment of the present invention; and
- Figure 9 shows a block diagram of a storage system with modular memory density.

[0015] Figure 2 shows a storage system 20, according to a first embodiment of the present invention, for an electronic device 27. The storage system 20 comprises a controller 21, at least one embedded storage device 23, and at least one removable memory 24.

[0016] The embedded storage device 23 is connected to the electronic device 27 in a non-removable way. In particular, the embedded storage device 23 and the controller 21 are provided in a same chip 22, represented schematically in Figure 2 by a dashed rectangle. Inside the chip 22, the embedded storage device 23 and the controller 21 occupy two physically distinct regions. The chip 22 (see also Figure 3) can be housed in a package 25, for example of a ball-grid-array (BGA) type, and then soldered to a printed circuit 26.

[0017] The removable storage device 24, for example a memory card, is instead removable from the electronic device 27, and, in a known way, may be housed in a purposely provided slot 28. The slot 28 has, inside, appropriate electrical contacts designed to interface with corresponding electrical contacts carried by the removable storage device 24. Conductive tracks 29 provided on the printed circuit 26 connect the removable storage device 24, when housed in the slot 28, to the controller 21.

[0018] The storage system 20 further comprises connections 30, designed to connect the controller 21 to other parts (not shown) of the electronic device 27.

[0019] In greater detail, the controller 21 comprises a microprocessor 31, which supervises operation of the controller 21, and a single interface 33, which communicates with the microprocessor 31 through an internal data bus 32. It should be emphasized that the controller 21 is not equipped with a data-management function, and a single interface 33 operates for the embedded storage device 23 and the removable storage device 24.

[0020] According to one aspect of the invention, the embedded storage device 23 and the removable storage device 24 have a similar architecture, and in particular are both provided with an integrated data-management function.

[0021] In detail, the embedded storage device 23 and the removable storage device 24 comprise an interface 35, a data manager 36, and a memory 37, constituted by an addressable array of memory cells, for example of a NAND flash type (in this case the data manager 36 implements the FTL). In particular (Figure 4), the data manager 36 comprises a microprocessor 38 provided with an integrated memory 39 (either ROM or RAM), which contains a firmware (or integrated software) programmed so as to obtain management of the data stored in the memory 37.

[0022] The interface 35, the data manager 36, and the memory 37 of the embedded storage device 23 are integrated in the chip 22; in particular, they are provided within the region of the chip 22 dedicated to the embedded storage device 23.

[0023] The storage system 20 further comprises an external data bus 40, which connects the embedded storage device 23 and the removable storage device 24, in particular the respective interfaces 35, to the interface 33 of the controller 21.

[0024] It is stressed that positioning the data manager 36 within the embedded storage device 23 allows the controller 21 not to depend upon the physical structure of the embedded storage device 23 and removable storage device 24. In particular, the controller 21 only needs to know the communication protocol used on the external data bus 40, and it does not have to know the physical structure of the storage devices. Therefore, the interface 33 within the controller 21 is just one, irrespective of the type and number of storage devices to which the controller 21 can be connected. Basically, the external data bus 40 carries only generic input and output signals and control signals so that the controller 21 could be a generic input/output controller instead of a dedicated (or application-specific) controller.

[0025] The external data bus 40 connected to the interface 33 of the controller 21 and to the interfaces 35 of the embedded and removable storage devices 23, 24 can use any protocol of a known type, for example an MMC (MultiMediaCard™) interface protocol, or an SPI (Serial Peripheral Interface) interface protocol or a USB (Universal Serial Bus) interface protocol. In particular, any desired number of storage devices, whether embedded or removable, can be connected to the external data bus 40 according to the protocol used.

[0026] According to a second embodiment of the present invention, illustrated in Figure 5, the controller 21 and the embedded storage device 23 are formed in two distinct chips, illustrated by dashed rectangles designated, respectively, with the reference numbers 41 and 42. The chips 41 and 42 can be both soldered to the PCB 26 and connected by conductive tracks, or can for example be stacked within a same package, for example a BGA package, using the stacked-chip technique.

[0027] In particular, the division of the controller 21 and of the embedded storage device 23 into two distinct chips enables a greater modularity and flexibility of the storage system 20, since the storage density may be varied more easily. The disadvantage of a solution of this sort may be represented by the higher production costs.

[0028] Figures 6 to 8 show, respectively, a third, a

fourth and a fifth embodiment of the present invention, which differ simply as regards the implementation of the embedded storage device 23.

[0029] In detail, in the third embodiment (Figure 6) the embedded storage device 23 is formed in two distinct chips 44, 45, one of which, for example the chip 44, integrates the interface 35, and the other, in the example the chip 45, integrates both the data manager 36 and the memory 37. Advantageously, in order to reduce overall dimensions, the two chips 44, 45 can be housed in a same package with the stacked-chip technique.

[0030] According to the fourth embodiment (Figure 7), the embedded storage device 23 is once again made in two distinct chips 47, 48. Unlike the third embodiment, one of the chips, for example the chip 47, integrates the interface 35 and the data manager 36, while the other chip, in the example the chip 48, integrates the memory 37.

[0031] According to the fifth embodiment (Figure 8), the embedded storage device is formed in three distinct chips 50, 51, 52, which integrate the interface 35, the data manager 36, and the memory 37, respectively.

[0032] According to a further aspect of the present invention (see Figure 9), the storage system 20, implemented according to any of the embodiments described previously, may further comprise a plurality of additional storage devices 60, connected to the embedded storage device 23 and to the removable storage device 24 to increase their respective storage density, in a modular way.

[0033] In particular, the additional storage devices 60 are formed by a simple storage element (for example, an addressable array of cells of a NAND flash type) and are not provided with advanced data-management functions. The additional storage devices 60 are connected to the data manager 36 of the embedded storage device 23 and of the removable storage device 24 via a respective connection bus 62. In this case, the embedded storage device 23 and the removable storage device 24 have a master function, because they have an integrated data-management function, while the additional storage devices 60 have a slave function, since they are managed by the data manager 36 of the respective embedded storage device 23 or removable storage device 24. The additional memories (slaves) 60 that are provided for expanding the removable memory 24 must be in the same box as the removable memory 24, in a different chip or in a different package.

[0034] Depending on the embodiment of the storage system 20, the additional storage devices 60 connected to the embedded storage device 23 can be integrated within the chip 22 (as illustrated in Figure 9), or each additional storage device 60 may be provided in a distinct chip. In the latter case, each additional storage device 60 may have a distinct package and be connected outside the master storage device, or alternatively, the various chips of the additional storage devices 60 can be stacked on the chip of the master storage device inside a same package.

[0035] Thereby, the storage system 20 is extremely modular and any desired number of additional storage devices 60 can be connected to the embedded and removable storage devices 23, 24 so as to expand the corresponding storage density as desired.

[0036] The advantages of the present invention are evident from the above.

[0037] In particular, the described storage system enables a simplification of the controller of the storage system, which does not perform a data management function, thus can be a controller of a general-purpose type, and hence a low-cost one. Moreover, the controller has a single interface for all the different storage devices comprised in the storage system, which are all connected to the same data bus. In particular, in this way there is no need to replace the controller in the case where new types of storage devices are used.

[0038] The storage system is moreover optimized since each storage device, whether embedded or removable, has a data manager and an interface optimized for the specific use of the storage device.

[0039] Finally, the storage system is extremely modular and enables addition of any desired number of additional storage devices to increase the storage density of the system.

[0040] It is clear that modifications and variations may be made to what has been described and illustrated herein, without thereby departing from the scope of the present invention, as defined in the attached claims.

[0041] In particular, it is evident that the storage system is not tied to the use of a particular type of memory (flash memories of a NOR type, or any other type of electrically writeable and erasable non-volatile memory, could for example be used instead of flash memories of a NAND type) or of a particular production technique.

Claims

1. A storage system (20) for an electronic device (27), comprising an embedded storage device (23), a controller (21) configured for supervising writing and reading operations in said embedded storage device (23), and a data manager (36) configured for providing a high-level abstraction of the physical organization of the embedded storage device (23) through the definition of an own logic map, **characterized in that** said data manager (36) is external to said controller (21).

2. The storage system according to claim 1, wherein said embedded storage device (23) comprises said data manager (36), in particular said data manager (36) is integrated in said embedded storage device (23).

3. The storage system according to claim 2, wherein

said embedded storage device (23) further comprises an interface (35) and at least one memory (37), and wherein said data manager (36) is arranged between said interface (35) and said memory (37).

4. The storage system according to any one of the preceding claims, further comprising a plurality of distinct storage elements (60), connected to said data manager (36) via a data bus (62); and wherein said data manager (36) interacts with said storage elements (60) according to a master-slave modality.

5. The storage system according to any one of the preceding claims, wherein said data manager (36) comprises a microprocessor (38) having a memory (39) storing a data-management firmware.

6. The storage system according to any one of the preceding claims, further comprising at least one removable storage device (24) connected to said embedded storage device (23) and to said controller (21) through a data bus (40).

7. The storage system according to claim 6, wherein said removable memory (24) comprises an own data manager (36); said storage system further comprising a plurality of distinct storage elements (60), connected to said data manager (36) of said removable memory (24) via a respective data bus (62); and wherein said data manager (36) interacts with said storage elements (60) according to a master-slave modality.

8. The storage system according to any one of the preceding claims, wherein said controller (21) is formed in a first semiconductor material region, said embedded storage device (23) is formed in a second semiconductor material region distinct from said first semiconductor material region, and said data manager (36) is formed in a third semiconductor material region distinct from said first semiconductor material region.

9. The storage system according to claim 8, wherein said third semiconductor material region is arranged within said second semiconductor material region.

10. The storage system according to claim 8 or 9, wherein said first and third semiconductor material regions are formed in a same chip (22).

11. The storage system according to claim 8 or 9, wherein said first and third semiconductor material regions are provided in distinct chips (41, 42; 45; 47; 51).

12. The storage system according to claim 11, wherein said embedded storage device (23) further comprises an interface (35) and at least one memory (37); and wherein said interface (35), said memory (37), and said data manager (36) are provided in distinct chips (50, 51, 52).

13. The storage system according to claim 11, wherein said embedded storage device (23) further comprises an interface (35) and at least one memory (37); and wherein said interface (35) and said data manager (36) are formed in a first chip (47) , and said memory (37) formed in a second chip (48) distinct from the first chip (47).

14. The storage system according to claim 11, wherein said embedded storage device (23) further comprises an interface (35) and at least one memory (37); and wherein said memory (37) and said data manager (36) are formed in a first chip (45), and said interface (35) is provided in a second chip (44) distinct from the first chip (45).

15. The storage system according to any one of the preceding claims, wherein said controller (21) is of a general-purpose type.

16. An embedded storage device (23) for a storage system (20) for an electronic device (27), **characterized by** a data manager (36) configured for providing a high-level abstraction of the physical organization of the embedded storage device (23) through the definition of an own logic map.

17. The embedded storage device according to claim 16, further comprising an interface (35) and at least one memory (37), and wherein said data manager (36) is arranged between said interface (35) and said memory (37).

18. The storage device according to claim 17, further comprising a plurality of distinct storage elements (60), connected to said data manager (36) via a data bus (62); and wherein said data manager (36) interacts with said storage elements (60) according to a master-slave type modality.

19. The storage device according to any of claims 16-18, wherein said data manager (36) comprises a microprocessor (38) having a memory (39) storing a data-management firmware.

20. The embedded storage device according to any of claims 16-19, for a storage system (20) comprising a controller (21) configured for supervising writing and reading operations in said embedded storage device (23) and formed in a first semiconductor material region, wherein said embedded storage device (23) is formed in a second semiconductor material region distinct from said first semiconductor material region, and said data manager (36) is formed in a

third semiconductor material region distinct from said first semiconductor material region.

21. The embedded storage device according to claim 20, wherein said third semiconductor material region is arranged within said second semiconductor material region.

22. The embedded storage device according to claim 20 or 21, wherein said first and third semiconductor material regions are formed in a same chip (22).

23. The embedded storage device according to claim 20 or 21, wherein said first and third semiconductor material regions are provided in distinct chips (41, 42).

24. The embedded storage device according to claim 23, further comprising an interface (35) and at least one memory (37), and wherein said interface (35), said memory (37), and said data manager (36) are formed in distinct chips (50, 51, 52) .

25. The embedded storage device according to claim 23, further comprising an interface (35) and at least one memory (37), and wherein said interface (35) and said data manager (36) are formed in a first chip (47) and said memory (37) is formed in a second chip (48) distinct from the first chip (47).

26. The embedded storage device according to claim 23, further comprising an interface (35) and at least one memory (37), and wherein said memory (37) and said data manager (36) are provided in a first chip (45), and said interface (35) is provided in a second chip (44) distinct from the first chip (45).

27. An electronic device (27) incorporating a storage system (20) according to any one of claims 1-14.

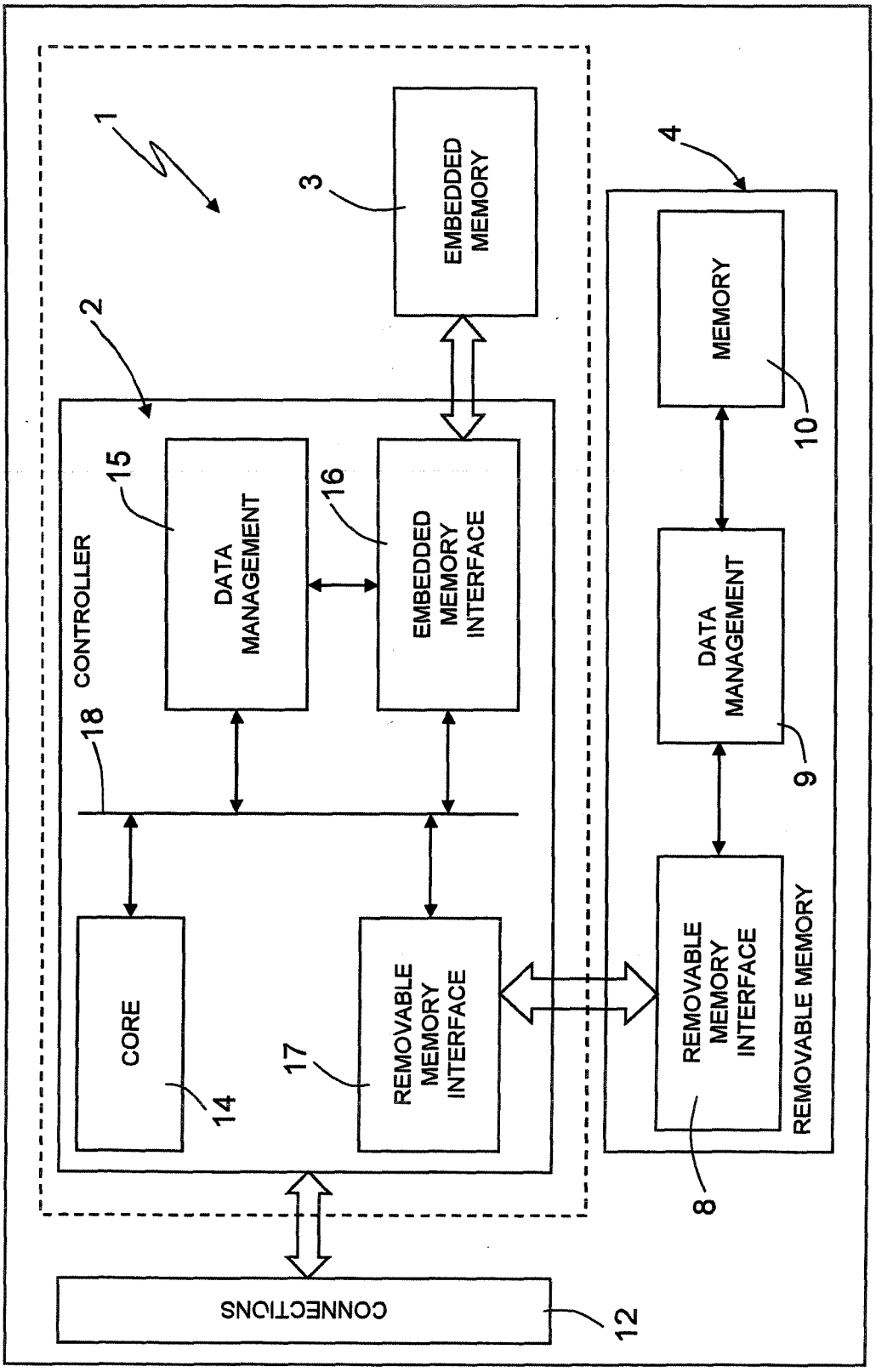
1
2
3
EMBEDDED MEMORY
4
MEMORY
10
CONTROLLER
15
DATA MANAGEMENT
16
EMBEDDED MEMORY INTERFACE
18
DATA MANAGEMENT
9
CORE
14
17
REMOVABLE MEMORY INTERFACE
REMOVABLE MEMORY INTERFACE
8
REMOVABLE MEMORY
CONNECTIONS
12

Fig.1

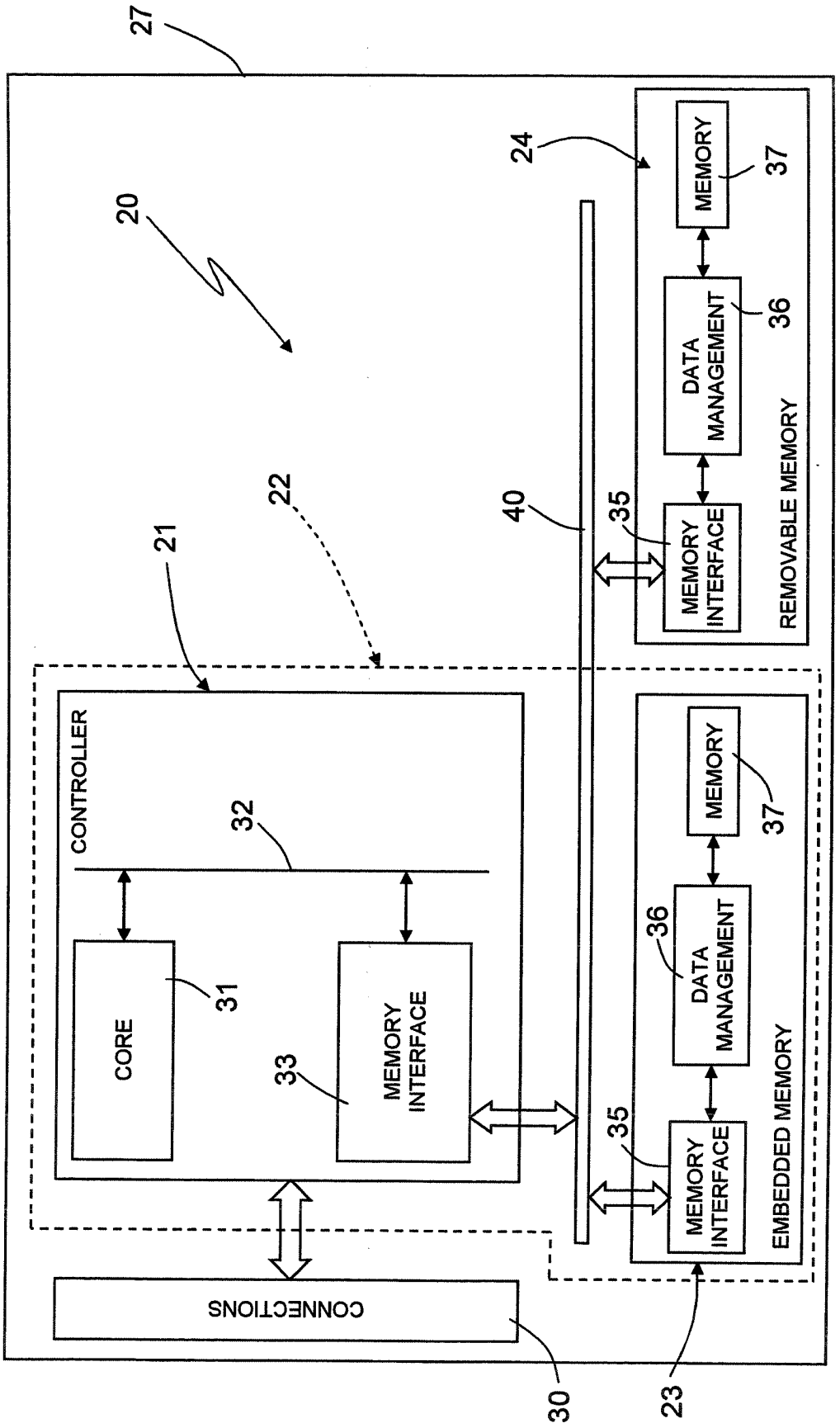
27
20
22
21
24
40
35
MEMORY
37
DATA MANAGEMENT
36
MEMORY INTERFACE
REMOVABLE MEMORY
CONTROLLER
32
CORE
31
MEMORY INTERFACE
33
MEMORY
37
DATA MANAGEMENT
36
MEMORY INTERFACE
35
EMBEDDED MEMORY
CONNECTIONS
30
23

Fig.2

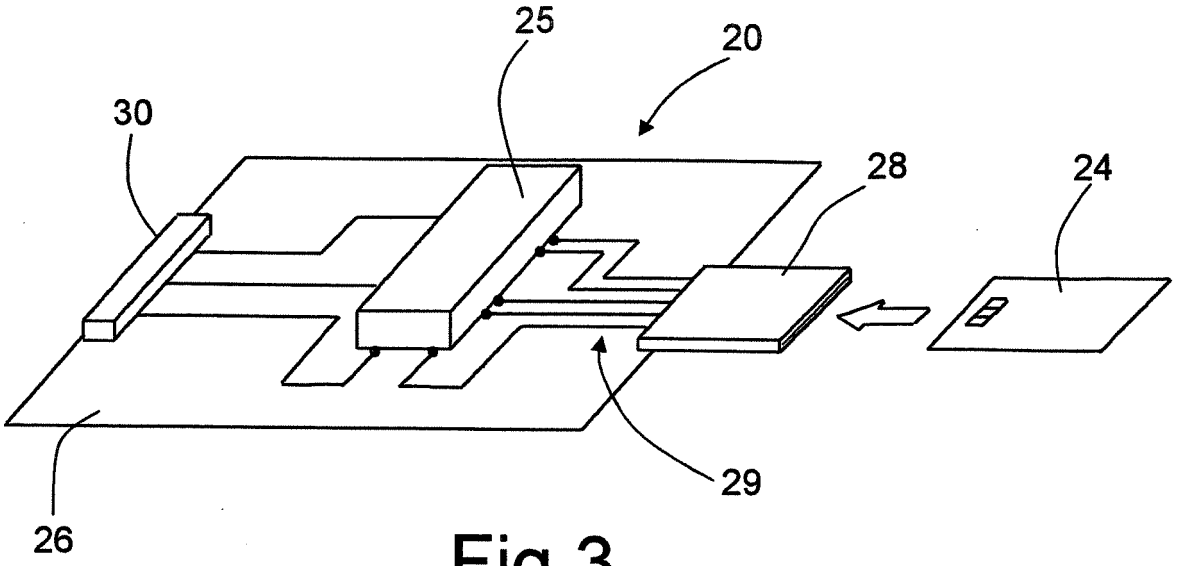

Fig.3

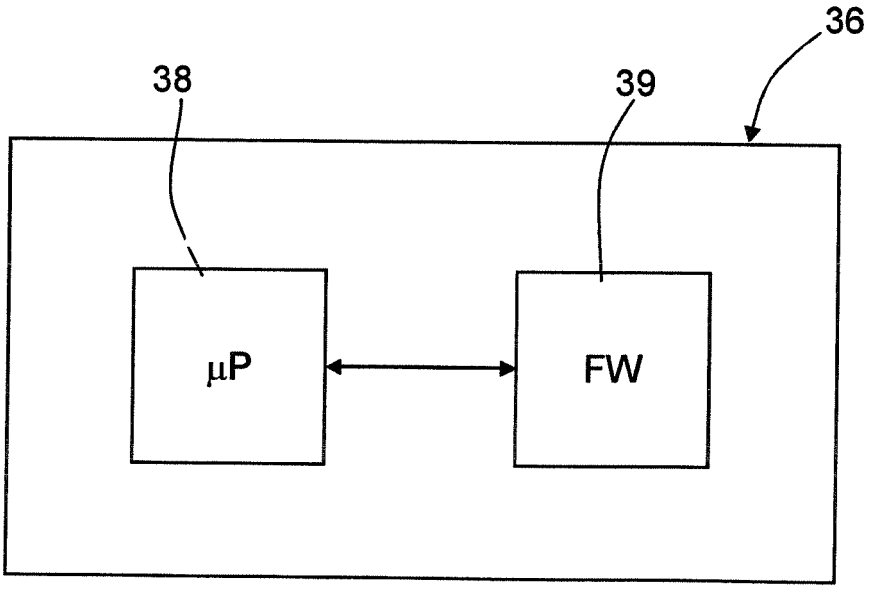

Fig.4

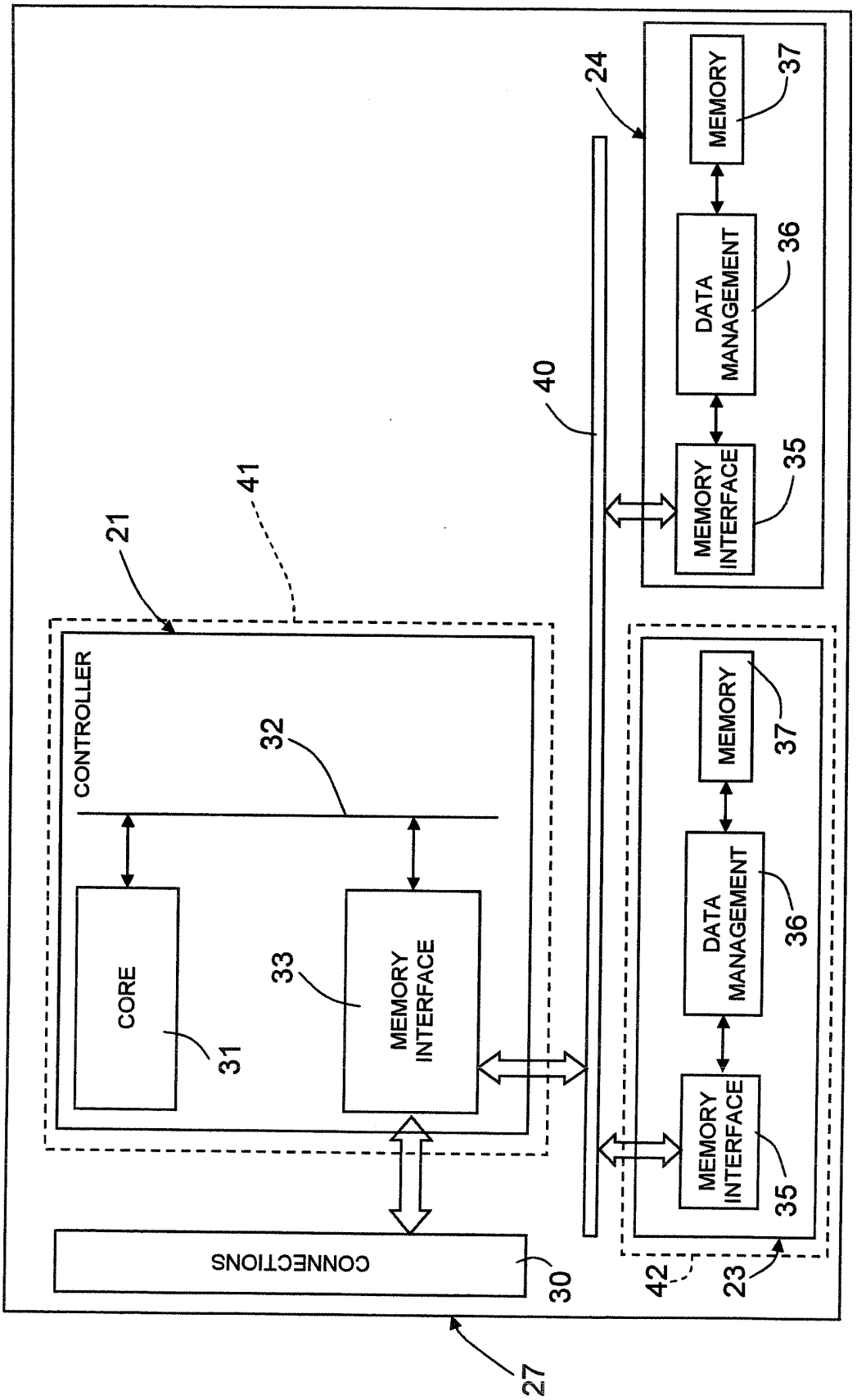
CONTROLLER
CORE
31
32
33
MEMORY INTERFACE
CONNECTIONS
30
21
41
27
24
40
MEMORY
37
DATA MANAGEMENT
36
MEMORY INTERFACE
35
42
23

Fig.5

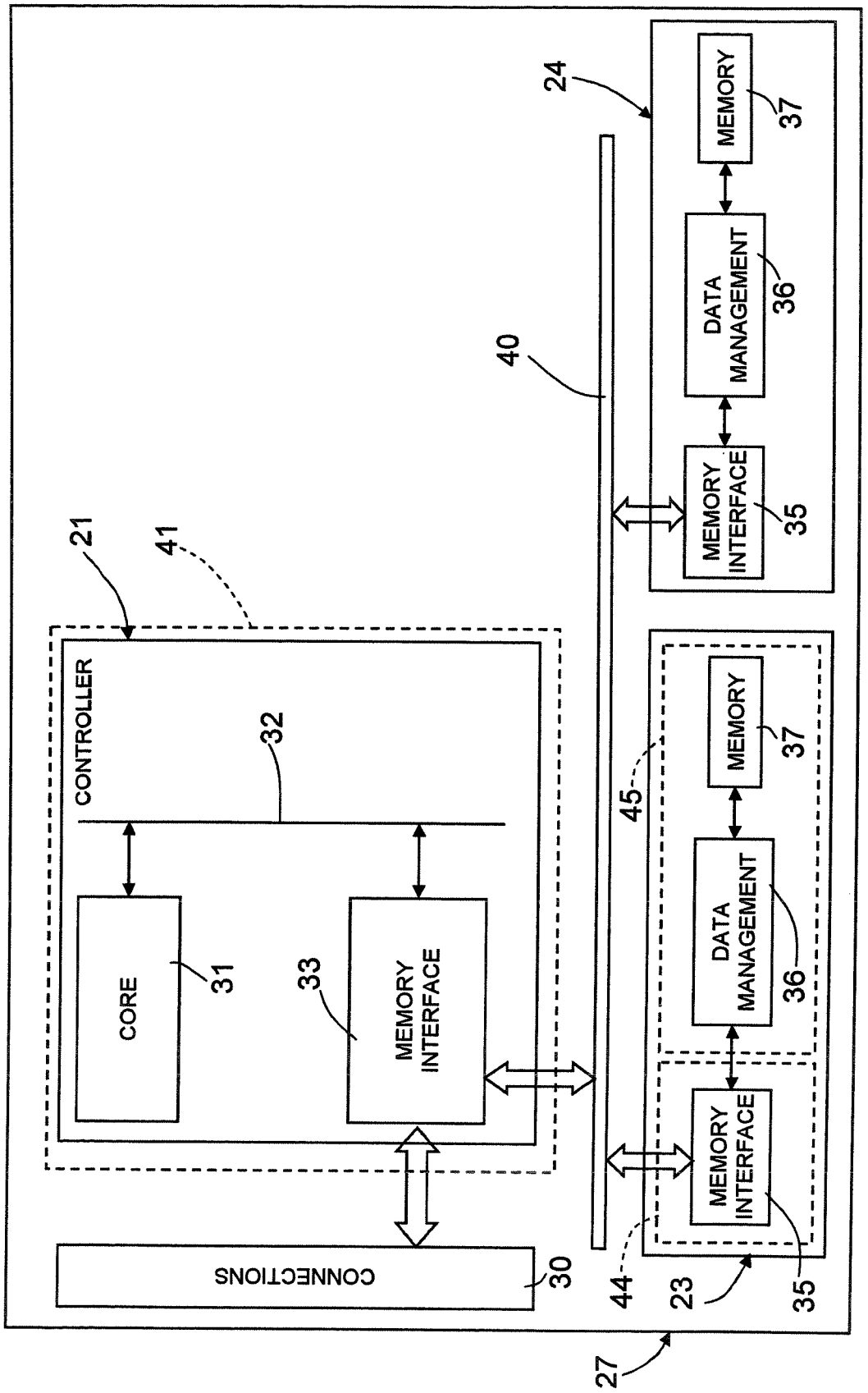
24
MEMORY
37
DATA MANAGEMENT
36
MEMORY INTERFACE
35
40
21
41
CONTROLLER
32
CORE
31
33
MEMORY INTERFACE
45
MEMORY
37
DATA MANAGEMENT
36
MEMORY INTERFACE
35
CONNECTIONS
30
44
23
27

Fig.6

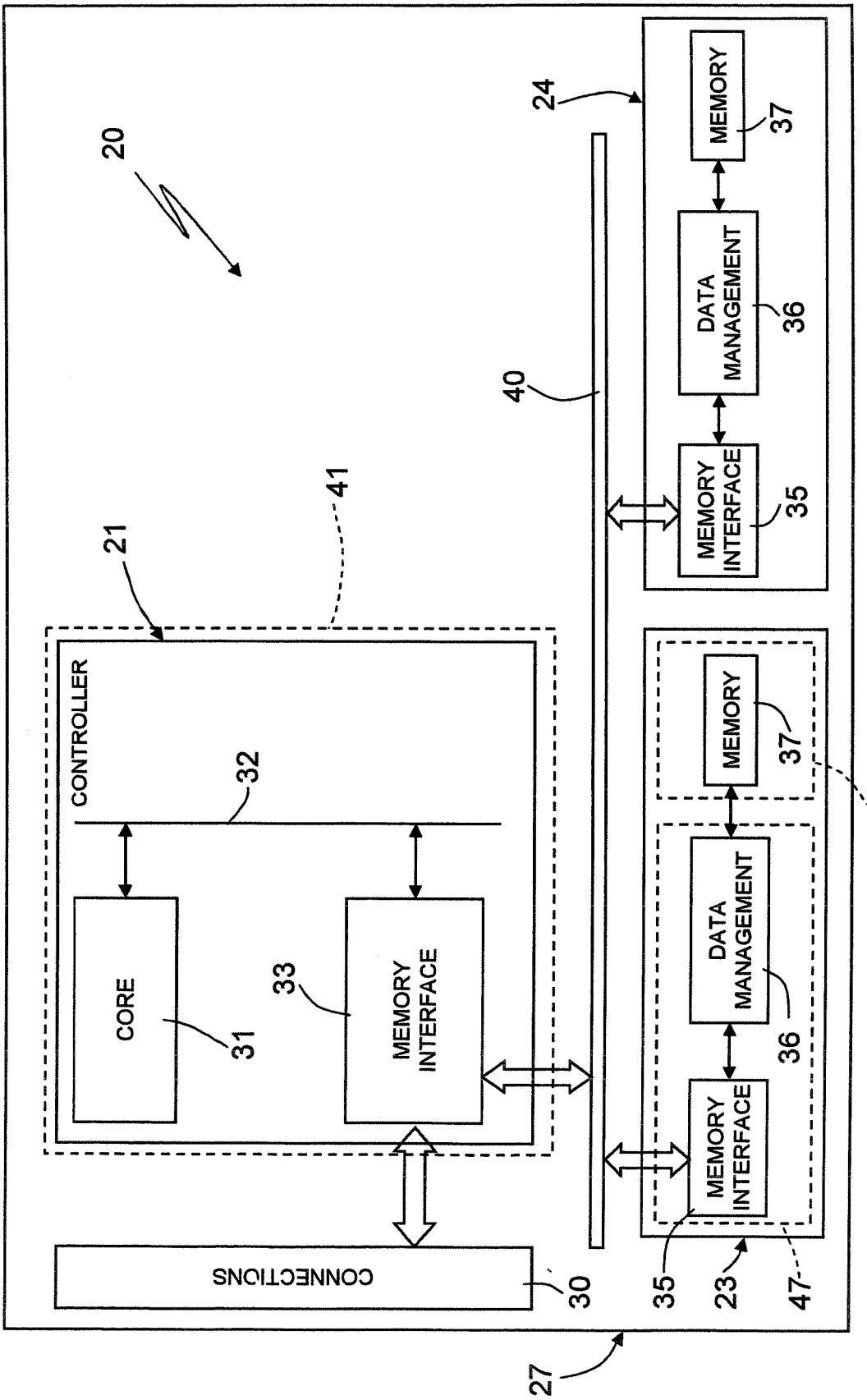
20
24
MEMORY
37
DATA MANAGEMENT
36
MEMORY INTERFACE
35
40
41
21
CONTROLLER
32
CORE
31
33
MEMORY INTERFACE
CONNECTIONS
30
27
MEMORY
37
48
DATA MANAGEMENT
36
MEMORY INTERFACE
35
23
47

Fig.7

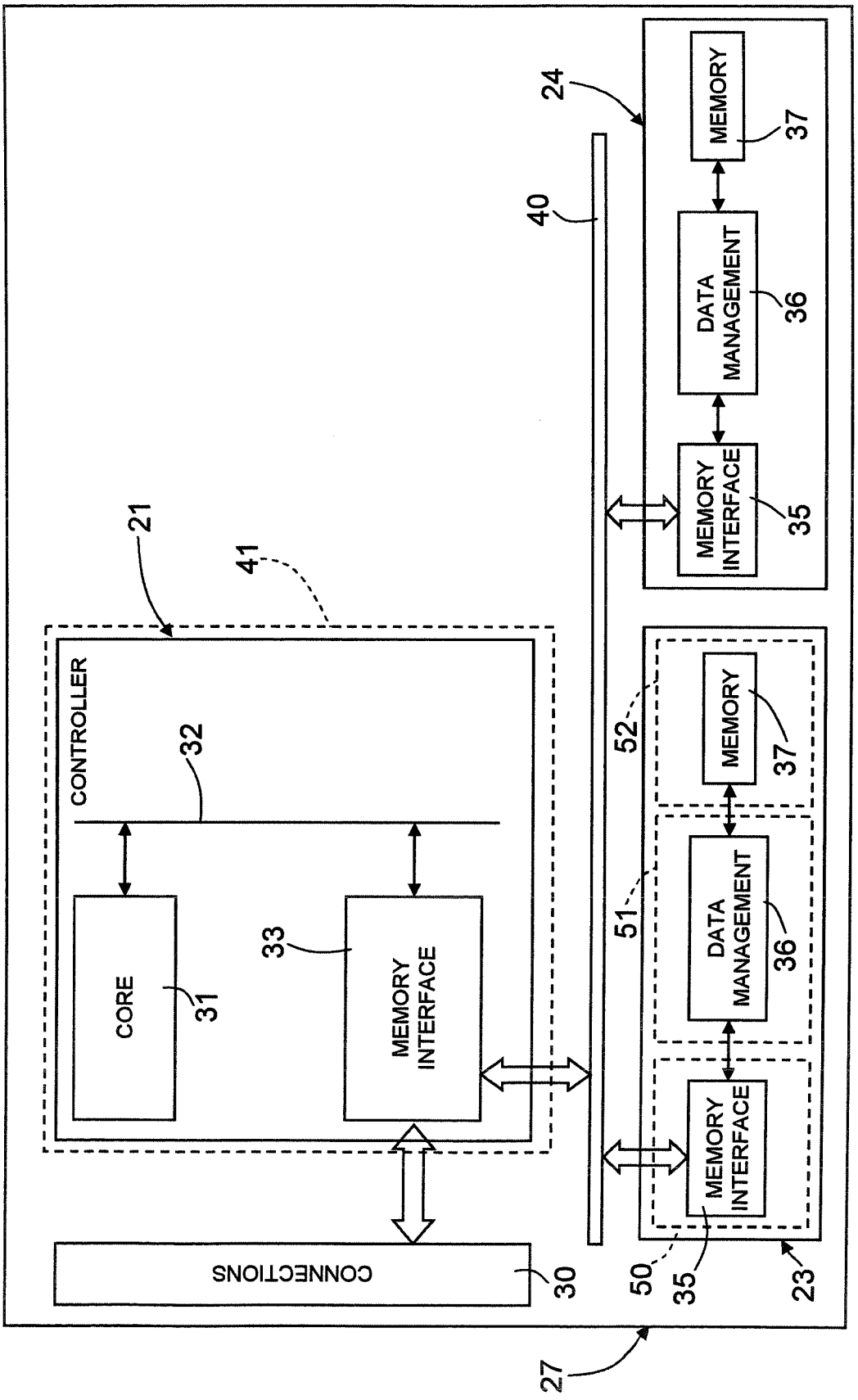
24
MEMORY
37
40
DATA MANAGEMENT
36
MEMORY INTERFACE
35
21
41
CONTROLLER
32
CORE
31
33
MEMORY INTERFACE
52
MEMORY
37
51
DATA MANAGEMENT
36
MEMORY INTERFACE
CONNECTIONS
30
50
35
23
27

Fig.8

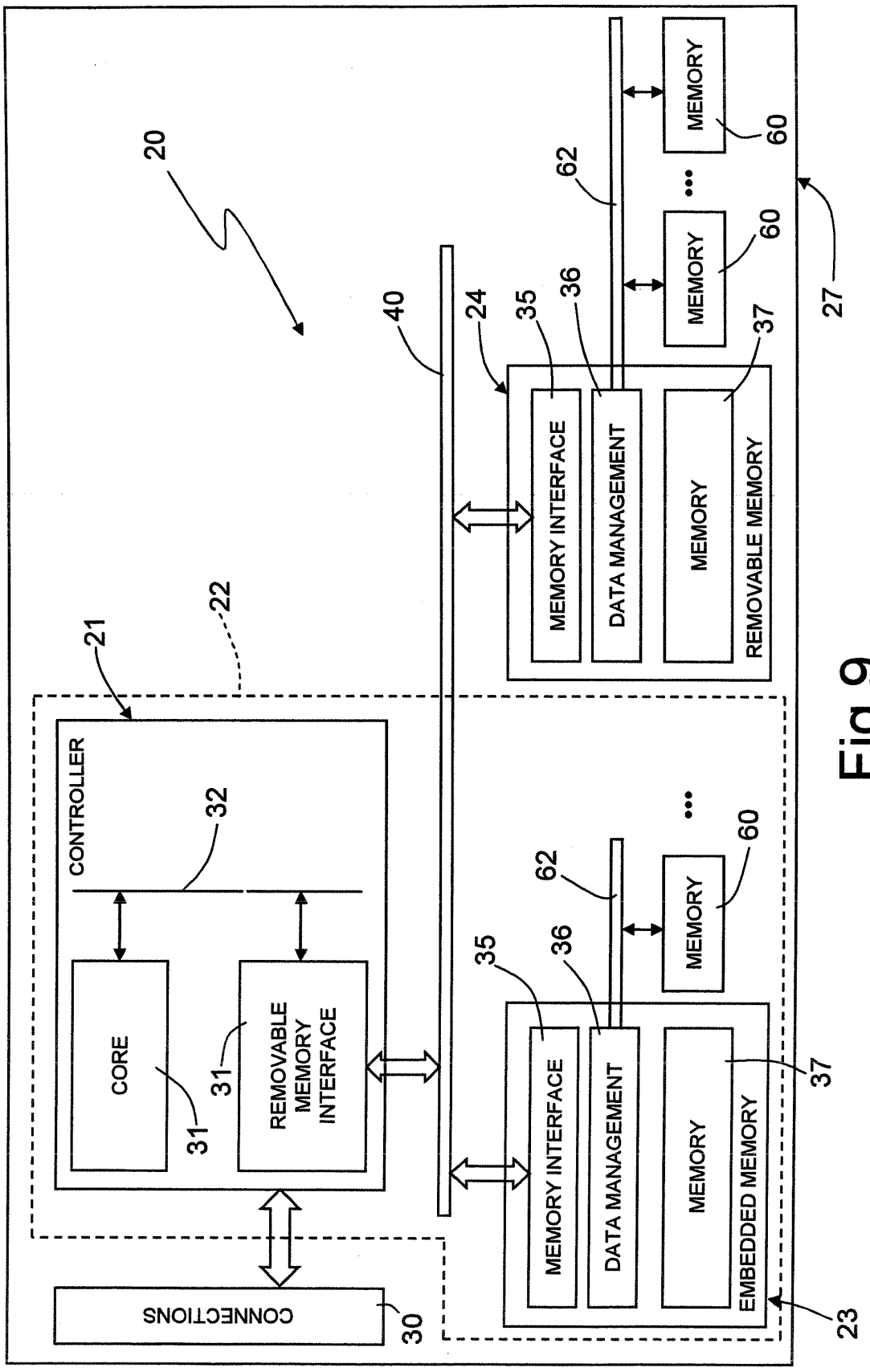
20
21
22
CONTROLLER
32
CORE
31
31
REMOVABLE MEMORY INTERFACE
CONNECTIONS
30
40
24
35
36
37
MEMORY INTERFACE
DATA MANAGEMENT
MEMORY
REMOVABLE MEMORY
62
60
MEMORY
27
EMBEDDED MEMORY
23

Fig.9

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 04 42 5643

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
X	WO 2004/040431 A (SANDISK CORPORATION; CHANG, ROBERT, C; QAWAMI, BAHMAN; SABET-SHARGHI,) 13 May 2004 (2004-05-13) * the whole document *	1-27	G06F3/06
X	EP 0 745 995 A (STMICROELECTRONICS S.R.L) 4 December 1996 (1996-12-04) * column 8, line 50 - column 9, line 24; figure 9 *	16-26	
X	EP 0 977 121 A (SONY CORPORATION) 2 February 2000 (2000-02-02) * the whole document *	1,16,27	
X	US 6 757 800 B1 (ESTAKHRI PETRO ET AL) 29 June 2004 (2004-06-29) * figure 6 *	1,16,27	
X	EP 0 613 151 A (KABUSHIKI KAISHA TOSHIBA; TOKYO SHIBAURA ELECTRIC CO) 31 August 1994 (1994-08-31) * the whole document *	1,6,7	
A	US 6 151 247 A (ESTAKHRI PETRO [US] ET AL) 21 November 2000 (2000-11-21) * column 5, lines 1-10 * * column 6, lines 1-7 *	1-27	TECHNICAL FIELDS SEARCHED (Int.Cl.7) G06F G11C
A	EP 0 973 097 A (TOKYO ELECTRON LIMITED) 19 January 2000 (2000-01-19) * the whole document *	1-27	

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
The Hague	25 May 2005	Czarik, D

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

EPO FORM 1503 03.82 (P04C01)

ANNEX TO THE EUROPEAN SEARCH REPORT ON EUROPEAN PATENT APPLICATION NO. EP 04 42 5643

This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report. The members are as contained in the European Patent Office EDP file on
The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

25-05-2005

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
WO 2004040431 A	13-05-2004	AU 2003270530 A1	25-05-2004
		WO 2004040431 A2	13-05-2004
EP 0745995 A	04-12-1996	EP 0745995 A1	04-12-1996
		DE 69520665 D1	17-05-2001
		DE 69520665 T2	30-08-2001
		JP 9106688 A	22-04-1997
		US 5748528 A	05-05-1998
EP 0977121 A	02-02-2000	JP 2000047932 A	18-02-2000
		EP 0977121 A2	02-02-2000
		KR 2000011959 A	25-02-2000
		RU 2243588 C2	27-12-2004
		US 2002124130 A1	05-09-2002
		US 6591328 B1	08-07-2003
US 6757800 B1	29-06-2004	US 6397314 B1	28-05-2002
		US 6202138 B1	13-03-2001
		US 6081878 A	27-06-2000
		US 5930815 A	27-07-1999
		US 5907856 A	25-05-1999
		US 5845313 A	01-12-1998
		US 6728851 B1	27-04-2004
		US 2004199714 A1	07-10-2004
		US 6801979 B1	05-10-2004
		US 6172906 B1	09-01-2001
		AU 2975099 A	15-09-1999
		EP 0983550 A2	08-03-2000
		JP 2000510634 T	15-08-2000
		JP 2004342126 A	02-12-2004
		WO 9944113 A2	02-09-1999
		AU 1517799 A	27-04-1999
		EP 1029278 A1	23-08-2000
		WO 9918509 A1	15-04-1999
		AU 6873898 A	22-10-1998
		EP 0980551 A1	23-02-2000
		JP 2002508862 T	19-03-2002
		WO 9844420 A1	08-10-1998
		US 5953737 A	14-09-1999
		US 6128695 A	03-10-2000
		US 6587382 B1	01-07-2003
		US 6145051 A	07-11-2000
		US 6122195 A	19-09-2000
		US 6223308 B1	24-04-2001
		US 6151247 A	21-11-2000
		US 6411546 B1	25-06-2002

EPO FORM P0459

For more details about this annex : see Official Journal of the European Patent Office, No. 12/82

ANNEX TO THE EUROPEAN SEARCH REPORT ON EUROPEAN PATENT APPLICATION NO. EP 04 42 5643

This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report. The members are as contained in the European Patent Office EDP file on
The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

25-05-2005

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 6757800 B1		US 2005055497 A1	10-03-2005
		US 2001029564 A1	11-10-2001
		US 5838614 A	17-11-1998
		US 6125435 A	26-09-2000
		US 5924113 A	13-07-1999
		US 6115785 A	05-09-2000
		US 6230234 B1	08-05-2001
		US 2004117586 A1	17-06-2004
EP 0613151 A	31-08-1994	JP 6250799 A	09-09-1994
		JP 2530102 B2	04-09-1996
		JP 7078056 A	20-03-1995
		EP 0613151 A2	31-08-1994
		US 5812814 A	22-09-1998
US 6151247 A	21-11-2000	US 6122195 A	19-09-2000
		US 6034897 A	07-03-2000
		US 6145051 A	07-11-2000
		US 5907856 A	25-05-1999
		US 6587382 B1	01-07-2003
		US 6411546 B1	25-06-2002
		AU 5474100 A	02-01-2001
		EP 1410399 A1	21-04-2004
		WO 0077791 A1	21-12-2000
		AU 4061700 A	23-10-2000
		EP 1228510 A1	07-08-2002
		WO 0060605 A1	12-10-2000
		US 6141249 A	31-10-2000
		US 6134151 A	17-10-2000
		US 6262918 B1	17-07-2001
		US 2005055497 A1	10-03-2005
		AU 6873898 A	22-10-1998
		EP 0980551 A1	23-02-2000
		JP 2002508862 T	19-03-2002
		US 6081878 A	27-06-2000
		US 6757800 B1	29-06-2004
		US 6801979 B1	05-10-2004
		WO 9844420 A1	08-10-1998
		US 5953737 A	14-09-1999
		US 6728851 B1	27-04-2004
		US 6128695 A	03-10-2000
		US 6202138 B1	13-03-2001
		US 6223308 B1	24-04-2001
		US 6172906 B1	09-01-2001
		US 6397314 B1	28-05-2002
		US 2004199714 A1	07-10-2004

EPO FORM P0459

For more details about this annex : see Official Journal of the European Patent Office, No. 12/82

ANNEX TO THE EUROPEAN SEARCH REPORT ON EUROPEAN PATENT APPLICATION NO. EP 04 42 5643

This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report. The members are as contained in the European Patent Office EDP file on
The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

25-05-2005

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 6151247 A		US 2001029564 A1	11-10-2001
		US 5838614 A	17-11-1998
		US 5930815 A	27-07-1999
		US 6125435 A	26-09-2000
EP 0973097 A	19-01-2000	EP 0973097 A1	19-01-2000
		US 6477632 B1	05-11-2002
		WO 9930239 A1	17-06-1999
		TW 400476 B	01-08-2000

EPO FORM P0459

For more details about this annex : see Official Journal of the European Patent Office, No. 12/82