(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 1 653 473 A2

(12) EUROPEAN PATENT APPLICATION

(43) Date of publication:
03.05.2006 Bulletin 2006/18

(51) Int Cl.:
G11C 11/22 *(2006.01)*

(21) Application number: **05255059.7**

(22) Date of filing: **16.08.2005**

(84) Designated Contracting States:
AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HU IE IS IT LI LT LU LV MC NL PL PT RO SE SI SK TR
Designated Extension States:
AL BA HR MK YU

(30) Priority: **02.11.2004 KR 2004088163**

(71) Applicant: **Samsung Electronics Co., Ltd.**
Suwon-si, Gyeonggi-Do (KR)

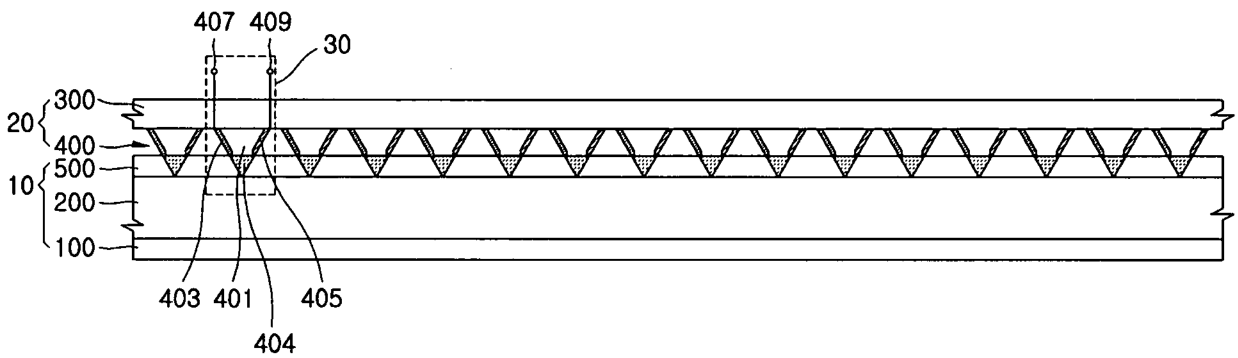
(72) Inventors:
- **Hong, Seung-bum**
  dong
  Bundang-gu, Seongnam-si
  Gyeonngi-do (KR)
- **Ko, Hyoung-soo**
  Seoul (KR)
- **Jung, Ju-hwan**
  Seocho-gu
  Seoul (KR)
- **Park, Hong-sik**
  Songpa-gu
  Seoul (KR)

(74) Representative: **Greene, Simon Kenneth**
Elkington and Fife LLP,
Prospect House,
8 Pembroke Road
Sevenoaks,
Kent TN13 1XR (GB)

(54) Resistive memory device having array of probes and method of manufacturing the resistive memory device

(57) Provided are a resistive memory device having a probe array and a method of manufacturing the resistive memory device. The resistive memory device includes a memory part (10) having a bottom electrode (100) and a ferroelectric layer (200) sequentially formed on a first substrate; a probe part (20) having an array of resistive probes (400) arranged on a second substrate (300), with the tips of the resistive probes facing the ferroelectric layer (200) such that they can write and read data on the ferroelectric layer; and a binding layer (500) which grabs and fixes the resistive probes on or above the ferroelectric layer. The method of manufacturing the resistive memory device includes forming a bottom electrode and a ferroelectric layer sequentially on a first substrate; forming an array of resistive probes for writing and reading data on a second substrate; and wafer level bonding the first substrate to the second substrate using a binding layer such that tips of the resistive probes face the surface of the ferroelectric layer.

FIG. 1



EP 1 653 473 A2

Description

BACKGROUND OF THE INVENTION

[0001] The present invention relates to a memory device and a method of manufacturing the memory device, and more particularly, to a resistive memory device having a multi probe array and a method of manufacturing the resistive memory device.

[0002] The growing popularity of portable electronic products, such as portable communication terminals and digital cameras, demands ever more highly integrated memory devices and high capacity recording devices. Such memory devices in portable electronic products need high density writing and reading and good shock and wear resistance.

[0003] However, conventional devices in the form of hard disks cannot easily be made small, and non-volatile memory devices such as FeRAM devices cannot be highly integrated. Thus, developments of new memory devices, such as MRAM devices, are suggested.

[0004] Recording devices have been tried using a technique of detecting charge distribution on the surface of a recording layer by scanning probes. It is expected that these recording or memory devices using the probes can write data at a higher density than FeRAM or similar devices. However, the structures of the scanning probes make these recording devices relatively weak against shock and wear

SUMMARY OF THE INVENTION

[0005] According to an aspect of the present invention, there is provided a resistive memory device in which a ferroelectric layer is used as a memory layer, and resistive probes face the memory layer and write and read data on the memory layer. The resistive memory device comprises: a memory part having a bottom electrode and a ferroelectric layer sequentially formed on a first substrate; a probe part having an array of resistive probes arranged on a second substrate, with the tips of the resistive probes facing the ferroelectric layer such that they can write and read data on the ferroelectric layer; and a binding layer which grabs and fixes the resistive probes on or above the ferroelectric layer.

[0006] According to another aspect of the present invention, there is provided a method of manufacturing a resistive memory device, comprising: forming a bottom electrode and a ferroelectric layer sequentially on a first substrate; forming an array of resistive probes for writing and reading data, on a second substrate; and wafer level bonding the first substrate to the second substrate using a binding layer such that the tips of the resistive probes face the surface of the ferroelectric layer.

[0007] Each of the resistive probes may comprise a resistive region at the tip, the resistance of which changes according to the direction of remanent polarization in a domain of the ferroelectric layer corresponding to the tip; and a first electrode region and a second electrode region, which are separated from each other on inclined surfaces of the probe and have the resistive region interposed therebetween, the first and the second electrode regions being used to detect the resistance of the resistive region when reading data.

[0008] For example, each of the resistive probes may have a body in the shape of a cone or a polygonal cone, containing silicon doped with a first impurity, and the first and the second electrode regions may comprise regions doped with a second impurity of the opposite conduction type to the first impurity, on the separated inclined surfaces. The resistive region may comprise a region doped with the second impurity at a lower concentration than the first and second electrode regions.

[0009] The probe part may further comprise interconnections which are respectively connected to the first and second electrode, are formed behind the probe array, and function as terminals for selecting one of the resistive probes and applying a current to the selected resistive probe. The probe part may further comprise bit lines which are respectively connected to the first and second electrodes and formed behind the probe array; and selection transistors which control the application of a current to the bit lines.

[0010] In the above method, forming the resistive probe array may comprises:

> forming a silicon layer doped with a first impurity on the second substrate;
> ion-implanting a second impurity, which has the opposite conduction type to the first impurity, into at least two adjacent portions in the silicon layer to form regions of the second impurity; diffusing the ion-implanted second impurity from the regions of the second impurity to form a diffusion region of the second impurity between the regions of the second impurity, the diffusion region containing a lower concentration of the second impurity than the regions of the second impurity; forming tip masks covering the diffusion region; and isotropically etching portions of the silicon layer which are exposed through the tip masks, to form the resistive probes.

[0011] In this case, each of the resistive probe may be formed by isotropic etching such that its tip is positioned at the diffusion region of the second impurity and the first and the second electrode regions are respectively positioned at the regions of the second impurity.

[0012] The bonding the first substrate to the second substrate may comprise forming a binding layer comprising a polymer layer on the ferroelectric layer; penetrating the tips of the resistive probes into the polymer layer; and curing the polymer layer to grab and fix the resistive probes.

[0013] The present invention provides a memory device which can write and read data at high density while possessing the shock and wear resistance needed for the environment of portable electronic products, and a method of manufacturing the memory device.

BRIEF DESCRIPTION OF THE DRAWINGS

[0014] The above and other features and advantages of the present invention will become more apparent by describing in detail exemplary embodiments thereof with reference to the attached drawings in which:

FIG. 1 is a schematic cross-sectional view of a memory device according to an embodiment of the present invention;
FIGS. 2 through 4 are views for explaining the structure and operation of a memory cell in a resistive memory device according to an embodiment of the present invention;
FIG. 5 through 14 are schematic plan views for explaining the process of forming an array of probes used in a resistive memory device according to an embodiment of the present invention;
FIG. 15 through 18 are schematic cross-sectional views for explaining the process of forming an array of probes used in a resistive memory device according to an embodiment of the present invention; and
FIG. 19 is a schematic view for explaining the process of wafer level bonding to form a resistive memory device according to an embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

[0015] Hereinafter, exemplary embodiments of the present invention will be described in more detail with reference to the attached drawings. However, these embodiments may be changed in form and are not intended to limit the scope of the invention. It should be understood that these embodiments are given to fully illustrate of the present invention to those of ordinary skill in the art.

[0016] In an embodiment of the present invention, there is provided a resistive memory device in which a ferroelectric layer is used as a memory layer, to which resistive probes are matched, and writing and reading on the memory layer is realized using the resistive probes.

[0017] Each of the resistive probes may comprise a resistive region at its tip and two electrode regions which are separated from each other, on inclined surfaces adjacent to the tip, having the resistive region interposed therebetween. For example, each of the resistive probes may have the shape of a cone, a tetragonal cone, or a polygonal cone, with a pointed tip, and may comprise the two electrode regions which are separated from each other on the inclined surfaces of the probe body and doped with impurity, and have the resistive region interposed therebetween. In this case, the probe body may be doped with a first impurity, and the electrode regions doped with a second impurity of the opposite conduction type.

[0018] The resistive region at the tip between the two electrode regions may comprise an impurity region doped with the second impurity at a lower concentration than the two electrode regions, or a region doped with the first impurity which has the opposite conduction type to the second impurity with which the electrode regions are doped. The charge distribution on the surface of the memory layer which faces the tip generates an electric field which in turn generates a depletion layer, and this affects the resistance of the resistive region.

[0019] The charge distribution on the surface of the memory layer is changed according to the direction of remanent polarization in the domain of a ferroelectric layer used as the memory layer. For example, the direction of the electric field which acts on the tip may be reversed according to the remanent polarization. Thus, according to the remanent polarization, the depletion layer may or may not form in the resistive region comprising the tip. The electrical resistance of the resistive region, i.e. the resistance between the two electrode regions, changes depending on whether or not the depletion layer is generated. A memory device can be realized by setting two states of the resistance values to "0" and "1". The remanent polarization state of the ferroelectric layer can be changed for each domain of the ferroelectric layer, and thus, the minimum memory region recorded on the ferroelectric layer can be greatly reduced according to the size of the domain. Thus, a very high writing density can be realized.

[0020] When a voltage of at least a coercive voltage of the remanent polarization of a domain, or an electric field of at least a coercive field, is applied to the tip of the probe, the direction of polarization in the domain of the ferroelectric layer corresponding to the tip can be reversed. Thus, data can be written on the ferroelectric layer using the probe.

[0021] In an embodiment of the present invention, an array of the probes are introduced in the ferroelectric layer, and thus, the ferroelectric layer and one probe can comprise a memory cell. Thus, writing and reading of data on the ferroelectric layer can be performed separately in each memory cell. An interconnection structure which comprises selection transistor devices for selecting a memory cell, bit lines and word lines, and interconnection contacts is substantially located over the memory cells, i.e., behind the probes, and thus, the data can be selectively written and read by selecting individual memory cells.

[0022] FIG. 1 is a schematic cross-sectional view of a memory device according to an embodiment of the present invention. Referring to FIG. 1, the memory device is formed by binding a memory part 10 to a probe part 20 using a binding layer 500.

[0023] The memory part 10 comprises a bottom electrode 100 formed on a wafer or a first substrate (not shown) and a ferroelectric layer 200 as a memory layer formed on the bottom electrode 100. The ferroelectric layer 200 has a vertical dielectric polarization direction, and may be made of a ferroelectric material such as PZT, BTO($BaTiO_3$), or similar. The bottom electrode 100 is formed to apply an electric field to the ferroelectric layer 200 or for grounding.

[0024] After the formation of the ferroelectric layer 200, the binding layer 500 for wafer level bonding on the ferroelectric layer 200 is formed. The binding layer 500 is introduced to grab and fix the probes on the ferroelectric layer 200 in a subsequent process. The ferroelectric layer 200 is formed such that the probes can relatively easily penetrate into it, and can then be cured in a relatively simple manner by a thermal process, UV light irradiation or similar, to grab and fix the probes on or above the ferroelectric layer 200. The binding layer 500 may be made of an adhesive resin or a polymer or polymer-like material.

[0025] The probe part 20 comprises an array of probes 400 formed on a wafer or a second substrate 300. Tips of probes 400 are bound to the memory part 10 to face the surface of the ferroelectric layer 200. The array of probes 400 corresponds to an array of memory cells 30. Each of the probes 400 has a body 401 in a pointed shape. The body 401 is made of a semiconductor material and may have the shape of a cone, a tetragonal cone, or a polygonal cone.

[0026] Each of the probes 400 can be composed of a resistive semiconductor probe. For example, each of the probes 400 comprises a resistive region 404 at the tip of the body 401, and two electrode regions 403 and 405 separated from each other on the left and right inclined surfaces with a resistive region 404 interposed therebetween. In this case, the body 401 may be made of a semiconductor material, for example, silicon. The two electrode regions 403 and 405 may be doped with an n-type or p-type impurity. In this case, the body 401 may be doped with an impurity of the opposite conduction type to the two electrode regions 403 and 405.

[0027] The tip of the body 401 between the two electrode regions 403 and 405 is assigned as the resistive region 404 and may have a higher resistance than the two electrode regions 403 and 405. For example, when the two electrode regions 403 and 405 are n^+-type doped, the resistive region 404 may be n^--type doped.
At this time, the body 401 may be p-type doped.

[0028] Then, the resulting probe part 20 is bound to the memory part 10 such that the tips of the probes 400 face the surface of the ferroelectric layer 200. The bonding is performed using wafer level bonding in which a wafer is bound to another wafer. During the wafer level bonding, the tips of the probes 400 penetrate into the binding layer 500 formed on the ferroelectric layer 200 of the memory part 10, and are thus stuck into the binding layer 500. Then, the polymer of the binding layer 500 is cured to fix the probes 400. Thus, the array of the probes 400 on the second substrate 300 are arranged such that the tips of the probes 400 face the ferroelectric layer 200.

[0029] The binding layer 500 may function as an insulating layer, and simultaneously shield the ferroelectric layer 200 from charged particles and atmospheric humidity. Since the ferroelectric layer 200 is formed on a separate wafer or substrate from the probe part 20, the ferroelectric layer 200 can be deposited at a higher temperature, and thus its properties can be improved. In general, when the ferroelectric layer 200 and the sensor part, for example, the probes 400, are formed simultaneously, doping regions of the probes 400 are likely to be adversely effected by the high temperature, and thus, the deposition temperature of the ferroelectric layer 200 is greatly limited. The embodiment of the present invention overcomes this temperature limitation for the deposition of the ferroelectric layer 200.

[0030] In the resistive memory device according to an embodiment of the present invention, the selection and operation of one of the memory cells 30 may be performed by applying a predetermined voltage to two terminals 407 and 409 which are electrically connected to the two electrode regions 403 and 405 of the probes 400, respectively. The bottom electrode 100 on the bottom surface of the ferroelectric layer 200 may be grounded. The two electrode regions 403 and 405 are electrically connected to the interconnections, such as bit lines, to apply the necessary voltages to the probes 400 to select the memory cells 30, write data to the memory cells 30, and read data from the memory cells 30. For example, an interconnection structure in which word lines and bit lines intersect to form a matrix (not shown) is buried in the second substrate 300 which is behind the array of the probes 400, as in the conventional memory devices, and the first terminal 407 is connected to one of the word lines and the second terminal 409 is connected to one of the bit lines, thus performing the selection of one of the memory cells 30, writing data to the memory cell 30, and reading data from the memory cell 30.

[0031] The basic operation concept of the resistive memory device according to an embodiment of the present invention will now be described.

[0032] FIG. 2 is a schematic view for explaining the cell structure in a resistive memory device according to an embodiment of the present invention. FIG. 3 is a schematic view for explaining writing data to a cell in a resistive memory device according to an embodiment of the present invention. FIG. 4 is a schematic view for explaining reading data from a cell in a resistive memory device according to an embodiment of the present invention.

[0033] Referring to FIG. 2, a probe 400 writes and reads data using the difference in an electric field according to dielectric polarization generated in a domain of a ferroelectric layer 200. For this, the probe 400 comprises a resistive region 404 at its tip, between a first electrode region 403 and a second electrode region 405. The resistive region 404 is fixed in a binding layer 500 of FIG. 1 and contacts or is very close to the surface of the ferroelectric layer 200. A protective layer 501 may be further formed on the ferroelectric layer 200.

[0034] A depletion layer may be generated in the resistive region 404 at the tip due to the effects of the electric field, which varies according to the dielectric polarization in the ferroelectric layer 200 facing the tip. As a result, the resistance between the first and the second electrode regions 403 and 405 is recognized as one of the two states "0" and "1.

[0035] Referring to FIG. 3, the data is written to a specific domain region of the ferroelectric layer 200 by generating a dielectric polarization in a specific direction in a portion of the ferroelectric layer 200 which faces the resistive region 404. For this, voltage of the same polarity are simultaneously applied to the first and second electrode regions 403 and 405. At this time, at least the voltage required to change the direction of the dielectric polarization, i.e., a coercive voltage (V_c), must be applied to the first and the second electrode regions 403 and 405. In this case, at least the electric field required to change the direction of the dielectric polarization, i.e., a coercive electric field (E_c), is generated between the grounded bottom electrode 100 and the tip of the probe 400. Thus, vertical dielectric polarization is generated in the domain region of the ferroelectric layer 200 facing the tip of the probe 400. Voltages for writing are applied to the first and the second electrode regions 403 and 405 through the two terminals 407 and 409, and according to the polarity of the applied voltage, the direction of polarization in a domain of the ferroelectric layer 200 is reversed.

[0036] Referring to FIG. 4, when different voltages are applied to the two terminals 407 and 409, if the direction of alignment of the domain of the ferroelectric layer 200 is upward, the resistance of the resistive region 404 is relatively low, and thus, a relatively large current flows through the resistive region 404. In this case, for example, the resistive region 404 is n--type doped and the first and the second electrode regions 403 and 405 are n^+-type doped. On the other hand, if the direction of alignment of the domain is downward, a depletion layer is generated in the resistive region 404 due to the effects of the electric field according to the remanent polarization. Thus, the resistance of the resistive region 404 is high, and thus, a small current flows through the resistive region 404. Data of "0" and "1" can be read using the two current states, i.e., the higher current and the lower current.

[0037] Again, referring to FIG. 1, to select one of the memory cells 30 and apply a voltage to the probes 400 for selecting one of the memory cells 30 and writing and reading data on the memory cells 30, the interconnection structure may be formed in the second substrate 300 behind the array of probes 400. The interconnection structure may be constructed such that word lines intersect with bit lines to connect specific wires to the two terminals 407 and 409 of each of the probes 400. Alternatively, the interconnection structure may be constructed such that each of the word lines intersects two parallel bit lines, and a selection transistor is connected to the word line. The process of forming the probes 400 will be explained based on the example in which the interconnection structure accompanied by selection transistors is installed in the second substrate 300.

[0038] FIGS. 5 through 14 are schematic plan views for explaining the process of forming an array of probes in a resistive memory device according to an embodiment of the present invention. FIGS. 15 through 18 are schematic cross-sectional views for explaining the process of forming an array of probes in a resistive memory device according to an embodiment of the present invention.

[0039] Referring to FIG. 5, active regions 301 are assigned on a second substrate 300, which is a semiconductor substrate made of silicon (Si), using a device separation process from a method of forming transistors. Referring to FIG. 6, word lines 310 are formed to cross the active regions 301 using a process of forming transistor gates. The word lines 310 are made of a polycrystalline silicon or other suitable material. A gate oxide layer (not shown) may be formed between the active regions 301 and the word lines 310. Thus, selection transistors for selecting a probe 400 are formed.

[0040] Referring to FIG. 7, bit line plugs 321 are formed near the word lines 310 to be electrically connected to adjacent active regions 301. An insulating layer (not shown) is formed to cover the word lines 310, and the bit line plugs 321, which are conductive, are electrically connected to the active regions 301 through the insulating layer. Referring to FIG. 8, conductive bit lines 320 are formed to intersect the word lines 310. The bit lines 320 are electrically connected to the bit line plugs 321. The bit lines 320 and the word lines 310 intersect to form a matrix.

[0041] Referring to FIG. 9, conductive cell plugs 330 are formed to pass through the second substrate 300 in the vicinity of the bit lines 320 and the word lines 310 such that the cell plugs 330 are electrically connected to the active regions 301. The cell plugs 330 contact the active regions 301 through an insulating layer covering the bit lines 320 and the insulating layer covering the word lines 310. Thus, an interconnection structure is formed for selecting individual memory cells 30 and writing and reading data on the memory cells 30 (see FIG. 1).

[0042] Referring to FIG. 10, a silicon layer 350 is formed on the second substrate 300 which has the cell plugs 330 formed thereon. The silicon layer 350 may be formed by deposition. The silicon layer 350 may be doped with an impurity of the opposite conduction type to that of the two electrode regions 403 and 405 of the probes 400 (see FIG. 1). For example, the silicon layer 350 may be doped with a p-type impurity.

[0043] Referring to FIGS. 11 through 15, a mask 610 for ion implantation is formed on the silicon layer 350. The mask 610 exposes portions of the silicon layer 350 above the cell plugs 330. Impurity regions 640 are formed in the exposed portions of the silicon layer 350 by the ion implantation. The impurity may be n-type. As a result, the impurity regions 640 are electrically connected to the cell plugs 330.

[0044] Referring to FIGS. 12 and 16, the impurity is diffused from the impurity regions 640 to form impurity diffusion regions 641 having a lower concentration of the impurity than the impurity regions 640. The diffusion of the impurity is controlled such that the impurities diffused from adjacent impurity regions 640 meet in the middle and overlap each other, that is, the diffusion profile is controlled such that both the impurity diffusion regions 641 meet near the surface of the silicon layer 350 below the mask 610, and the silicon layer 350 is present below the overlapping impurity diffusion regions 641. In general, the diffusion rate of the impurity in portions adjacent to the surfaces of the impurity diffusion regions 641 is faster than below such portions. Thus, the diffusion profile of the impurity may be formed such that the surface of the silicon layer 350 has a convex form as illustrated in FIG. 16.

[0045] Referring to FIG. 13, tip masks 650 are used to etch the silicon layer 350 for forming the probes 400 (see FIG. 1). The tip masks 650, are hard masks, and are formed to cover the silicon layer 350 above portions between the cell plugs 330, i.e., to cover portions between the impurity regions 640. The tip masks 650 are formed to cover portions in which the probes 400 are to be formed.

[0046] Referring to FIGS. 14 and 17, the portions of the silicon layer 350 exposed through the tip masks 650 are isotropically etched to form the probes 400 with tips pointing upward. When the tip masks 650 are square, the probes 400 formed using isotropic etching will have the shape of tetragonal cones. The tips of the probes 400 are resistive regions 404, which correspond substantially to portions of the impurity diffusion regions 641 (see FIG. 16). The first and second electrode regions 403 and 405 which are formed to face to each other on the inclined surfaces of the probes 400 corresponds to portions of the impurity regions 640.

[0047] The isotropic etching may be performed until a layer below the silicon layer 350 is exposed. Alternatively, a portion of the silicon layer 350 may be allowed to remain after the isotropic etching. When some of the silicon layer 350 remains, the first and the second electrode regions 403 and 405 are respectively electrically connected to the cell plugs 330 through the impurity regions 640 which remain below the first and the second electrode regions 403 and 405.

[0048] As illustrated in FIG. 14, the first electrode regions 403 are electrically connected to the active regions 301 through the cell plugs 330 to contact the selection transistors. Thus, the first electrode region 403 are electrically connected to the bit lines 320 through the bit line plugs 321 according to control or switching of the word lines 310 by the selection transistors. The second electrode regions 405 contact the other selection transistors through the other cell plugs 330 to be electrically connected to the other adjacent bit lines 320 through the other bit line plugs 321 according to the control or switching by the same word lines 310. In such an interconnection structure, by selecting one of the word lines 310, a row of probes 400 connected to the word line 310 is selected. Then, a pair of bit lines 320 which are respectively connected to the first and the second electrode regions 403 and 405 select one of the probes 400 in the selected row. The bit lines 320 are used as two terminals for the probes 400, to apply voltages to the selected probe 400.

[0049] As explained above, the resistive memory device according to an embodiment of the present invention is formed by binding the second substrate 300 (see FIG. 1) having the array of probes 400 to the first substrate 100 having the ferroelectric layer 200.

[0050] FIG. 19 is a schematic view for explaining the process of wafer level bonding to form a resistive memory device according to an embodiment of the present invention.

[0051] Referring to FIG. 19, a probe part 20 having an array of probes 400 formed on a second substrate 300 is bound to a memory part 10 having a ferroelectric layer 200 formed on a first substrate (not shown) by wafer level bonding. During the wafer level bonding, the tips of the probes 400 penetrate a binding layer 500 comprising a layer of polymer or polymer-like material formed on the ferroelectric layer 200, such that the tips of the probes 400 contact or are adjacent to the surface of the ferroelectric layer 200. Then, the polymer layer of the binding layer 500 is cured to fix the probes 400 on or adjacent to the ferroelectric layer 200.

[0052] As described above, the present invention provides a memory device comprising resistive probes and a memory layer, which is a ferroelectric layer. The memory device has no mechanical parts, and thus has the high impact and abrasion resistance required for use in reliable portable electronic products.

[0053] Since the probe array is bound to the ferroelectric layer by wafer level bonding using the binding layer, the binding layer can efficiently shield the ferroelectric layer from charged particles and moisture. Furthermore, since the ferroelectric layer is deposited on a separate wafer, it can be deposited at a high temperature, thus improving its properties and reliability. The integration degree and writing density of the memory device depend on the density of probes in the probe array, and thus, the memory according to the present invention can guarantee a higher writing density than conventional FeRAM devices.

[0054] While the present invention has been particularly shown and described with reference to exemplary embodiments thereof, it will be understood by those of ordinary skill in the art that various changes in form and details may be made therein without departing from the scope of the present invention as defined by the following claims.

Claims

1. A resistive memory device comprising:

a memory part having a bottom electrode and a ferroelectric layer sequentially arranged on a first substrate;
a probe part having an array of resistive probes arranged on a second substrate, with the tips of the resistive probes facing the ferroelectric layer such that they can write and read data on the ferroelectric layer; and
a binding layer which holds and fixes the resistive probes on or above the ferroelectric layer.

2. The resistive memory device of claim 1, wherein each of the resistive probes comprises:

a resistive region at the tip, the resistance of which changes according to the direction of remanent polarization in a domain of the ferroelectric layer corresponding to the tip; and
a first electrode region and a second electrode region, which are separated from each other on inclined surfaces of the probe and have the resistive region interposed therebetween, the first and the second electrode regions being used to detect the resistance of the resistive region when reading data.

3. The resistive memory device of claim 2, wherein each of the resistive probes has a body in the shape of a cone or a polygonal cone, containing silicon doped with a first impurity, and
the first and the second electrode regions comprise regions doped with a second impurity of the opposite conduction type to the first impurity, on the separated inclined surfaces.

4. The resistive memory device of claim 3, wherein the resistive region comprises a region doped with the second impurity at a lower concentration than the first and second electrode regions.

5. The resistive memory device of any preceding claim, wherein the probe part further comprises: interconnections which are respectively connected to the first and second electrode, are formed behind the probe array, and function as terminals for selecting one of the resistive probes and applying a current to the selected resistive probe.

6. The resistive memory device of any preceding claim, wherein the probe part further comprises:

bit lines which are respectively connected to the first and second electrodes and formed behind the probe array; and
selection transistors which control the application of a current to the bit lines.

7. The resistive memory device of any preceding claim, wherein the binding layer comprises a polymer layer.

8. A resistive memory device according to claim 1:

wherein each of the resistive probes has a body in the shape of a cone or a polygonal cone, containing silicon doped with a first impurity, and comprises;
a resistive region at the tip, the resistance of which changes according to the direction of remanent polarization in a domain of the ferroelectric layer corresponding to the tip;
a first electrode region and a second electrode region, which are separated from each other on inclined surfaces of the body and have the resistive region interposed therebetween, the first and the second electrode regions being used to detect the resistance of the resistive region when reading data, and the resistive region comprising a region doped with a second impurity at a lower concentration than the first and second electrode regions;
bit lines which are respectively connected to the first and second electrodes, are formed behind the probe array, and function as terminals for selecting one of the resistive probes and applying a current to the selected resistive probe; and
selection transistors which control the application of a current to the bit lines.

9. A method of manufacturing a resistive memory device, comprising:

forming a bottom electrode and a ferroelectric layer sequentially on a first substrate;
forming an array of resistive probes for writing and reading data, on a second substrate; and
wafer level bonding the first substrate to the second substrate using a binding layer such that the tips of the resistive probes face the surface of the ferroelectric layer.

10. The method of claim 9, wherein forming the resistive probe array comprises:

forming a silicon layer doped with a first impurity on the second substrate; ion-implanting a second impurity, which has the opposite conduction type to the first impurity, into at least two adjacent portions in the silicon layer to form regions of the second impurity;
diffusing the ion-implanted second impurity from the regions of the second impurity to form a diffusion region of the second impurity between the regions of the second impurity, the diffusion region containing a lower concentration of the second impurity than the regions of the second impurity;

forming tip masks covering the diffusion region; and

isotropically etching portions of the silicon layer which are exposed through the tip masks, to form the resistive probes.

11. The method of claim 10, wherein each of the resistive probe is formed by isotropic etching such that its tip is positioned at the diffusion region of the second impurity and the first and the second electrode regions are respectively positioned at the regions of the second impurity.

12. The method of claim 10 or 11, further comprising, prior to forming the silicon layer:

forming interconnections which are respectively connected to the first and second electrodes, on the second substrate, the interconnections functioning as terminals for selecting one of the resistive probes and applying a current to the selected probe.

13. The method of claim 10, 11 or 12, further comprising, prior to forming the silicon layer:

forming bit lines which are respectively connected to the first and second electrodes, on the second substrate; and

forming selection transistors which control the application of current to the bit lines, below the bit lines.

14. The method of claim 9, 10, 11, 12 or 13, wherein bonding the first substrate to the second substrate comprises:

forming a binding layer comprising a polymer layer on the ferroelectric layer;

penetrating the tips of the resistive probes into the polymer layer; and

curing the polymer layer to grab and fix the resistive probes.

15. The method of claim 14, wherein the tips of the resistive probes penetrate into the polymer layer such that they contact or are adjacent to the surface of the ferroelectric layer.

FIG. 1

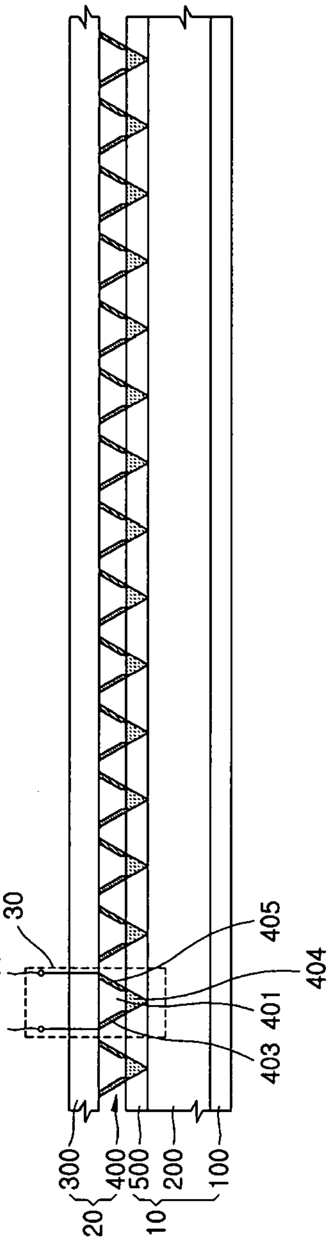


FIG. 2

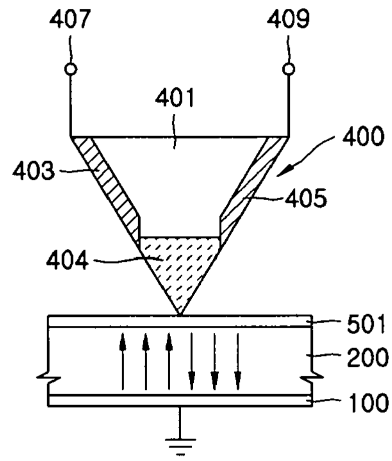

407
409
401
400
403
405
404
501
200
100

FIG. 3

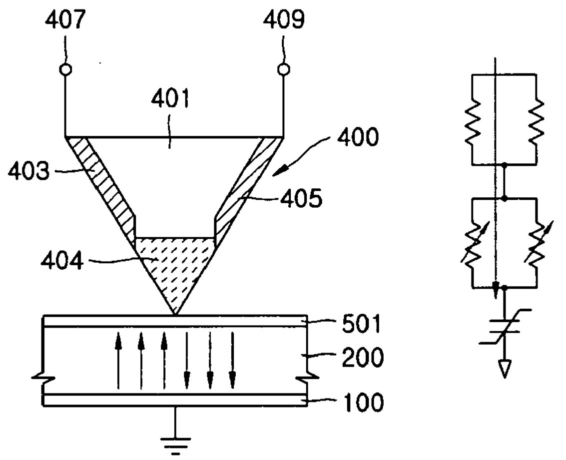

407
409
401
400
403
405
404
501
200
100

FIG. 4

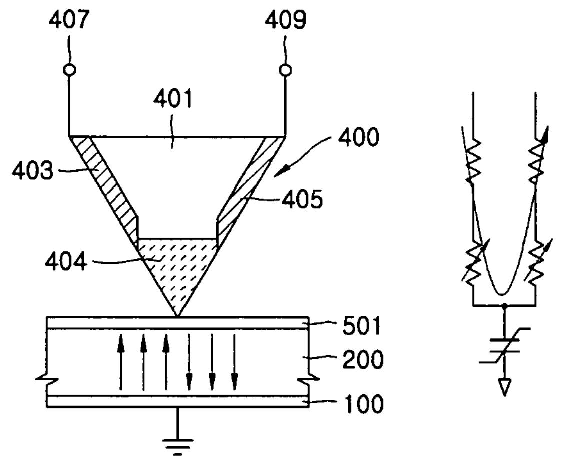


FIG. 5

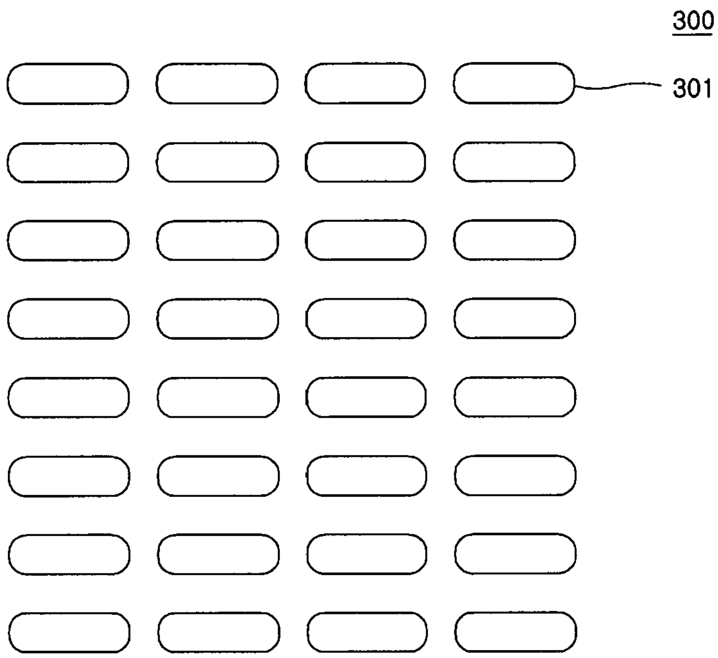


FIG. 6

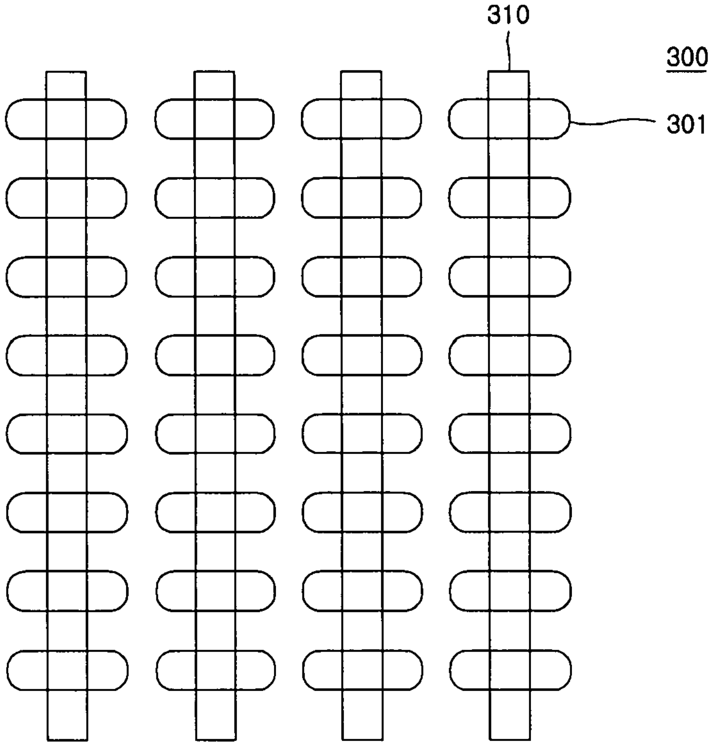


FIG. 7

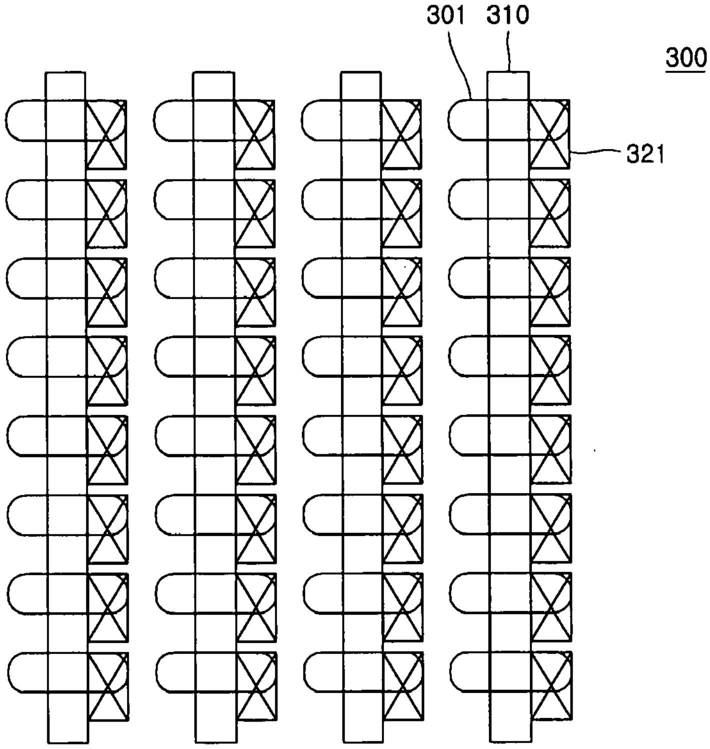


FIG. 8

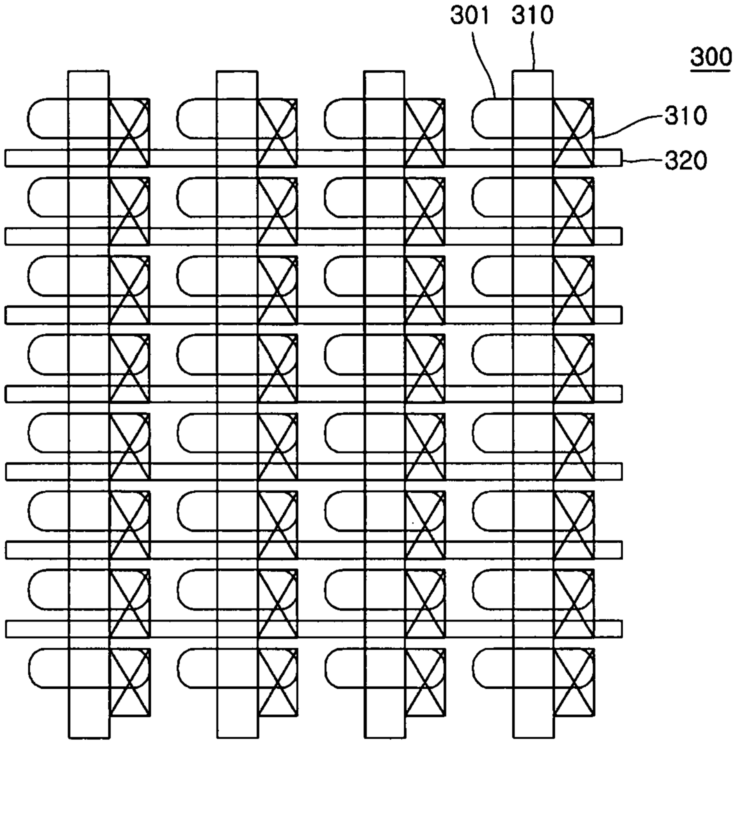


FIG. 9

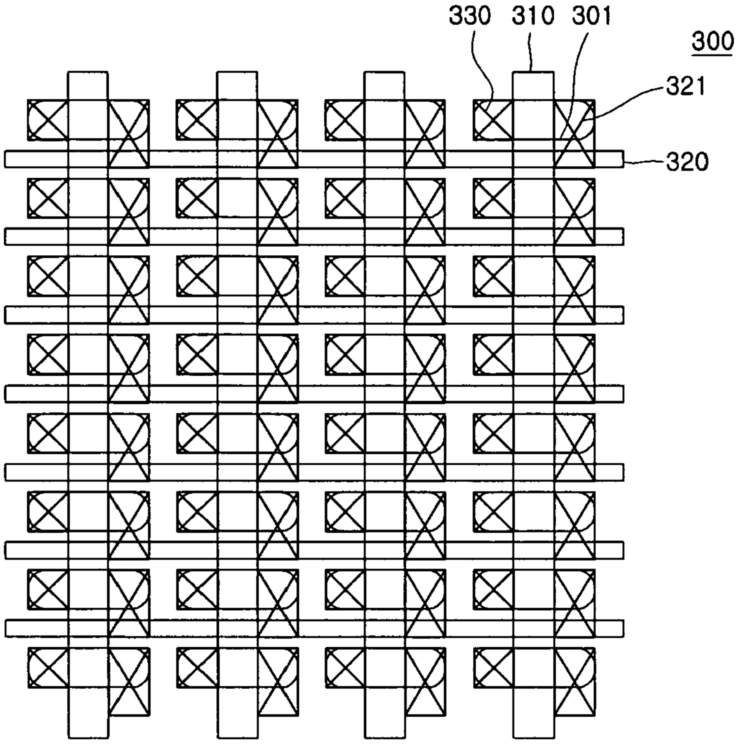


FIG. 10

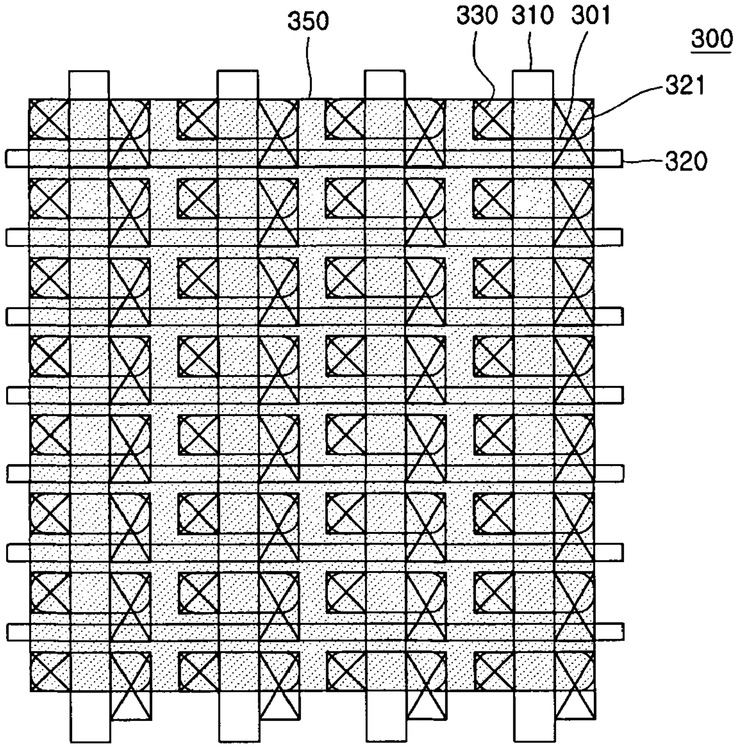


FIG. 11

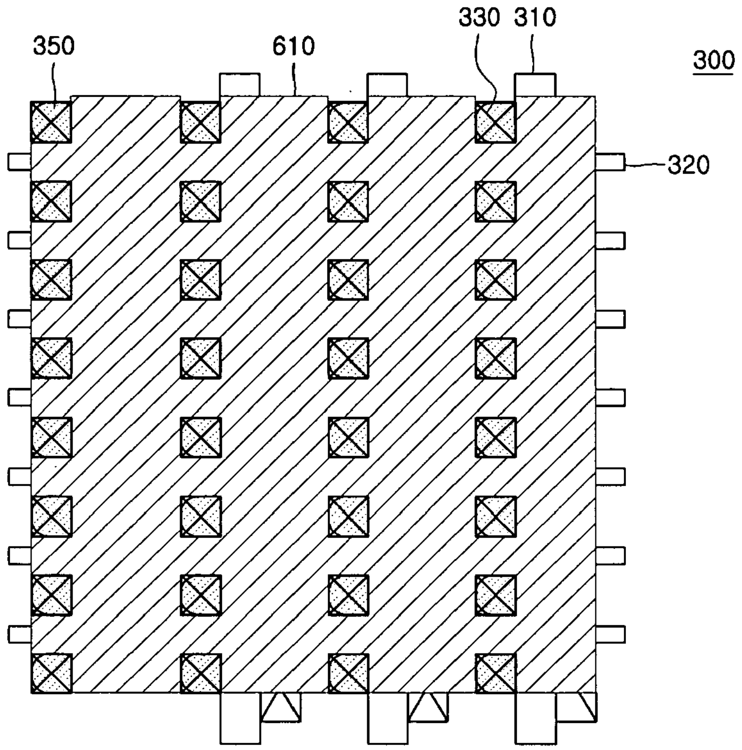


FIG. 12

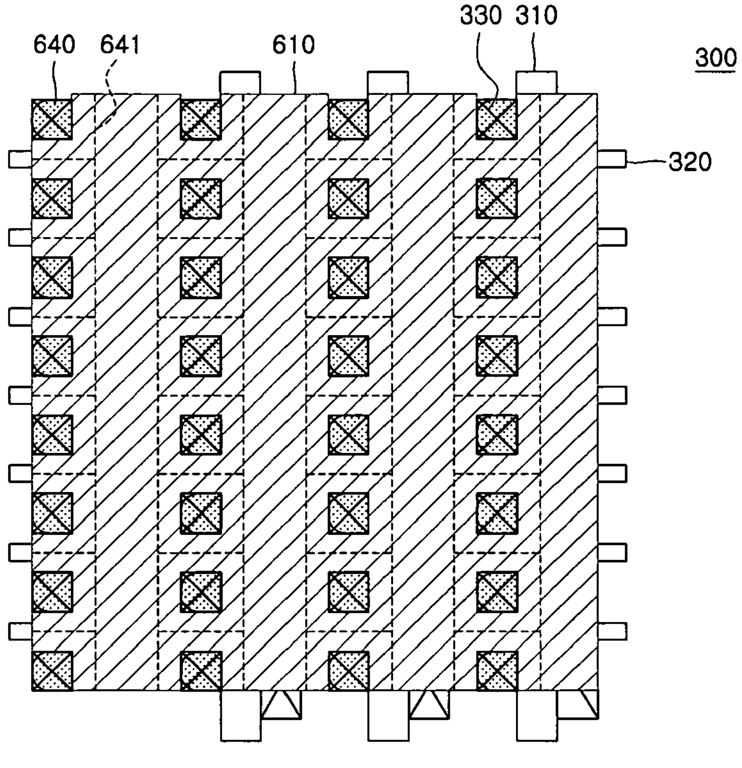


FIG. 13

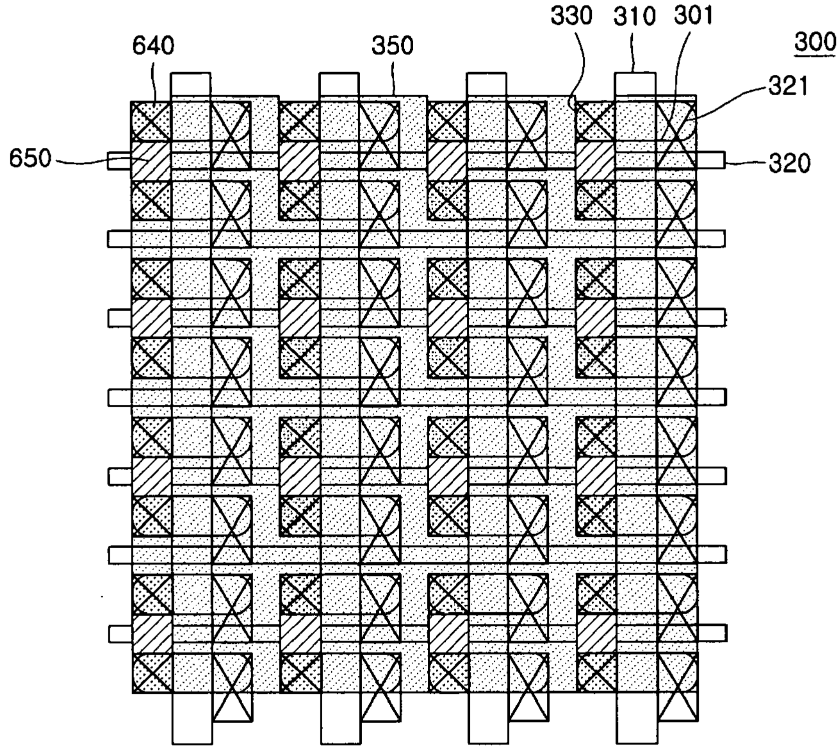


FIG. 14

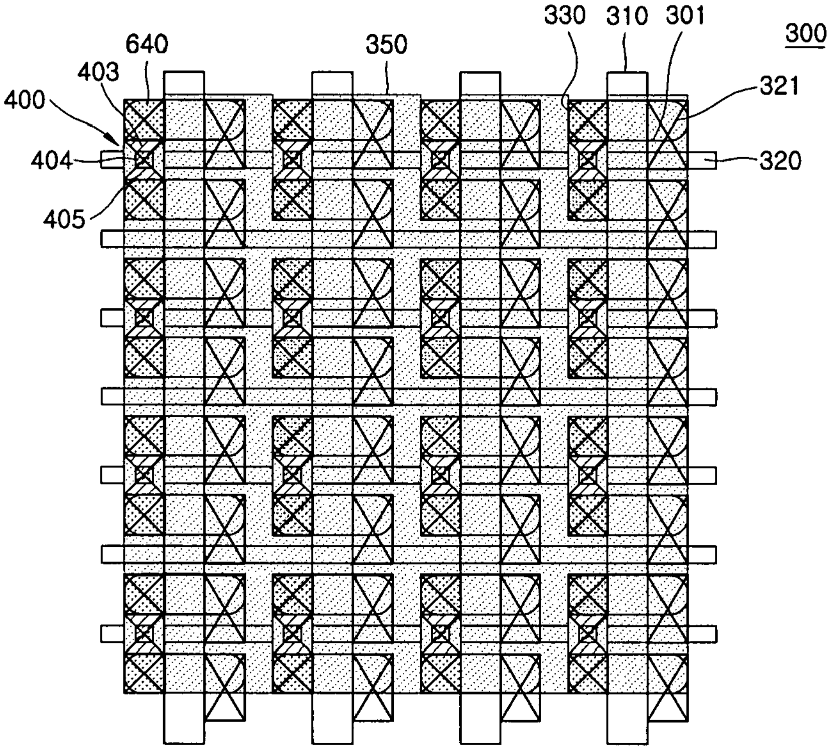


FIG. 15

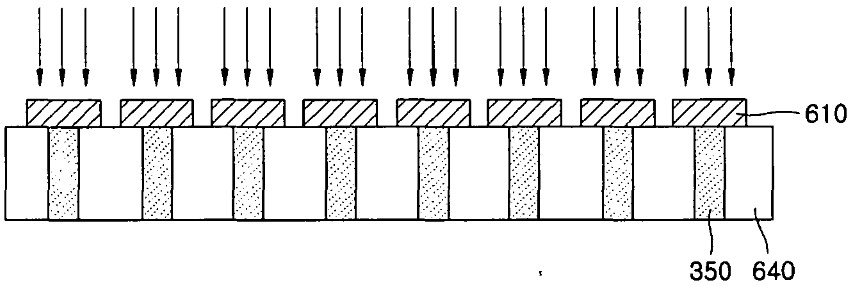


FIG. 16

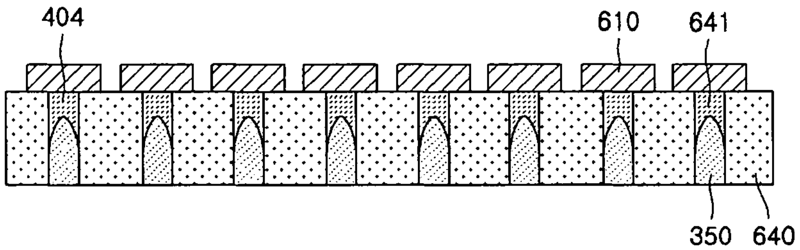


FIG. 17

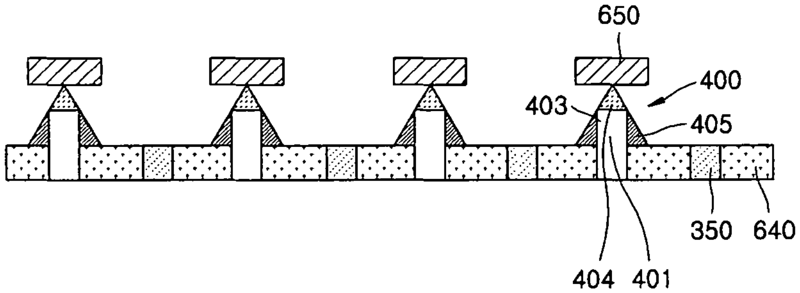


FIG. 18

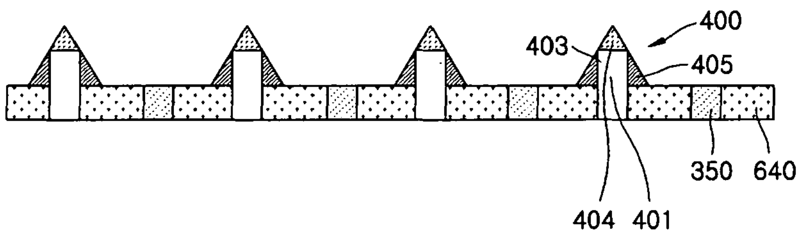


FIG. 19