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(54) Display driver

(57) A driver for controlling cells of an electrochromic display is disclosed. The driver is connected to each cell of the display which is to be controlled to drive each cell according to a charging state associated with the cell; and to provide a characteristic of a selected cell to a sensor. The driver can operate in a sense and a programming mode. In sense mode the driver determines the characteristic of a selected cell; and in programming mode the driver sets the charging state of the cells.

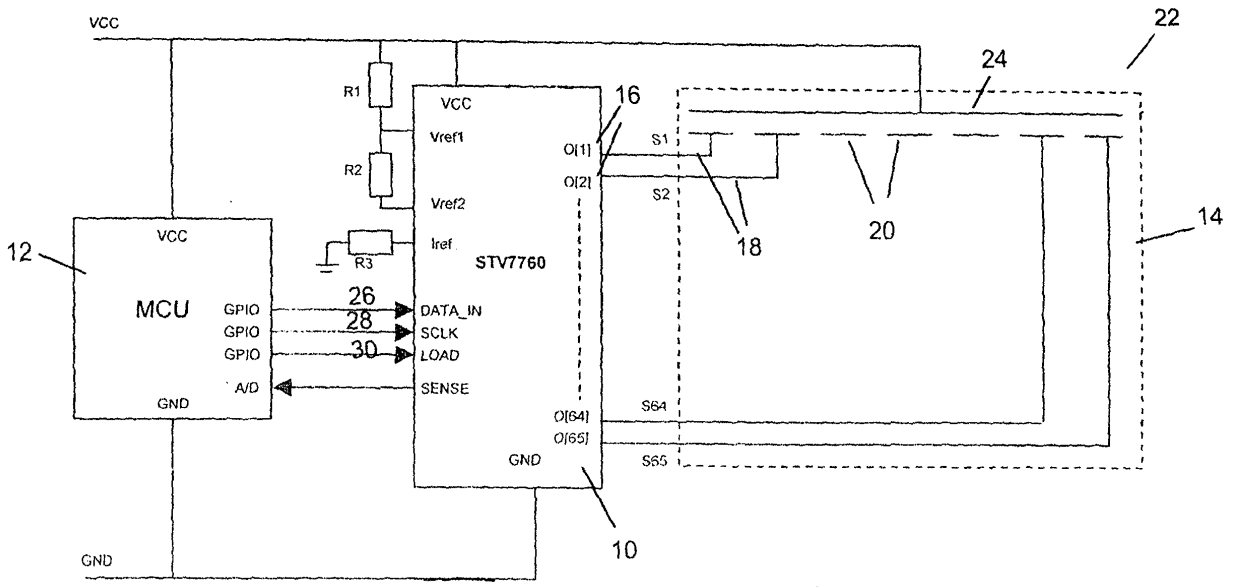

FIG. 1

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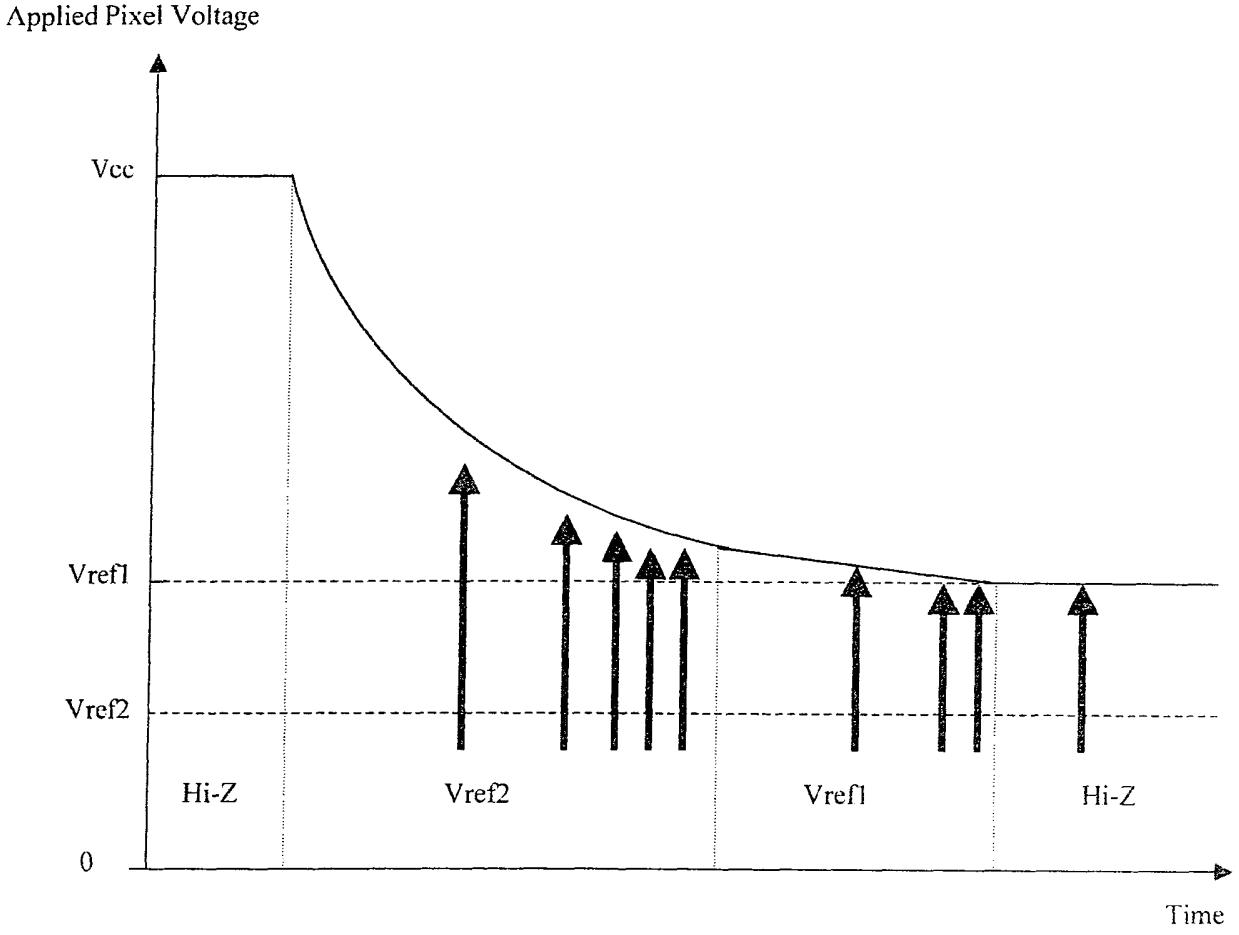
Applied Pixel Voltage
Vcc
Vref1
Vref2
0
Hi-Z
Vref2
Vref1
Hi-Z
Time

Fig. 5

Description

[0001] The present invention relates to a driver, in particular a driver for driving electrochromic displays. An electrochromic display comprises a glass display screen, a substrate, tracks and electrochromic segments or pixels, which change colour upon application of an electrical potential.

[0002] An electrochromic pixel comprises a first electrode made of nanostructured films of semiconducting metal oxides with a self-assembled monolayer of electrochromic viologen molecules. The charge to colour the electrochromic molecules is supplied by a second nanostructure counter electrode, comprised of a doped semiconductor. Between the electrodes there is a reflector made of a porous film of Titanium Dioxide.

[0003] Electrochromic displays are typically dc driven devices. A voltage can be applied to each individual segment or pixel of the display via a transparent conductive track leading to the pixel from the edge of the glass screen. The transparent conductive tracks are usually fabricated from Indium Tin-Oxide and as such behave in a manner similar to that of a resistor in series with the pixel.

[0004] The electrochromic pixel has similar characteristics to that of a capacitor in that it has the ability to store charge. The pixel is turned on or charged by applying a voltage to its anode. The charge capacity of a pixel is proportional to the area of the pixel. Once charged, the pixel can be left in open circuit and remain on. This characteristic of the electrochromic display is called bistability. Like a capacitor, however, the charge will slowly dissipate after time, resulting in deterioration of the pixel colouration.

[0005] This capacitor-resistor arrangement governs the rate at which the pixel can be charged as according to Ohms Law, dV/dt = V/RC. Thus the rate at which individual pixels turn on is inversely proportional to the area of the pixel and the resistance of the associated track. As such, individual pixels may charge at different rates. Pixels, like capacitors, can be damaged when exposed to applied voltages exceeding their capacity. Thus, due to this limitation on the applied voltage, and large ITO track resistances combined with large capacitances, the response time to the switching of electrochromic displays can be quite slow.

[0006] Exposure to UV light and voltage coupling from neighbouring pixels being switched on results in potentially dangerous variations within the individual pixels. As such, the pixels can reach their voltage capacity while still being driven, resulting in damage to the pixels

[0007] It is therefore an object of the present invention to mitigate one or more disadvantages of the prior art.

[0008] According to the present invention there is provided a driver according to claim 1.

[0009] Using the present invention, potentially dangerous variations within the pixels, caused by photoelectric effect, voltage coupling from other pixels being turned on or the like, can be sensed and compensated for. The response time of the pixels is improved by using higher driving voltages in a safe controlled environment. Once charged the pixel can be left in an open-circuit state ensuring improved lifetime for the pixels. Leakage current from and between the pixels can be detected using voltage sensing and measures can be taken to maintain the correct appearance of the display.

[0010] Embodiments of the invention will now be described, by way of example, with reference to the accompanying drawings, in which:

Fig. 1 is a system diagram of a driver of the present invention connected to a micro-control unit and an electrochromic display;

Fig. 2 illustrates a block diagram of the driver of Fig. 1 according to the present invention;

Fig. 3(a) is a timing diagram of the driver of Fig. 1 operating in programming mode;

Fig. 3(b) is a timing diagram of the driver of Fig. 1 operating in sense mode;

Fig. 4 is a plot of an applied pixel voltage against time; and

Fig.5 is a plot of an applied pixel voltage against time including sensing incidents.

[0011] Referring now to Fig. 1 of the accompanying drawings, a system diagram of a driver is indicated, generally at 10, connected to a micro control unit 12 and an electrochromic display 14.

[0012] The nanostructured film electrode of the electrochromic display pixel comprises an enormous surface area with a high number of electrochromic viologen molecules bound to the surface, enabling the viologens to be switched from colourless to coloured and vice versa very quickly. The high number of viologen molecules attached gives strong colouration and the high speed of electron transfer gives high switching speeds. Different colours can be achieved through using different viologen molecules. The doped semiconductor electrode can store charge due to its high capacitance and as such the display device is endowed with a memory, resulting in bistability and low power consumption.

[0013] According to the preferred embodiment of the invention, the driver 10 comprises 65 output channels 16, labelled as O[1], O[2], ...O[64], O[65]. Each output channel 16 is connected via a corresponding transparent conductive track 18 to a cathode 20 of one of 65 segments or pixels 22 of the electrochromic display 14. It will be appreciated that fewer than the 65 pixels may be used. Likewise, more than 65 pixels can be used by joining or cascading a number of ICs together.

[0014] In the embodiment, the pixels 22 can be turned

on or off by application of a dc voltage to the cathodes 20, A common anode 24, corresponding to the cathodes 20 is connected to a supply voltage Vcc.

[0015] By connecting the anode to a positive voltage relative to ground, the requirement of a negative pixel voltage can be avoided. When the pixel is on, the pixel voltage applied to the cathode 20 is positive but lower than Vcc.

[0016] The output channels 16 have been designed as voltage sources that source and sink current in order to get the connected pixel 22 to the applied voltage as quickly as possible. The 65 output channels 16 each support 4 voltage states; two 'on' voltage states, Vref1 and Vref2, an open circuit or high impedance (Hi-Z) state and an 'off' voltage state.

[0017] The two 'on' voltages are defined by the voltages at pins Vref1 and Vref2, located on the driver 10. An internal circuit and an external current reference resistor R3 define a constant current source that sinks through Vref2 allowing a pair of resistors, R1 and R2, to be used to accurately define the voltages at Vref1 and Vref2. The voltage drop at Vref1 and Vref2 will remain constant relative to Vcc as they will always have a constant current flowing through them, ensuring that the contrast of the electrochromic display 14 will not change if the supply voltage Vcc varies.

[0018] The constant current is defined by the value of the resistor R3, connected between ground and an Iref pin located on the driver 10. In this embodiment, the equation for the constant current is 1.25/R3. For example, if resistor R3 has a value of 270KΩ, the current flowing through resistors R1 and R2 will be 4.6μA. Similarly, if resistor R3 has a value of 888KΩ, the current flowing through resistors R1 and R2 will be 1.43μA. The values of R1 and R2 are then set accordingly to provide the required voltage drop from Vcc to drive the display 14. In this embodiment, Vref1 should be set to a value of 0.8V below Vcc and Vref2 should be set between 1.5V and 2V below Vcc.

[0019] The pixels 22 assume the open circuit or Hi-Z State when the output channels 16 are disconnected from the pixels 22. Once the 'turn on' voltage has been applied to the pixels 22, the pixels can assume the Hi-Z state without any change to the display image. This is due to the ability of the pixels to store charge and is known as bistability. The same display image will be maintained for a period of time before the voltage eventually changes due to charge leakage, causing the pixel image to fade. Depending on the characteristics of the pixel, the image could fade in a matter of minutes or days.

[0020] The 'off' state is achieved by setting the state for the output channel 16 to Vcc, thus eliminating the voltage drop across the terminals of the pixel, and causing the pixel to turn off. In general, once the pixels reach a voltage of approximately 400mV or less, they are assumed to be off. Once the pixel has turned off, it should be set to the Hi-Z State.

[0021] The driver 10 further comprises three inputs, DATA_IN, SCLK and LOAD, which are connected to corresponding outputs, 26, 28, and 30 respectively, located on the micro control unit 12. An output, SENSE, provided on the driver 10 is connected to an Analogue-to-Digital converter, A/D, located on the micro control unit 12.

[0022] The driver 10 operates in one of two modes at any one time, programming mode or sense mode. In order to program the state of some or all of the pixels of the display 14, the driver needs to operate in the programming mode. In programming mode, the driver 10 is provided with information representing the pixels at its input DATA_IN in accordance with the clock signal provided to the input SCLK. The driver 10 operates in the sense mode to monitor the behaviour of each of the pixels 22. In sense mode, a signal representing the state of a pixel is provided at the SENSE output and fed to the analog-to-digital converter A/D, where it is compared with a reference value. This mode enables the MCU 12 to sense variations in pixel voltage due to exposure to UV light, voltage coupling from neighbouring pixels being switched on, irregularities in the pixel, response to the applied voltage and other varying factors.

[0023] Referring now to Fig. 2 there is provided a block diagram of the driver 10, according to the preferred embodiment of the invention.

[0024] The driver 10 comprises a control logic unit, 32 and a 130-bit shift register 34. The register 34 is connected to a 130-bit latch 36. The content of the 130-bit latch 36 is fed to 65 2-to-4-bit decoders 38, the outputs of which are connected to 65 corresponding CD (chromodynamic, i.e. electrochromic) drivers 40. The NCD drivers are in turn connected to the output channels 16. The truth table for the operation of each decoder 38 is depicted below as Table 1.

Table 1.

Inputs		
A	B	State
0	0	Hi-Z
0	1	Vref1
1	0	Vref2
1	1	Vcc

[0025] The 130-bit shift register 34 is also connected to a 7-bit latch 44. The content of the 7-bit latch 44 is fed to a 7-to-65-bit decoder 46. The outputs of the decoder 46 are connected to 65 respective switches 42, which control the monitoring of the pixels. The 65 NCD drivers 40 are connected to the 65 switches 42, which in turn provide an input to the output SENSE.

[0026] The input DATA_IN is connected to the 130-bit shift register and the inputs SCLK and LOAD are connected to the control logic unit 32, which is in turn connected to the 130-bit shift register 34 at two points. The

SCLK input is a clocked input and is controlled by the MCU 12. In the preferred embodiment, the maximum frequency of the SCLK is 10MHz. The LOAD input can assume a high or low signal value and is also controlled by the MCU 12. The value of the LOAD input determines whether the shift register 34 is filled with 7-bits or 130-bits.

[0027] For the driver 10 to operate in the programming mode, the micro control unit must send a low signal value to the control logic unit 32 via the driver input LOAD as illustrated in Fig. 3(a). The micro control unit 12 then feeds 130-bits into the register 34, via the input DATA_IN. Each 2-bit binary value of the 130 bits represents the desired state of one of the 65 pixels.

[0028] Data, representing the desired state for each of the 65 pixels, is shifted from the DATA_IN input into the register 34 at each low to high transition of the SCLK clock. Once the shift register 34 is filled with 130-bit binary values, the MCU 12 provides a high signal value at the LOAD input, causing the content of the shift register to be loaded into the 130-bit latch 36. The decoders 38 decode the data, and supply the corresponding NCD drivers 40 with the desired state information for each pixel. The NCD drivers 40 provide the output channels 16 with the requested voltage, according to Table 1, which is applied to the pixels.

[0029] When the driver input LOAD is supplied with a high signal value, the mode of operation changes from programming mode to sense mode, as illustrated in Fig. 3(b). In sense mode, each bit of a 7-bit binary value representing the pixel number to be sensed is loaded into the shift register 34 on every low to high transition of the SCLK clock. After 7 clocked shifts, the LOAD input signal changes momentarily from high to low before returning to the high state. This causes the 7-bit binary value to be loaded into the 7-bit latch 44, from where it is decoded by the decoder 46 and applied to one of the 65 switches 42 corresponding to the pixel number. This switch 42 disconnects the corresponding NCD driver 40 from the corresponding output channel 16. This causes the pixel 22 to assume the Hi-Z state enabling its voltage to be sensed. The sensed voltage is applied to the SENSE output and fed to the Analogue-to-Digital Converter A/D located on the micro control unit. The A/D converts the signal to a digital value, which is compared with a fixed reference value, the outcome of which determines whether it is required to change the state of the pixel 22. When sensing is finished, the NCD driver 40 is reconnected to its associated output channel 16.

[0030] Referring now to Fig. 4 there is illustrated a plot of the applied pixel voltage against time. In order to accelerate switching and increase the responsiveness of the display 12, the required pixels are driven by a voltage Vref2, which exceeds the safe voltage limit of the pixels. Ideally before the pixels become fully charged, the safe voltage Vref1 is applied to ensure that the pixels don't exceed their voltage capacity for too long.

[0031] In a first embodiment, as depicted in Fig. 5 the driver 10 will operate in the sense mode during charging until it is sensed that a pixel voltage is within a predefined range of a fixed reference voltage or Vref1, and that the applied voltage thus needs to be changed from Vref2 to Vref1 to avoid overcharging. It will be appreciated however, that the sense mode can also be used to determine whether a pixel voltage in the Hi-Z state has drifted and thus requires a voltage, Vref1 or Vref2, to be applied to return the pixel voltage to the desired level. The MCU 10 will then send a low signal to the LOAD input causing the driver 10 to change to programming mode and the required voltage (including open circuiting) will be applied to the associated pixel output channel 16 by setting the input bits for the pixel to the required state. The driver 10 will then return to sense mode.

[0032] In another embodiment, the MCU 12 contains timing information relating to each individual pixel of the display 12. This timing information is derived from the known capacitance of each pixel and the resistance of its associated ITO track and provides the MCU 12 with an estimated time period for the application of both Vref1 and Vref2. In this embodiment, the MCU 12 timing information also contains an estimated time for which the display 14 will remain coloured. This timing information is used to schedule the sensing of the pixels. If a pixel is sensed according to the schedule, and it is determined that due to voltage variations, it has not reached the predefined range which defines the necessity to change the applied voltage, the timing information associated with that pixel voltage is incremented by a predefined amount, and the schedule is updated accordingly. Similarly, if a pixel is sensed according to the schedule, and it is determined that due to voltage variations, it has passed the predefined range which defines the necessity to change the applied voltage, the timing information associated with that pixel voltage is decremented by a predefined amount, the schedule is updated accordingly and the required voltage (including open circuiting) is applied to the pixel. Likewise, if the MCU 12 detects that a pixel in the Hi-Z state has leaked charge, it will adjust the related timing information, update the schedule and change the mode of operation of the driver 10 to programming mode in order to apply the required safe voltage to 'top up' the pixel.

[0033] In the preferred embodiment, the driver 10 will operate in programming mode in order to change the applied voltage of one or more of the pixels in accordance with both the estimated timing information stored in the MCU 12 and the outcome of the sensing operation.

[0034] In an another embodiment, the timing information is incremented or decremented by an amount directly related to the approximate rate of charge of the pixel at the time the pixel is sensed. In order to determine the rate of charge of a pixel, the MCU 12 stores the time at which each pixel enters each state.

[0035] In another embodiment, when the sensing function is carried out on a pixel, the MCU determines the time and associated voltage of the pixel. The same pixel is sensed again, and again the MCU determines the time

and associated voltage of the pixel. The MCU can then use these two results to determine the rate of charge of the pixel and update the timing information as appropriate.

[0036] In another embodiment, each time the sensing function is used, the MCU determines a first time and associated voltage of the pixel, then momentarily reconnects the pixel output channel to its NCD driver before determining a second time and associated voltage for the pixel. These values are then used to determine the rate of charge of the pixel and update the timing information as appropriate.

[0037] In an alternative embodiment, the Analogue-to-Digital Converter located on the MCU 12 is replaced with a comparator, which compares the sensed voltage signal with the safe voltage Vref1.

[0038] In the preferred embodiment, the driver can be set to a standby state. This is achieved by setting all of the output channels to the Hi-Z state and setting the driver to programming mode. In this state, the constant current source that provides the Vref1 and Vref2 voltages is shut down, enabling the driver 10 to achieve very low power consumption.

[0039] The present invention is not limited to the embodiments described herein, which may be amended or modified without departing from the scope of the present invention.

Claims

1. A driver for controlling at least one cell of a display, the driver being arranged to connect to the or each cell of the display which is to be controlled, and the driver comprising:

   means for driving the or each cell according to a charging state associated with the cell; and
   a signal path for receiving a characteristic of a selected cell and providing said characteristic to a sensor.

2. A driver according to claim 1 wherein said driver is arranged to operate in a sense mode and in a programming mode;
   said sense mode in which said characteristic of a selected one of said cells is determined; and
   said programming mode in which said charging state of one or more of the cells is set.

3. The driver according to claim 2, wherein said driver is operatively associated with a controller which acts as the sensor.

4. The driver according to claim 3 wherein said driver is operable in said sense mode to provide a signal indicative of said characteristic said selected cell to the controller.

5. The driver according to claim 3 or 4 wherein said driver is operable in said programming mode to receive a signal indicative of a required charging state of one or more of the cells from the controller.

6. The driver according to any one of claims 3-5 wherein the operating mode of said driver is determined by a logic signal received from said controller.

7. The driver according to any one of claims 3-6 wherein the mode of operation changes from the sense mode to the programming mode when at least one of the characteristics of one or more of the cells is determined to be within a reference range.

8. The driver according to any one of claims 3-7 further comprising a shift register for storing information received from the controller.

9. The driver according to claim 8 wherein said driver is responsive to a clock signal to successively load information into the shift register.

10. The driver according to claim 9 wherein, when said driver is operating in programming mode, said information comprises cell charging state information indicative of each of the cells required charging state; and, when said driver is operating in sense mode, said information comprises an identifier of said selected cell.

11. The driver according to claim 1 or 2 in which said charging state is one of an 'off' state, an 'on' state and a high impedance state.

12. The driver according to claim 11 wherein said 'on' state can be one of a slow charging state and a fast charging state.

13. The driver according to claim 11 as dependent on claim 2 wherein, when said driver is operating in sense mode, the cell to be sensed is set to the high impedance state.

14. A control system for a display comprising a driver according to any previous claim and a controller, wherein said controller is arranged to store timing information for the or each cell derived from said characteristic for said cell.

15. A control system as claimed in claim 14 wherein said controller is arranged to schedule the driver to switch to sensing mode according to said timing information.

16. A control system according to claim 14 wherein said controller is arranged to adjust said timing information periodically.

17. A control system according to claim 14 wherein said driver is the driver as claimed in claim 4, wherein said controller is arranged to adjust said timing information in response to said signal received from said driver.

18. A method for controlling at least one cell of a display, comprising the steps of:

connecting to the or each cell of the display which is to be controlled;
driving the or each cell according to a charging state associated with the cell;
receiving a characteristic of a selected cell; and
providing said characteristic to a sensor.

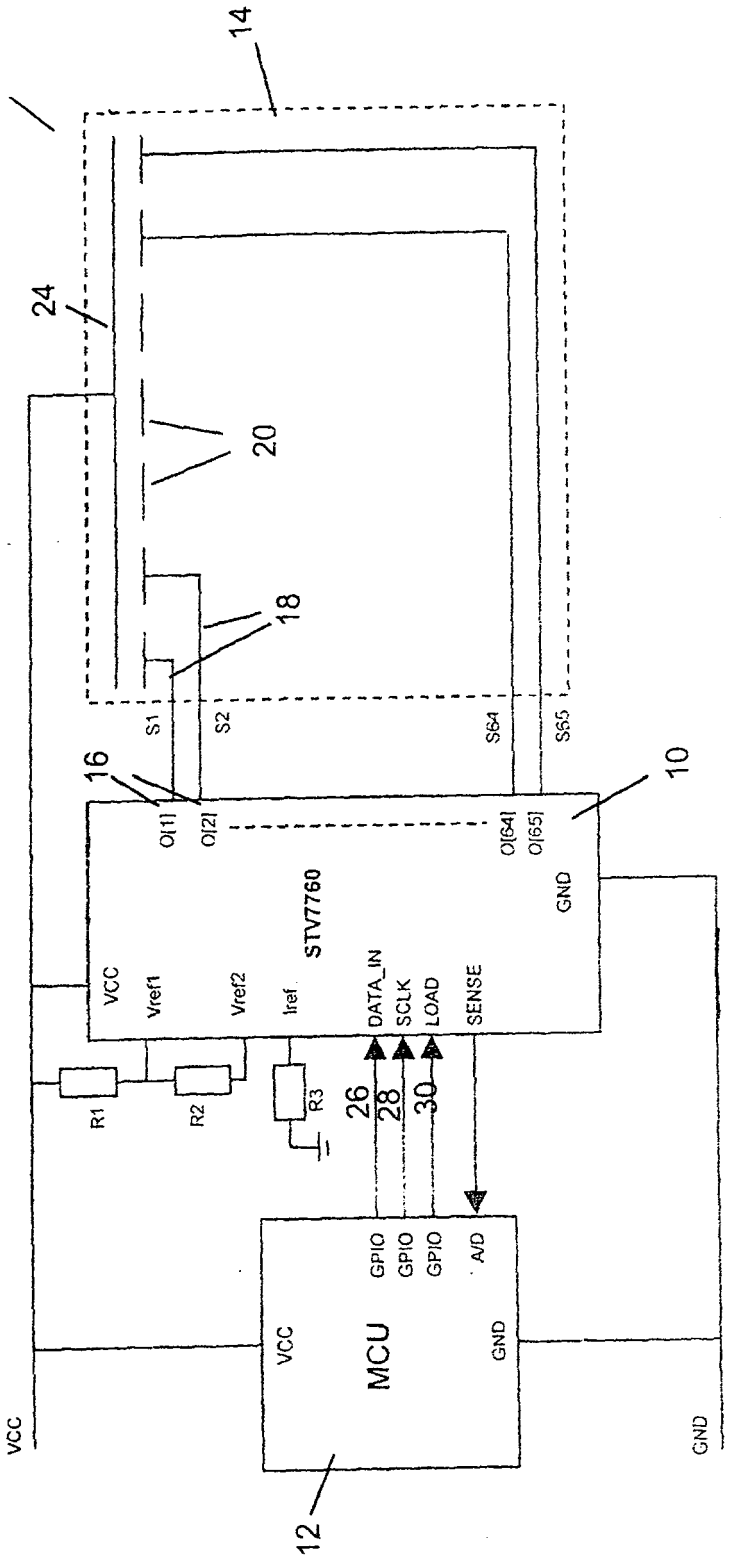
22
14
24
20
18
S1
S2
S64
S65
16
O[1]
O[2]
O[64]
O[65]
10
GND
STV7760
VCC
Vref1
Vref2
Iref
DATA_IN
SCLK
LOAD
SENSE
R1
R2
R3
26
28
30
GPIO
GPIO
GPIO
A/D
VCC
MCU
GND
VCC
GND
12

FIG. 1

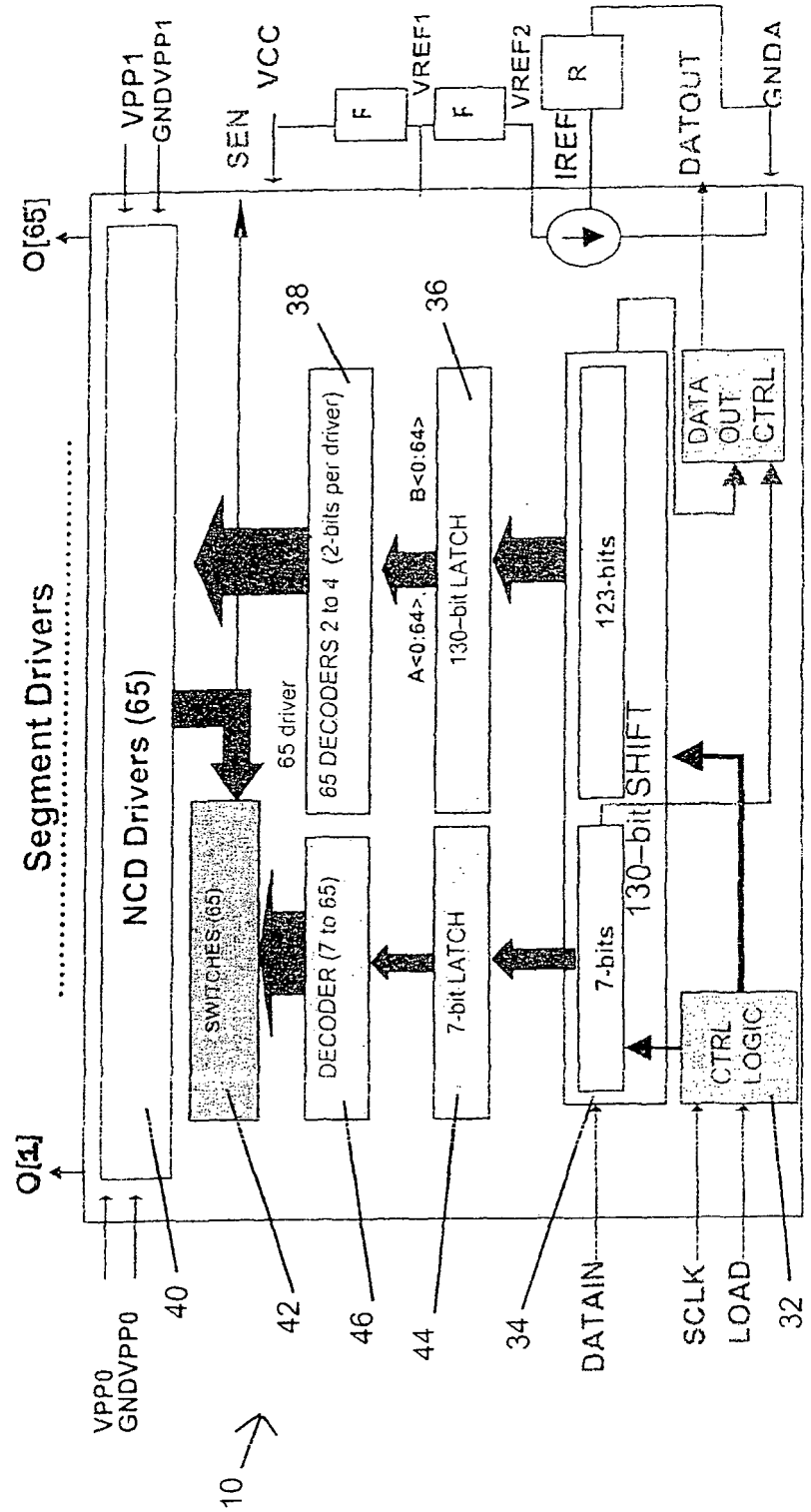
Segment Drivers
NCD Drivers (65)
O[65]
O[1]
VPP1
GNDVPP1
SEN
VCC
VREF1
VREF2
IREF
R
F
F
DATOUT
GNDA
38
36
65 driver
65 DECODERS 2 to 4 (2-bits per driver)
A<0:64>
B<0:64>
130-bit LATCH
123-bits
DATA OUT CTRL
SWITCHES (65)
DECODER (7 to 65)
7-bit LATCH
7-bits
130-bit SHIFT
CTRL LOGIC
VPP0
GNDVPP0
40
42
46
44
34
DATAIN
SCLK
LOAD
32
10

FIG. 2

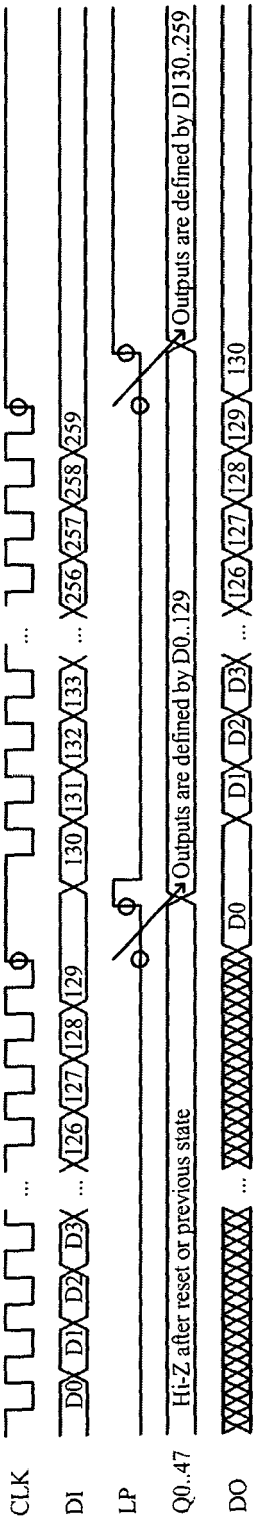
CLK
DI
LP
Q0..47
DO
D0
D1
D2
D3
126
127
128
129
130
131
132
133
256
257
258
259
Hi-Z after reset or previous state
Outputs are defined by D0..129
Outputs are defined by D130..259

FIG 3(a)

CLK
DI
LP
SENS
DO
S0
S1
S2
S3
S4
S5
S6
S7
S8
S9
S10
S11
S12
S13
Hi-Z after reset or previous state
Connected to output selected by S0..6
Connected to output selected by S7..13

FIG 3(b)

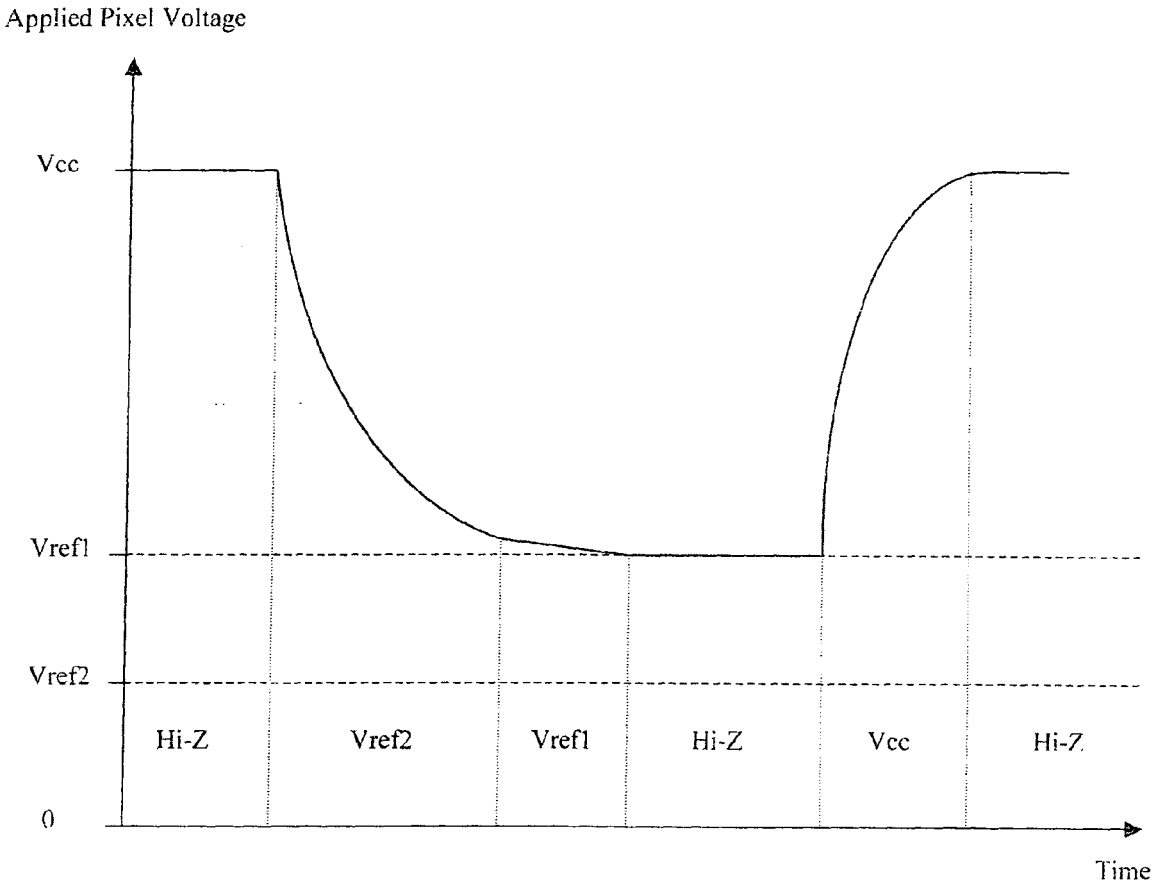
Applied Pixel Voltage
Vcc
Vref1
Vref2
0
Hi-Z
Vref2
Vref1
Hi-Z
Vcc
Hi-Z
Time

Fig. 4

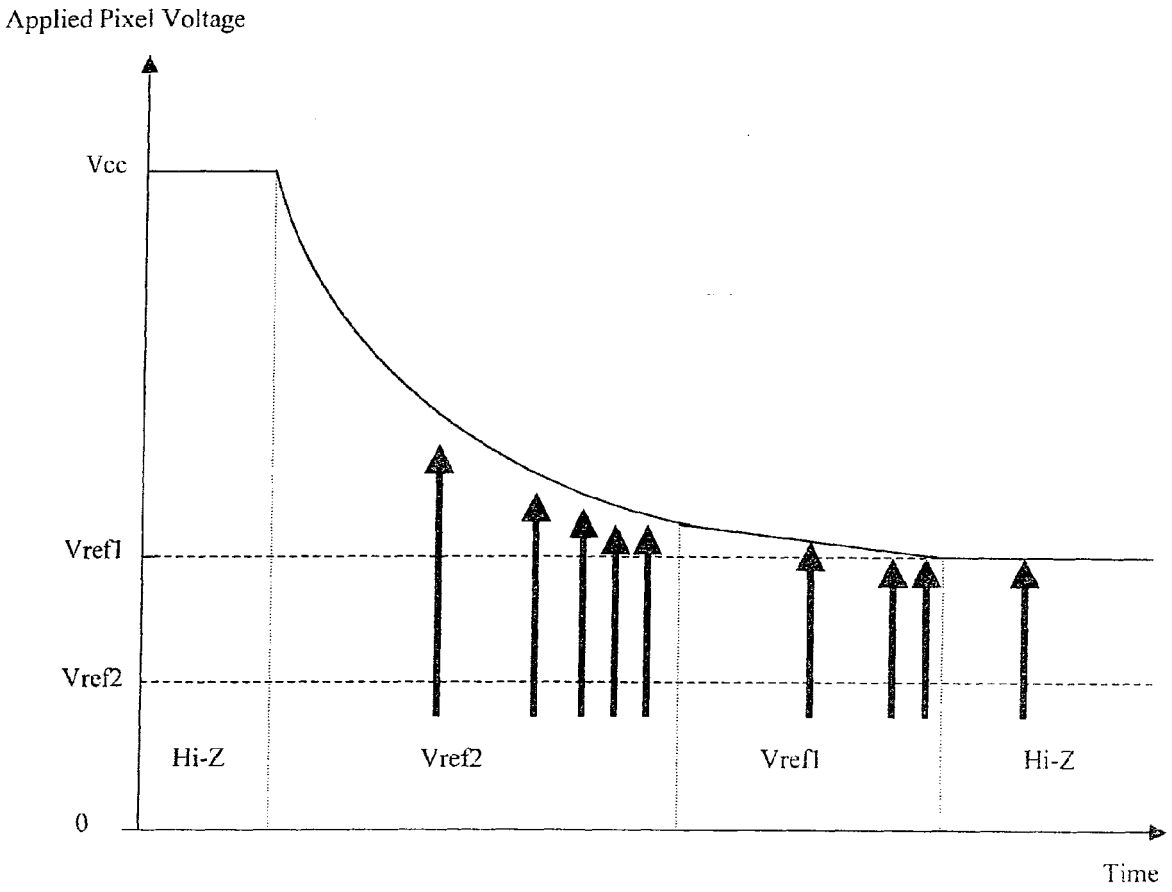
Applied Pixel Voltage
Vcc
Vref1
Vref2
0
Hi-Z
Vref2
Vref1
Hi-Z
Time

Fig. 5

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 04 39 4068

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
X Y	US 5 973 819 A (PLETCHER ET AL) 26 October 1999 (1999-10-26) * column 10, line 26 - line 56; figure 6 * * column 13, line 44 - line 53 * * column 14, line 1 - line 54 * * column 15, line 48 - line 54 * * column 19, line 26 - line 56; figure 6 * -----	1-13,18 12	G09G3/38
Y	EP 0 490 658 A (DONNELLY CORPORATION) 17 June 1992 (1992-06-17) * figure 11 * -----	12	

TECHNICAL FIELDS SEARCHED (Int.Cl.7)

G09G

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
Munich	19 April 2005	Gundlach, H

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
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ANNEX TO THE EUROPEAN SEARCH REPORT ON EUROPEAN PATENT APPLICATION NO. EP 04 39 4068

This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report. The members are as contained in the European Patent Office EDP file on
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19-04-2005

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 5973819 A	26-10-1999	WO 0017703 A1	30-03-2000
EP 0490658 A	17-06-1992	US 5220317 A	15-06-1993
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EPO FORM P0459

For more details about this annex : see Official Journal of the European Patent Office, No. 12/82