



(11)

EP 1 669 968 A2

(12)

EUROPEAN PATENT APPLICATION

(43) Date of publication:
14.06.2006 Bulletin 2006/24

(51) Int Cl.:
G09G 3/20 (2006.01)

(21) Application number: 05257533.9

(22) Date of filing: 07.12.2005

(84) Designated Contracting States:
AT BE BG CH CY CZ DE DK EE ES FI FR GB GR
HU IE IS IT LI LT LU LV MC NL PL PT RO SE SI
SK TR
Designated Extension States:
AL BA HR MK YU

(30) Priority: 09.12.2004 JP 2004356417

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(54) Automatic image correction circuit

(57) An automatic image correction circuit is provided which automatically performs image correction on received image data and includes a resolution detection unit that detects resolutions of the image data; a set value

calculation unit that calculates a set value to be used in the image correction based on the resolutions; and an image correction unit that performs the image correction on the image data based on the set value.

FIG. 1

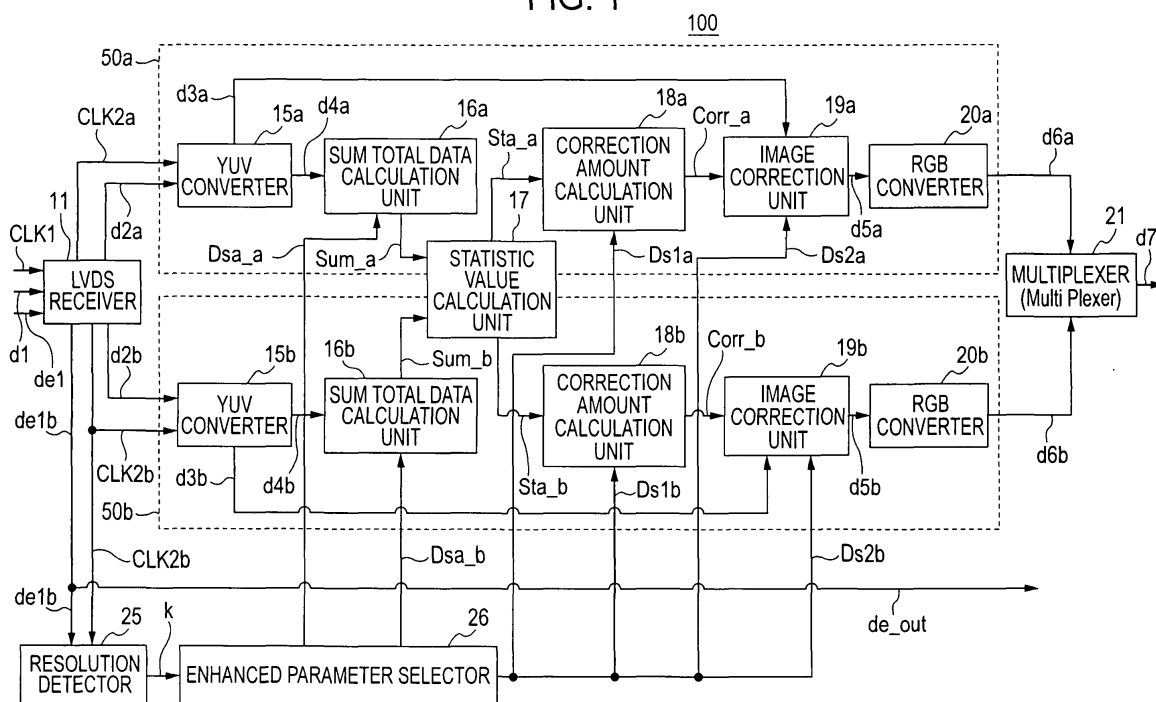


FIG. 10

SPECIFICATION	HORIZONTAL RESOLUTION hsc [dot]	VERTICAL RESOLUTION vsc [dot]	APERTURE RATIO [%]	LIGHTNESS CORRECTION INTENSITY (COEFFICIENT)
VGA	640	480	95	0.8
SVGA	800	600	90	0.83
XGA	1024	768	80	0.90
WXGA	1280	768	75	1.0
WXGA+	1366	768	75	1.0
SXGA	1280	1024	70	1.2
SXGA+	1400	1050	70	1.2
UXGA	1600	1200	60	1.5

Description

[0001] The present invention relates to an automatic image correction circuit that automatically performs image correction by detecting resolutions of input image data.

[0002] An automatic image correction circuit that automatically performs image correction on input image data has been known. The automatic image correction circuit is a circuit that calculates statistic values of received image data, such as luminance and chroma, and performs image correction suitable for images, which are being received, based on the statistic values. The automatic image correction circuit enhances images to be displayed through image correction, such as level correction, gamma correction, or contrast correction.

[0003] The automatic image correction circuit sometimes performs image data correction by calculating statistic values using resolutions of image data or by changing a set value. In a general automatic image correction circuit, a user inputs resolutions of image data to a register, etc. in advance and the automatic image correction circuit then performs image correction on image data based on the resolutions input in advance. However, the method in which a user inputs resolutions every image data is not preferred in terms of user-friendly aspect and accuracy. Furthermore, this method cannot cope with a case where resolutions of input image data are dynamically changed.

[0004] An advantage of some aspects of the invention is that it provides an automatic image correction circuit that detects resolutions of input image data and automatically performs image correction appropriate for the detected resolutions.

[0005] According to an aspect of the invention, an automatic image correction circuit is an automatic image correction circuit that automatically performs image correction on received image data. The circuit includes a resolution detection unit that detects resolutions of the image data, a set value calculation unit that calculates a set value to be used in the image correction based on the resolutions, and an image correction unit that performs the image correction on the image data based on the set value.

[0006] The automatic image correction circuit is a circuit that receives image data, such as still images or moving images, and automatically performs image correction on these image data. The automatic image correction circuit includes the resolution detection unit that detects resolutions of the received image data, i.e., a horizontal resolution and a vertical resolution. The resolution detection unit can detect resolutions from a clock signal and a data enable signal of the image data. Furthermore, the automatic image correction circuit includes the set value calculation unit. The set value calculation unit can calculate a set value, which is used to perform image correction, from the resolutions detected by the resolution detection unit. The image correction unit performs correction on image data with respect to, e.g., luminance based on the calculated set value. Therefore, a variety of settings, which are needed every resolution in the related art, can be automatically performed.

[0007] In the automatic image correction circuit according to the aspect of the invention, preferably, the set value calculation unit calculates a set value of a position of a sampling area, which is a part or the entire of the image data. Therefore, positional information of a region from which statistic values used to perform image correction will be calculated (hereinafter simply referred to as a "sampling area") can be automatically calculated according to resolutions obtained by the resolution detection unit.

[0008] In the automatic image correction circuit according to the aspect of the invention, preferably, the set value calculation unit calculates the position of the sampling area, which is a part or the entire of the image data, on the basis of a horizontal resolution and a vertical resolution so that the sampling area is located at a central region of an image. A viewer generally sees a central region of an image. Therefore, if image data sampled from the central region are used for image correction, it is possible to perform effective image correction.

[0009] As a preferred example, the set value calculation unit sets the range of the sampling area, which is a part or the entire of the image data, to on value of the powers of 2. Therefore, it is possible to detect only bits set, and to reduce the size of the circuit.

[0010] In the automatic image correction circuit according to the aspect of the invention, preferably, the set value calculation unit calculates a lightness correction coefficient based on a horizontal resolution and a vertical resolution of the image data in a set value for correcting a brightness of the image data. Therefore, image data can be automatically set to an appropriate brightness every resolution.

[0011] In the automatic image correction circuit according to the aspect of the invention, preferably, the automatic image correction circuit further includes a storage unit that stores the size of a display panel, a resolution comparison unit that compares the size of the display panel and the resolutions of the image data, an image magnification process unit that magnifies the image data, and an image reduction process unit that reduces the image data. Further, the image correction unit performs image correction on image data that are obtained by reducing the image data by the image reduction process unit when the size of the display panel is smaller than the resolutions of the image data, and performs image correction on image data that are enlarged by the image magnification process unit when the size of the display panel is larger than the resolutions of the image data. The automatic image correction circuit further includes the resolution comparison unit. The resolution comparison unit stores the size of a display panel in advance and compares the size

of the display panel with detected resolutions of image data. If the resolutions of the image data are greater than the size of the display panel, the image reduction process unit performs a reduction process on image data after a correction process is carried out. Meanwhile, if the resolutions of the image data are smaller than the size of the display panel, the image magnification process unit performs a magnification process on image data before a correction process is performed. Therefore, the three kinds of processes, such as the magnification process, the reduction process and the correction process, can be automatically performed on image data according to resolutions.

[0012] Embodiments of the invention will now be described by way of further example only and with reference to the accompanying drawings, wherein like numbers reference like elements:-

[0013] Fig. 1 schematically shows the construction of an automatic image correction circuit according to a first embodiment of the invention.

[0014] Fig. 2 is a view for illustrating a method of detecting resolutions.

[0015] Fig. 3 is a timing chart of clock signals and data enable signals, which are input to a resolution detector.

[0016] Fig. 4 is a view for illustrating a method of calculating a sampling area.

[0017] Fig. 5 is a table showing the relation between resolutions and the sizes of sampling areas.

[0018] Fig. 6 is a table showing resolutions, the sizes of sampling areas and sampling ratios.

[0019] Fig. 7 is a view for illustrating a method of calculating a sampling area.

[0020] Fig. 8A is a view for illustrating a method of calculating a sampling area.

[0021] Fig. 8B is a view for illustrating a method of calculating a sampling area.

[0022] Fig. 8C is a view for illustrating a method of calculating a sampling area.

[0023] Fig. 9A is a view for illustrating a method of calculating an enhanced parameter.

[0024] Fig. 9B is a view for illustrating a method of calculating an enhanced parameter.

[0025] Fig. 10 is a table showing the relation between resolutions and lightness correction coefficients.

[0026] Fig. 11 schematically shows the construction of an automatic image correction circuit according to a second embodiment of the invention.

[0027] Fig. 12A is a view for illustrating a method of a magnification/reduction process.

[0028] Fig. 12B is a view for illustrating another method of a magnification/reduction process.

[0029] Fig. 12C is a view for illustrating another method of a magnification/reduction process.

[0030] Fig. 13 is a flowchart for illustrating a method of an image magnification/reduction process.

[0031] Fig. 14 is a circuit block diagram of an electronic apparatus to which the automatic image correction circuit of the invention is applied.

[0032] Fig. 15A shows an example of an electronic apparatus to which the automatic image correction circuit of the invention is applied.

[0033] Fig. 15B shows another example of the electronic apparatus to which the automatic image correction circuit of the invention is applied.

[0034] The invention will now be described in detail in connection with preferred embodiments with reference to the accompanying drawings.

First Embodiment

[0035] An automatic image correction circuit 100 according to a first embodiment of the invention will be described with reference to Fig. 1. Fig. 1 is a block diagram schematically showing the construction of the automatic image correction circuit 100 according to a first embodiment of the invention.

Construction of Automatic Image Correction Circuit

[0036] The automatic image correction circuit 100 mainly includes a Low Voltage Differential Signal (LVDS) receiver 11, a resolution detector 25, an enhanced parameter selector 26, statistic value calculation unit 17, image correction blocks 50a and 50b, and a multiplexer 21.

[0037] The automatic image correction circuit 100 is a circuit that receives image data of still images or moving images, and automatically performs image correction on these image data on a frame basis. The automatic image correction circuit 100 mainly performs an image correction process for enhancing images to be displayed. Furthermore, the automatic image correction circuit 100 can be mounted in an electronic apparatus, etc., which has an image display unit. For example, in a portable telephone or a portable terminal having a liquid crystal panel, etc. as an image display unit, the automatic image correction circuit 100 can be installed within an image processor that supplies display image data to the image display unit or the driver of the liquid crystal panel.

[0038] The LVDS receiver 11 receives image data d1 that must be processed by the automatic image correction circuit 100, a clock signal CLK1 serving as a reference upon processing within the automatic image correction circuit 100, and a data enable signal de1 indicating the valid period of the image data d1 from the outside. The LVDS receiver 11 outputs

data whose voltage is controlled as a small swing because EMI (Electroluminescence Interference) is generated within the circuit if the image data d1 are output as a full swing voltage when the image data d1 are input at high speed. Furthermore, the received image data d1 are data of RGB form, e.g., data of 24 bits/pixels.

[0039] The LVDS receiver 11 divides the received image data d1 into image data d2a and image data d2b, and supplies those data to the image correction block 50a and the image correction block 50b, respectively. The LVDS receiver 11 also supplies a clock signal CLK2a and a clock signal CLK2b to the image correction blocks 50a and 50b, respectively.

[0040] The LVDS receiver 11 also supplies the clock signal CLK2b that has been supplied to the image correction block 50b and a data enable signal delb, which indicates the valid period of the image data d2b, to the resolution detector 25. The data enable signal delb is also supplied to the image display unit as a data enable signal de_out. In this case, the LVDS receiver 11 can also supply the clock signal CLK2a and the image data d2a, which have been supplied to the image correction block 50a, and a data enable signal of the image data d2a (not shown).

[0041] Furthermore, the LVDS receiver 11 can receive image data that have been divided into two groups from two systems. At this time, the LVDS receiver 11 can supply the image data d2a and d2b to the image correction blocks 50a and 50b, respectively, without dividing them. In addition, the automatic image correction circuit 100 is not limited to the construction in which the image data d1 are received by a single LVDS receiver 11, but may have a construction in which image data divided into plural groups are received by a plurality of LVDS receivers.

[0042] The resolution detector 25 detects a horizontal resolution and a vertical resolution of the image data d2b from the clock signal CLK2b and the data enable signal delb, which are received from the LVDS receiver 11. The resolution detector 25 supplies the horizontal resolution and the vertical resolution of the image data d2b to the enhanced parameter selector 26 as resolution data k. Furthermore, the method of detecting a horizontal resolution and a vertical resolution in the resolution detector 25 will be described in detail below.

[0043] The enhanced parameter selector 26 generates a set value for image correction in the automatic image correction circuit 100 based on the resolution data k (i.e., the horizontal resolution and the vertical resolution of the image data d2b), which are received from the resolution detector 25. For example, the enhanced parameter selector 26 can calculate positional information of a region from which statistic values, which are used to perform image correction by the image correction blocks 50a and 50b, will be calculated (hereinafter simply referred to as a "sampling area"), from the horizontal resolution and the vertical resolution of the image data d2b. The sampling area is set to a position serving as a central region of an image. The calculated positional information of the sampling area is supplied as sampling area data Dsa_a and Dsa_b from the enhanced parameter selector 26 to the sum total data calculation units 16a and 16b. The enhanced parameter selector 26 can automatically perform a variety of settings, which were needed every resolution.

[0044] In another example of data generation of the enhanced parameter selector 26, a set value for correcting brightness is generated using the horizontal resolution and the vertical resolution of the image data d2b. The higher the resolution of an image, the smaller one pixel. It is, however, difficult to miniaturize a TFT element or a circuit for driving pixels accordingly in view of its electrical characteristics. Due to this, the aperture ratio of one pixel is lowered that much. It is therefore necessary to supplement lowered brightness according to a lowered aperture ratio by raising brightness as much as the aperture ratio is lowered. The enhanced parameter selector 26 calculates a coefficient for correcting such brightness (hereinafter simply referred to as a "lightness correction coefficient"), and supplies the generated lightness correction coefficient to correction amount calculation units 19a and 19b as set values Ds2a and Ds2b. Furthermore, the method of generating data in the enhanced parameter selector 26 will be described in detail below.

[0045] The automatic image correction circuit 100 performs an image correction process on the two image data groups d2a and d2b through the two blocks: the image correction block 50a and the image correction block 50b, respectively. That is, the automatic image correction circuit 100 performs an image correction process on the received image data d1 using a plurality of blocks. In particular, the image correction block 50a and the image correction block 50b calculate a gray level value histogram, a luminance sum total and a chroma sum total (i.e., "sum total data") with respect to each of the input image data d2a and d2b and supply the sum total data to the statistic value calculation unit 17. The statistic value calculation unit 17 calculates statistic values of the image data from the sum total data and supplies the calculated statistic value to the image correction blocks 50a and 50b, respectively. In addition, the image correction blocks 50a and 50b find a correction amount based on the statistic value received from the statistic value calculation unit 17 and perform an image correction process on the image data using the correction amount. Image data d6a and d6b, which have experienced the image correction process through the image correction block 50a and the image correction block 50b, are supplied to the multiplexer 21.

[0046] The multiplexer 21 generates image data d7 by combining two image data d6a and d6b into one, and outputs the generated image data d7 to an image display unit (not shown) such as a Liquid Crystal Display (LCD) panel. The image display unit (not shown) displays the image data d7 received from the multiplexer 21.

[0047] Furthermore, the automatic image correction circuit 100 can output the two image data d6a and d6b to the image display unit without combining them. In this case, the automatic image correction circuit 100 may not include the multiplexer 21, and the image data d6a and d6b respectively output from the image correction blocks 50a and 50b are supplied to the image display unit without change.

[0048] An image process that is executed in the image correction blocks 50a and 50b and the statistic value calculation unit 17 will be described in detail below.

[0049] The image correction block 50a includes a YUV converter 15a, a sum total data calculation unit 16a, a correction amount calculation unit 18a, an image correction unit 19a, and a RGB converter 20a. In the same manner, the image correction block 50b includes a YUV converter 15b, a sum total data calculation unit 16b, a correction amount calculation unit 18b, an image correction unit 19b, and a RGB converter 20b.

[0050] The image data d2a and the clock signal CLK2a are input to the YUV converter 15a. The input image data d2b and the clock signal CLK2b are input to the YUV converter 15b. The YUV converters 15a and 15b convert the RGB type image data d2a and d2b into YUV type image data (YUV conversion). The YUV converters 15a and 15b supply YUV-converted image data d3a and d3b, which are obtained by the YUV conversion, to the image correction units 19a and 19b, respectively, and also supply YUV converted image data d4a and d4b to the sum total data calculation units 16a and 16b, respectively.

[0051] The sum total data calculation units 16a and 16b calculate sum total data for the received image data d4a and d4b. In particular, the sum total data calculation units 16a and 16b calculate a sampling area, i.e., a central region of an image from the image data d4a and d4b by using the sampling area data Dsa_a and Dsa_b that are received from the enhanced parameter selector 26. The sum total data calculation units 16a and 16b calculate a luminance sum total and a chroma sum total while generating a gray level value histogram from the data of the sampling area of the image data d4a and d4b. The reason why only a central region of an image not the whole image is used, as described above, is that as a viewer usually sees a central region of an image, it is effective to perform an image correction process based on image data of the central region. Sum total data Sum_a and Sum_b calculated as described above are output to the statistic value calculation unit 17.

[0052] The statistic value calculation unit 17 calculates statistic values Sta_a and Sta_b with respect to luminance and chroma of the image data d4a and d4b on the basis of the received sum total data Sum_a and Sum_b. In particular, the statistic value calculation unit 17 calculates statistic values, such as the highest value and the lowest value of luminance, the mean values of luminance and chroma, and standard deviation of luminance.

[0053] The statistic values Sta_a and Sta_b calculated as described above are supplied to the correction amount calculation units 18a and 18b. The correction amount calculation units 18a and 18b calculate the intensity of correction for image data (i.e., a correction amount) based on the received statistic values Sta_a and Sta_b, and set values Ds1a and Ds1b, which are received from the enhanced parameter selector 26. In particular, the correction amount calculation units 18a and 18b calculate a level correction coefficient, a gamma correction amount, a contrast correction amount, and a chroma correction amount. Signals Corr_a and Corr_b corresponding to the calculated correction amounts are output to the image correction units 19a and 19b. Furthermore, the correction amount calculation units 18a and 18b perform scene detection on image data, while calculating the correction amount.

[0054] The image correction units 19a and 19b are supplied with the set values Ds2a and Ds2b from the enhanced parameter selector 26, the correction amounts Corr_a and Corr_b from the correction amount calculation units 18a and 18b, and the YUV-converted image data d3a and d3b from the YUV converters 15a and 15b. The image correction units 19a and 19b perform an image correction process on the image data d3a and d3b on the basis of the correction amounts Corr_a and Corr_b and the set values Ds2a and Ds2b. In particular, the image correction units 19a and 19b perform correction processes, such as level correction, gamma correction, contrast correction, and chroma correction, on the image data d3a and d3b. Image data d5a and d5b, which have experienced the image correction process, are output to the RGB converters 20a and 20b.

[0055] The RGB converters 20a and 20b convert the received image data d5a and d5b of YUV form into data of RGB form (i.e., "RGB conversion"). The RGB converters 20a and 20b supply the RGB-converted image data d6a and d6b to the multiplexer 21. The multiplexer 21 outputs the image data d7 that is obtained by combining the two image data d6a and d6b into one.

[0056] As described above, the automatic image correction circuit 100 according to the first embodiment includes the resolution detector 25 and the enhanced parameter selector 26. The resolution detector 25 can detect resolutions of received image data, and the enhanced parameter selector 26 can automatically calculate set values, such as a sampling area and a lightness correction coefficient, based on the detected resolutions. As a result, the automatic image correction circuit 100 can automatically perform a variety of settings, which were needed on a resolution basis in the related art, and can perform an image correction process appropriate for respective image data.

Method of Detecting Horizontal Resolution and Vertical Resolution

[0057] A method of detecting a horizontal resolution and a vertical resolution, which is performed in the resolution detector 25, will be described below with reference to Figs. 2 and 3.

[0058] Fig. 2 schematically shows the construction of the resolution detector 25 according to a first embodiment. The resolution detector 25 includes a horizontal resolution detection circuit 25h and a vertical resolution detection circuit 25v.

The data enable signal delb and the clock signal CLK2b, which are received from the LVDS receiver 11, are first input to the horizontal resolution detection circuit 25h. The horizontal resolution detection circuit 25h calculates a line end flag Lef using the clock signal CLK2b and a horizontal counter from the data enable signal delb. At this time, a horizontal resolution can be detected from a value of the horizontal counter. The line end flag Lef output from the horizontal resolution detection circuit 25h resets the counter of the horizontal resolution detection circuit 25h as a reset signal Lef_r and is simultaneously supplied to the vertical resolution detection circuit 25v. The horizontal resolution detection circuit 25h also calculates a frame end flag Fef and supplies the flag signal to the vertical resolution detection circuit 25v. The vertical resolution detection circuit 25v receives the line end flag Lef and the frame end flag Fef from the horizontal resolution detection circuit 25h, and also receives the clock signal CLK2b from the LVDS receiver 11. The vertical resolution detection circuit 25v detects a vertical resolution on the basis of these signals.

[0059] The signals, which are input to and output from the horizontal resolution detection circuit 25h and the vertical resolution detection circuit 25v, will be described in more detail with reference to the timing chart shown in Fig. 3.

[0060] Fig. 3 shows input and output signals in the resolution detection circuit 25 when detecting a horizontal resolution and a vertical resolution. (a) of Fig. 3 shows the data enable signal delb input to the horizontal resolution detection circuit 25h. (b) of Fig. 3 shows the line end flag Lef. (c) of Fig. 3 shows the frame end flag Fef. (d) of Fig. 3 shows the vertical counter. Figs. 3(e) to 3(g) show enlarged signals in one line period. (e) of Fig. 3 shows the clock signal CLK2b input to the horizontal resolution detection circuit 25h and the vertical resolution detection circuit 25v. (f) of Fig. 3 shows the image data d2b. (g) of Fig. 3 shows an enlarged signal of the data enable signal of (a) of Fig. 3 per one line period and also the valid period of the image data d2b shown in (f) of Fig. 3. (h) of Fig. 3 shows that the data enable signal of (g) of Fig. 3 is shifted by one counter. (i) of Fig. 3 shows the horizontal counter. (j) of Fig. 3 shows an enlarged signal of the line end flag Lef of (b) of Fig. 3 per one line period. (k) of Fig. 3 shows an enlarge signal of the vertical counter of (d) of Fig. 3 per one line period.

[0061] The horizontal resolution detection circuit 25h counts one line period from the rise to the fall of the data enable signal of (g) of Fig. 3 by using the horizontal counter of (i) of Fig. 3, according to the clock signal CLK2b of (e) of Fig. 3, and then generates the line end flag. In particular, the horizontal resolution detection circuit 25h generates a signal that is shifted by one counter from the data enable signal shown in (h) of Fig. 3, while counting 1 line period of the data enable signal of (g) of Fig. 3 using the horizontal counter, and then generates the line end flag Lef of (j) of Fig. 3 through a logical operation of the two signals. At this time, the value of the horizontal counter becomes a horizontal resolution (for example, the value can correspond to the value "640" of the horizontal counter in (i) of Fig. 3). The generated line end flag Lef is supplied to the vertical resolution detection circuit 25v. Furthermore, the value of the horizontal counter is reset according to the line end flag Lef. At this time, if the counter value of the horizontal counter reaches '2048', the horizontal resolution detection circuit 25h determines that the frame is ended and generates the frame end flag Fef shown in (c) of Fig. 3. The frame end flag Fef is supplied to the vertical resolution detection circuit 25v in the same manner as the line end flag Lef.

[0062] The vertical resolution detection circuit 25v counts the line end flag Lef received from the horizontal resolution detection circuit 25h by using the vertical counter of (k) of Fig. 3. The vertical resolution detection circuit 25v stops the counting of the line end flag Lef when the frame end flag Fef is received. The value of the vertical counter at that time becomes a vertical resolution (e.g., the value can correspond to the value "480" of the vertical counter in (d) of Fig. 3).

[0063] The horizontal resolution and the vertical resolution can be detected from the data enable signal delb and the clock signal CLK2b, as described above. Even in the case where the data enable signal dela and the clock signal CLK2a are used, a horizontal resolution and a vertical resolution can be obtained through this method.

Furthermore, the method of detecting a horizontal resolution and a vertical resolution in the resolution detector 25 is not limited to the above method. It is to be understood that the horizontal resolution and the vertical resolution can be detected by other methods. The horizontal resolution and the vertical resolution detected by the resolution detector 25 are supplied to the enhanced parameter selector 26 as the resolution data k.

Method of Calculating Sampling Area

[0064] The enhanced parameter selector 26 generates parameter data for performing the setting of image correction in the automatic image correction circuit 100 by using the resolutions detected by the resolution detector 25.

[0065] A method of calculating a sampling area in the enhanced parameter selector 26 will be first described. Fig. 4 shows an example of a sampling area. In Fig. 4, a sampling area Samp1 indicates a central region of an image G1. As stated above, the sum total data calculation units 16a and 16b calculate a luminance sum total and a chroma sum total while generating a gray level value histogram, from the data of the sampling area.

[0066] In Fig. 4, the length hsc of the image G1 in a horizontal direction is a horizontal resolution and the length vsc of the image G1 in a vertical direction is a vertical resolution. To automatically calculate the position or size of the sampling area Samp1, it is necessary to know the horizontal resolution and the vertical resolution of the image G1. Therefore, the enhanced parameter selector 26 calculates a position or size of a sampling area in an image through the following

method on the basis of the resolution data k received from the resolution detector 25, i.e., the horizontal resolution and the vertical resolution.

[0067] In Fig. 4, it is assumed that a point at the top left corner of the image G1 is a point G1a and a point at the bottom right corner, i.e., on a diagonal line of the point G1a is a point G1b. Assuming that a coordinate of the point G1a is a starting point, the axis pointing from the point G1a toward the right side of the image G1 in the horizontal direction is an X-axis, and the axis pointing from the point G1a toward the lower side of the image G1 in the vertical direction is a Y-axis. Assuming that the length of the image G1 in the horizontal direction is hsc and the length of the image G1 in the vertical direction is vsc, a coordinate of the point G1b at the bottom right corner of the image G1 is a point G1b (hsc, vsc). The position of the sampling area Samp1 can be found by deciding coordinates of two points on the diagonal line of the sampling area Samp1 on the image G1, e.g., a coordinate of each of a point Sala (Sa1a_x, Sa1a_y) and a point Sa1b (Sa1b_x, Sa1b_y) in Fig. 4. The method of calculating the sampling area will be described with reference to the example of Fig. 4.

[0068] In a first embodiment, the highest values of the powers of 2, which do not exceed the values of the horizontal resolution and the vertical resolution received from the resolution detector 25, respectively, are set to the length sh of the sampling area Samp1 in the horizontal direction and the length sv of the sampling area Samp1 in the vertical direction. When the highest values are converted to binary numbers, it is possible to detect only bits having a logic level 1, that is, bits set, and to reduce the size of the circuit. That is why the powers of 2 are used. Furthermore, the reason why the highest values are used is that a greater amount of data needs to be sampled in order to increase detection accuracy in each image.

[0069] The relation among the horizontal resolution hsc, the vertical resolution vsc, the length sh of the sampling area Samp1 in the horizontal direction, and the length sv of the sampling area Samp1 in the vertical direction is shown in Fig. 5. There is shown in Fig. 5 resolutions and the sizes of sampling areas. As described above, the length sh of the sampling area Samp1 in the horizontal direction, and the length sv of the sampling area Samp1 in the vertical direction are set to the highest values of the powers of 2, which do not exceed the values of the horizontal resolution hsc and the vertical resolution vsc, respectively. For example, assuming that the value of the horizontal resolution hsc is 640 dots and the value of the vertical resolution vsc is 480 dots, the length sh of the sampling area Samp1 in the horizontal direction is 512 dots, i.e., the highest value of the powers of 2, which does not exceed 640 dots. The length sv of the sampling area Samp1 in the vertical direction is 256 dots, i.e., the highest value of the powers of 2, which does not exceed 480 dots. By doing so, the length of the sampling area Samp1 in the horizontal direction and the length of the sampling area Samp1 in the vertical direction are decided based on the horizontal resolution and the vertical resolution. Practically, however, these values can be obtained by calculating the powers of 2 using a circuit and can also be found by maintaining a table indicating the relation between resolutions and the sizes of sampling areas in Fig. 5 and referring to the table from the resolutions received from the resolution detector 25.

[0070] Fig. 6 shows a detailed example. In this example, the lengths of sampling areas in horizontal directions and the lengths of the sampling areas in vertical directions are obtained with respect to the specifications of main resolutions through the above method. Furthermore, in Fig. 6, the term "sampling area ratio" indicates the ratio occupied by the sampling area, of the entire image. For example, in the case of SVGA specification, the value of the horizontal resolution hsc is 800 dots and the value of the vertical resolution vsc is 600 dots. At this time, the length sh of the sampling area in the horizontal direction is 512 dots and the length sv of the sampling area in the vertical direction is 512 dots. Therefore, the sampling area ratio is $512 \times 512 / 800 \times 600$, i.e., 0.55. Furthermore, in the case of SVGA specification, the value of the horizontal resolution hsc can be 820 dots. Even in this case, the length sh of the sampling area in the horizontal direction can be decided as 512 dots and the length sv of the sampling area in the vertical direction can be decided as 512 dots, from the table that indicates the relation between the resolutions and the sizes of the sampling area in Fig. 5. As can be seen from Fig. 6, 40% or more of an image can be sampled through this method.

[0071] The position of the sampling area is then decided. In the first embodiment, the coordinates of the point Sala (Sala_x, Sala_y) and the point Sa1b (Sa1b_x, Sa1b_y), which are defined as two points on the diagonal line of the sampling area on the image G1 can be decided using the following equations.

[0072]

$$\text{Sala_x} = (\text{hsc} - \text{sh}) / 2 \quad (1)$$

$$\text{Sala_y} = (\text{vsc} - \text{sv}) / 2 \quad (2)$$

$$Sa1b_x = Sala_x + sh \quad (3)$$

$$Sa1b_y = Sala_y + sv \quad (4)$$

[0073] Equations (1) to (4) are calculation equations for locating a sampling area at a central region of an image. In other words, the method of calculating the position of a sampling area is not limited to the above, but can include any calculation method of enabling a sampling area to be placed at a central region of an image.

[0074] Fig. 7 shows, as a concrete example, the position of a sampling area, which is obtained by the above-mentioned calculation method when the resolutions of an image supplied from the resolution detector 25 correspond to VGA specification (the value of the horizontal resolution hsc is 640 and the value of the vertical resolution vsc is 480). In this case, the length sh of the sampling area in the horizontal direction is 512 and the length sv of the sampling area in the vertical direction is 256 according to the table indicating the relation between the resolutions and the sizes of the sampling area in Fig. 5. Therefore, the coordinates of two points that decide the sampling area in the image G1 can be decided as a point Sala (64, 112) and a point Sa1b (576, 368) in accordance with Equations (1) to (4).

[0075] In the automatic image correction circuit 100 according to the first embodiment, the LVDS receiver 11 divides the image data d1 into two groups, and two blocks; the image correction block 50a and the image correction block 50b respectively perform an image correction process on the image data d2a and d2b, which are obtained by dividing the image data d1 into two groups. At this time, the LVDS receiver 11 divides the image data d1 into odd-numbered dot clocks and even-numbered dot clocks. Fig. 8A shows an example in which the LVDS receiver 11 divides the image data d1 into odd-numbered and even-numbered dot clocks. Image data GI2a corresponding to the even-numbered dot clock are input to the image correction block 50a and image data GI2b corresponding to the odd-numbered dot clock are input to the image correction block 50b.

[0076] At this time, the resolution detector 25 is supplied with the data enable signal de1b and the clock signal CLK2b of the image data GI2b that are input to the image correction block 50b. Therefore, the image data GI2b become a valid sampling pixel. Fig. 8B shows a case where the resolutions of the image data d1 correspond to UXGA specification (the horizontal resolution is 1600 dots and the vertical resolution is 800 dots). Fig. 8C shows the image data GI2b obtained by dividing image data d1 of UXGA specification. In this case, although the horizontal resolution is 1600 dots, the image data are divided upon sampling. Therefore, the sampling is performed in the image data GI2b in which the horizontal resolution is 800 dots. In particular, the length of a horizontal direction is 1024 dots and the length of a vertical direction is 1024 dots in a sampling area Samp2 of the image data d1, as shown in Fig. 8B, whereas the length of a horizontal direction is 512 dots and the length of the vertical direction is 1024 dots in a sampling area Samp3 of the image data GI2b, as shown in Fig. 8C. Therefore, the automatic image correction circuit 100 can thin out sampling data by 1/2.

[0077] By finding the point Sala and the point Sa1b from the horizontal resolution hsc, the vertical resolution vsc, the length sh of the sampling area in the horizontal direction, and the length sv of the sampling area in the vertical direction, as described above, the position of the sampling area can be automatically decided. Information on the position of the sampling area obtained as described above is supplied to the sum total data calculation units 16a and 16b as the sampling area data Dsa_a and Dsa_b.

Method of Calculating Lightness Correction Coefficient

[0078] A method of calculating a lightness correction coefficient in the enhanced parameter selector 26 will now be described.

[0079] Figs. 9A and 9B show exemplary schematic diagrams of pixels of liquid crystal apparatuses. Fig. 9A shows the pixel of the liquid crystal apparatus with a low resolution and Fig. 9B shows the pixel of the liquid crystal apparatus with a high resolution. As shown in Fig. 9A, one pixel Sga of the liquid crystal apparatus includes a source line 201a that supplies a signal voltage to the pixel SGa in order to drive liquid crystal of a pixel SGa, a TFT element 203a that controls the current, which is supplied from the source line 201a to the pixel SGa, and a gate line 202a that supplies a control current to the TFT element 203a. In the liquid crystal apparatus with a high resolution, it is necessary to make small the area of the pixel SGa. However, the TFT element 203a, the source line 201a, and the gate line 202a cannot be made small at the same rate as the pixel SGa. This is because if these elements and circuit are made small at the same rate as the pixel SGa, electrical characteristics are deteriorated. Therefore, as shown in Fig. 9B, in the liquid crystal apparatus with a high resolution, the ratio occupied by the TFT element 203b, the source line 201b, and the gate line 202b, in the total area of the pixel SGb, becomes high. For this reason, in the liquid crystal apparatus with a high resolution, the aperture ratio of a pixel is lowered, which results in decreased brightness. In a display apparatus employing

a TFT element board, such an organic EL apparatus, the aperture ratio is also lowered.

[0080] Therefore, in a first embodiment, an image correction operation for supplementing decreased brightness, which is incurred by the reduction in the aperture ratio of a pixel in an image with a high resolution, is performed. In particular, a coefficient, i.e., a lightness correction coefficient for supplementing such decrease in brightness using a horizontal resolution and a vertical resolution of image data, which are detected by the resolution detector 25, is calculated.

[0081] Fig. 10 is a table listing the resolutions of main specifications, which are detected by the resolution detector 25, aperture ratios at that time, and lightness correction coefficients suitable for supplementing a decrease in brightness. The table of resolutions and lightness correction coefficients shown in Fig. 10 is previously maintained in the enhanced parameter selector 26. The enhanced parameter selector 26 then selects an appropriate lightness correction coefficient from the table of the resolutions and the lightness correction coefficients of Fig. 10 based on a horizontal resolution and a vertical resolution of image data, which are detected by the resolution detector 25. In this case, as the aperture ratio becomes low, the lightness correction coefficient becomes high since it is necessary to increase the brightness of image data. For example, when the image data correspond to UXGA specification with a high resolution (a horizontal resolution is 1600 dots and a vertical resolution is 1200 dots), the aperture ratio drops to 60% since the ratio occupied by the above-mentioned elements and circuit is increased, as shown in Fig. 10. Therefore, an appropriate lightness correction coefficient for supplementing such decrease in brightness is 1.5.

[0082] The lightness correction coefficients calculated in the above-mentioned manner are supplied to the image correction units 19a and 19b as the set values Ds2a and Ds2b. However, the calculated lightness correction coefficients can be supplied to the image correction units 18a and 18b as the set values Ds1a and Ds1b. Therefore, the automatic image correction circuit 100 can automatically correct the brightness of an image according to the lightness correction coefficients, and can display an image at a proper brightness every resolution.

[0083] In the first embodiment, the automatic image correction circuit having two image correction blocks has been described. The invention is, however, not limited to the above embodiment. The resolution correction unit and the enhanced parameter selector can be assembled even in an automatic image correction circuit having one image correction block. Furthermore, in the first embodiment, a sampling area and a lightness correction coefficient have been described as enhanced parameters. The invention is, however, not limited to the above example. A user can decide enhanced parameters, such as other image correction coefficients using detected resolutions of image data.

Second Embodiment

[0084] In a second embodiment, the above-described resolution detector is further provided outside the automatic image correction circuit 100 according to the first embodiment so that images can be automatically enlarged or reduced.

[0085] Fig. 11 is a block diagram of an automatic image correction circuit 500 according to a second embodiment of the invention.

[0086] The automatic image correction circuit 500 includes the automatic image correction circuit 100 according to the first embodiment, an image magnification processor 110 that enlarges an image, an image reduction processor 120 that reduces an image, an image display device 130, and a resolution detector 25.

[0087] The input side of the automatic image correction circuit 100 is connected to the image magnification processor 110. The output side of the automatic image correction circuit 100 is connected to the image reduction processor 120.

[0088] The image display device 130 is connected to the image reduction processor 120. The resolution detector 25 is connected to the image magnification processor 110 and the image reduction processor 120.

[0089] The resolution detector 25 detects the horizontal resolution and the vertical resolution of received image data d0 from a clock signal CLK0 and a data enable signal de0 of the received image data d0. The resolution detector 25 has the display size of the image display unit 130 previously stored therein. If the resolutions are smaller than the display size, the resolution detector 25 supplies a control signal S_out1 to the image magnification processor 110 so that the magnification process can be performed. If the resolutions are greater than the display size of the image display unit 130, the resolution detector 25 supplies a control signal S_out2 to the image reduction processor 120 so that the reduction process can be performed.

[0090] If the control signal S_out1 is received from the resolution detector 25, the image magnification processor 110 performs the image magnification process on the received image data d0 and supplies the processed result to the automatic image correction circuit 100 as image data D_in1.

[0091] If the control signal S_out2 is received from the resolution detector 25, the image reduction processor 120 performs the image reduction process on the image data D_out1 received from the automatic image correction circuit 100 and outputs the processed result to the image display apparatus 130 as image data D_out2.

[0092] In the case where image data are enlarged or reduced by using the automatic image correction circuit 500, the automatic image correction circuit 100 performs an enhancement process on the image data after the magnification process or before the reduction process. This is because, in the case of the image magnification process, it is appropriate to perform the enhancement process after information of original image data is enlarged. Meanwhile, this is because,

in the case of the image reduction process, it is appropriate to perform the reduction process on the image data after the enhancement process is performed. For this reason, in the automatic image correction circuit 500 according to the second embodiment, the image magnification processor 110 is connected to the input side of the automatic image correction circuit 100 and the image reduction processor 120 is connected to the output side of the automatic image correction circuit 100.

[0093] The method of enlarging or reducing image data in the image magnification processor 110 or the image reduction processor 120 will be described below in detail. In the case where the magnification process or the reduction process is performed on received image data, image data after the process need to be found by interpolation from image data of a lattice point around the received image data on the received image data. Hereinafter, three kinds of methods including the nearest neighbor interpolation method, the bi-linear interpolation method and the cubic convolution interpolation method will be described as several examples of the method of finding image data after conversion.

[0094] It is assumed that coordinates of image data after conversion, i.e., coordinates of points of a pixel to be interpolated are (u, v) and image data after conversion is P. It is also assumed that pixels of image data before conversion are sequentially numbered in order of a X direction and a Y direction, the number of the X direction is i, the number of the Y direction is j, and the positions of the pixels at these points are indicated by P_{ij}.

[0095] Fig. 12A schematically shows a case where the nearest neighbor interpolation method is applied. As shown in Fig. 12A, in the nearest neighbor interpolation method, image data that are the nearest to a point to be interpolated are decided as image data after conversion. For instance, in this method, information of one pixel of pixel data is allocated to four pixels without change and the allocated information are then represented as information of the pixels after magnification. This can be expressed in the following Equations (5) to (7).

$$P = P_{ij} \quad (5)$$

$$i = [u + 0.5] \quad (6)$$

$$j = [v + 0.5] \quad (7)$$

[0097] This method is advantageous in that input image data can be kept intact and an algorithm can be simplified although error of a maximum 1/2 pixel occurs.

[0098] Fig. 12B schematically shows a case where the bi-linear interpolation method is applied. As shown in Fig. 12B, in the bi-linear interpolation method, interpolation is carried out using image data of four points around a point to be interpolated in accordance with Equations (8) to (10).

[0099]

$$\begin{aligned} P = & \{ (i + 1) - u \} \{ (j + 1) - v \} P_{ij} \\ & + \{ (i + 1) - u \} \{ v - j \} P_{i,j+1} \\ & + (u - i) \{ (j + 1) - v \} P_{i+1,j} \\ & + (u - i) (v - j) P_{i+1,j+1} \end{aligned} \quad (8)$$

$$i = [u] \quad (9)$$

$$j = [v] \quad (10)$$

[0100] This method is advantageous in that an image can be smoothed because of averaging.

[0101] Fig. 12C schematically shows a case where the cubic convolution interpolation method is applied. As shown in Fig. 12C, in the cubic convolution interpolation method, interpolation is performed using image data of 16 points around a point to be interpolated. In this method, after image data of the point to be interpolated are found, images data of four points, which are the nearest to the point to be interpolated, of the image data of the 16 points, are more weighted than image data of 12 points that surround the image data of the four points. This can be expressed in the following Equations (11) to (13).

[0102]

$$P = [f(y_1) \ f(y_2) \ f(y_3) \ f(y_4)] \begin{bmatrix} P_{11} & P_{12} & P_{13} & P_{14} \\ P_{21} & P_{22} & P_{23} & P_{24} \\ P_{31} & P_{32} & P_{33} & P_{34} \\ P_{41} & P_{42} & P_{43} & P_{44} \end{bmatrix} \begin{bmatrix} f(x_1) \\ f(x_2) \\ f(x_3) \\ f(x_4) \end{bmatrix} \quad (11)$$

$$f(t) = \sin(\pi t) / (\pi t)$$

$$\approx \begin{cases} 1 - 2|t|^2 + |t|^3 \\ 4 - 8|t| + 5|t|^2 - |t|^3 \\ 0 \end{cases} \quad (12)$$

$$\begin{cases} x_1 = 1 + (u - [u]) & y_1 = 1 + (v - [v]) \\ x_2 = (u - [u]) & y_2 = (v - [v]) \\ x_3 = 1 - (u - [u]) & y_3 = 1 - (v - [v]) \\ x_4 = 2 - (u - [u]) & y_4 = 2 - (v - [v]) \end{cases} \quad (13)$$

[0103] This method is advantageous in that an image can be smoothed and sharpened.

[0104] The image magnification processor 110 or the image reduction processor 120 uses the above-described method and can thus obtain image data after magnification conversion or reduction conversion from input image data. The invention is, however, not limited to the above method, but can include other methods capable of finding image data after magnification conversion or reduction conversion.

[0105] The image magnification/reduction processes will be described below with reference to the flowchart of Fig. 13. The resolution detector 25 detects a horizontal resolution and a vertical resolution of the image data d0 from a clock signal CLK0 and the data enable signal de0 of the image data d0, which are input to the automatic image correction circuit 500 (step S1). The resolution detector 25 determines whether the detected resolutions are greater than a display size of the image display unit 130 (step S2). If it is determined that the detected resolutions are greater than the display size of the image display unit 130 (step S2: Yes), the resolution detector 25 supplies the control signal S_out2 to the image reduction processor 120 so that the image reduction process can be performed. On the other hand, the image

magnification processor 110 outputs the image data d0 as the image data D_in1 without performing any process. Thereafter, the image data D_in1 are input to the automatic image correction circuit 100 and then undergo the enhancement process (step S3). The image reduction processor 120 receives the image data D_out1, which have experienced the enhancement process through the image correction circuit 100, performs the image reduction process on the received image data D_out1 and outputs the processed result to the image display device as the image data D_out2 (step S4).

[0106] Meanwhile, if it is determined that the detected resolutions of the image data d0 are smaller than the display size of the image display unit 130 (step S2: No), the resolution detector 25 supplies the control signal S_out1 to the image magnification processor 110 so that the magnification process can be performed. The image magnification processor 110 performs the magnification process on the image data d0 and outputs the processed result to the image correction circuit 100 as the image data D_in1 (step S5). Thereafter, the image data D_in1 are input to the image correction circuit 100 and then undergo the enhancement process (step S6). The image reduction processor 120 receives the image data D_out1, which have experienced the enhancement process, from the image correction circuit 100, and then outputs the image data D_out1 to the image display apparatus 130 as the image data D_out2 without performing any process. As described above, the resolutions of the image data are detected, and the detected resolutions are compared with the size of the display panel. It is thus possible to automatically decide which one of the magnification process and the reduction process will be performed.

Electronic apparatus

[0107] Hereinafter, an example of an electronic apparatus to which the automatic image correction circuit 100 or 500 of the invention is applied will be described. Fig. 14 schematically shows an overall construction of an electronic apparatus to which the invention is applied. The electronic apparatus shown in Fig. 14 includes a liquid crystal display apparatus 700 as an image display unit, and a control unit 410 that controls the liquid crystal display apparatus 700. In this case, the liquid crystal display apparatus 700 is shown with it being conceptually divided into a panel structure 403 and a driving circuit 402 comprised of a semiconductor IC, etc. The automatic image correction circuit 100 or 500 of the invention can be disposed within the driving circuit 402. The control unit 410 includes a display information output source 411, a display information processing circuit 412, a power supply circuit 413, and a timing generator 414.

[0108] The display information output source 411 includes a memory such as Read Only Memory (ROM) or Random Access Memory (RAM), a storage unit such as a magnetic recording disk or an optical recording disk, and a tuning circuit that outputs a digital image signal in a synchronous manner. The display information output source 411 is constructed to supply display information, such as an image signal of a predetermined format, to the display information processing circuit 412 according to various clock signals generated by the timing generator 414.

[0109] The display information processing circuit 412 includes a variety of known circuits, such as a serial/parallel conversion circuit, an amplification/inversion circuit, a rotation circuit, a gamma correction circuit, and a clamp circuit. The display information processing circuit 412 processes received display information, and supplies the processed image information to the driving circuit 402 along with a clock signal CLK. The driving circuit 402 includes a scanning line driving circuit, a data line driving circuit, and a test circuit. Furthermore, the power supply circuit 413 supplies a predetermined voltage to each of the above-mentioned elements.

[0110] Concrete examples of the electronic apparatus to which the invention is applied will be described with reference to Figs. 15A to 15B.

[0111] An example in which the automatic image correction circuit 100 or 500 according to the invention is applied to a portable personal computer (so-called a notebook computer) will be described. Fig. 15A is a perspective view illustrating the construction of the personal computer. As shown in Fig. 15A, the personal computer 710 includes a main body 712 having a keyboard 711, and a display unit 713 to which a liquid crystal display panel according to the invention is applied.

[0112] An example in which the automatic image correction circuit 100 or 500 according to the invention is applied to a portable telephone will be described below. Fig. 15B is a perspective view illustrating the construction of the portable telephone. As shown in Fig. 15B, the portable telephone 720 includes a plurality of manipulation buttons 721, an earpiece 722, a mouthpiece 723, and a display unit 724 using a liquid crystal apparatus according to the invention.

[0113] Furthermore, electronic apparatuses to which the automatic image correction circuit 100 according to the invention can be applied may include a liquid crystal television, a video phone, and so on.

Claims

1. An automatic image correction circuit that automatically performs image correction on received image data, comprising:

a resolution detection unit that detects resolution of the image data;

a set value calculation unit that calculates a set value to be used in the image correction based on the resolutions;
and
an image correction unit that performs the image correction on the image data based on the set value.

5 **2.** The automatic image correction circuit according to Claim 1, wherein the set value calculation unit calculates a set value of a position of a sampling area, which is a part or the entire of the image data.

10 **3.** The automatic image correction circuit according to Claim 2, wherein the set value calculation unit calculates the position of the sampling area, which is a part or the entire of the image data, on the basis of a horizontal resolution and a vertical resolution so that the sampling area is located at a central region of an image.

15 **4.** The automatic image correction circuit according to Claim 2, wherein the set value calculation unit sets the range of the sampling area, which is a part or the entire of the image data, to a value that is a powers of 2.

20 **5.** The automatic image correction circuit according to Claim 1, wherein the set value calculation unit calculates a lightness correction coefficient based on a horizontal resolution and a vertical resolution of the image data in a set value for correcting a brightness of the image data.

25 **6.** The automatic image correction circuit according to Claim 1, further comprising:

30 a storage unit that stores the size of a display panel;
 a resolution comparison unit that compares the size of the display panel and the resolutions of the image data;
 an image magnification process unit that magnifies the image data; and
 an image reduction process unit that reduces the image data,

35 wherein the image correction unit performs image correction on image data that are obtained by reducing the image data by the image reduction process unit when the size of the display panel is smaller than the resolution of the image data, and performs image correction on image data that are enlarged by the image magnification process unit when the size of the display panel is larger than the resolution of the image data.

40 **7.** An electronic apparatus comprising:

45 the automatic image correction circuit according to Claims 1; and
 an image display unit that displays image data on which image correction is performed by the automatic image correction circuit.

FIG. 1

100

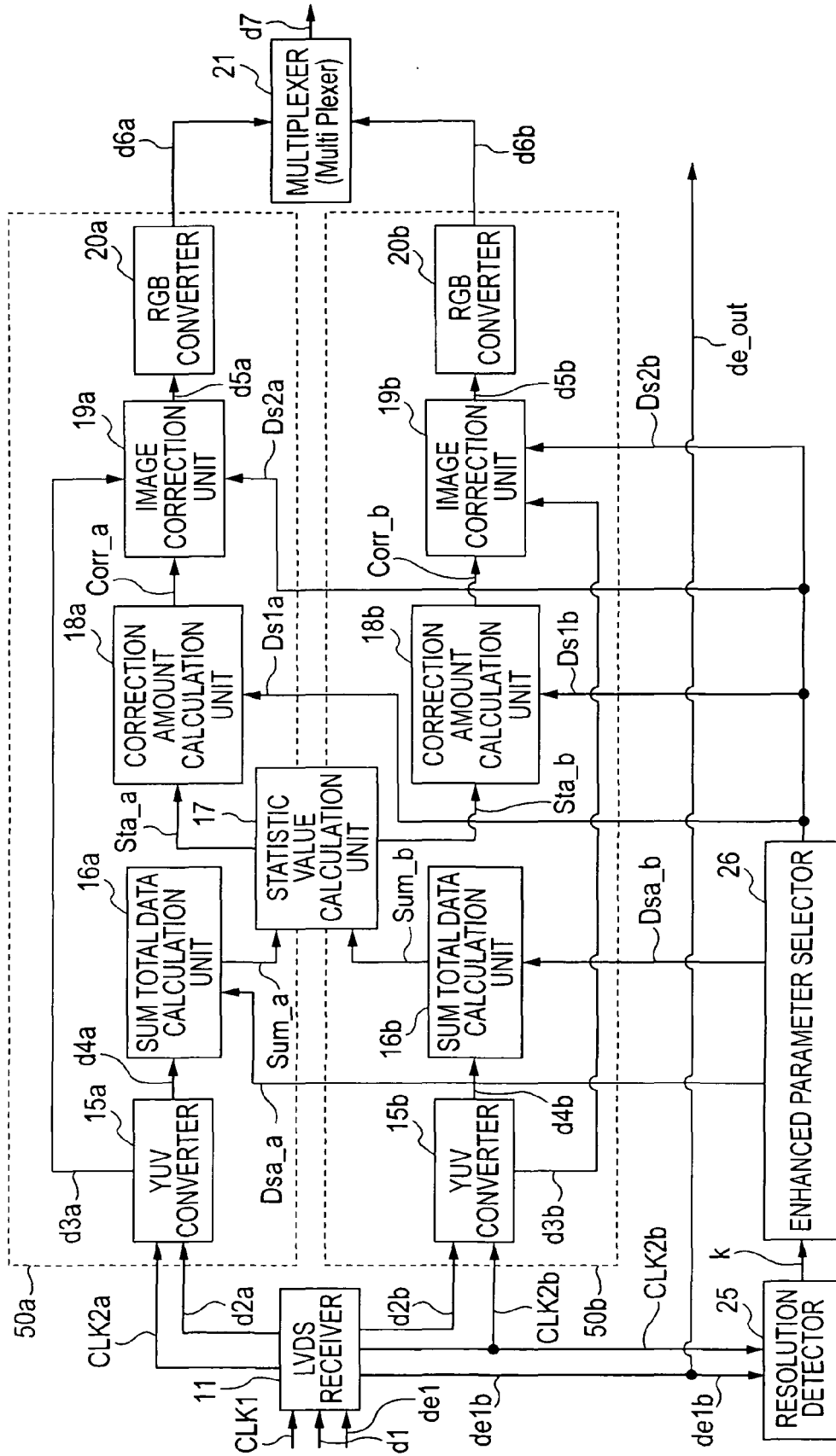


FIG. 2

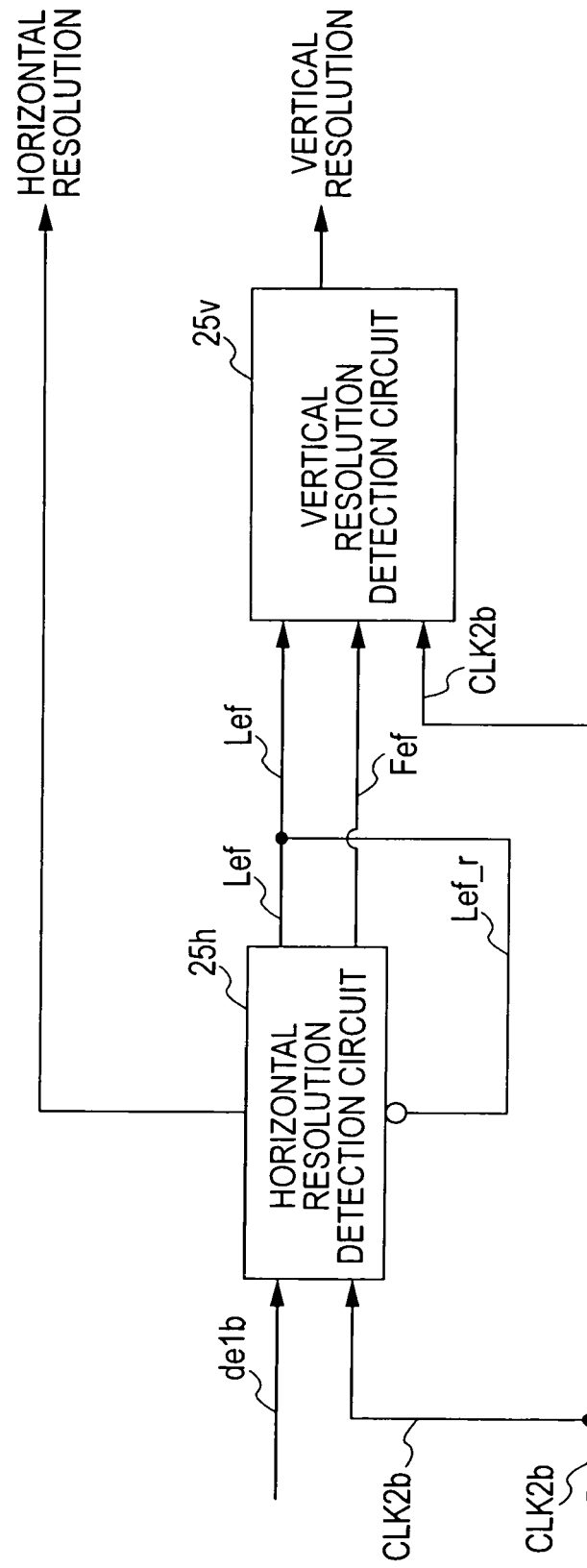
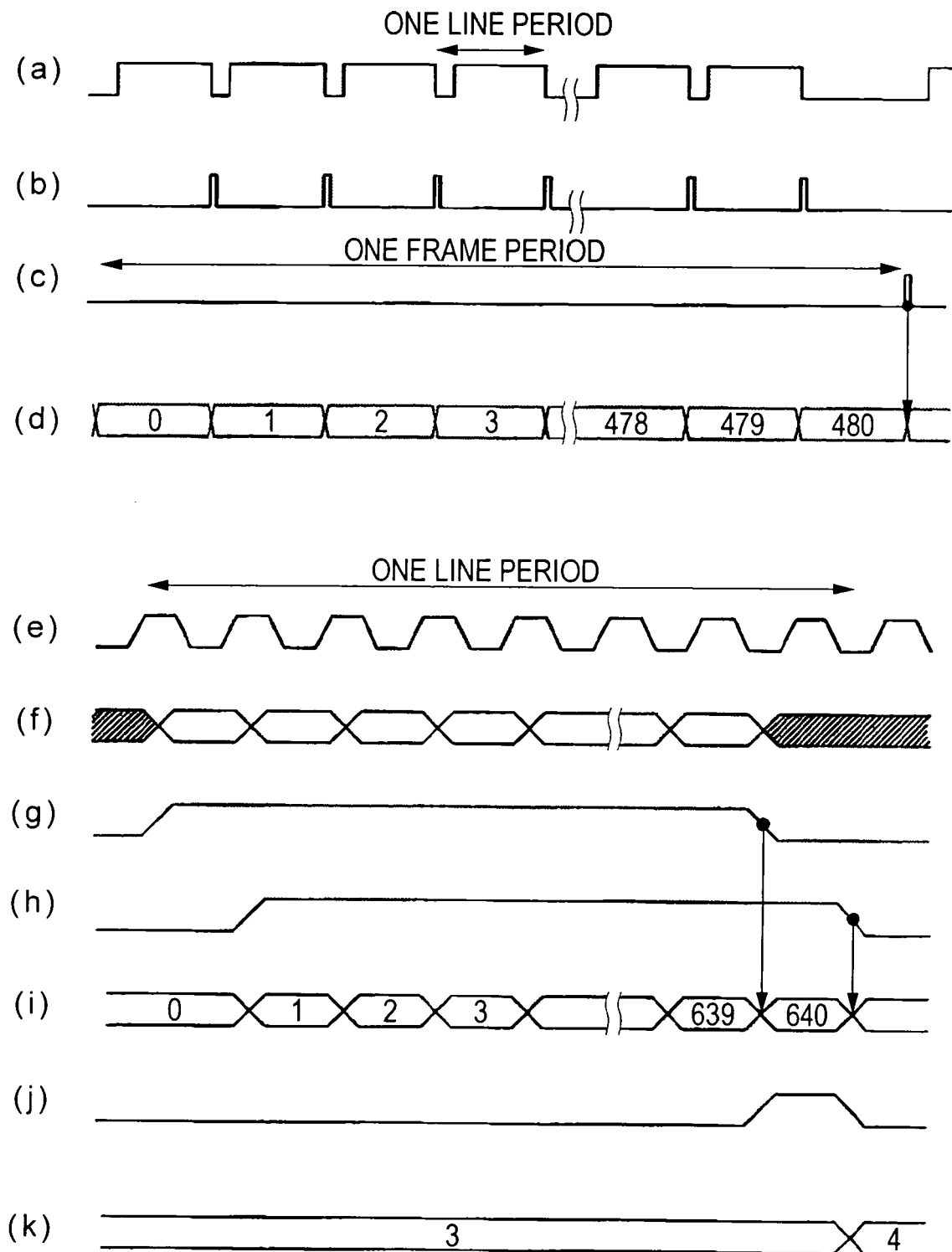
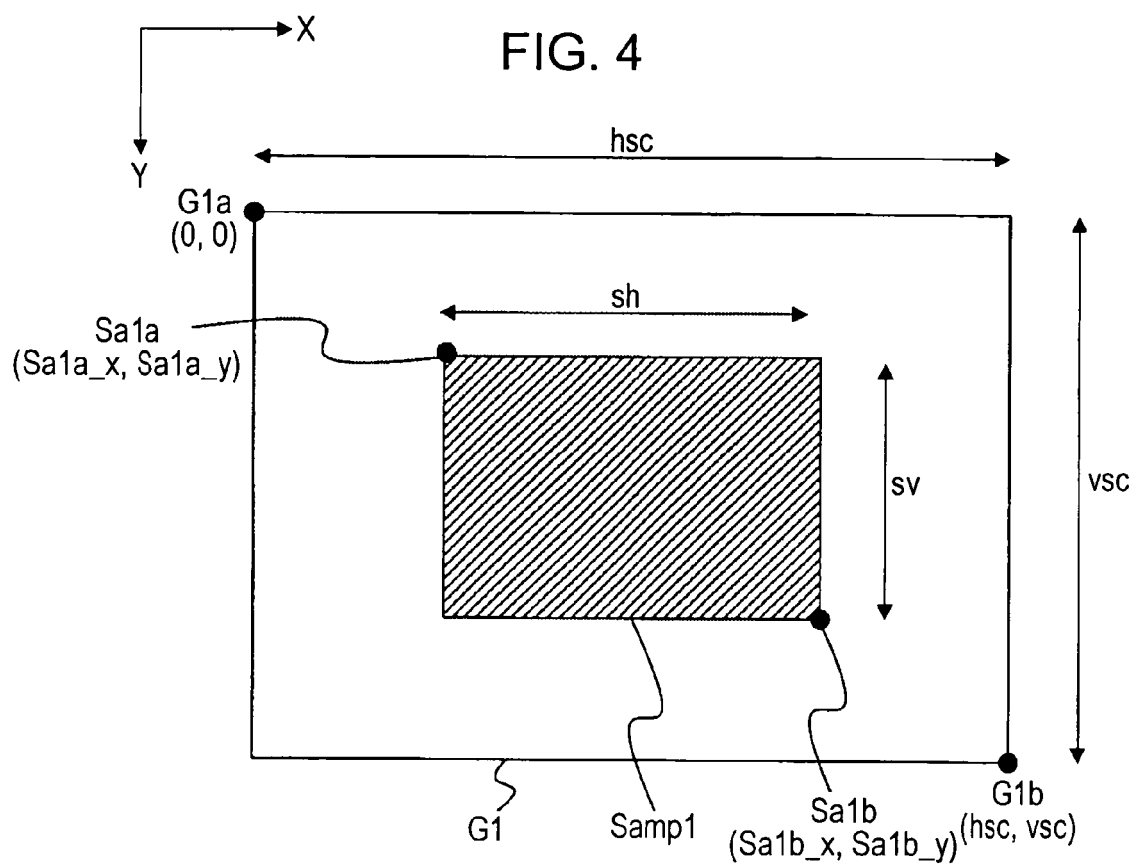


FIG. 3



**FIG. 5**

HORIZONTAL RESOLUTION hsc [dot]	LENGTH sh OF SAMPLING AREA IN HORIZONTAL DIRECTION [dot]	VERTICAL RESOLUTION vsc [dot]	LENGTH vh OF SAMPLING AREA IN VERTICAL DIRECTION [dot]
—	—	—	—
—	—	256 TO 511	256
512 TO 1023	512	512 TO 1023	512
1024 TO 1600	1024	1024 TO 1600	1024

FIG. 6

SPECIFICATION	HORIZONTAL RESOLUTION hsc [dot]	VERTICAL RESOLUTION vsc [dot]	LENGTH sh OF SAMPLING AREA IN HORIZONTAL DIRECTION [dot]	LENGTH vh OF SAMPLING AREA IN VERTICAL DIRECTION [dot]	SAMPLING AREA RATIO
VGA	640	480	512	256	0. 43
SVGA	800	600	512	512	0. 55
XGA	1024	768	1024	512	0. 67
WXGA	1280	768	1024	512	0. 53
WXGA+	1366	768	1024	512	0. 50
SXGA	1280	1024	512	1024	0. 80
SXGA+	1400	1050	512	1024	0. 71
UXGA	1600	1200	512	1024	0. 55

FIG. 7

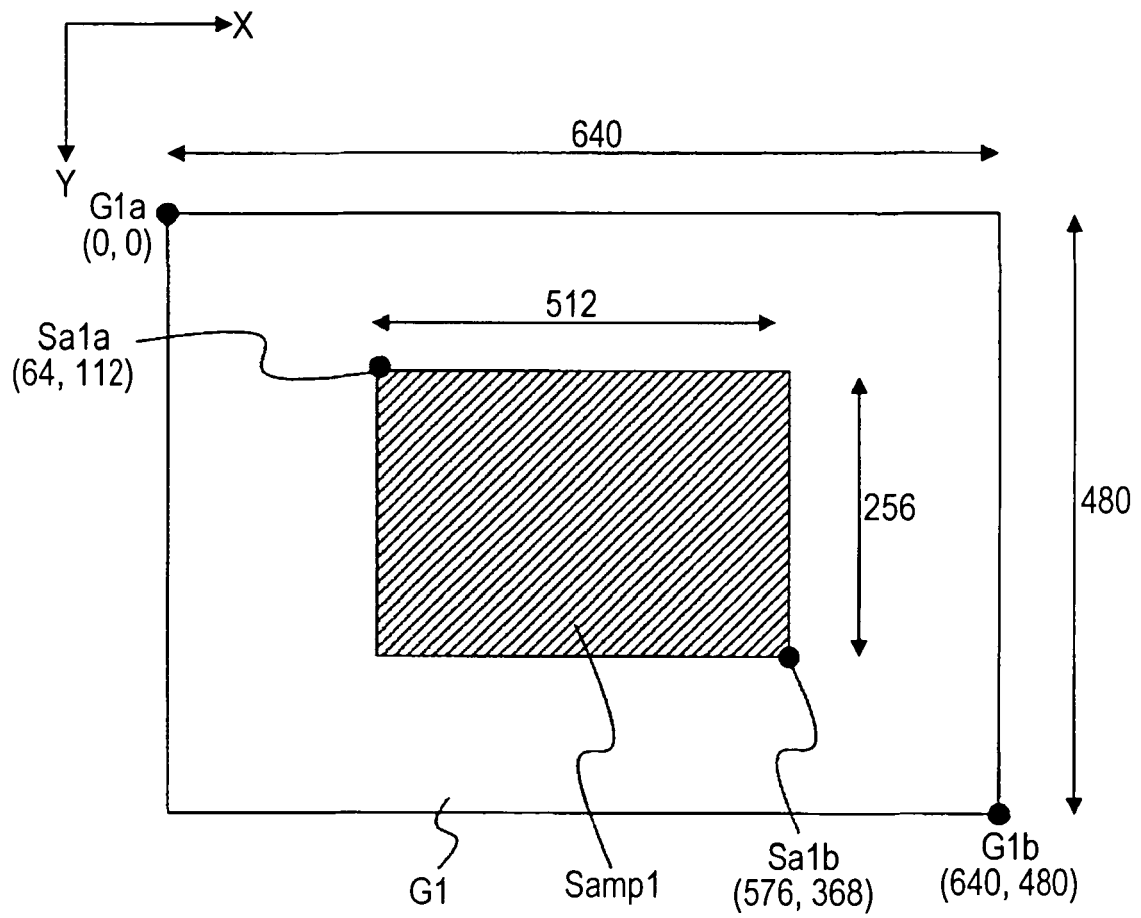


FIG. 8A

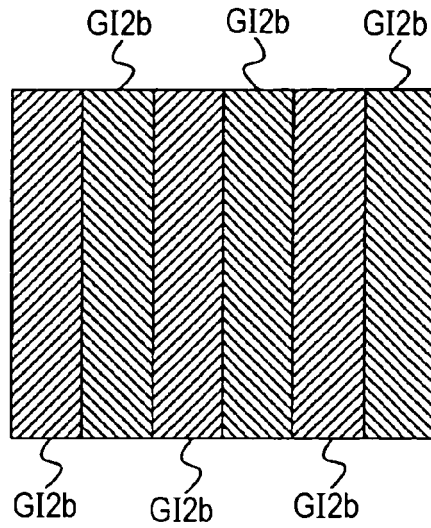


FIG. 8B

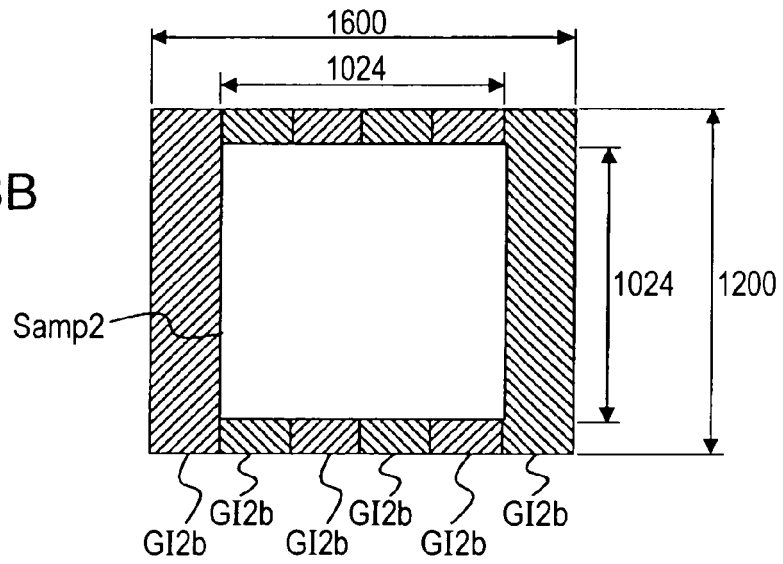


FIG. 8C

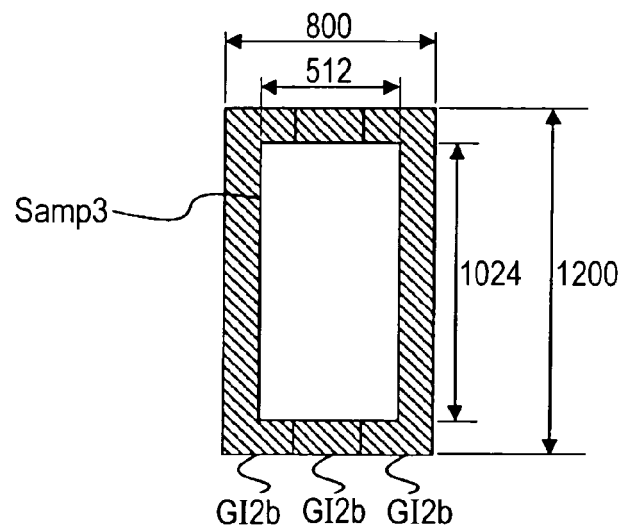


FIG. 9A

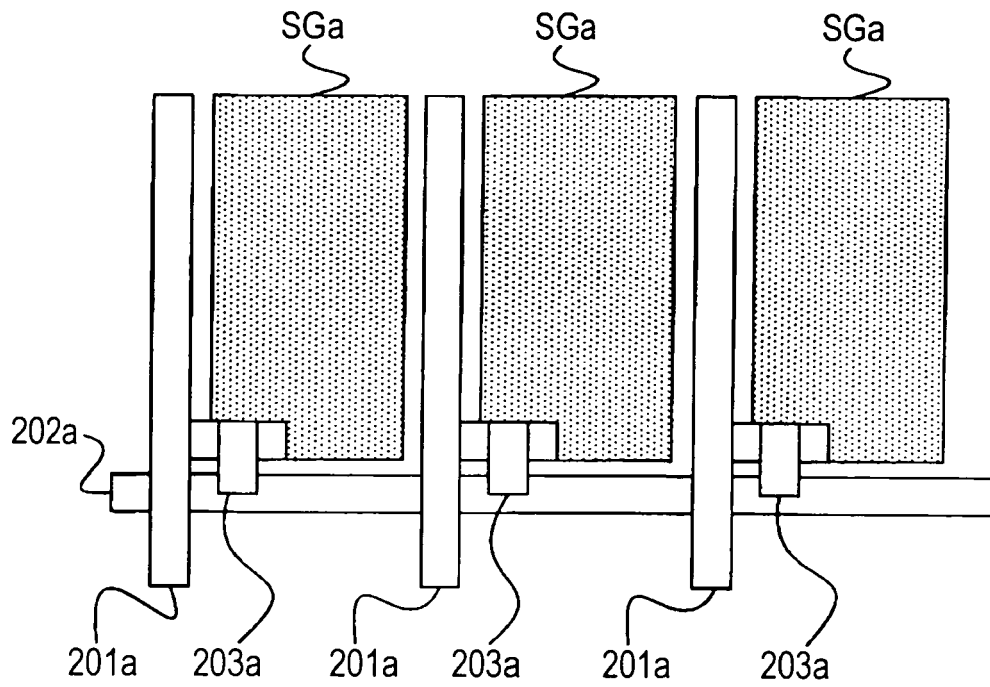


FIG. 9B

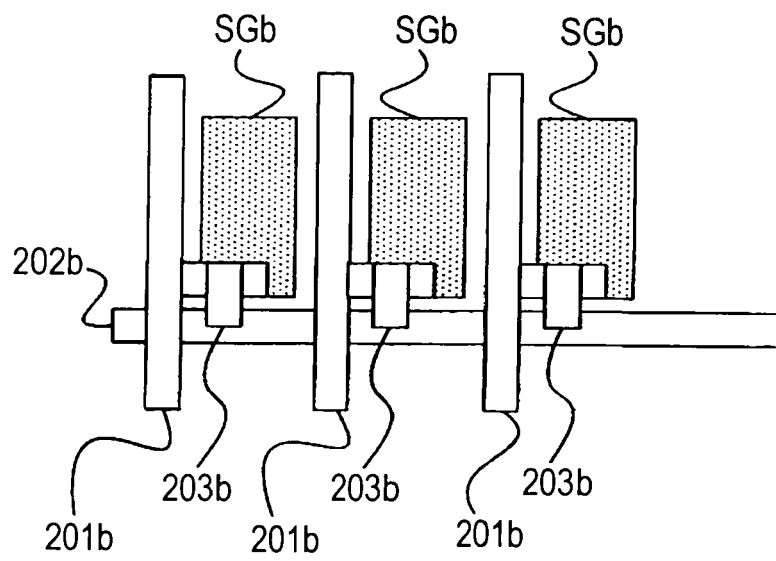


FIG. 10

SPECIFICATION	HORIZONTAL RESOLUTION hsc [dot]	VERTICAL RESOLUTION vsc [dot]	APERTURE RATIO [%]	LIGHTNESS CORRECTION INTENSITY (COEFFICIENT)
VGA	640	480	95	0.8
SVGA	800	600	90	0.83
XGA	1024	768	80	0.90
WXGA	1280	768	75	1.0
WXGA+	1366	768	75	1.0
SXGA	1280	1024	70	1.2
SXGA+	1400	1050	70	1.2
UXGA	1600	1200	60	1.5

FIG. 11

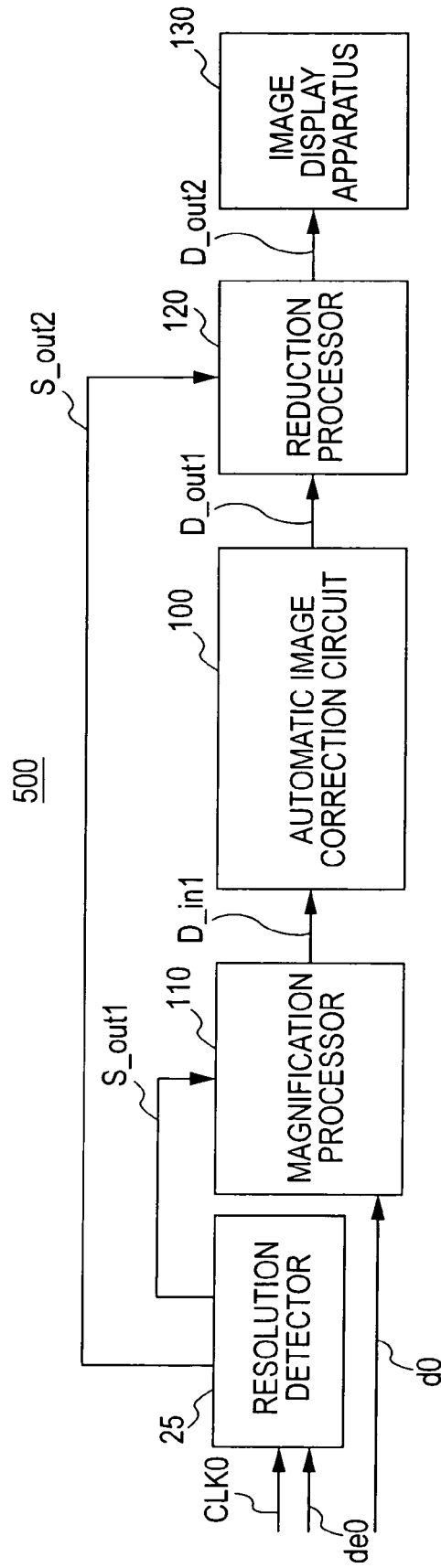


FIG. 12A

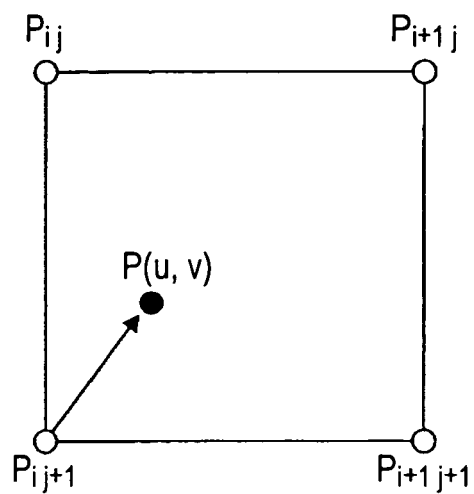


FIG. 12B

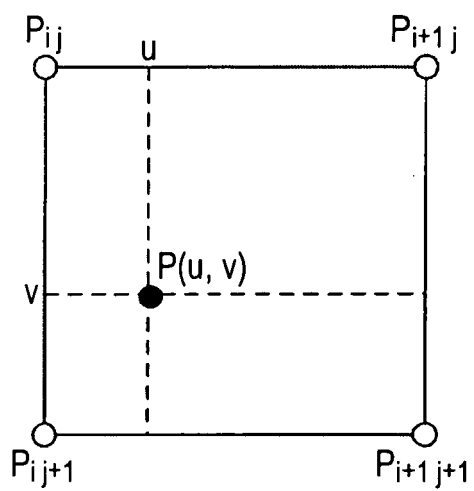


FIG. 12C

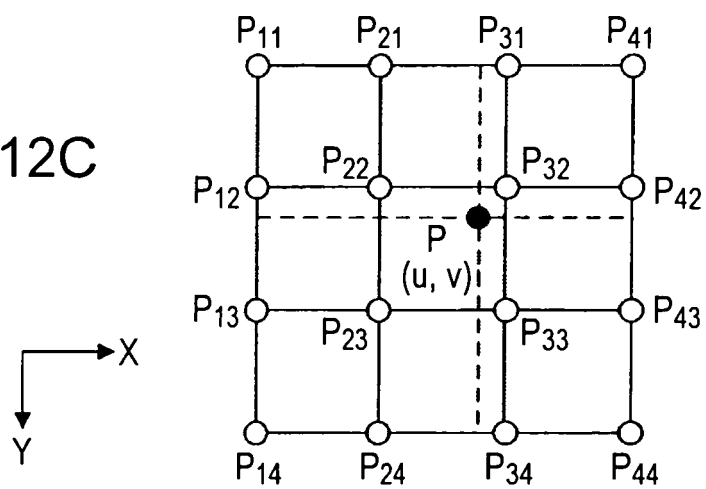


FIG. 13

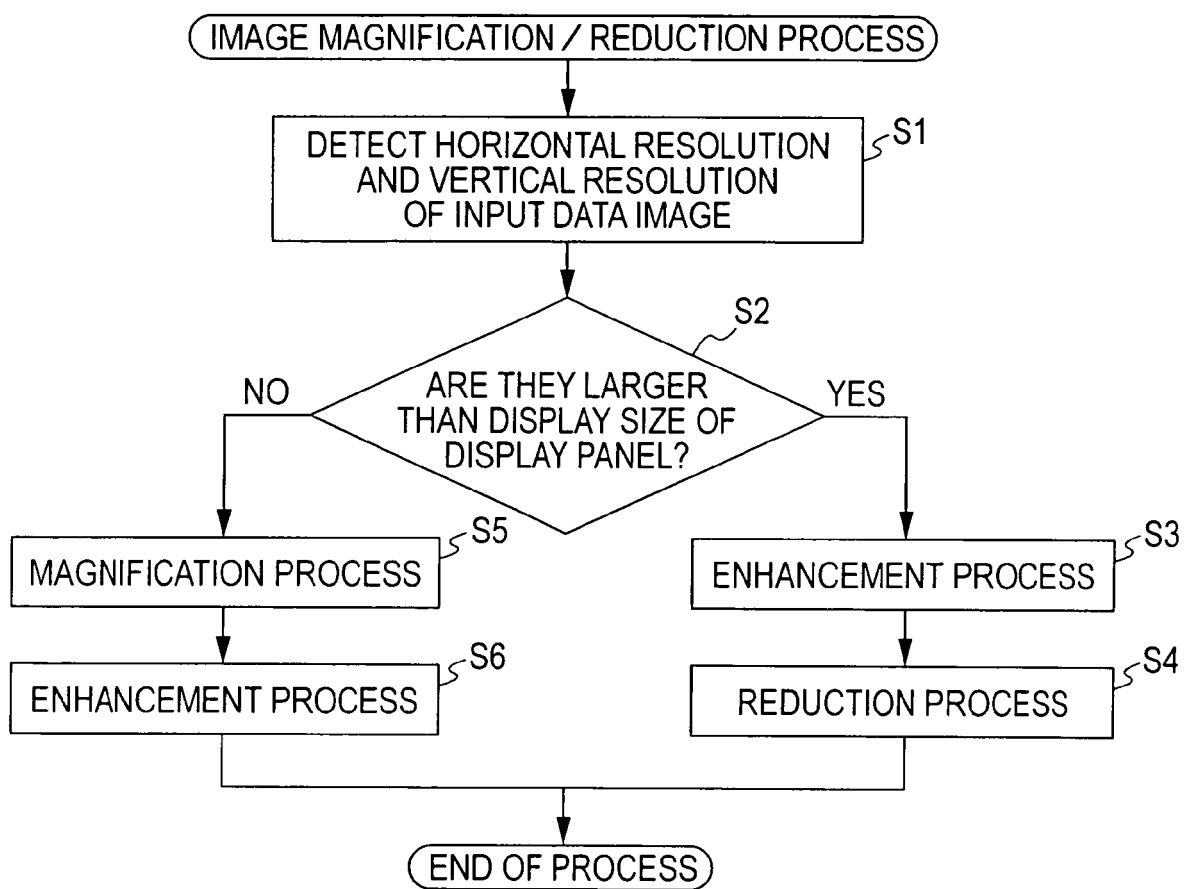


FIG. 14

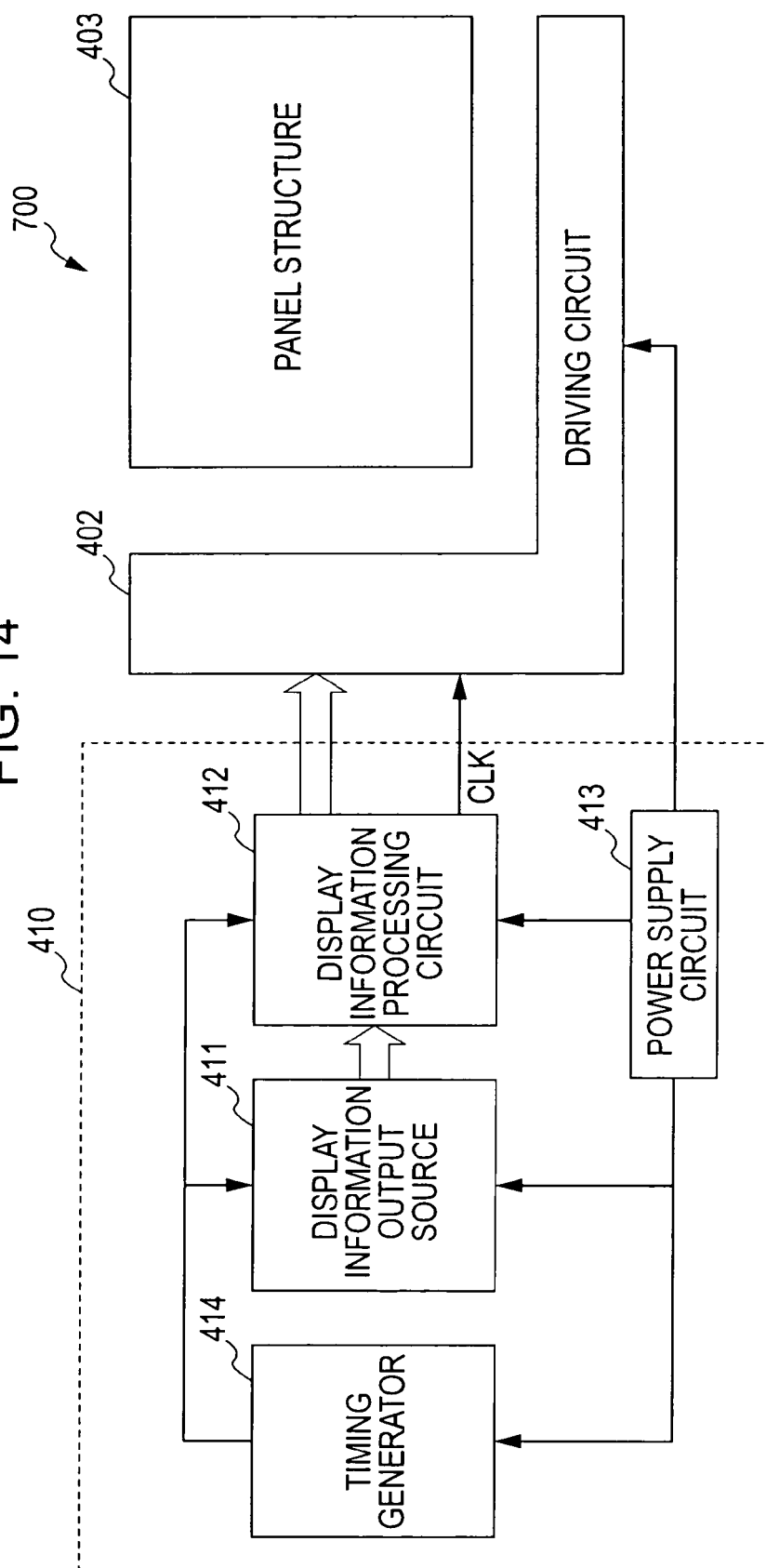


FIG. 15A

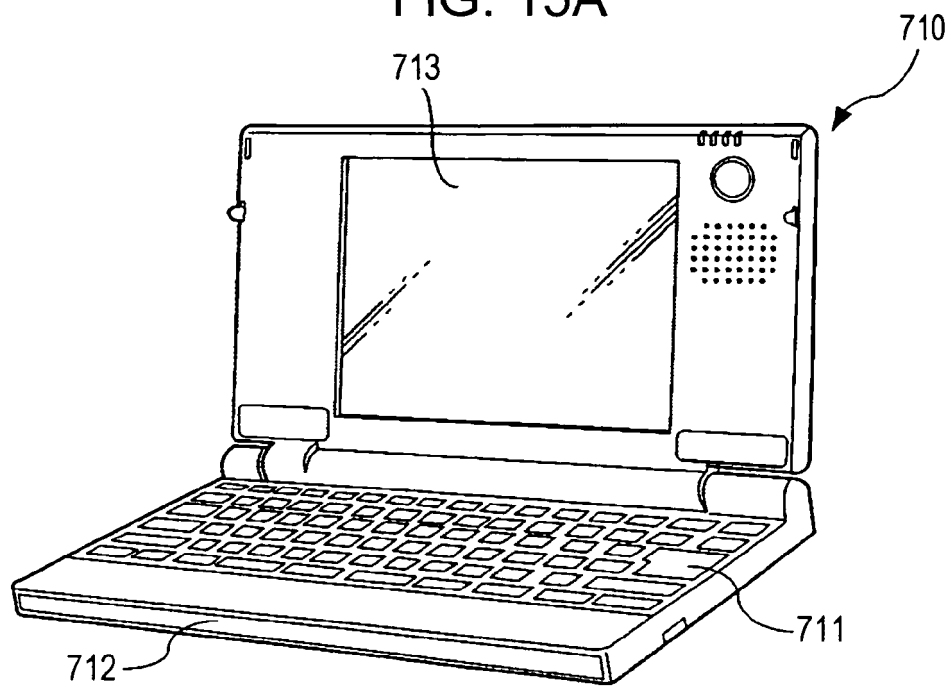


FIG. 15B

