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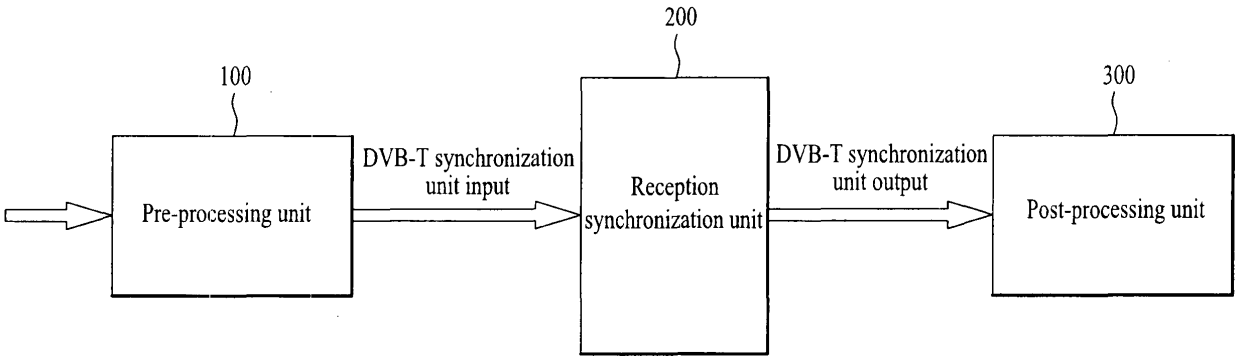
(54) Apparatus for synchronization acquisition in digital receiver and method thereof

(57) An apparatus for system synchronization acquisition in a digital receiver and method thereof are disclosed, by which a synchronization unit is precisely locked and by which fast tracking performance is provided. The present invention includes a pre-processing unit digitally converting a reception signal by processing the reception signal in an analog area, a reception synchronization unit comprising a plurality of different synchronization units, each performing a different synchronization process sequentially by receiving the pre-processed signal, the reception synchronization unit controlling a start of the synchronization process of a next synchronization unit according to a presence or non-presence of the synchronization acquisition of a current synchronization unit, and a post-processing unit decoding the synchronization-acquired signal.

FIG. 1



EP 1 672 909 A2

Description

[0001] This application claims the benefit of the Korean Patent Application No. 10-2004-0107722, filed on December 17, 2004, which is hereby incorporated by reference as if fully set forth herein.

BACKGROUND OF THE INVENTION

Field of the Invention

[0002] The present invention relates to a synchronization acquisition, and more particularly, to an apparatus for synchronization acquisition and method thereof.

Discussion of the Related Art

[0003] Generally, the European transmission system standard of terrestrial channel of digital TV is DVB-T (digital video broadcasting-terrestrial). And, the DVB-T adopts the OFDM (orthogonal frequency division multiplexing) transmission system.

[0004] The OFDM transmission system is strong against channel distortion caused by multi-path in a wireless broadband broadcasting system.

[0005] However, the OFDM transmission system is sensitive to synchronizations (symbol synchronization, frequency synchronization, timing synchronization). In case of failing in performing accurate synchronization between transmission and reception, the OFDM transmission system brings about a problem of distortion of a reception signal. Hence, many efforts are made to solve the problem.

[0006] Specifically, stable and fast synchronization acquisition is very important to design a DVB-T receiver. Hence, the demand for a systematic synchronization acquiring apparatus and method thereof has risen.

SUMMARY OF THE INVENTION

[0007] Accordingly, the present invention is directed to an apparatus for synchronization acquisition and method thereof that substantially obviate one or more problems due to limitations and disadvantages of the related art.

[0008] An object of the present invention is to provide an apparatus for system synchronization acquisition in a digital receiver, by which a synchronization unit is precisely locked and by which fast tracking performance is provided.

[0009] Another object of the present invention is to provide a method of system synchronization acquisition in a digital receiver, by which a lock process can be smoothly performed between elements and by which an optimal convergence time is provided.

[0010] Additional advantages, objects, and features of the invention will be set forth in part in the description which follows and in part will become apparent to those having ordinary skill in the art upon examination of the following or may be learned from practice of the invention. The objectives and other advantages of the invention may be realized and attained by the structure particularly pointed out in the written description and claims hereof as well as the appended drawings.

[0011] To achieve these objects and other advantages and in accordance with the purpose of the invention, as embodied and broadly described herein, an apparatus for synchronization acquisition in a digital receiver includes a pre-processing unit digitally converting a reception signal by processing the reception signal in an analog area, a reception synchronization unit comprising a plurality of different synchronization units, each performing a different synchronization process sequentially by receiving the pre-processed signal, the reception synchronization unit controlling a start of the synchronization process of a next synchronization unit according to a presence or non-presence of the synchronization acquisition of a current synchronization unit, and a post-processing unit decoding the synchronization-acquired signal.

[0012] In another aspect of the present invention, in receiving a digital signal, a method of synchronization acquisition in a digital receiver includes a step (a) of converting a received analog signal to a digital signal, a step (b) of sequentially performing different synchronization processes by receiving the digital signal and controlling a start of a next synchronization process according to a presence or non-presence of the synchronization acquisition of a current synchronization process, and a step (c) of decoding the synchronized signal.

[0013] It is to be understood that both the foregoing general description and the following detailed description of the present invention are exemplary and explanatory and are intended to provide further explanation of the invention as claimed.

BRIEF DESCRIPTION OF THE DRAWINGS

[0014] The accompanying drawings, which are included to provide a further understanding of the invention and are incorporated in and constitute a part of this application, illustrate embodiment(s) of the invention and together with the description serve to explain the principle of the invention. In the drawings:

[0015] FIG. 1 is a block diagram of an apparatus for synchronization acquisition in a digital receiver according to the present invention;

[0016] FIG. 2 is a block diagram of a reception synchronization unit of an apparatus for synchronization acquisition according to the present invention; and

[0017] FIG. 3A and FIG. 3B are flowcharts of a method of synchronization acquisition in a digital receiver according to the present invention.

DETAILED DESCRIPTION OF THE INVENTION

[0018] Reference will now be made in detail to the preferred embodiments of the present invention, examples of which are illustrated in the accompanying drawings. Wherever possible, the same reference numbers will be used throughout the drawings to refer to the same or like parts.

[0019] The present invention provides an apparatus for synchronization acquisition in a digital receiver, characterized in including a pre-processing unit digitally converting a reception signal by processing the reception signal in an analog area, a reception synchronization unit comprising a plurality of different synchronization units, each performing a different synchronization process sequentially by receiving the pre-processed signal, the reception synchronization unit controlling a start of the synchronization process of a next synchronization unit according to a presence or non-presence of the synchronization acquisition of a current synchronization unit, and a post-processing unit decoding the synchronization-acquired signal.

[0020] According to another embodiment of the present invention, provided is a method of synchronization acquisition in a digital receiver in receiving a digital signal, which is characterized in including a step (a) of converting a received analog signal to a digital signal, a step (b) of sequentially performing different synchronization processes by receiving the digital signal and controlling a start of a next synchronization process according to a presence or non-presence of the synchronization acquisition of a current synchronization process, and a step (c) of decoding the synchronized signal.

[0021] Therefore, the present invention optimizes synchronization acquisition of a reception signal by reducing the instability of a receiver and the excessive sync time taken for tracking.

[0022] FIG. 1 is a block diagram of an apparatus for synchronization acquisition in a digital receiver according to the present invention and FIG. 2 is a block diagram of a reception synchronization unit of an apparatus for synchronization acquisition according to the present invention.

[0023] Referring to FIG. 1, a digital receiver includes a pre-processing unit 100, a reception synchronization (synchronization acquisition) unit 200 and a post-processing unit 300.

[0024] The pre-processing unit 100 includes a reception unit receiving an analog signal, a tuner converting the received analog signal to an intermediate frequency, and an A/D converter converting the converted analog signal to a digital signal to deliver to the reception synchronization unit 200.

[0025] In the pre-processing unit 100, the reception unit receives a 50MHz~860MHz RF (radio frequency) signal in an analog area. The tuner (not shown in the drawing) receives the RF signal from the reception unit and then converts it to an intermediate (IF) signal. The A/D converter (not shown in the drawing) converts the IF signal to a digital signal to deliver to the reception synchronization unit 200. In this case, a SAW (surface acoustic wave) filter is generally provided to a rear end of the tuner. The SAW filter mainly includes an electrode coated on a crystal. Since an acoustic wave propagates on a surface of the crystal at a considerably low speed (about 10^{-5} of free space propagation speed), the SAW filter is configured suitable for a signal processing on a relatively small area. Thus, the digital signal is inputted to the reception synchronization unit 200 via the pre-processing unit 100.

[0026] Referring to FIG. 2, the reception synchronization unit 200 includes an AGC (Automatic Gain Control) unit 201, a CSTS (Coarse Symbol Timing Synchronization) unit 203, an FCFS (Fine Carrier Frequency Synchronization) unit 205, an FFT (Fast Fourier Transform) unit 207, an ICFS (Integer Carrier Frequency Synchronization) unit 209, a SFS (Sampling Frequency Synchronization) unit 213, an SPOE (Scattered Pilot Order Estimation) unit 215, a FSTS (Fine Symbol Timing Synchronization) unit 217, a channel equalizer 219 and a lock signal control unit 211.

[0027] A gain of the digitally converted signal outputted from the pre-processing unit 100 is compensated by the automatic gain control unit 201. The automatic gain control unit 201 is to compensate a gain of a signal so that the A/D converter (not shown in the drawing) can normally convert the analog signal to the digital signal since the IF signal having passed through the SAW filter (not shown in the drawing) of the pre-processing unit 100 is weak. By the automatic gain control unit 201 according to the present invention, as shown in FIG. 2, the gain value is calculated in a digital area to be fed back to the pre-processing unit 100.

[0028] Meanwhile, the automatic gain control unit 201 includes a lock detector measuring an average of a reception power from reception input data to decide a difference from a preset reference power. The automatic gain control unit 201 carries out acquisition decision and tracking of a gain through the lock detector. And, the lock detector outputs an AGC lock signal to the lock signal control unit 211.

[0029] The signal, of which gain is recovered by the automatic gain control unit 201, is inputted to the coarse symbol timing synchronization unit 203. The coarse symbol timing synchronization unit 203 extracts a valid data sample only except a guard interval from a gain-covered reception signal sample and then delivers the extracted valid data sample to the FFT unit 207 provided to its rear end. Coarse symbol timing synchronization, which is carried out in a time domain followed by the FFT unit 207, is very sensitive to a channel. Hence, it is difficult to estimate a precise FFT window location. Yet, an approximate FFT window location can be estimated.

[0030] The coarse symbol timing synchronization unit 203 includes a lock detector. And, the lock detector recognizes the AGC lock signal delivered from the lock sig-

nal control unit 211 as a start signal of coarse symbol timing synchronization acquisition, estimates a symbol timing synchronization, measures a correlation average power, and then decides a difference from a preset reference value. If the calculated correlation power is greater than the reference value, a symbol timing lock signal is outputted to the lock signal control unit 211. The lock detector outputs a coarse symbol timing lock signal to the lock signal control unit 211.

[0031] The fine carrier frequency synchronization unit 205 having received the symbol timing lock signal from the lock signal control unit 211 removes frequency offset and phase jitter of a carrier caused by the tuner and mixer of the analog reception unit (pre-processing unit 100) and plays a role in converting a band pass digital signal to a baseband digital signal. The fine carrier frequency synchronization unit 205 can estimate a frequency offset amounting to a half or less of a subcarrier interval. The fine carrier frequency synchronization unit 205 includes a lock detector. And, the lock detector recognizes the coarse symbol timing lock signal received from the lock signal control unit 211 as a start signal of fine carrier frequency synchronization, estimates fine frequency synchronization, and then decides a difference between a timing error average and a preset reference value. Fine carrier frequency acquisition is decided using the lock detector. In particular, if the timing error average is smaller than the preset value, the lock detector outputs a lock signal of the fine carrier frequency synchronization unit 205 to the lock signal control unit 211.

[0032] The signal, on which the fine carrier frequency synchronization is carried out, is converted to a signal of a frequency area by the fast Fourier transform (FFT) unit 207 according to each mode (2k/8k) of the DVB-T receiver.

[0033] The signal converted into the frequency area is inputted to the integer carrier frequency synchronization unit 209. The integer carrier frequency synchronization unit 209 recognizes the fine carrier frequency lock signal delivered from the lock signal control unit 211 as a start signal of integer carrier frequency synchronization and then estimates integer frequency synchronization. The integer carrier frequency synchronization unit 209 includes a lock detector deciding a difference from a preset correlation average power and decides integer carrier frequency acquisition through the lock detector.

[0034] If the correlation average power is greater than a reference value, a lock signal of integer carrier frequency recovery is outputted to the lock signal control unit 211. In doing so, two carrier frequency synchronizations are not simultaneously acquired. This is because the ± 0.5 problem is brought about due to the OFDM modulation/demodulation characteristics if the integer is simultaneously activated prior to acquiring the fine carrier frequency.

[0035] The integer-frequency-synchronized signal is inputted to the sampling frequency synchronization unit 213. As sampling frequency synchronization carried out by the sampling frequency synchronization unit 213 employs a resampler to convert analog data to digital data of a fixed frequency. And, clock recovery of entire sample sequences is carried out by the resampler. Thus, a whole process is digitally carried out. Thus, the sampling frequency synchronization unit 213 needs no other analog devices but an analog/digital converter. Hence, the sampling frequency synchronization unit 213 can be simply implemented and has a characteristic of eliminating device noise.

[0036] The sampling frequency synchronization unit 213 performs sampling with a regular cycle interval given as a sampling frequency in an inputted continuous OFDM signal. And, the sampling frequency synchronization unit 213 recognizes the integer carrier frequency lock signal delivered from the lock signal control unit 211 as an acquisition start signal of the sampling frequency synchronization and then estimates the sampling frequency synchronization.

[0037] Moreover, the sampling frequency synchronization unit 213 includes a lock detector deciding a difference from a preset timing error average and decides an acquisition of the sampling frequency using the lock detector. The lock detector compares a timing error average value to a preset reference value. If the timing error average value is smaller than the reference value, the lock detector outputs a lock signal of the sampling frequency synchronization unit to the lock signal control unit 211.

[0038] Subsequently, the sampling-frequency-synchronized signal is inputted to the scattered pilot order estimation unit 215.

[0039] A DVB-T transmission frame has a structure that reference pilots (continuous pilot, scattered pilot) are inserted in its data payload. The scattered pilot within the frame is repeated each four OFDM symbols [k = 3 * (1mod4) + 12p, where p is an integer].

[0040] Hence, an order of the repeated scattered pilots (index1, index2, index3, index4) needs to be estimated. The scattered pilot order estimation unit 215 recognizes the sampling frequency lock signal delivered from the lock signal control unit 211 as a start signal of scattered pilot order estimation acquisition and then estimates a scattered pilot order.

[0041] The scattered pilot order estimation unit 215 includes a lock detector. The scattered pilot order estimation unit 215 decides whether a preset scattered pilot order index1 is equal to an estimated scattered pilot order index. And, the scattered pilot order estimation unit 215 decides an acquisition of the scattered pilot order estimation unit 215 using the lock detector.

[0042] If the estimated scattered pilot order index1 is equal to the preset scattered pilot order index1, the lock detector outputs a lock signal of the scattered pilot order estimation unit 215 to the lock signal control unit 211.

[0043] Subsequently, the fine symbol timing synchronization unit 217 performs a function of estimating a remaining FFT window offset remaining in the coarse symbol timing synchronization unit 203 using the scattered

pilot. In particular, the fine symbol timing synchronization unit 217 recognizes the scattered pilot order estimation lock signal delivered from the lock signal control unit 211 as a fine symbol timing synchronization acquisition start signal and then estimates fine symbol timing synchronization.

[0044] In doing so, the fine symbol timing synchronization unit 217 needs not to use a separate lock detector unlike other synchronization units. Yet, the fine symbol timing synchronization unit 217 generates a fine symbol offset valid signal t output to the lock signal control unit 211.

[0045] The fine-symbol-timing-synchronized signal is inputted to the channel equalizer 219 connected to its rear end. In the digital transmission system such as HDTV, a bit detection error is brought about in a receiving side by a distortion caused by a transmission signal passing through a multi-path channel, an interference caused by a PAL signal, a distortion caused by a transceiver system and the like. In particular, the signal propagation via the multi-path brings about inter-symbol interference to become a major cause of the bit detection error. Hence, to correct the signal distortion, a channel equalizing process is carried out.

[0046] The channel equalizer 219 recognizes the fine symbol offset valid signal delivered from the lock signal control unit 211 as an acquisition start signal of the channel equalizer and then executes the channel equalization.

[0047] As mentioned in the above description, the major objects of the reception synchronization blocks of the DVB-T receiver according to the present invention are to remove the corresponding noises (gain offset, timing offset, frequency offset, phase offset, ghost, etc.) and to minimize MSE (means-square error).

[0048] Hence, a reference for deciding whether the units correctly eliminate the corresponding noises is needed. And, the lock detectors are used as the decision means, correspondingly.

[0049] The lock detectors can be divided into a manual type and an auto type. Compared to the auto type lock detector, the manual type lock detector fails in effectively coping with a channel environment and randomness of system. Hence, the manual type lock detector has difficulty in being used in general communication demodulations (OFDM, VSB, QAM, QPSK, etc.). Hence, the auto type lock detectors are employed. In the DVB-T receiver including the various units, each having the lock detector, of the reception synchronization unit, the lock signal control unit 211 optimized in aspect of the system is used to secure the system stability and fast convergence speed.

[0050] The lock signal control unit 211 carries out a systematic acquisition processing to secure the system stability and the optimal convergence time in the sequential and dependent signal flow of each of the element units.

[0051] Meanwhile, the reception signal through the channel equalization is decoded by the post-processing unit (channel decoder) 300. The decoded A/V data is displayed on a screen 9not shown in the drawing).

[0052] FIG. 3A and FIG. 3B are flowcharts of a transition process of a systematic synchronization acquisition processor according to the present invention. A method of synchronization acquisition in a digital receiver according to the present invention is explained with reference to FIG. 3A and FIG. 3B as follows.

[0053] In receiving a digital signal, a method of synchronization acquisition in a digital receiver according to the present invention includes the steps of receiving an analog signal to digitally convert, detecting a first lock signal by recovering a gain of the digitally converted signal and by deciding whether a corresponding noise is removed, detecting a second lock signal by performing coarse symbol timing synchronization in a manner of recognizing the first lock signal as a start signal and extracting valid data of the gain-recovered signal only to deliver and by deciding whether a corresponding noise is removed, detecting a third lock signal by performing fine carrier frequency synchronization to convert a baseband digital signal to a pass band digital signal in a manner of recognizing the second lock signal as a start signal and eliminating a frequency offset and phase noise of the extracted valid data and by deciding whether a corresponding noise is removed, converting the pas band digital signal into a frequency domain, detecting a fourth lock signal by performing integer carrier frequency synchronization to compensate the frequency-domain-converted signal in a manner of recognizing the third lock signal as a start signal and estimating an integer multiplication of a subcarrier interval closest to an initial frequency offset and by deciding whether a corresponding noise is removed, detecting a fifth lock signal by performing sampling frequency synchronization to carry out sampling on the compensated signal in a manner of recognizing the fourth lock signal as a start signal and by deciding whether a corresponding noise is removed, detecting a sixth lock signal by estimating an order of a scattered pilot signal included in the received signal in a manner of recognizing the fifth lock signal as a start signal and by deciding whether a corresponding noise is removed, performing fine symbol timing synchronization to estimate a remaining FFT window offset using the estimated scattered pilot in a manner of recognizing the sixth signal as a start signal, and performing channel equalization to correct a distortion of the received signal.

[0054] Referring to FIG. 3A and FIG. 3B, a gain of a signal, which was digitally converted and outputted from the pre-processing unit 100, is compensated by the automatic gain control unit 210 (S10). For the gain-compensated signal, an average reception power is compared to a preset reference value (S20). If the average reception power is equal to the reference value, coarse symbol timing synchronization is carried out on the gain-compensated signal (S30). For the coarse-symbol-timing-synchronizes signal, a correlation power is compared to the preset reference value (S40). If the correlation pow-

er is greater than the reference value, fine carrier frequency synchronization is carried out (S50). For the fine-carrier-frequency-synchronized signal, a timing error average is compared to a preset reference value (S60). If the timing error average is smaller than the reference value, integer carrier frequency synchronization is carried out (S70). For the integer-carrier-frequency-synchronized signal, the correlation power is compared to the preset reference value (S80). If the correlation power is greater than the reference value, sampling frequency synchronization is carried out (S90). For the sampling-frequency-synchronized signal, the timing error average is compared to the preset reference value (S100). If the timing error average is smaller than the reference value, a scattered pilot order is estimated (S110). If the estimated scattered pilot order index is equal to a preset scattered pilot order index 1 (S120). Fine symbol timing synchronization is carried out (S130). Channel equalization is carried out on the fine-symbol-timing-synchronized signal (S140) to acquire a synchronization of a reception signal.

[0055] Meanwhile, although the DVB-T receiver is explained in the above description, the present invention is applicable to a DVB-H receiver as well.

[0056] It will be apparent to those skilled in the art that various modifications and variations can be made in the present invention without departing from the spirit or scope of the inventions. Thus, it is intended that the present invention covers the modifications and variations of this invention provided they come within the scope of the appended claims and their equivalents.

Claims

1. An apparatus for synchronization acquisition in a digital receiver, comprising:

   a pre-processing unit digitally converting a reception signal by processing the reception signal in an analog area;
   a reception synchronization unit comprising a plurality of different synchronization units, each performing a different synchronization process sequentially by receiving the pre-processed signal, the reception synchronization unit controlling a start of the synchronization process of a next synchronization unit according to a presence or non-presence of the synchronization acquisition of a current synchronization unit; and
   a post-processing unit decoding the synchronization-acquired signal.

2. The apparatus of claim 1, the pre-processing unit comprising:

   a tuner tuning a broadcast signal of a specific channel to convert to an intermediate frequency signal; and
   an A/D converter converting the converted intermediate frequency signal to a digital signal to deliver to the reception synchronization unit.

3. The apparatus of claim 1, the reception synchronization unit comprising:

   a lock signal control unit outputting a control signal for controlling the start of the synchronization process of the next synchronization unit according to the presence or non-presence of the synchronization acquisition of the current synchronization unit; and
   a lock detector outputting a result of a presence or non-presence of the synchronization acquisition of a corresponding reception signal to the lock signal control unit wherein the presence or non-presence of the synchronization acquisition is decided by each of the synchronization units of the reception synchronization unit.

4. The apparatus of claim 3, wherein the reception synchronization unit comprises at least one selected from the group consisting of an automatic gain control unit, a coarse symbol timing synchronization unit, a fine carrier frequency synchronization unit, an integer carrier frequency synchronization unit, a sampling frequency synchronization unit, a scattered pilot extracting unit and a fine symbol timing synchronization unit.

5. The apparatus of claim 4, wherein the automatic gain control unit compensates a gain in a digital area by receiving the digitally converted signal from the pre-processing unit, wherein the lock detector of the automatic gain control unit measures an average value of a reception power of the reception signal to decide a difference from a preset reference value, and wherein if the average value of the reception power is equal to the preset reference value, the lock detector of the automatic gain control unit outputs a lock signal to the lock signal control unit.

6. The apparatus of claim 4, wherein the coarse symbol timing synchronization unit recognizes a lock signal of the automatic gain control unit inputted from the lock signal control unit as a start signal of a coarse symbol timing synchronization acquisition and extracts rest valid data except a guard interval from the gain-compensated signal.

7. The apparatus of claim 4, wherein the lock detector of the coarse symbol timing synchronization unit decides a difference from a preset reference value by measuring a correlation average power value and outputs a lock signal to the lock signal control unit if the measured correlation average power value is

greater than the preset reference value.

8. The apparatus of claim 4, wherein the fine carrier frequency synchronization unit recognizes a lock signal of the coarse symbol timing synchronization unit inputted from the lock signal control unit as a start signal of a fine carrier frequency synchronization acquisition, eliminates a frequency offset and phase jitter of the pre-processing unit, and converts a band pass digital signal to a baseband digital signal.

9. The apparatus of claim 4, wherein the lock detector of the fine carrier frequency synchronization unit decides a difference from a preset reference value by measuring a timing error average value and outputs a lock signal to the lock signal control unit if the measured timing error average value is smaller than the preset reference value.

10. The apparatus of claim 4, wherein the integer carrier frequency synchronization unit recognizes a lock signal of the coarse symbol timing synchronization unit inputted from the lock signal control unit as a start signal of an integer carrier frequency synchronization acquisition and compensates the signal processed by the fine carrier frequency synchronization unit by estimating an integer multiplication of an interval of a subcarrier closest to an initial frequency offset.

11. The apparatus of claim 4, wherein the lock detector of the integer carrier frequency synchronization unit decides a difference from a preset reference value by measuring a correlation average power value and outputs a lock signal to the lock signal control unit if the measured correlation average power value is greater than the preset reference value.

12. The apparatus of claim 4, wherein the sampling frequency synchronization unit recognizes a lock signal of the integer carrier frequency synchronization unit inputted from the lock signal control unit as a start signal of a sampling frequency synchronization acquisition and performs sampling the integer carrier frequency synchronized signal.

13. The apparatus of claim 4, wherein the lock detector of the sampling frequency synchronization unit decides a difference from a preset reference value by measuring a timing error average value and outputs a lock signal to the lock signal control unit if the measured timing error average value is smaller than the preset reference value.

14. The apparatus of claim 4, wherein the scattered pilot estimation unit recognizes a lock signal of the sampling frequency synchronization unit inputted from the lock signal control unit as a start signal of a scattered pilot estimation and estimates an order of a scattered pilot signal included in the sampled signal.

15. The apparatus of claim 4, wherein the lock detector of the scattered pilot estimation unit decides a difference between an estimated scattered pilot order index and a preset scattered pilot index 1 and wherein if the estimated scattered pilot order index is equal to the preset scattered pilot index 1, the lock detector of the scattered pilot estimation unit outputs a lock signal to the lock signal control unit.

16. The apparatus of claim 4, wherein the fine symbol timing synchronization unit recognizes a lock signal of the scattered pilot estimation unit inputted from the lock signal control unit as a start signal of a fine symbol timing synchronization acquisition and estimates a remaining window offset of the coarse symbol timing synchronization unit based on the estimated scattered pilot.

17. The apparatus of claim 4, wherein the fine symbol timing synchronization unit generates a fine symbol offset valid signal to output to the lock signal control unit.

18. In receiving a digital signal, a method of synchronization acquisition in a digital receiver, comprising:

a step (a) of converting a received analog signal to a digital signal;
a step (b) of sequentially performing different synchronization processes by receiving the digital signal and controlling a start of a next synchronization process according to a presence or non-presence of the synchronization acquisition of a current synchronization process; and
a step (c) of decoding the synchronized signal.

19. The method of claim 18, wherein the step (b) comprises at least one selected from the group consisting of an automatic gain control step, a coarse symbol timing synchronization step, a fine carrier frequency synchronization step, an integer carrier frequency synchronization step, a sampling frequency synchronization step, a scattered pilot estimation step, a fine symbol timing synchronization step and a channel equalization step, wherein each of the steps initiates the synchronization process according to a start control signal provided to a corresponding step, and wherein the start control signal according to a decision result resulting from deciding the presence or non-presence of the synchronization acquisition to the next synchronization process.

20. The method of claim 19, the step (b) comprising the steps of:

detecting a first lock signal by recovering a gain of the digitally converted signal and by deciding whether a corresponding noise is removed;
detecting a second lock signal by performing coarse symbol timing synchronization in a manner of recognizing the first lock signal as a start signal and extracting valid data of the gain-recovered signal only to deliver and by deciding whether a corresponding noise is removed;
detecting a third lock signal by performing fine carrier frequency synchronization to convert a baseband digital signal to a pass band digital signal in a manner of recognizing the second lock signal as a start signal and eliminating a frequency offset and phase noise of the extracted valid data and by deciding whether a corresponding noise is removed;
converting the pass band digital signal into a frequency domain;
detecting a fourth lock signal by performing integer carrier frequency synchronization to compensate the frequency-domain-converted signal in a manner of recognizing the third lock signal as a start signal and estimating an integer multiplication of a subcarrier interval closest to an initial frequency offset and by deciding whether a corresponding noise is removed;
detecting a fifth lock signal by performing sampling frequency synchronization to carry out sampling on the compensated signal in a manner of recognizing the fourth lock signal as a start signal and by deciding whether a corresponding noise is removed;
detecting a sixth lock signal by estimating an order of a scattered pilot signal included in the received signal in a manner of recognizing the fifth lock signal as a start signal and by deciding whether a corresponding noise is removed;
performing a fine symbol timing synchronization to estimate a remaining window offset using the estimated scattered pilot in a manner of recognizing the sixth signal as a start signal; and
performing a channel equalization to correct a distortion of the received signal.

21. The method of claim 20, wherein in the fine symbol timing synchronization performing step, a fine symbol offset valid signal is generated to be outputted and wherein in the channel equalization performing step, the fine symbol offset valid signal is recognized as the start signal.

FIG. 1

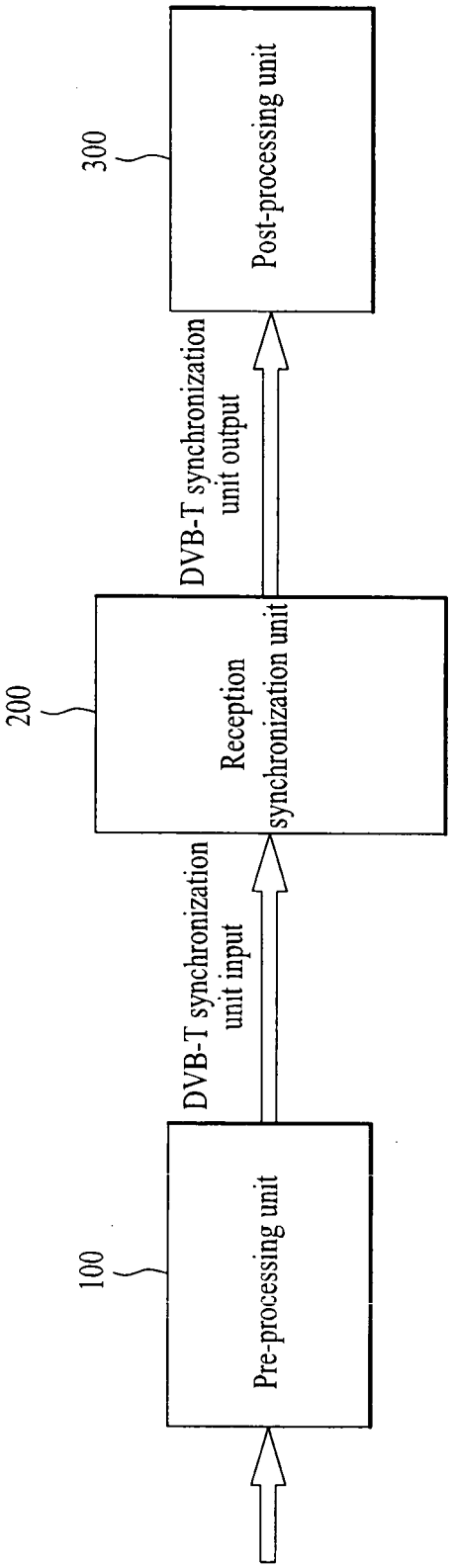

100
Pre-processing unit
DVB-T synchronization unit input
200
Reception synchronization unit
DVB-T synchronization unit output
300
Post-processing unit

FIG. 2

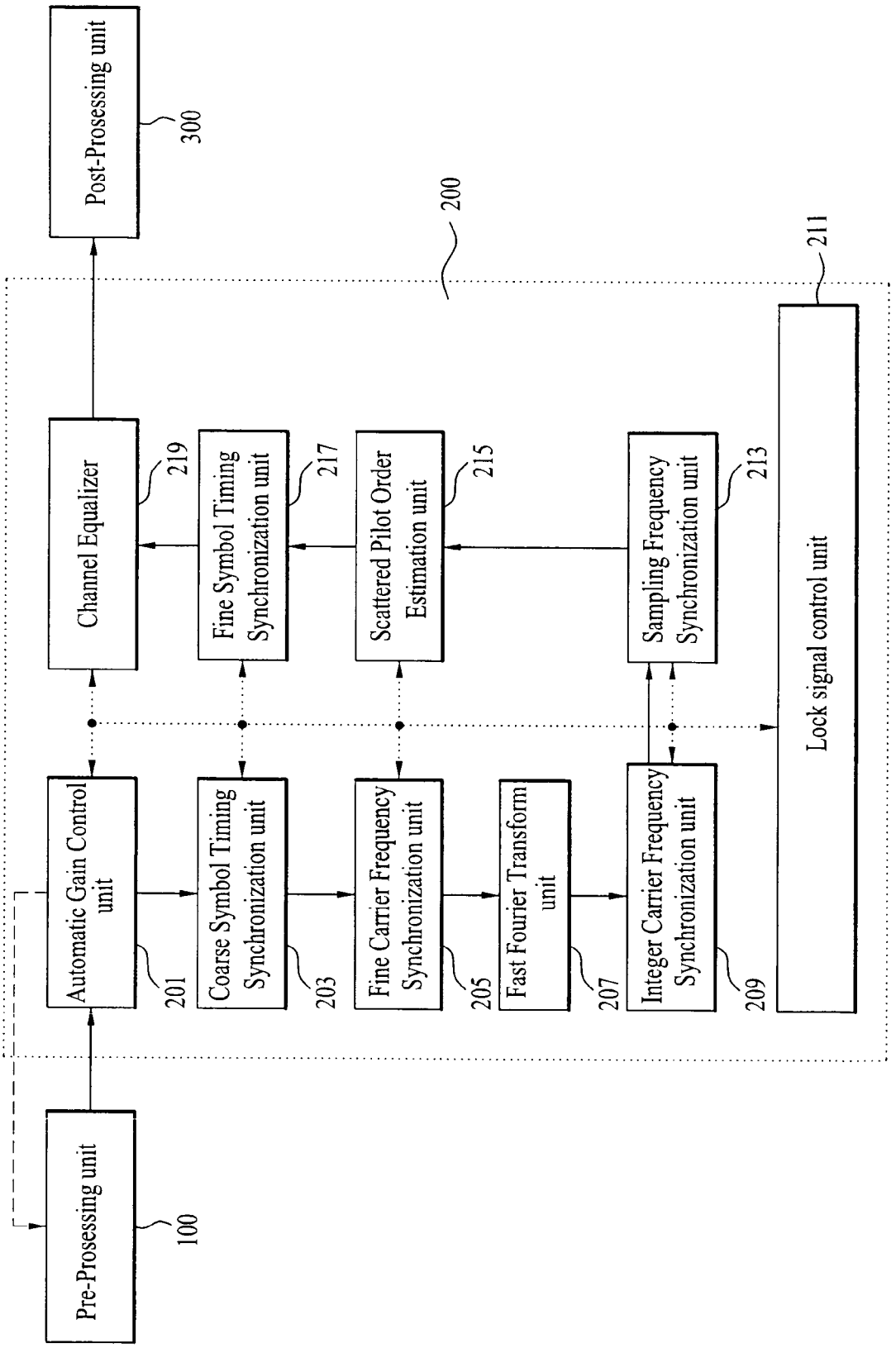

Pre-Prosessing unit
100
Automatic Gain Control unit
201
Coarse Symbol Timing Synchronization unit
203
Fine Carrier Frequency Synchronization unit
205
Fast Fourier Transform unit
207
Integer Carrier Frequency Synchronization unit
209
Lock signal control unit
211
Sampling Frequency Synchronization unit
213
Scattered Pilot Order Estimation unit
215
Fine Symbol Timing Synchronization unit
217
Channel Equalizer
219
200
Post-Prosessing unit
300

FIG. 3A

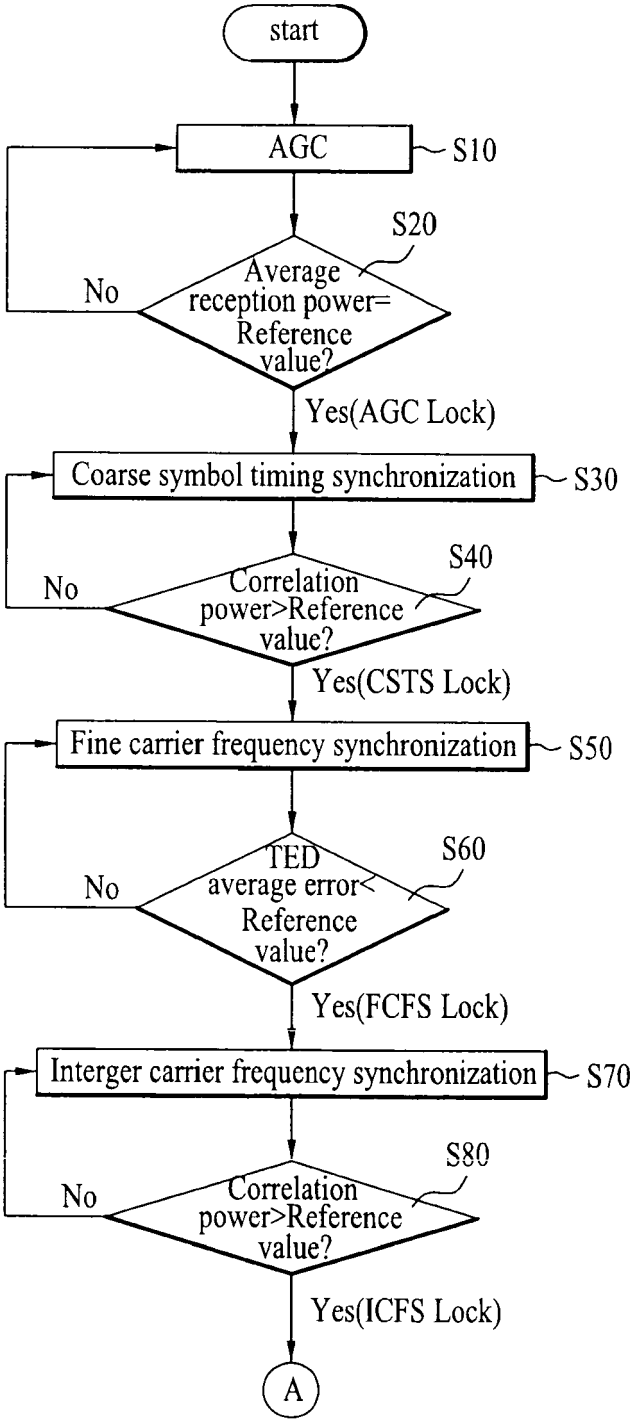
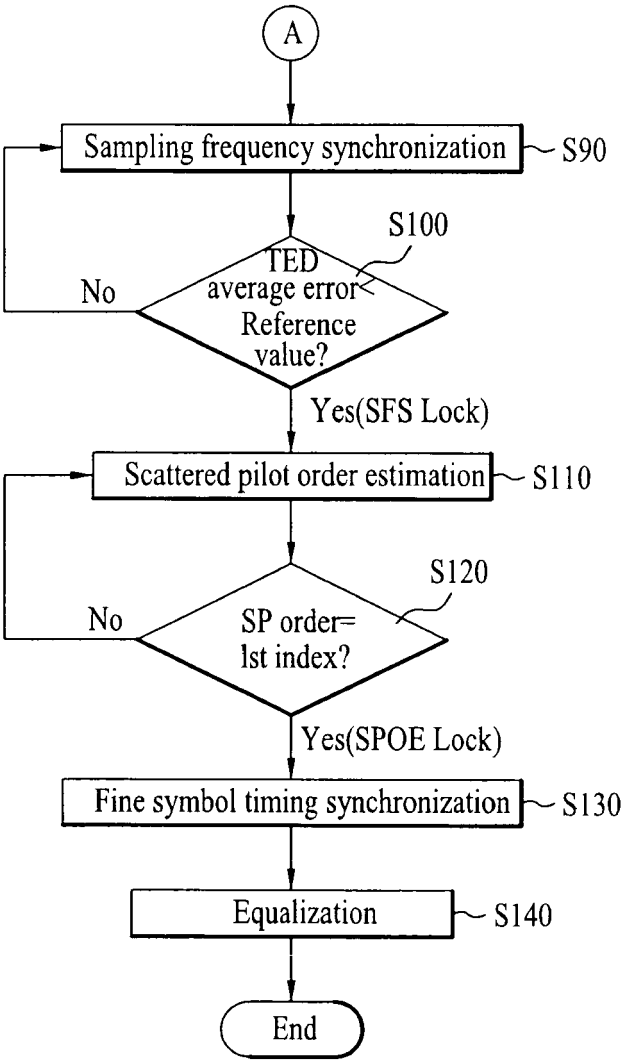

start
AGC
S10
S20
Average reception power= Reference value?
No
Yes(AGC Lock)
Coarse symbol timing synchronization
S30
S40
Correlation power>Reference value?
No
Yes(CSTS Lock)
Fine carrier frequency synchronization
S50
TED average error< Reference value?
S60
No
Yes(FCFS Lock)
Interger carrier frequency synchronization
S70
S80
Correlation power>Reference value?
No
Yes(ICFS Lock)
A

FIG. 3B


A
Sampling frequency synchronization
S90
S100
TED average error < Reference value?
No
Yes(SFS Lock)
Scattered pilot order estimation
S110
S120
SP order= lst index?
No
Yes(SPOE Lock)
Fine symbol timing synchronization
S130
Equalization
S140
End