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(71) Applicant: **FUJITSU LIMITED**
Kawasaki-shi,
Kanagawa 211-8588 (JP)

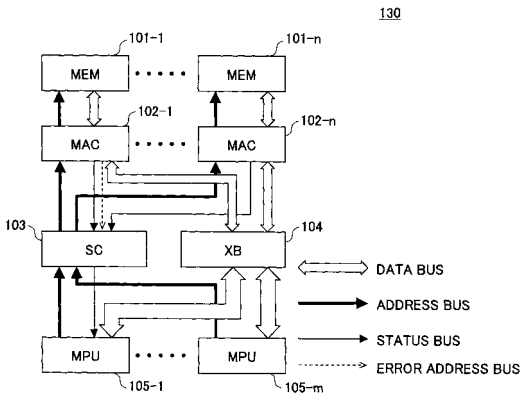
(72) Inventors:
- **Suzuki, Kenji,**
  c/o Fujitsu Limited
  Kawasaki-shi
  Kanagawa 211-8588 (JP)
- **Honda, Yasufumi,**
  c/o Fujitsu Limited
  Kawasaki-shi
  Kanagawa 211-8588 (JP)
- **Koguchi, Takashi,**
  c/o Fujitsu Limited
  Kawasaki-shi
  Kanagawa 211-8588 (JP)

(74) Representative: **Fenlon, Christine Lesley et al**
Haseltine Lake LLP
Lincoln House, 5th Floor
300 High Holborn
London WC1V 7JH (GB)

(54) Techniques for soft error correction

(57) A soft error correction method is described for a memory system having memory access controllers accessing memories for storing bytesliced data in cycle synchronism, and a system controller receiving a memory access from an arbitrary one of MPUs and issuing a memory address to the memory access controllers. When a correctable error is detected in data read from one memory, an error address where the error was detected is held within a memory access controller, and an error notification is made to the system controller from the memory access controller. In response to the error notification, the memory access controller holds the error address from the system controller without intervention from the MPUs, and reads, corrects and rewrites the data to the error address.

FIG.4



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