(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 1 708 166 A2

(12) EUROPEAN PATENT APPLICATION

(43) Date of publication:
04.10.2006 Bulletin 2006/40

(51) Int Cl.:
G09G 3/36 *(2006.01)*

(21) Application number: **06002941.0**

(22) Date of filing: **14.02.2006**

(84) Designated Contracting States:
AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HU IE IS IT LI LT LU LV MC NL PL PT RO SE SI SK TR
Designated Extension States:
AL BA HR MK YU

(30) Priority: **31.03.2005 CN 200510062825**

(71) Applicant: **Himax Technologies, Inc.**
Hsinhua
Tainan
County 712 (TW)

(72) Inventors:
- **Chen, Chien-Ru**
  Hsinhua
  Tainan County 712 (TW)
- **Chen, Jung-Zone**
  Hsinhua
  Tainan County 712 (TW)
- **Chen, Ying-Lieh**
  Hsinhua
  Tainan County 712 (TW)

(74) Representative: **Schaeberle, Steffen**
Hoefer & Partner,
Patentanwälte,
Gabriel-Max-Strasse 29
81545 München (DE)

(54) Chip-on-glass liquid crystal display and data transmission method for the same

(57) A liquid crystal display (LCD) comprising a glass substrate, a plurality of serial-connected source drivers (212) and at least one gate driver (214), disposed on the glass substrate by chip-on-glass technology, a timing controller (225) for generating image data and a control signal, and at least one flexible printed circuit board (230,232). The flexible printed circuit board receives the image data and the control signal for transmitting to the corresponding source driver. Then the corresponding source driver transmits the image data and the control signal to the neighboring source drivers such that all the source drivers respectively get the image data and the control signal. The flexible printed circuit board is disposed such that delays and distortions of the image data and the control signal are acceptable to the source drivers e.g. by connecting to the centre source driver of the series-connected source drivers.

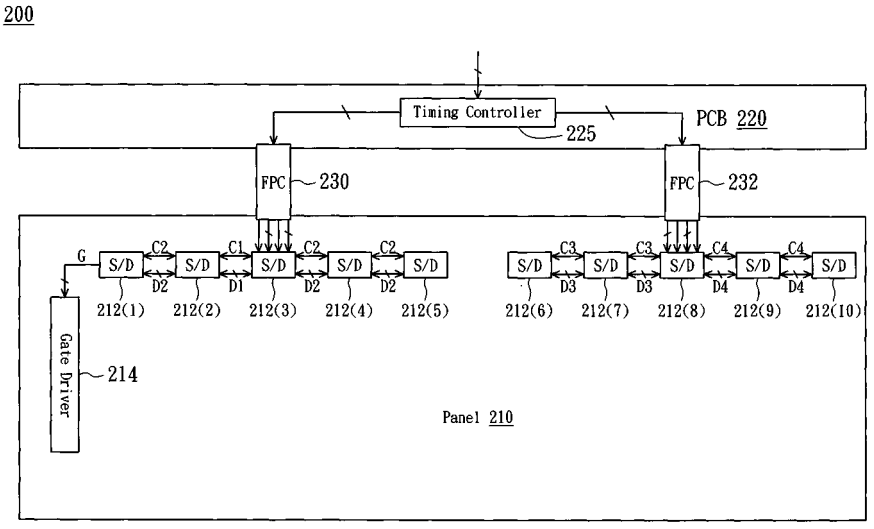

FIG. 2A

EP 1 708 166 A2

Description

[0001] This application claims the benefit of People's Republic of China application Serial No. 200510062825.7, filed March 31, 2005, the subject matter of which is incorporated herein by reference.

BACKGROUND OF THE INVENTION

Field of the Invention

[0002] The invention relates in general to the liquid crystal display, and more particularly to the chip-on-glass liquid crystal display.

Description of the Related Art

[0003] Liquid crystal displays (LCD) have become more and more popular in the computer monitors or TVs due to the light weight, flatness and low radiation, compared with the CRT monitor. In addition to improve the display quality of LCDs, such as color, contrast and brightness, the manufacturers try to improve the manufacturing process to reduce the cost and manufacturing time.

[0004] The LCD includes a timing controller, source drivers and at least one gate driver to drive its liquid crystal panel. The timing controller is welded on a control print circuit board, the source drivers are welded on a X-board, and the gate driver is welded on a Y-board conventionally. The control print circuit board connects to the X-board via flexible printed circuit boards (FPCs), while the X-board and the Y board each connects to the liquid crystal panel via other FPCs. Therefore, the conventional LCD requires at least three boards to be connected to the panel and the manufacturing process is thus complex. In order to simplify the manufacturing process, the chip-one-glass (COG) LCD has been developed.

[0005] FIG. 1 is diagram of a conventional COG LCD. The COG LCD 100 includes a panel 110, a plurality of source drivers 112, at least one gate driver 114, a printed circuit board 120 and a plurality of flexible printed circuit board 130. The source drivers 112 and the gate driver 114 are disposed on the glass substrate of the panel 110 and electrically connects to the printed circuit board 120 via the flexible printed circuit boards 130. The timing controller (not shown in FIG. 1) is disposed on the printed circuit board 120, outputs image data and the control signal to the source drivers 112 and the gate driver 114. In COG LCD 100, only one board (PCB 120), instead of three, is required to connect to the panel 110 via the FPCs 130, therefore, the manufacturing process is simplified.

[0006] However, the manufacturing process of COG LCD is still not simplified enough because a plurality of the flexible printed circuit boards are needed, and in the above example in FIG. 1, the number of the flexible printed circuit board is 11. Besides, the flexible printed boards need a plurality of contact points with the liquid crystal panel and the possibility of electrical contact failure is thus increased.

SUMMARY OF THE INVENTION

[0007] It is therefore an object of the invention to provide a COG LCD that reduces the number of the flexible printed circuit boards and a transmission method for the LCD.

[0008] The invention achieves the above-identified objects by providing a new liquid crystal display (LCD) comprising a glass substrate, a plurality of serial-connected source drivers and at least one gate driver, disposed on the glass substrate by chip-on-glass technology, a timing controller for generating image data and a control signal, and at least one flexible printed circuit board. The flexible printed circuit board receives the image data and the control signal for transmitting to the corresponding source driver. Then the corresponding source driver transmits the image data and the control signal to the neighboring source drivers such that all the source drivers respectively get the image data and the control signal. The flexible printed circuit board is disposed such that delays and distortions of the image data and the control signal are acceptable to the source drivers.

[0009] Other objects, features, and advantages of the invention will become apparent from the following detailed description of the preferred but non-limiting embodiments. The following description is made with reference to the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0010] FIG. 1 is diagram of a conventional COG LCD.

[0011] FIG. 2A is a diagram of a chip-on-glass (COG) liquid crystal display (LCD) according to a preferred embodiment of the invention.

[0012] FIG. 2B is a diagram of a COG LCD according to another preferred embodiment of the invention.

[0013] FIG. 3 is a diagram of control signals of the source drivers and the gate drivers of the LCD.

[0014] FIG. 4 is a format diagram of a control packet.

[0015] FIG. 5A is a diagram of the source driver according to the preferred embodiment of the invention.

[0016] FIG. 5B is a block diagram of the wave generator in FIG. 5A.

[0017] FIG. 5C is a block diagram of the ID recognizer in FIG. 5B.

[0018] FIG. 5D is a waveform diagram of control signal POL.

[0019] FIG. 5E is a waveform diagram of the generation of the control signal TP.

[0020] FIG. 6A is a flowchart of a convergent transmission method for power saving.

[0021] FIG. 6B is a flowchart of a divergent transmission method for power saving.

DETAILED DESCRIPTION OF THE INVENTION

[0022] FIG. 2A is a diagram of a chip-on-glass (COG) liquid crystal display (LCD) according to a preferred embodiment of the invention. The LCD 200 includes a panel 210, a plurality of source drivers (S/D) 212(1)-212(10), at least one gate driver 214, a printed circuit board 220 and flexible printed circuit board (FPC) 230 and 232. The source drivers 212 and gate driver 214 are disposed on the glass substrate of the panel 210 by the chip-on-glass technology. The timing controller 225 is disposed on the printed circuit board 220 for outputting image data and control signals both to source drivers 212(3) and 212(8) respectively via the flexible printed circuit boards 230 and 232. Then, via the wires on the glass substrate, the source driver 212(3) transmits the image data and the control signals to the neighboring source drivers 212(1), 212(2), 212(4) and 212(5), and the source driver 212(8) transmits the image data and the control signals to the neighboring source drivers 212(5), 212(6), 212(7), 212 (8) and 212(10). Based on the control signals, one of the source drivers, such as the source driver 212(1), which is nearest to the gate driver 214, can generate gate control signals G to the gate driver 214. The reason to choose the source driver nearest to the gate driver 212 is to reduce the length of the wire therebetween so as to effectively reduce the distortions and delays of the gate control signals G. It is worthy of noting that other source drives can also be used to generate the gate control signals G, not just limited to the source driver 212(1). In this embodiment, the number of the flexible printed circuit boards are greatly reduced to 2 because the LCD uses the wires disposed on the glass substrate for transmitting the image data and the control signals.

[0023] The source drivers 212 each has a first operation mode and a second operation mode. The source driver 212(3) and the source driver 212(8) are set to the first operation mode to execute the dual-way transmission. That is, the source driver 212(3) and the source driver 212(8) each receives the image data and control signals from the timing controller 225 and transmits them to the neighboring source drivers at both the right side and the left side thereof. Take the source driver 212(3) for example, the source driver 212(3) can simultaneously transmit the image data and control signals to both the neighboring source driver 212(2) and 212(4), which are located at the two sides of the source driver 212(3). The source drivers 212(1), 212(2), 212(4)-212(7), 212(9) and 212(10) are set to the second operation mode to execute the single-way transmission, and are not directly connected to the timing controller 225. That is, the source drivers 212(1), 212(2), 212(4)-212(7), 212(9) and 212 (10) each can receive the image data and the control signals from the right (or left) source driver and transmit them to the left (or right) source driver. Take the source driver 212(2) for example, it receives the image data and the control signals from the source driver 212(3) at right side thereof and transmits them to the source driver 212 (1) at the left side thereof. In the embodiment, the LCD 200 is a big screen monitor having 10 source drivers and two flexible printed circuit board 230 and 232. The number of flexible printed circuit boards is not limited to two as long as the distortions and delays of signals is acceptable.

[0024] In the embodiment, the source drivers are divided into a left group including source drivers 212(1)-212(5) and a right group including source drivers 212(6)-212(10). The flexible printed circuit boards 230 connects to the center source drivers 212(3) of the left group, and the flexible printed circuit boards 232 connects to the center source drivers 212(8) of the right group, such that the distortions and delays of signals, caused by the parasitic capacitance and resistance, can be minimized. On the other hand, the source drivers can also be divided into more than three groups and each group directly connects to the timing controller via a flexible printed circuit board, so long as the distortions and delays of the signals are acceptable.

[0025] FIG. 2B is a diagram of a COG LCD 250 according to another preferred embodiment of the invention. Compared with the LCD 200, the LCD 250 further includes a gate driver 216 at the right side of the panel 210. The gate driver 214 and 216 together drivers the panel 210 from two sides thereof. The other elements of LCD 250 is the same with that of the LCD 200 and are not described here again.

[0026] FIG. 3 is a diagram of control signals of the source drivers and the gate drivers of the LCD. The control signals includes gate control signals G and source control signals S. The gate control signals G includes a gate driver start signal STV for representing the start of a frame, a gate clock signal CPV for enabling a gate line, and a gate driver output enable signal OEV for defining the enabled duration of the gate line. The source control signals S includes a source driver start signal STH for notifying the source driver to start to prepare the data of a horizontal line, a data enable signal DE for starting to receive data, a load signal TP for starting to output driving voltages to the data lines, and a polarization control signal POL for controlling the polarization inversion.

[0027] When the source driver start signal STH is asserted, the source driver 212 start to prepare to receive data, and after a period td1, the data enable signal DE is asserted such that the timing controller 225 starts to output the image data to the source drivers 212. The source drivers 212 generates the driving voltage with the polarization designated by the polarization control signal POL and then outputs the driving voltages to the panel 210 according to the load signal Tp.

[0028] In the convention LCD 100, the control signals are outputted by the timing controller directly to each source driver 112 and the gate driver 114. Each control signal conventionally needs at least one wire to transmit, and thus a plurality of wires are required. And, the control signals are easily distorted and delayed because the wires between the timing controller and the source driv-

ers and the gate driver have parasitic capacitance and resistance.

[0029] In the embodiment, the timing controller 225 integrates the control signals into a control bitstream C and transmits it by a wire to the source drivers 212. For example, the control signals can be packed into a plurality of control packets, each representing an event relevant to a control signal. The timing controller 225 can designate one source driver 212 to receive the control packet by a target identification. The target identification is, for example, included in the control packet for each source driver to identify. After receiving the control packet, the source driver 212 can decode the control packet to generate the control signal. Therefore, the number of the wires required to transmit the control signals is thus greatly reduced in the embodiment.

[0030] The source driver 212 has a built-in identification so as to identify whether the received control packet is for its own by comparing the target identification of the control packet with the built-in identification.

[Transmission protocol of the control bitstream]

[0031] Conventionally the control signals are each transmitted by a wire from the timing controller to the source driver/gate driver. The source drivers and the gate driver each needs a plurality of control signals and thus the number of the wires for transmitting the control signals is great. Therefore number of wires in the conventional flexible printed circuit board is also great, so the cost and quality of the conventional flexible printed circuit board is also increased. Besides, the lengths of the wires between the timing controller and the source drivers/gate driver are so long that the delays and distortions of the signals are easily occurred.

[0032] In the embodiment, the timing controller 225 transmits the control bitstream C to the source driver only via at least one wire. The control bitstream C includes a plurality of control packets, each representing an event of one corresponding control signal, such as a pull high event or a pull low event. After receiving the control packet, the source driver 212 generates the corresponding control signal by pulling high or pulling low accordingly.

[0033] FIG. 4 is a format diagram of a control packet. A control packet includes a header field 310 and a control item, which includes a control field 312 and a data field 314. The header field 310 records a predetermined pattern for identifying the start of a packet, the predetermined pattern is 0x11111 for example. The control field 312 records the type of the event, such as the STH event, the TP event, the pull high event, the pull low event and the initialization event. The data field 314 records the parameters of the event.

[0034] In the embodiment, each control packet has 16 bits. If receiving the control packet by dual-edge sampling, it takes 8 clock to read one control packet. That is, the control signal generated by a pull high event and a pull low event must remain at high level for at least a duration of 8 clocks. The control signals POL, CPV, STV, OEV can each be generated by a pull high event and a pull low event. The control signals that has the duration less than 8 clocks, such as control signals STH and TP, are generated respectively by the STH event and the TP event. After receiving the STH event/TP event, the source driver pulls high the control signal STH/TP for a pre-determined period td2/tw1 and then pulls low the control signal STH/TP. It is worth noticing that the sampling method for receiving the control packet is not limited to dual-edge sampling, rising-edge sampling or falling-edge sampling can also be used.

[0035] In regard to the control packet having the control field 312 recording the STH event, the data field 314 thereof records the target identification. For example, the source drivers 212(1)-212(10) have the built-in identifications of 0x0001-0x1010, respectively. After receiving the control packet with STH event, the source driver compares the target identification of this control packet with the built-in identification, pull high the control signal STH if the comparison is matched, and then pull low the control signal STH after a period td2.

[0036] From FIG. 3, it can be seen that the control signals TP and CPV are pulled high at the same time, so after receiving the control packet with TP event, control signals TP and CPV are pulled high. The control signal TP is then pulled low after a period tw1, and the control signal CPV is pulled low after receiving the control packet with pull low event of CPV.

[0037] Control signals POL, STV and OEV are generated by a pull high event and a pull low event. In regard to the control packet with the control field 312 recording a pull high event, its data field 314 designates which signal is to be pulled high. In regard to the control packet with the control field 312 recording a pull low event, its data field 314 designates which signal is to be pulled low.

[0038] In regard to the control packet with the control field 312 recording an initialization event, it is for setting several kinds of initialization, such as the fan out of the source drivers. Other kinds of events can also be represented by the control packets and would not be described herein.

[0039] In the embodiment, only at least one wire is required to transmit the control bitstream C, so the number of wires connecting the timing controller and the source drivers are greatly reduced, the layout of the circuit is simplified, and the stability is enhanced. In addition, the control bitstream C can integrate only a part of the control signals and leave other part of the control signals to be transmitted respectively in independent wires. Although not all the control signals are integrated to the control bitstream, the number of wires can also be reduced.

[Source drivers]

[0040] FIG. 5A is a diagram of the source driver according to the preferred embodiment of the invention. The source driver 212 includes a receiver 410, 412, a

transceiver 413, 415, a bus switch 422, a wave generator 420, 421, and a driving unit 434. The transceiver 413 includes a control transceiver 414 and a data transceiver 424, and the transceiver 415 includes a control transceiver 416 and a data transceiver 426.

[0041] The bus switch 422 includes two switches SW1 and SW2. When the source driver, 212(3) or 212(8) in this embodiment, operates at the first operation mode, the bus switch turns off the switches SW1 and SW2 such that the control transceiver 414 and 416 are disconnected and the data transceiver 424 and 426 are disconnected. Thus, the control bitstream C1 and the image data D1 received by the receiver 410 are transmitted to the control transceiver 414 and the data transceiver 424, respectively, and the control bitstream C2 and the image data D2 received by the receiver 410 are transmitted to the control transceiver 416 and the data transceiver 426, respectively.

[0042] When the source driver, 212(1)-212(2), 212(4)-212(7), 212(9), or 212(10) in this embodiment, operates in the second operation mode, the receivers 410 and 412 are disabled, and the bus switch turns on the switches SW1 and SW2 such that the transceivers 413 and 415 are connected, that is, the data transceivers 424 and 426 are connected and the control transceivers 414 and 416 are connected. Thus, the source driver can transmit the control bitstream and the image data received to the next adjacent source driver in response to the designated transmission direction.

[0043] The wave generator 420 and 421 receives the control bitstream C1 and C2 respectively for generating source control signals S, such as STH(1), STH(2), POL(1), POL(2), TP(1) and TP(2), etc., and thus generating the gate control signals G, such as CPV(1), CPV(2), STV(1), STV(2), OEV(1), OEV(2) and etc. The control signals G are generated by one of the source drivers. In the LCD 200 in FIG. 2A, one of the source drivers 212, such as 212(1) that is nearest to the gate driver 214, generates the gate control signals G, while the other source drivers 212 do not. In addition, in the LCD 250 in FIG. 2B, two source drivers, such as 212(1) and 212(10) that are respectively nearest to the gate drivers 214 and 216, generate the gate control signals G respectively for the gate drivers 214 and 216, while others do not.

[0044] When receiving the signal STH, the driving unit 434 starts to latch image data D for converting to analog driving voltages in response to the signal POL, and then transmits the analog driving signals to the panel 210 after receiving the load signal TP.

[0045] In the first-operation-mode source driver, such as 212(3), the wave generators 420 and 421 are both activated to receive the control bitstreams C1 and C2 respectively and generate the source control signals S and the gate control signals G, while the control bitstream C1 and C2 are independent, and image data D1 and D2 are independent. On the other hand, in second-operation-mode source driver, such as 212(2) or 212(4), the control bitstream C1 is the control bitstream C2, and the image data D1 is the image data D2, so only one of the wave generators 420 and 421 is activated to generate the source control signals S and the gate control signals G. The other wave generator in the second-operation-mode source driver can be disabled, omitted or still activated to generate the source control signals S and the gate control signals G.

[0046] FIG. 5B is a block diagram of the wave generator in FIG. 5A. Each of the wave generators 420 and 412 includes a parser 451, an ID recognizer 453, a signal generator 460 and an initiator 470. The parser 451 receives the control bitstream C to parse the control item, including the control field 312 and a data field 314, of a control packet, and sends the parsed control item to the ID recognizer 453, the signal generator 460 or the initiator 470 correspondingly: the control item with the identity event, which is the STH event in this embodiment, is sent to the ID recognizer 453; the control item with the pull high event or the pull low event is set to the signal generator 460; the control item with the initialization event is sent to the initiator 470.

[0047] FIG. 5C is a block diagram of the ID recognizer in FIG. 5B. The recognizer 453 includes a comparator 456. Each source driver has a unique chip identity IDp. The chip identity IDp is set externally, for example by, respectively, pulling high or pulling low the pins of the source driver on the glass substrate. The comparator 456 triggers the signal STH when the comparison of the chip identity IDp with a target identity IDt extracted from the control packet is matched. The duration time td2 of the signal STH can be pre-determined in the comparator 456.

[0048] The signal generator 460 pulls high the corresponding signal after receiving the control item with the pull high event. The level of the pull-high signal is maintained until the signal generator 460 receives the corresponding control item with the pull low event. Take generation of the control signal POL for example. FIG. 5D is a waveform diagram of control signal POL. When receiving the control item with the pull high event H, the signal generator 460 pulls high the signal PH; when receiving the control with the corresponding pull low event L, the signal generator 460 pulls low the signal PL. Then, the coupling of the signal PH and the signal PL is the signal POL. The other control signals, such as CPV, STV, OEV, are also generated by the above-mentioned procedure.

[0049] But, the control signal is not suitable to be generated by the pull high event and the pull low event if the duration time of the high level of the control signal is less than 8 clocks, such as the control signal TP, since that it takes 8 clocks for the wave generator to read a control packet. FIG. 5E is a waveform diagram of the generation of the control signal TP. When receiving the control item with the pull high event H of the control signal TP, the signal generator 460 pulls high the signal TH, then counts for a pre-determined period tw1, and then pulls low the signal TL. The coupling of the signal TH and the signal TL is the control signal TP.

[0050] In addition to generate by the pull high event

and the pull low event as described in the last paragraph, the gate control signals G can also be generated according to the source control signals, such as STH or TP. Please refer to FIG. 3. First, take the generation of the signal CPV according to the control signal STH for example: when the control signal STH of the source driver 212(1) is asserted, the counter thereof is activated, and the signal CPV is pulled high after a period td6 passed, and, after a period tw4 passed, the signal CPV is pulled low. Second, take the generation of the signal STV according to the control signal STH for example: when the control signal STH of the source driver 212(1) is asserted, the signal STV is pulled high after a period td7 and then pulled low after a period tw5. Third, take the generation of the signal OEV according to the control signal STH for example: when the control signal STH of the source driver 212(1) is asserted, the signal OEV is pulled high after a period td8 passed and pulled low after a period tw6 passed.

[0051] After receiving the control item with the initialization event, the initiator 470 outputs a DC value to set the corresponding parameter.

[0052] The source driver of the embodiment can reduce the control signal decay because the source control signals is generated by the source driver itself, not by the timing controller conventionally.

[0053] In addition, the embodiment can save the number of wires from the timing controller to the gate driver because the source driver can generate the gate control signals and directly send to the gate driver via the wires on the glass substrate. The quality of the gate control signals are thus improved because the lengths of the transmission wires are reduced.

[Power Management]

[0054] FIG. 6A is a flowchart of a convergent transmission method for power saving. Take the source drivers 212(1)-212(5) in FIG. 2A for example. First, at step 610, the source drivers 212(1) and 212(5), which have the farthest distances away from the timing controller 225, receive the image data transmitted by the timing controller 225 via the source drivers, and then enter the power-saving mode, which turns of the power for the data transceivers 424 and 426 of the source drivers 212(1) and 212(5), for example. Next, at step 612, the source drivers 212(2) and 212(4), which are the active ones having the farthest distances away from the timing controller 225, receive the image data and then enter the power-saving mode, which turns of the power for the data transceivers 424 and 426 of the source drivers 212(2) and 212(4), for example. Next, at step 614, the source driver 212(3) receives the image data from the timing controller 225 and then enters the power-saving mode. It is noted that, in the power-saving mode, the power for the control transceiver 416 and 414 of the source driver should not be turned off. Then, at step 616, each of the source drivers 212(1)-212(5) receives the load signal TP and then is waked up to start to drive the panel 210. The transmission method can also apply to the source drivers 212(6)-212(10) and would not be repeated here.

[0055] FIG. 6B is a flowchart of a divergent transmission method for power saving. Take the source drivers 212(1)-212(5) in FIG. 2A for example. First, the source drivers 212(1)-212(5) enter the power-saving mode. Next, at step 622, the source driver 212(3), which is nearest to the timing controller 225, is waked up to receive the image data transmitted by the timing controller 225. Next, at step 624, the source drivers 212(2) and 212(4) are waked up to receive the image data. Next, at step 626, the source drivers 212(1) and 212(5) are waked up to receive the image data. The transmission method can also apply to the source drivers 212(6)-212(10) and would not be repeated again.

[0056] In the power-saving mode, at least the power for data transceivers and the driving unit can be turned off. The data transceivers transmit the image data, which has large voltage swings and high frequency that make the power consumption great. Thus the power-saving convergent/divergent transmission methods can reduce unnecessary data transmission for saving power. The power for the control transceivers of the source driver should not be turned off such that the source driver can still receive the control bitstream and operate responsively.

[0057] The convergent transmission method and the divergent transmission method can be applied at the same time. For example, the source drivers 212(1)-212(3) can use the convergent transmission method, while the source drivers 212(4)-212(5) use the divergent transmission method, or vice versa. The other modifications can be implemented by the ordinary skill in the art according to the invention and would not be listed here.

[0058] While the invention has been described by way of example and in terms of a preferred embodiment, it is to be understood that the invention is not limited thereto. On the contrary, it is intended to cover various modifications and similar arrangements and procedures, and the scope of the appended claims therefore should be accorded the broadest interpretation so as to encompass all such modifications and similar arrangements and procedures.

Claims

1. A liquid crystal display (LCD) comprising:

a glass substrate;
a plurality of serial-connected source drivers and at least one gate driver, disposed on the glass substrate by chip-on-glass technology;
a timing controller for generating image data and a control signal; and
at least one flexible printed circuit board receiving the image data and the control signal for

transmitting to the corresponding source driver, and then the corresponding source driver transmitting the image data and the control signal to the neighboring source drivers such that all the source drivers respectively get the image data and the control signal;

wherein the flexible printed circuit board is disposed such that delays and distortions of the image data and the control signal are acceptable to the source drivers.

2. The LCD according to claim 1, wherein the corresponding source driver is a dual-way transmission source driver for transmitting the image data and the control signal to the neighboring source drivers at two sides thereof.

3. The LCD according claim 1, wherein the neighboring source drivers are single-way transmission source driver for transmitting the image data and the control signal from the neighboring source driver at one side thereof to the neighboring source driver at the other side thereof.

4. The LCD according to claim 1, wherein the at least one flexible printed circuit board is disposed at the center one of the source drivers.

5. A source driver for driving a liquid crystal display (LCD), the LCD having a timing controller for generating image data and a control signal, the source driver comprising:

a first receiver and a second receiver for receiving the image data and the control signal from the timing controller;
a first transceiver and a second transceiver electrically connected to neighboring source drivers at the two sides of the source driver;
a driving unit receiving the image data and the control signal for generating driving voltages to drive the LCD; and
a bus switch selectively connecting the first transceiver and the second transceiver, whereby the first transceiver and the second transceiver are disconnected when the source driver is in a dual-way transmission mode such that the first transceiver receives the image data and the control signal from the first receiver and that the second transceiver receivers the image data and the control signal form the second receiver, whereby the first transceiver and the second transceiver are connected when the source driver is in a single-way transmission mode such that the image data and the control signal received by the first transceiver are transmitted to the second transceiver.

6. The source driver according to claim 5 further comprising:

a first wave generator and a second wave generator for generating a source control signal and a gate control signal according to the control signal.

7. The source driver according to claim 6, wherein the first wave generator is disabled when the source driver is in the single-way transmission mode, and the second wave generator generates the source control signal and the gate control signal.

8. The source driver according to claim 6, wherein the first receiver and the second receiver receives the control signal simultaneously when the source driver is in the single-way transmission mode.

9. The source driver according to claim 5, wherein the first transceiver comprises a first control transceiver and a first data transceiver, and the second transceiver comprises a second control transceiver and a second data transceiver.

10. A transmission method for a liquid crystal display (LCD), the LCD having a plurality of source drivers and at least one gate driver disposed by chip-on-glass technology, the method comprising:

selecting at least one source driver;
inputting image data and a control signal via the selected source driver to the LCD; and
transmitting the image data and the control signal by the selected source driver to the neighboring source drivers at two sides of the selected source driver.

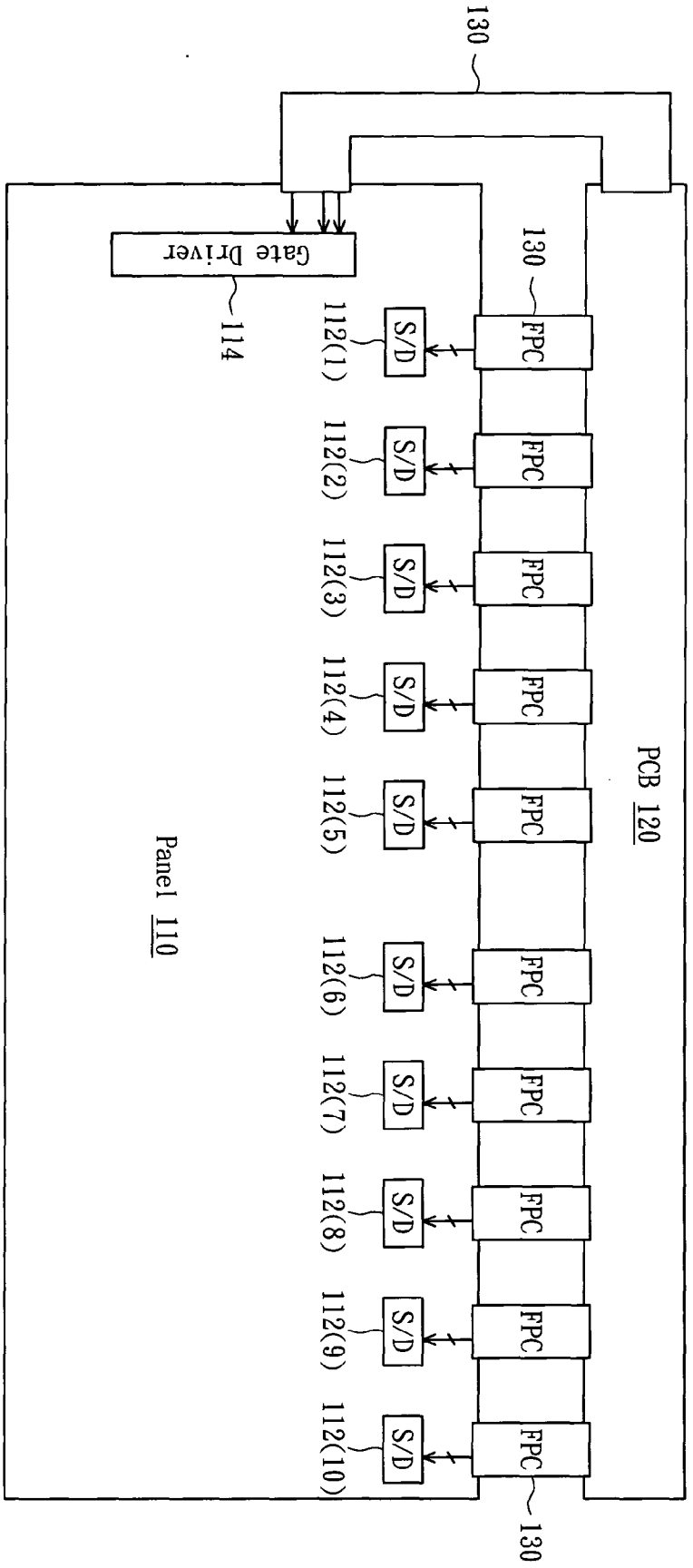

FIG. 1(PRIOR ART)

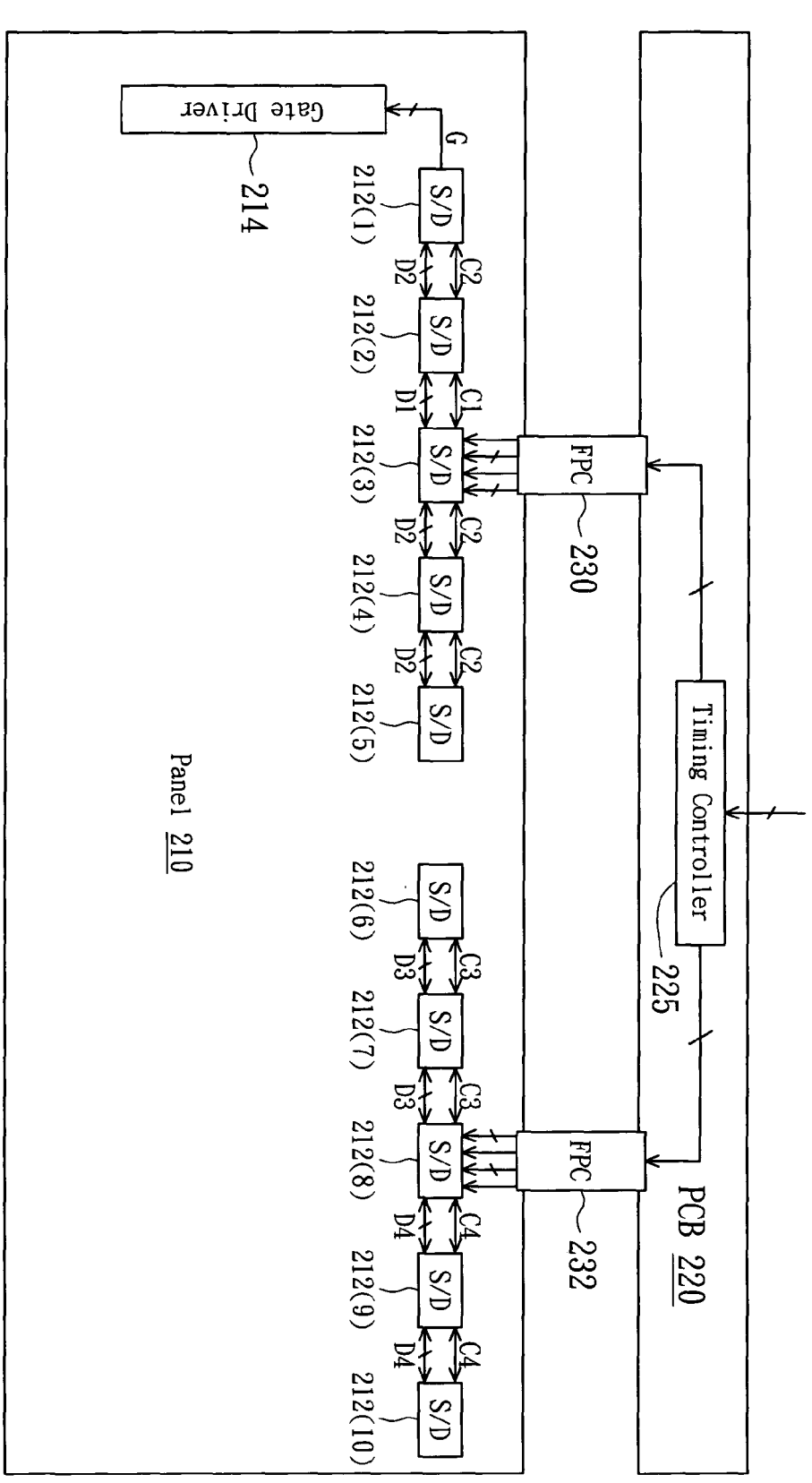
200
Timing Controller
225
PCB 220
FPC
230
FPC
232
Gate Driver
214
G
S/D
212(1)
212(2)
212(3)
212(4)
212(5)
212(6)
212(7)
212(8)
212(9)
212(10)
C1
C2
C3
C4
D1
D2
D3
D4
Panel 210

FIG. 2A

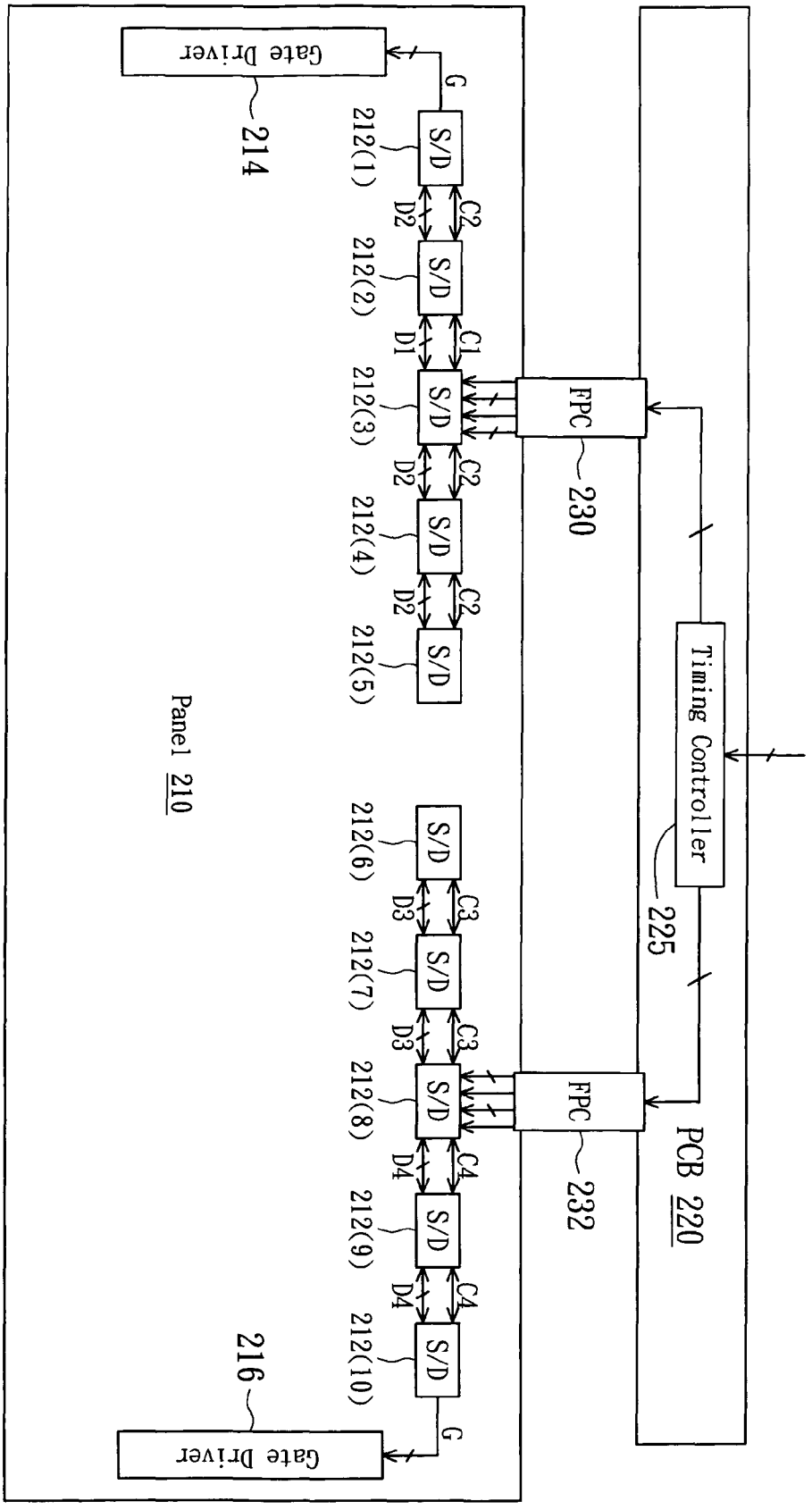
200
Gate Driver
214
G
212(1)
S/D
D2
C2
212(2)
212(3)
D1
C1
212(4)
212(5)
FPC
230
Timing Controller
225
PCB 220
Panel 210
212(6)
D3
C3
212(7)
212(8)
FPC
232
D4
C4
212(9)
212(10)
216
Gate Driver

FIG. 2B

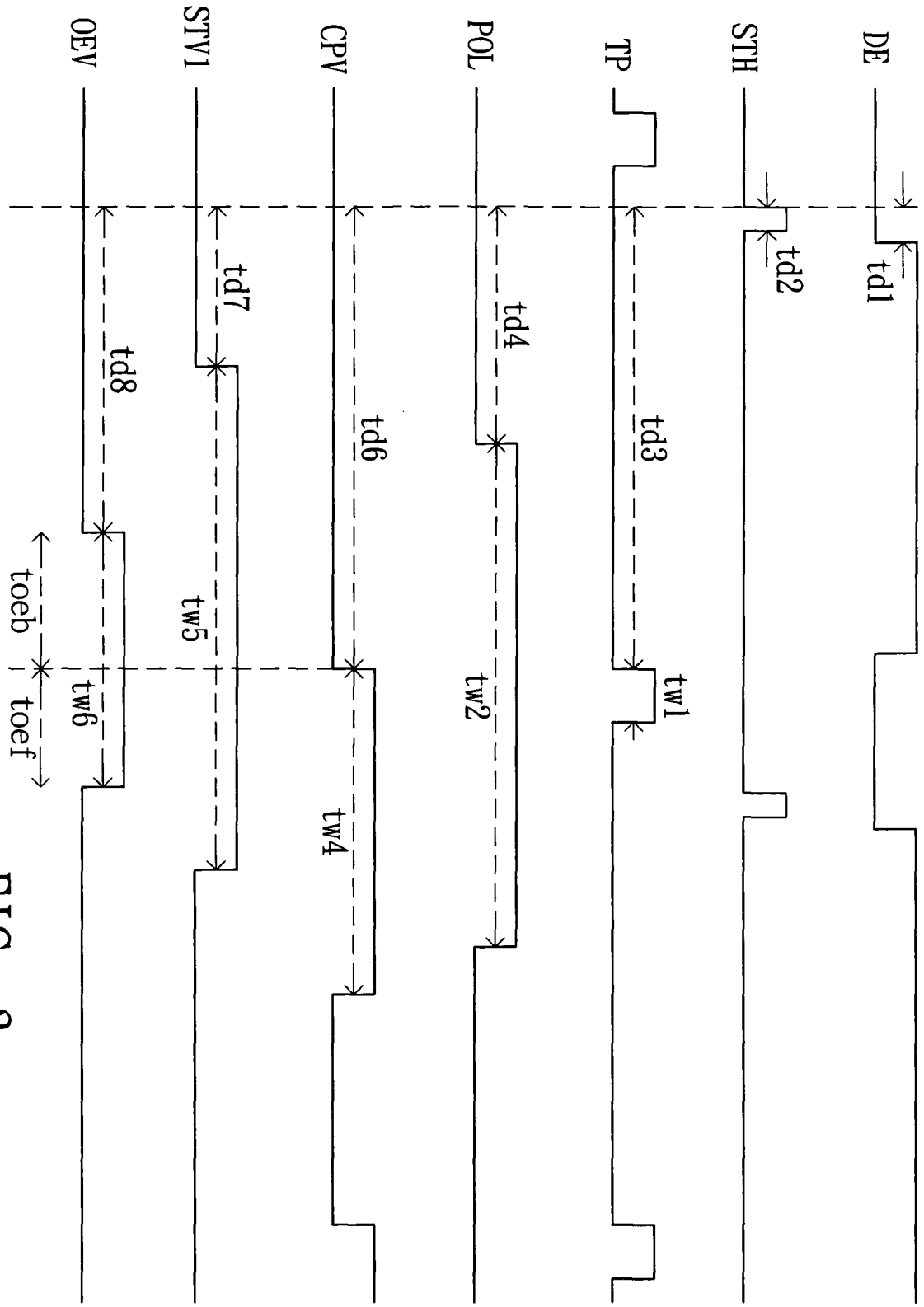
DE
STH
TP
POL
CPV
STV1
OEV
td1
td2
td3
td4
td6
td7
td8
tw1
tw2
tw4
tw5
tw6
toeb
toef

FIG. 3

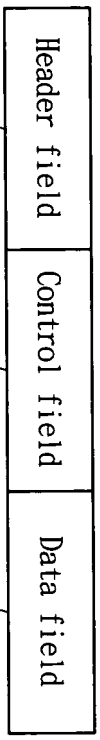

FIG. 4

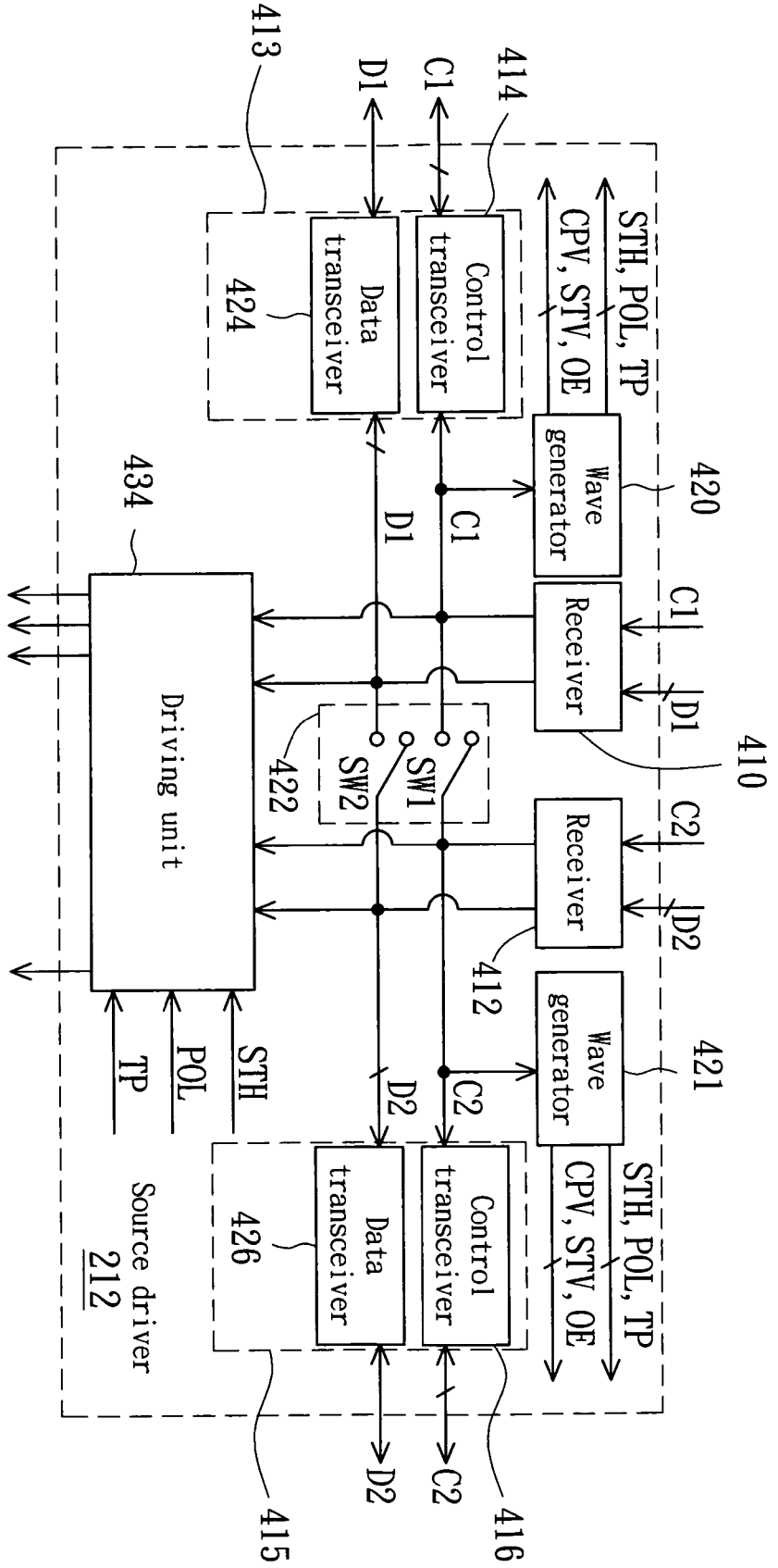
410
420
421
412
413
414
415
416
422
424
426
434
212
Source driver
Driving unit
Wave generator
Receiver
Control transceiver
Data transceiver
STH, POL, TP
CPV, STV, OE
SW1
SW2
C1
C2
D1
D2
STH
POL
TP

FIG. 5A

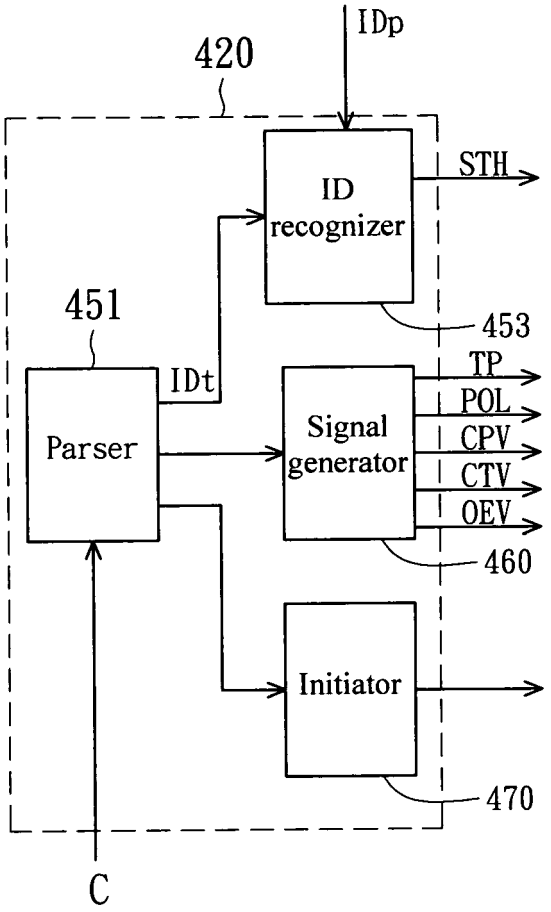
IDp
420
ID recognizer
STH
453
451
IDt
Parser
Signal generator
TP
POL
CPV
CTV
OEV
460
Initiator
470
C

FIG. 5B

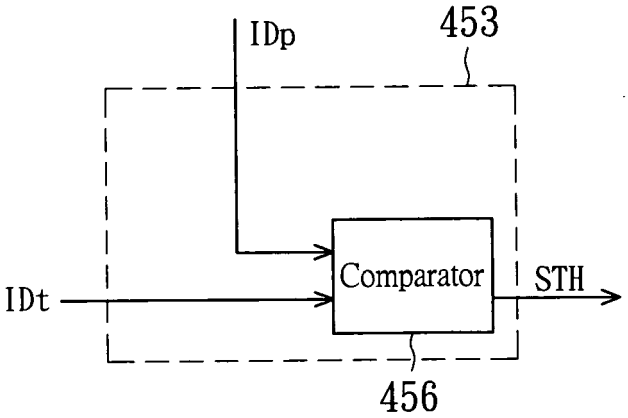
IDp
453
Comparator
IDt
STH
456

FIG. 5C

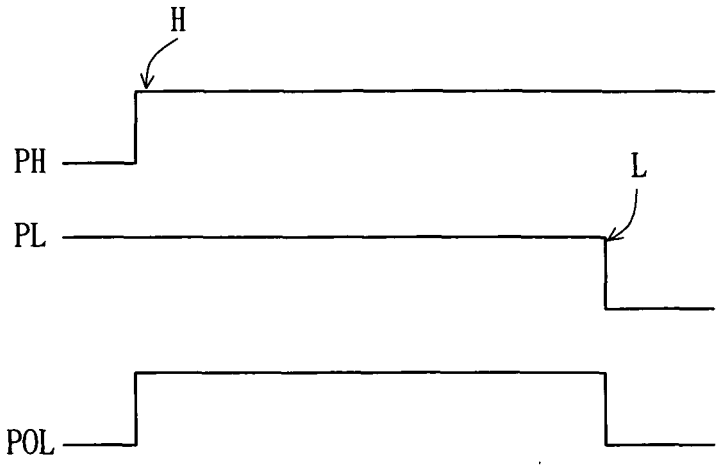

FIG. 5D

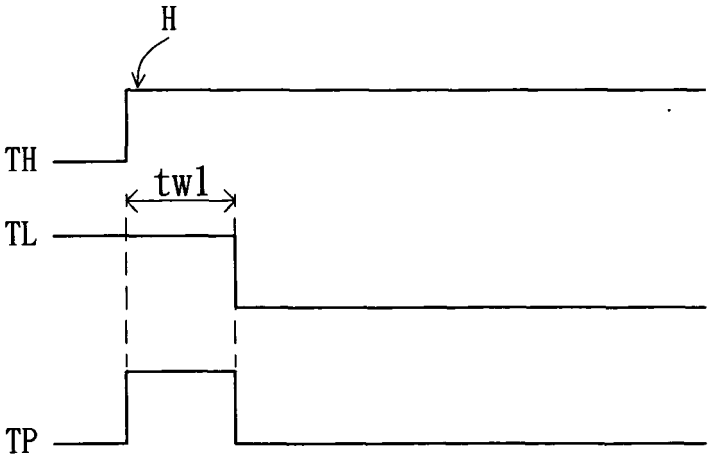

FIG. 5E

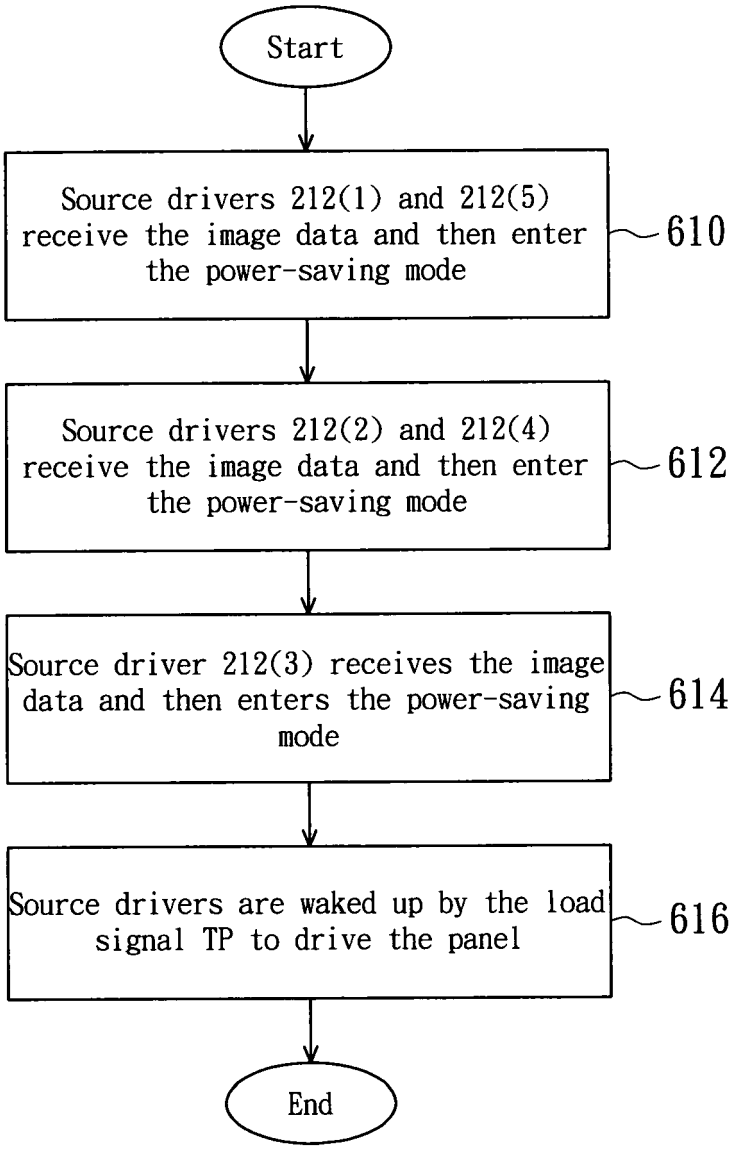
Start
Source drivers 212(1) and 212(5) receive the image data and then enter the power-saving mode
610
Source drivers 212(2) and 212(4) receive the image data and then enter the power-saving mode
612
Source driver 212(3) receives the image data and then enters the power-saving mode
614
Source drivers are waked up by the load signal TP to drive the panel
616
End

FIG. 6A

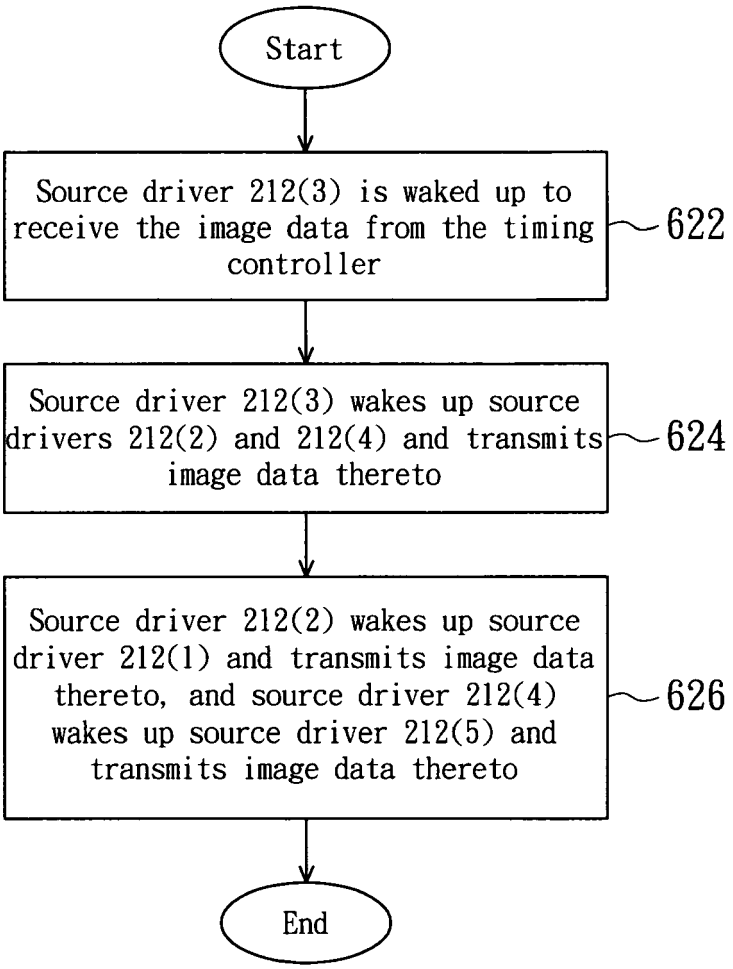
Start
Source driver 212(3) is waked up to receive the image data from the timing controller
622
Source driver 212(3) wakes up source drivers 212(2) and 212(4) and transmits image data thereto
624
Source driver 212(2) wakes up source driver 212(1) and transmits image data thereto, and source driver 212(4) wakes up source driver 212(5) and transmits image data thereto
626
End

FIG. 6B

REFERENCES CITED IN THE DESCRIPTION

This list of references cited by the applicant is for the reader's convenience only. It does not form part of the European patent document. Even though great care has been taken in compiling the references, errors or omissions cannot be excluded and the EPO disclaims all liability in this regard.

Patent documents cited in the description

- CN 200510062825 **[0001]**