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(54) **Method and apparatus for generating gate control signal of liquid crystal display**

Verfahren und Vorrichtung zur Erzeugung eines Gatesteuersignals einer Flüssigkristallanzeige

Procédé et appareil permettant de générer un signal de contrôle de porte d'un affichage à cristaux liquides

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## Description

**[0001]** This application claims the benefit of People's Republic of China application Serial No. 200510062825.7, filed March 31, 2005, the subject matter of which is incorporated herein by reference.

BACKGROUND OF THE INVENTION

Field of the Invention

**[0002]** The invention relates in general to a liquid crystal display, and more particularly to a chip-on-glass liquid crystal display.

Description of the Related Art

**[0003]** Liquid crystal displays (LCD) have become more and more popular in computer monitors or TVs due to their light weight, flatness and low radiation, compared with the CRT monitor. In addition to improving the display quality of LCDs, such as color, contrast and brightness, the manufacturers try to improve the manufacturing process to reduce the cost and manufacturing time.

**[0004]** The LCD includes a timing controller, source drivers and at least one gate driver to drive its liquid crystal panel. Conventionally, the timing controller is welded on a control print circuit board, the source drivers are welded on an X-board, and the gate driver is welded on a Y-board. The control print circuit board connects to the X-board via flexible printed circuit boards (FPCs), while the X-board and the Y board each connects to the liquid crystal panel via other FPCs. Therefore, the conventional LCD requires at least three boards to be connected to the panel and the manufacturing process is thus complex. In order to simplify the manufacturing process, the chip-on-glass (COG) LCD has been developed.

**[0005]** FIG. 1 is diagram of a conventional COG LCD. The.COG LCD 100 includes a panel 110, a plurality of source drivers 112, at least one gate driver 114, a printed circuit board 120 and a plurality of flexible printed circuit boards 130. The source drivers 112 and the gate driver 114 are disposed on the glass substrate of the panel 110 and electrically connected to the printed circuit board 120 via the flexible printed circuit boards 130. The timing controller (not shown in FIG. 1) is disposed on the printed circuit board 120, and outputs image data and control signals to the source drivers 112 and the gate driver 114. In COG LCD 100, only one board (PCB 120), instead of three, is required to connect to the panel 110 via the FPCs 130. Therefore, the manufacturing process is simplified.

**[0006]** However, the manufacturing process of COG LCD is still not simplified enough because a plurality of flexible printed circuit boards are needed, and in the above example in FIG. 1, the number of flexible printed circuit boards is 11. The flexible printed boards need a plurality of contact points with the liquid crystal panel and the possibility of electrical contact failure is thus increased.

**[0007]** US Patent Application Publication No. 2002/0075204, entitled "Plurality of column electrode driving circuits and display device including the same", discloses a plurality of column electrode driving circuits used in a matrix type display device including a plurality of row electrode driving circuits each for driving a plurality of row electrodes and the plurality of column electrode driving circuits each for driving a plurality of column electrodes. Each of the plurality of column electrode driving circuits includes a data input section for receiving a control data signal for the plurality of column electrodes; a timing control section for generating a timing control signal for controlling at least one of the row electrode driving circuit and the column electrode driving circuit; a selection section for selecting one of a signal in synchronization with the timing signal generated by the timing control section and the control data signal input to the data input section, based on the control data signal input to the data input section; and a data output section for outputting one of the signal in synchronization with the timing signal and the control data signal which is selected by the selection section. The data input section of a second column electrode driving circuit of the plurality of column electrode driving circuits is connected to the data output section of a first column electrode driving circuit of the plurality of column electrode driving circuits, and the data output section of the second column electrode driving circuit is connected to the data input section of a third column electrode driving circuit of the plurality of column electrode driving circuits.

**[0008]** US Patent Application Publication No. 2001/0013850, entitled "Liquid crystal display device, liquid crystal controller and video signal transmission method", reduces the number of inputs to an LCD driver and reduces manufacturing costs by employing the COG&WOA technique. For a liquid crystal display device, source driver ICs 20, among which video signals are transmitted and distributed via a video I/F 3, are cascade-connected, and the connection lines to the source driver ICs 20 are reduced as much as possible to employ the COG&WOA technique. That is, a liquid crystal display device comprises: a liquid crystal cell 2, which forms an image display area on a substrate, and a source driver 7, which applies a voltage to the liquid crystal cell 2 based on a video signal input via a video I/F 3. The source driver 7 includes a plurality of source driver ICs 20 that are mounted on the same substrate as the liquid crystal cell 2 and that are cascade-connected by signal lines.

**[0009]** US Patent Application Publication No. 2003/0103390, entitled "Semiconductor device equipped with transfer circuit for cascade connection", discloses a transfer circuit 25 including two sets of an input circuit 52A and an output circuit 53B, which allows bidirectional transfer. The input circuit 52A decomposes external input data signals DI11A and DI12A to signals on lines L11 to L14 in synchronism with a clock signal

CLK in order to reduce the frequency thereof. The output circuit 53B composes the decomposed signals in synchronism with the clock signal CLK to regenerate the original signals and output them as external output data signals DO11B and DO12B. Signals on either the lines L11 to L14 or L21 to L24 are selected by a multiplexer 57 to provide to a main body circuit.

## SUMMARY OF THE INVENTION

**[0010]** It is therefore an object of the invention to provide a COG LCD that reduces the number of flexible printed circuit boards and to provide a transmission method for the LCD.

**[0011]** It is another object of the invention to provide a method for generating gate control signals for reducing the number of flexible printed circuit boards.

**[0012]** Furthermore, it is another object of the invention to provide an identifier of the source driver of the COG LCD and an identifying method thereof.

**[0013]** It is another object of the invention to provide a source driver for single-way or dual-way transmission of the image data and the control signals from the timing controller.

**[0014]** It is another object of the invention to provide a method for transmitting control signals by packets so as to reduce the number of transmission lines to one or a limited number and reduce the number of flexible printed circuit boards.

**[0015]** It is another object of the invention to provide a method for power management so as to save power consumption of the COG LCD.

**[0016]** The invention achieves the above-identified objects by providing a liquid crystal display according to claim 1, in particular one that comprises a panel, a timing controller, source drivers and at least one gate driver. The panel has pixels arranged in a matrix. The timing controller outputs image data and a source control signal. The source drivers are connected in series and one of the source drivers is selected to generate a gate control signal by reference to the source control signal, a part of the source drivers which receive the image data and the source control signal directly from the timing controller being operated in a dual-way transmission mode for simultaneously transmitting signals to the neighboring source drivers at both sides thereof, while another part of the source drivers which are indirectly connected to the timing controller being operated in a single-way transmission mode for transmitting signals to the neighboring source driver at either one side thereof. The gate driver, along with the source drivers, drives the panel according to the gate control signal, wherein whether the source driver is operated in the dual-way transmission mode or the single-way transmission mode is related to connection of the source driver with the timing controller.

**[0017]** The invention achieves the above-identified objects by providing a method according to claim 6, in particular a method for generating a gate control signal of a liquid crystal display. The method first provides image data and a source control signal to the source drivers, a part of the source drivers which receive the image data and the source control signal directly from the timing controller being operated in a dual-way transmission mode for simultaneously transmitting signals to the neighboring source drivers at both sides thereof, while another part of the source drivers which are indirectly connected to the timing controller being operated in a single-way transmission mode for transmitting signals to the neighboring source driver at either one side thereof. Next, one source driver is selected to generate a gate control signal to the gate driver by reference to the source control signal for driving the panel by the gate driver and the source drivers, wherein whether the source driver is operated in the dual-way transmission mode or the single-way transmission mode is related to connection of the source driver with the timing controller.

**[0018]** The respective dependent claims define respective preferred embodiments thereof, respectively. Other objects, features, and advantages of the invention will become apparent from the following detailed description of the preferred but non-limiting embodiments. The following description is made with reference to the accompanying drawings.

## BRIEF DESCRIPTION OF THE DRAWINGS

**[0019]**

FIG. 1 is diagram of a conventional COG LCD.

FIG. 2A is a diagram of a chip-on-glass (COG) liquid crystal display

## DETAILED DESCRIPTION OF THE INVENTION

**[0020]** FIG. 2A is a diagram of a chip-on-glass (COG) liquid crystal display (LCD) according to a preferred embodiment of the invention. The LCD 200 includes a panel 210, a plurality of source drivers (S/D) 212(1)-212(10), at least one gate driver 214, a printed circuit board 220 and flexible printed circuit boards (FPC) 230 and 232. The source drivers 212 and gate driver 214 are disposed on the glass substrate of the panel 210 by chip-on-glass technology. The timing controller 225 is disposed on the printed circuit board 220 for outputting image data and control signals both to source drivers 212(3) and 212(8) respectively via the flexible printed circuit boards 230 and 232. Via the wires on the glass substrate, the source driver 212(3) transmits the image data and the control signals to the neighboring source drivers 212(1), 212(2), 212(4) and 212(5), and the source driver 212(8) transmits the image data and the control signals to the neighboring source drivers 212(5), 212(6), 212(7), 212(8) and 212(10). Based on the control signals, one of the source drivers, such as the source driver 212(1), which is nearest to the gate driver 214, can generate gate control signals

G to the gate driver 214. The reason to choose the source driver nearest to the gate driver 212 is to reduce the length of the wire therebetween so as to effectively reduce the distortions and delays of the gate control signals G. It is worthy of noting that other source drives can also be used to generate the gate control signals G, not just limited to the source driver 212(1). In this embodiment, the number of flexible printed circuit boards are greatly reduced to 2 because the LCD uses the wires disposed on the glass substrate for transmitting the image data and the control signals.

**[0021]** Each of the source drivers 212 has a first operation mode and a second operation mode. The source driver 212(3) and the source driver 212(8) are set to the first operation mode to execute the dual-way transmission. That is, the source driver 212(3) and the source driver 212(8) each receives the image data and control signals from the timing controller 225 and transmits them to the neighboring source drivers at both the right side and the left side thereof. Taking the source driver 212(3) for example, the source driver 212(3) can simultaneously transmit the image data and control signals to both the neighboring source driver 212(2) and 212(4), which are located at the two sides of the source driver 212(3). The source drivers 212(1), 212(2), 212(4)-212(7), 212(9) and 212(10) are set to the second operation mode to execute single-way transmission, and are not directly connected to the timing controller 225. That is, the source drivers 212(1), 212(2), 212(4)-212(7), 212(9) and 212(10) each can receive the image data and the control signals from the right (or left) source driver and transmit them to the left (or right) source driver. Taking the source driver 212(2) for example, it receives the image data and the control signals from the source driver 212(3) at the right side thereof and transmits them to the source driver 212(1) at the left side thereof. In the embodiment, the LCD 200 is a big screen monitor having 10 source drivers and two flexible printed circuit board 230 and 232. The number of flexible printed circuit boards is not limited to two as long as the distortions and delays of signals are acceptable.

**[0022]** In the embodiment, the source drivers are divided into a left group including source drivers 212(1)-212(5) and a right group including source drivers 212(6)-212(10). The flexible printed circuit board 230 connects to the center source drivers 212(3) of the left group, and the flexible printed circuit board 232 connects to the center source drivers 212(8) of the right group, such that the distortions and delays of signals, caused by the parasitic capacitance and resistance, can be minimized. On the other hand, the source drivers can also be divided into more than three groups and each group directly connects to the timing controller via a flexible printed circuit board, so long as the distortions and delays of the signals are acceptable.

**[0023]** FIG. 2B is a diagram of a COG LCD 250 according to another preferred embodiment of the invention. Compared with the LCD 200, the LCD 250 further includes a gate driver 216 at the right side of the panel 210. The gate drivers 214 and 216 together drive the panel 210 from two sides thereof. The other elements of LCD 250 are the same as those as described above.

**[0024]** FIG. 3 is a diagram of control signals of the source drivers and the gate drivers of the LCD. The control signals include gate control signals G and source control signals S. The gate control signals G include a gate driver start signal STV for representing the start of a frame, a gate clock signal CPV for enabling a gate line, and a gate driver output enable signal OEV for defining the enabled duration of the gate line. The source control signals S include a source driver start signal STH for notifying the source driver to start to prepare the data of a horizontal line, a data enable signal DE for starting to receive data, a load signal TP for starting to output driving voltages to the data lines, and a polarization control signal POL for controlling the polarization inversion.

**[0025]** When the source driver start signal STH is asserted, the source driver 212 starts to prepare to receive data, and after a period td1, the data enable signal DE is asserted such that the timing controller 225 starts to output the image data to the source drivers 212. The source drivers 212 generate the driving voltage with the polarization designated by the polarization control signal POL and then outputs the driving voltages to the panel 210 according to the load signal Tp.

**[0026]** In the conventional LCD 100, the control signals are outputted by the timing controller directly to each source driver 112 and the gate driver 114. Each control signal conventionally needs at least one wire to transmit, and thus a plurality of wires are required. The control signals are easily distorted and delayed because the wires between the timing controller and the source drivers and the gate driver have parasitic capacitance and resistance.

**[0027]** In the present embodiment, the timing controller 225 integrates the control signals into a control bitstream C and transmits it by a wire to the source drivers 212. For example, the control signals can be packed into a plurality of control packets, each representing an event relevant to a control signal. The timing controller 225 can designate one source driver 212 to receive the control packet by a target identification. The target identification is, for example, included in the control packet for each source driver to identify. After receiving the control packet, the source driver 212 can decode the control packet to generate the control signal. Therefore, the number of the wires required to transmit the control signals is thus greatly reduced in the present embodiment.

**[0028]** The source driver 212 has a built-in identification so as to identify whether a received control packet is for its own by comparing the target identification of the control packet with the built-in identification.

[Transmission protocol of the control bitstream]

**[0029]** Conventionally, the control signals are each

transmitted by a wire from the timing controller to the source driver/gate driver. The source drivers and the gate driver each needs a plurality of control signals and thus the number of the wires for transmitting the control signals is great. Therefore, number of wires in the conventional flexible printed circuit board is also great. The conventional structure thus requires a flexible printed circuit board of high-cost and quality. The lengths of the wires between the timing controller and the source drivers/gate driver are so long as to incur delays and distortions of the signals.

**[0030]** In the present embodiment, the timing controller 225 transmits the control bitstream C to the source driver a minimum of wires. The control bitstream C includes a plurality of control packets, each representing an event of one corresponding control signal, such as a pull high event or a pull low event. After receiving the control packet, the source driver 212 generates the corresponding control signal by pulling high or pulling low accordingly.

**[0031]** FIG. 4 is a format diagram of a control packet. A control packet includes a header field 310 and a control item, which includes a control field 312 and a data field 314. The header field 310 records a predetermined pattern for identifying the start of a packet, for example, 0x11111. The control field 312 records the type of the event, such as the STH event, the TP event, the pull high event, the pull low event and the initialization event. The data field 314 records the parameters of the event.

**[0032]** In the present embodiment, each control packet has 16 bits. If receiving the control packet by dual-edge sampling, it takes 8 clocks to read one control packet. That is, the control signal generated by a pull high event and a pull low event must remain at high level for at least a duration of 8 clocks. The control signals POL, CPV, STV, OEV can each be generated by a pull high event and a pull low event. The control signal that has a duration of less than 8 clocks, such as control signals STH and TP, are generated respectively by the STH event and the TP event. After receiving the STH event/TP event, the source driver pulls high the control signal STH/TP for a pre-determined period td2/tw1 and then pulls low the control signal STH/TP. It is worth noticing that the sampling method for receiving the control packet is not limited to dual-edge sampling. Rising-edge sampling or falling-edge sampling can also be used.

**[0033]** In regard to the control packet having the control field 312 recording the STH event, the data field 314 thereof records the target identification. For example, the source drivers 212(1)-212(10) have the built-in identifications of 0x0001-0x1010, respectively. After receiving the control packet with STH event, the source driver compares the target identification of this control packet with the built-in identification, pulls high the control signal STH if the comparison is matched, and then pulls low the control signal STH after a period td2.

**[0034]** From FIG. 3, it can be seen that the control signals TP and CPV are pulled high at the same time, so after receiving the control packet with TP event, control signals TP and CPV are pulled high. The control signal TP is then pulled low after a period tw1, and the control signal CPV is pulled low after receiving the control packet with pull low event of CPV.

**[0035]** Control signals POL, STV and OEV are generated by a pull high event and a pull low event. In regard to the control packet with the control field 312 recording a pull high event, its data field 314 designates which signal is to be pulled high. In regard to the control packet with the control field 312 recording a pull low event, its data field 314 designates which signal is to be pulled low.

**[0036]** In regard to the control packet with the control field 312 recording an initialization event, several kinds of initialization can be set, such as the fan out of the source drivers. Other kinds of events can also be represented by the control packets.

**[0037]** In the present embodiment, as a minimum of wires is required to transmit the control bitstream C, the number of wires connecting the timing controller and the source drivers are greatly reduced, the layout of the circuit is simplified, and stability is enhanced. In addition, the control bitstream C can integrate only a part of the control signals and leave other parts of the control signals to be transmitted respectively in independent wires. Although not all the control signals are integrated to the control bitstream, the number of wires can still be reduced.

[Source drivers]

**[0038]** FIG. 5A is a diagram of the source driver according to the preferred embodiment of the invention. The source driver 212 includes receivers 410, 412, transceivers 413, 415, a bus switch 422, wave generators 420, 421, and a driving unit 434. The transceiver 413 includes a control transceiver 414 and a data transceiver 424, and the transceiver 415 includes a control transceiver 416 and a data transceiver 426.

**[0039]** The bus switch 422 includes two switches SW1 and SW2. When the source driver, 212(3) or 212(8) in this embodiment, operates at a first operation mode, the bus switch turns off the switches SW1 and SW2 such that the control transceiver 414 and 416 are disconnected from each other and the data transceiver 424 and 426 are disconnected from each other. Thus, the control bitstream C1 and the image data D1 received by the receiver 410 are transmitted to the control transceiver 414 and the data transceiver 424, respectively, and the control bitstream C2 and the image data D2 received by the receiver 410 are transmitted to the control transceiver 416 and the data transceiver 426, respectively.

**[0040]** When the source driver, 212(1)-212(2), 212(4)-212(7), 212(9), or 212(10) in this embodiment, operates in a second operation mode, the receivers 410 and 412 are disabled, and the bus switch turns on the switches SW1 and SW2 such that the transceivers 413 and 415 are interconnected, that is, the data transceivers 424 and 426 are connected to each other and the control trans-

ceivers 414 and 416 are connected to each other. Thus, the source driver can transmit the control bitstream and the image data received to the next adjacent source driver in response to the designated transmission direction.

**[0041]** The wave generators 420 and 421 receive the control bitstream C1 and C2 respectively for generating source control signals S, such as STH(1), STH(2), POL(1), POL(2), TP(1) and TP(2), etc., and thus generating the gate control signals G, such as CPV(1), CPV(2), STV(1), STV(2), OEV(1), OEV(2) and etc. The control signals G are generated by one of the source drivers. In the LCD 200 in FIG. 2A, one of the source drivers 212, such as 212(1) that is nearest to the gate driver 214, generates the gate control signals G, while the other source drivers 212 do not. In the LCD 250 in FIG. 2B, two source drivers, such as 212(1) and 212(10) that are respectively nearest to the gate drivers 214 and 216, generate the gate control signals G respectively for the gate drivers 214 and 216, while others do not.

**[0042]** When receiving the signal STH, the driving unit 434 starts to latch image data D for converting to analog driving voltages in response to the signal POL, and then transmits the analog driving signals to the panel 210 after receiving the load signal TP.

**[0043]** In the first-operation-mode source driver, such as 212(3), the wave generators 420 and 421 are both activated to receive the control bitstreams C1 and C2, respectively, and generate the source control signals S and the gate control signals G, while the control bitstream C1 and C2 are independent, and image data D1 and D2 are independent. On the other hand, in the second-operation-mode source driver, such as 212(2) or 212(4), the control bitstream C1 is the control bitstream C2, and the image data D1 is the image data D2, so only one of the wave generators 420 and 421 is activated to generate the source control signals S and the gate control signals G. The other wave generator in the second-operation-mode source driver can be disabled, omitted or still activated to generate the source control signals S and the gate control signals G.

**[0044]** FIG. 5B is a block diagram of the wave generator in FIG. 5A. Each of the wave generators 420 and 421 includes a parser 451, an ID recognizer 453, a signal generator 460 and an initiator 470. The parser 451 receives the control bitstream C to parse the control item, including the control field 312 and a data field 314, of a control packet, and sends the parsed control item to the ID recognizer 453, the signal generator 460 or the initiator 470. The control item with the identity event, which is the STH event in this embodiment, is sent to the ID recognizer 453; the control item with the pull high event or the pull low event is set to the signal generator 460; the control item with the initialization event is sent to the initiator 470.

**[0045]** FIG. 5C is a block diagram of the ID recognizer in FIG. 5B. The recognizer 453 includes a comparator 456. Each source driver has a unique chip identity IDp. The chip identity IDp is set externally, for example by, respectively, pulling high or pulling low the pins of the source driver on the glass substrate. The comparator 456 triggers the signal STH when the comparison of the chip identity IDp with a target identity IDt extracted from the control packet is matched. The duration time td2 of the signal STH can be pre-determined in the comparator 456.

**[0046]** The signal generator 460 pulls high the corresponding signal after receiving the control item with the pull high event. The level of the pull-high signal is maintained until the signal generator 460 receives the corresponding control item with the pull low event. Taking generation of the control signal POL for example, FIG. 5D is a waveform diagram of control signal POL. When receiving the control item with the pull high event H, the signal generator 460 pulls high the signal PH; when receiving the control with the corresponding pull low event L, the signal generator 460 pulls low the signal PL. The coupling of the signal PH and the signal PL is the signal POL. The other control signals, such as CPV, STV, OEV, are also generated by the above-mentioned procedure.

**[0047]** The control signal is not suitable to be generated by the pull high event and the pull low event if the duration time of the high level of the control signal is less than 8 clocks, such as the control signal TP, since it takes 8 clocks for the wave generator to read a control packet. FIG. 5E is a waveform diagram of the generation of the control signal TP. When receiving the control item with the pull high event H of the control signal TP, the signal generator 460 pulls high the signal TH, then counts for a pre-determined period tw1, and then pulls low the signal TL. The coupling of the signal TH and the signal TL is the control signal TP.

**[0048]** The gate control signals G can also be generated according to the source control signals, such as STH or TP, as shown in FIG. 3. The signal CPV is generated according to the control signal STH. When the control signal STH of the source driver 212(1) is asserted, the counter thereof is activated, and the signal CPV is pulled high after a period td6, and, after a period tw4, the signal CPV is pulled low. The signal STV is generated according to the control signal STH. When the control signal STH of the source driver 212(1) is asserted, the signal STV is pulled high after a period td7 and then pulled low after a period tw5. The signal OEV is generated according to the control signal STH. When the control signal STH of the source driver 212(1) is asserted, the signal OEV is pulled high after a period td8 passed and pulled low after a period tw6 passed.

**[0049]** After receiving the control item with the initialization event, the initiator 470 outputs a DC value to set the corresponding parameter.

**[0050]** The source driver of the present embodiment can reduce the control signal decay because the source control signals are generated by the source driver itself, not by the timing controller in the conventional manner.

**[0051]** In addition, the present embodiment can reduce the number of wires from the timing controller to the gate driver because the source driver can generate the gate

control signals and directly send them to the gate driver via the wires on the glass substrate. The quality of the gate control signals are thus improved because the lengths of the transmission wires are reduced.

[Power Management]

**[0052]** FIG. 6A is a flowchart of a convergent transmission method for power saving. The source drivers 212(1)-212(5) in FIG. 2A are taken as an example. First, at step 610, the source drivers 212(1) and 212(5), which have the farthest distances away from the timing controller 225, receive the image data transmitted by the timing controller 225 via the source drivers. The power-saving mode is entered, which turns off the power for the data transceivers 424 and 426 of the source drivers 212(1) and 212(5), for example. Next, at step 612, the source drivers 212(2) and 212(4), which are the active ones having the farthest distances away from the timing controller 225, receive the image data and then enter the power-saving mode, which turns of the power for the data transceivers 424 and 426 of the source drivers 212(2) and 212(4), for example. Next, at step 614, the source driver 212(3) receives the image data from the timing controller 225 and then enters the power-saving mode. It is noted that, in the power-saving mode, the power for the control transceiver 416 and 414 of the source driver should not be turned off. Then, at step 616, each of the source drivers 212(1)-212(5) receives the load signal TP and then is activated to start to drive the panel 210. The transmission method can also apply to the source drivers 212(6)-212(10).

**[0053]** FIG. 6B is a flowchart of a divergent transmission method for power saving. The source drivers 212(1)-212(5) in FIG. 2A are taken as an example. First, the source drivers 212(1)-212(5) enter the power-saving mode. Next, at step 622, the source driver 212(3), which is nearest to the timing controller 225, is activated to receive the image data transmitted by the timing controller 225. Next, at step 624, the source drivers 212(2) and 212(4) are activated to receive the image data. Next, at step 626, the source drivers 212(1) and 212(5) are activated to receive the image data. The transmission method can also apply to the source drivers 212(6)-212(10).

**[0054]** In the power-saving mode, at least the power for data transceivers and the driving unit can be turned off. The data transceivers transmit the image data, which have large voltage swings and high frequency that make the power consumption great. Thus the power-saving convergent/divergent transmission methods can reduce unnecessary data transmission for saving power. The power for the control transceivers of the source driver should not be turned off, so that the source driver can still receive the control bitstream and operate responsively.

**[0055]** The convergent transmission method and the divergent transmission method can be applied at the same time. For example, the source drivers 212(1)-212(3) can use the convergent transmission method, while the source drivers 212(4)-212(5) use the divergent transmission method, or vice versa

**[0056]** While the invention has been described by way of example and in terms of a preferred embodiment, it is to be understood that the invention is not limited thereto. On the contrary, it is intended to cover various modifications and similar arrangements and procedures, and the scope of the appended claims therefore should be accorded the broadest interpretation so as to encompass all such modifications and similar arrangements and procedures.

## Claims

**1.** A liquid crystal display (200) comprising:

a panel (210) having an array of pixels;
a timing controller (225) for outputting image data and a source control signal;
a plurality of source drivers (212(1)-212(10)) connected in series, one of the source drivers configured to generate a gate control signal in response to the source control signal, a part of the source drivers which receive the image data and the source control signal directly from the timing controller being operated in a dual-way transmission mode for simultaneously transmitting signals to the neighboring source drivers at both sides thereof, while another part of the source drivers which are indirectly connected to the timing controller being operated in a single-way transmission mode for transmitting signals to the neighboring source driver at either one side thereof; and
at least one gate driver (214) for driving the panel pixels according to the gate control signal, wherein whether the source driver is operated in the dual-way transmission mode or the single-way transmission mode is related to connection of the source driver with the timing controller.

**2.** The LCD according to claim 1, wherein the source drivers and the gate driver are disposed on a glass substrate of the panel.

**3.** The LCD according to claim 1, wherein the source control signal is a source driver start signal (STH) or a load signal (TP).

**4.** The LCD according to claim 1, wherein the gate control signal comprises a gate clock signal (CPV), a gate driver start signal (STV) and a output enable signal (OEV).

**5.** The LCD according to claim 2, wherein the one source driver is the source driver nearest on the sub-

strate to the gate driver.

**6.** A method for generating a gate control signal of a liquid crystal display (200) having a panel (210), source drivers (212(1)-212(10)) connected in series and at least one gate driver (214), the method comprising the steps of:

providing image data and a source control signal from a timing controller (225) to the source drivers, a part of the source drivers which receive the image data and the source control signal directly from the timing controller being operated in a dual-way transmission mode for simultaneously transmitting signals to the neighboring source drivers at both sides thereof, while another part of the source drivers which are indirectly connected to the timing controller being operated in a single-way transmission mode for transmitting signals to the neighboring source driver at either one side thereof;
selecting one of the source drivers;
generating at the selected source driver a gate control signal;
applying the gate signal to the gate driver in response to receipt of the source control signal;
wherein the panel is driven by the gate driver and the source drivers; and
whether the source driver is operated in the dual-way transmission mode or the single-way transmission mode is related to connection of the source driver with the timing controller.

**7.** The method according to claim 6, wherein step for generating the gate control signal comprises:

setting a predetermined value;
upon receiving the source control signal, starting a count and asserting the gate control signal;
maintaining assertion of the gate control signal until the count attains the predetermined value; and
de-asserting the gate control signal after the count has attained the predetermined value.

**8.** The method according to claim 6, wherein the source control signal is a source driver start signal (STH) or a load signal (TP).

**9.** The method according to claim 6, wherein the gate control signal comprises a gate clock signal (CPV), a gate driver start signal (STV) and a output enable signal (OEV).

**10.** The method according claim 6, wherein the selected source driver is nearest to the gate driver on the panel.

**Patentansprüche**

**1.** Flüssigkristallanzeige (200) aufweisend:

ein Anzeigefeld (210), das eine Anordnung von Bildpunkten aufweist;
eine Zeitablaufsteuerung (225) zum Ausgeben von Bilddaten und eines Source-Steuersignals;
eine Mehrzahl von Source-Treibern (212(1)-212(10)), die in Serie verbunden sind, wobei einer der Source-Treiber eingerichtet ist, ein Gate-Steuersignal als Reaktion auf das Source-Steuersignal zu generieren, wobei ein Teil der Source-Treiber, welche die Bilddaten und das Source-Steuersignal direkt von der Zeitablaufsteuerung empfangen, in einer Zweiweg-Übertragungsbetriebsart für ein simultanes Übertragen von Signalen an die zu einem Source-Treiber benachbarten Source-Treiber auf dessen beiden Seiten davon betrieben wird, während ein anderer Teil der Source-Treiber, welche indirekt mit der Zeitablaufsteuerung verbunden sind, in einer Einweg-Übertragungsbetriebsart für ein Übertragen von Signalen an den zu einem Source-Treiber benachbarten Source-Treiber auf einer beliebigen von dessen Seiten betrieben wird; und
mindestens einen Gate-Treiber (214) für ein Treiben der Anzeigefeldbildpunkte gemäß dem Gate-Steuersignal, wobei, ob der Source-Treiber in der Zweiweg-Übertragungsbetriebsart oder in der Einweg-Übertragungsbetriebsart betrieben wird, von einer Verbindung des Source-Treibers mit der Zeitablaufsteuerung abhängt.

**2.** LCD gemäß Anspruch 1, wobei die Source-Treiber und der Gate-Treiber auf einem Glassubstrat des Anzeigefelds angeordnet sind.

**3.** LCD gemäß Anspruch 1, wobei das Source-Steuersignal ein Source-Treiber-Startsignal (STH) oder ein Ladesignal (TP) ist.

**4.** LCD gemäß Anspruch 1, wobei das Gate-Steuersignal ein Gate-Taktsignal (CPV), ein Gate-Treiber-Startsignal (STV) und ein Ausgabefreigabesignal (OEV) aufweist.

**5.** LCD gemäß Anspruch 2, wobei der eine Source-Treiber der Source-Treiber ist, der dem Gate-Treiber auf dem Substrat am nächsten liegt.

**6.** Verfahren für ein Generieren eines Gate-Steuersignals einer Flüssigkristallanzeige (200), die ein Anzeigefeld (210), in Serie verbundene Source-Treiber (212(1)-212(10)) und mindestens einen Gate-Treiber (214) aufweist, wobei das Verfahren die Schritte aufweist:

Bereitstellen von Bilddaten und eines Source-Steuersignals von einer Zeitablaufsteuerung (225) an die Source-Treiber, wobei ein Teil der Source-Treiber, welche die Bilddaten und das Source-Steuersignal direkt von der Zeitablaufsteuerung empfangen, in einer Zweiweg-Übertragungsbetriebsart für ein simultanes Übertragen von Signalen an die zu einem Source-Treiber benachbarten Source-Treiber auf dessen beiden Seiten betrieben wird, während ein anderer Teil der Source-Treiber, welche indirekt mit der Zeitablaufsteuerung verbunden sind, in einer Einweg-Übertragungsbetriebsart für ein Übertragen von Signalen an den zu einem Source-Treiber benachbarten Source-Treiber auf einer beliebigen von dessen Seiten betrieben wird;
Auswählen eines der Source-Treiber;
Generieren eines Gate-Steuersignals an dem ausgewählten Source-Treiber;
Anlegen des Gate-Signals an den Gate-Treiber als Reaktion auf einen Empfang des Source-Steuersignals;
wobei das Anzeigefeld durch den Gate-Treiber und die Source-Treiber gesteuert wird; und
ob der Source-Treiber in der Zweiweg-Übertragungsbetriebsart oder in der Einweg-Übertragungsbetriebsart betrieben wird, von einer Verbindung des Source-Treibers mit der Zeitablaufsteuerung abhängt.

**7.** Verfahren gemäß Anspruch 6, wobei der Schritt für ein Generieren des Gate-Steuersignals aufweist:

Einstellen eines vorbestimmten Werts;
Starten eines Zählers und Aktivieren des Gate-Steuersignals bei Empfangen des Source-Steuersignals;
Beibehalten der Aktivierung des Gate-Steuersignals bis der Zähler den vorbestimmten Wert erreicht; und
Deaktivieren des Gate-Steuersignals, nachdem der Zähler den vorbestimmten Wert erreicht hat.

**8.** Verfahren gemäß Anspruch 6, wobei das Source-Steuersignal ein Source-Treiber-Startsignal (STH) oder ein Ladesignal (TP) ist.

**9.** Verfahren gemäß Anspruch 6, wobei das Gate-Steuersignal ein Gate-Taktsignal (CPV), ein Gate-Treiber-Startsignal (STV) und ein Ausgabefreigabesignal (OEV) aufweist.

**10.** Verfahren gemäß Anspruch 6, wobei der ausgewählte Source-Treiber dem Gate-Treiber auf dem Anzeigefeld am nächsten liegt.

**Revendications**

**1.** Dispositif d'affichage à cristaux liquides (200) comprenant :

un panneau (210) ayant un réseau de pixels ;
un dispositif de commande de minutage (225) pour délivrer en sortie des données d'image et un signal de commande de source ;
une pluralité de pilotes de source (212(1)-212(10)) reliés en série, l'un des pilotes de source étant configuré pour générer un signal de commande de grille en réponse au signal de commande de source, une partie des pilotes de source qui reçoivent les données d'image et le signal de commande de source directement à partir du dispositif de commande de minutage étant actionnée dans un mode de transmission à double sens pour transmettre simultanément des signaux aux pilotes de source voisins sur les deux côtés de ceux-ci, tandis qu'une autre partie des pilotes de source qui sont indirectement reliés au dispositif de commande de minutage est actionnée dans un mode de transmission à sens unique pour transmettre des signaux au pilote de source voisin sur l'un des côtés de celui-ci ; et
au moins un pilote de grille (214) pour piloter les pixels de panneau selon le signal de commande de grille, où le fait que le pilote de source soit actionné dans le mode de transmission à double sens ou le mode de transmission à sens unique est lié à la liaison du pilote de source avec le dispositif de commande de minutage.

**2.** LCD selon la revendication 1, dans lequel les pilotes de source et le pilote de grille sont disposés sur un substrat en verre du panneau.

**3.** LCD selon la revendication 1, dans lequel le signal de commande de source est un signal de démarrage de pilote de source (STH) ou un signal de charge (TP).

**4.** LCD selon la revendication 1, dans lequel le signal de commande de grille comprend un signal d'horloge de grille (CPV), un signal de démarrage de pilote de grille (STV) et un signal de validation de sortie (OEV).

**5.** LCD selon la revendication 2, dans lequel le pilote de source est le pilote de source le plus proche sur le substrat du pilote de grille.

**6.** Procédé pour générer un signal de commande de grille d'un dispositif d'affichage à cristaux liquides (200) ayant un panneau (210), des pilotes de source (212(1)-212(10)) reliés en série et au moins un pilote de grille (214), le procédé comprenant les étapes qui

consistent :

à fournir des données d'image et un signal de commande de source à partir d'un dispositif de commande de minutage (225) aux pilotes de source, une partie des pilotes de source qui reçoivent les données d'image et le signal de commande de source directement à partir du dispositif de commande de minutage étant actionnée dans un mode de transmission à double sens pour transmettre simultanément des signaux aux pilotes de source voisins sur les deux côtés de ceux-ci, tandis qu'une autre partie des pilotes de source qui sont indirectement reliés au dispositif de commande de minutage est actionnée dans un mode de transmission à sens unique pour transmettre des signaux au pilote de source voisin sur l'un des côtés de celui-ci ;
à sélectionner l'un des pilotes de source ;
à générer au niveau du pilote de source sélectionné un signal de commande de grille ;
à appliquer le signal de grille au pilote de grille en réponse à la réception du signal de commande de source ;
où le panneau est piloté par le pilote de grille et les pilotes de source ; et
le fait que le pilote de source soit actionné dans le mode de transmission à double sens ou le mode de transmission à sens unique est lié à la liaison du pilote de source avec le dispositif de commande de minutage.

**7.** Procédé selon la revendication 6, dans lequel l'étape pour générer le signal de commande de grille comprend :

la fixation d'une valeur prédéterminée ;
le démarrage d'un comptage et l'assertion du signal de commande de grille, lors de la réception du signal de commande de source ;
le maintien d'assertion du signal de commande de grille jusqu'à ce que le comptage atteigne la valeur prédéterminée ; et
la non assertion du signal de commande de grille après que le comptage a atteint la valeur prédéterminée.

**8.** Procédé selon la revendication 6, dans lequel le signal de commande de source est un signal de démarrage de pilote de source (STH) ou un signal de charge (TP).

**9.** Procédé selon la revendication 6, dans lequel le signal de commande de grille comprend un signal d'horloge de grille (CPV), un signal de démarrage de pilote de grille (STV) et un signal de validation de sortie (OEV).

**10.** Procédé selon la revendication 6, dans lequel le pilote de source sélectionné est le plus proche du pilote de grille sur le panneau.

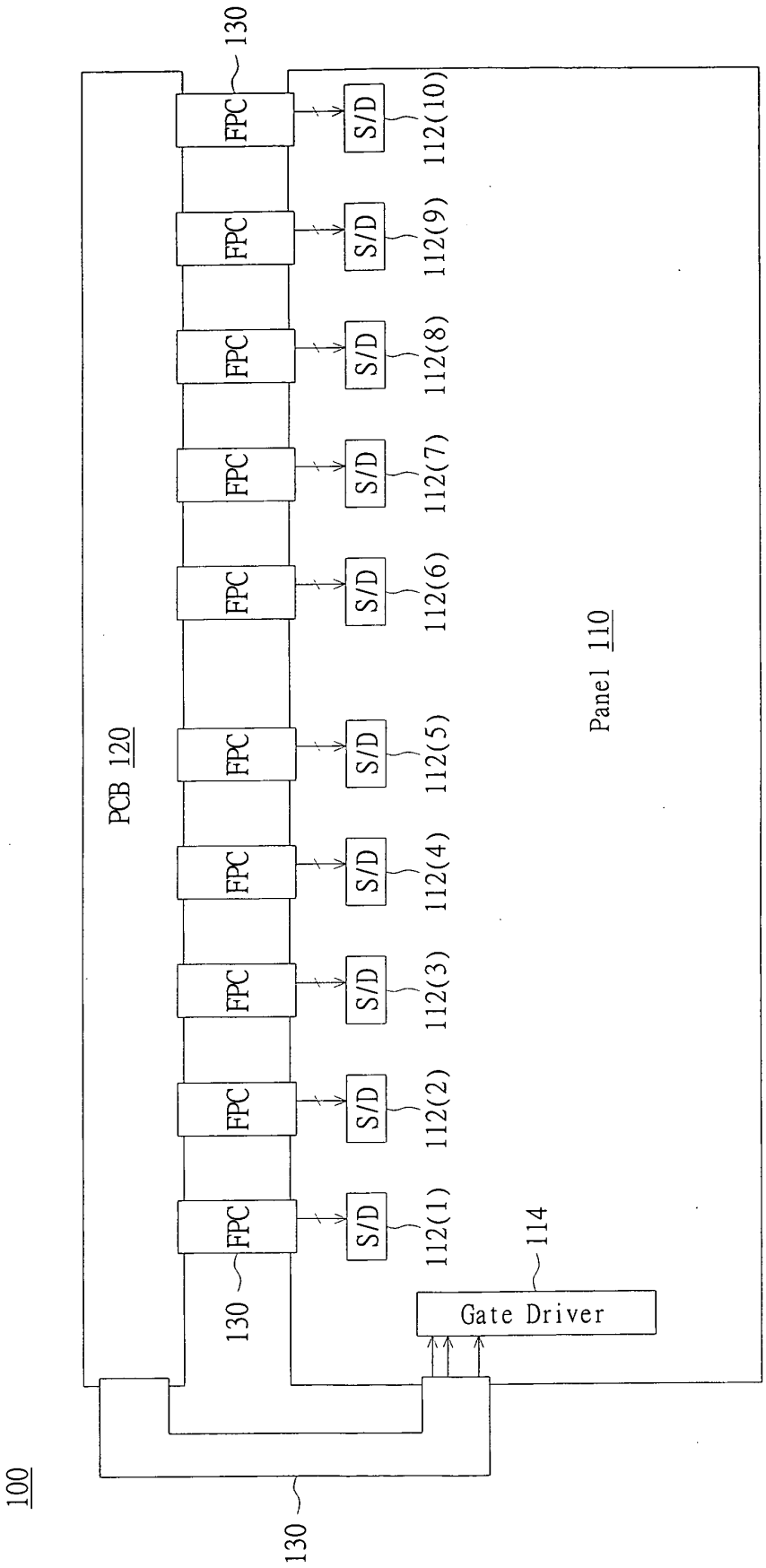



FIG. 1(PRIOR ART)

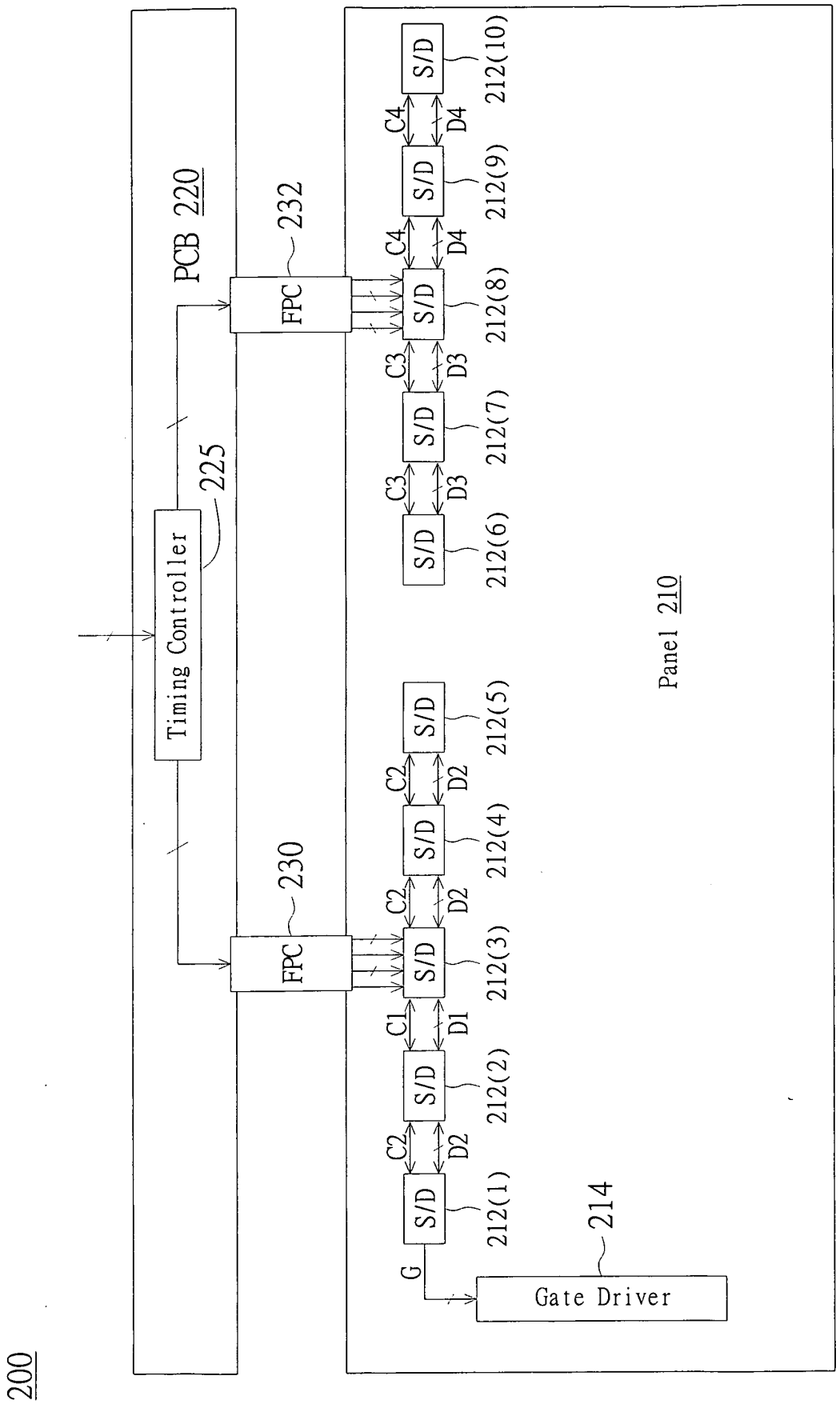

200
PCB 220
Timing Controller
225
FPC
230
FPC
232
Panel 210
S/D
212(1)
212(2)
212(3)
212(4)
212(5)
212(6)
212(7)
212(8)
212(9)
212(10)
C1
C2
C3
C4
D1
D2
D3
D4
G
214
Gate Driver

FIG. 2A

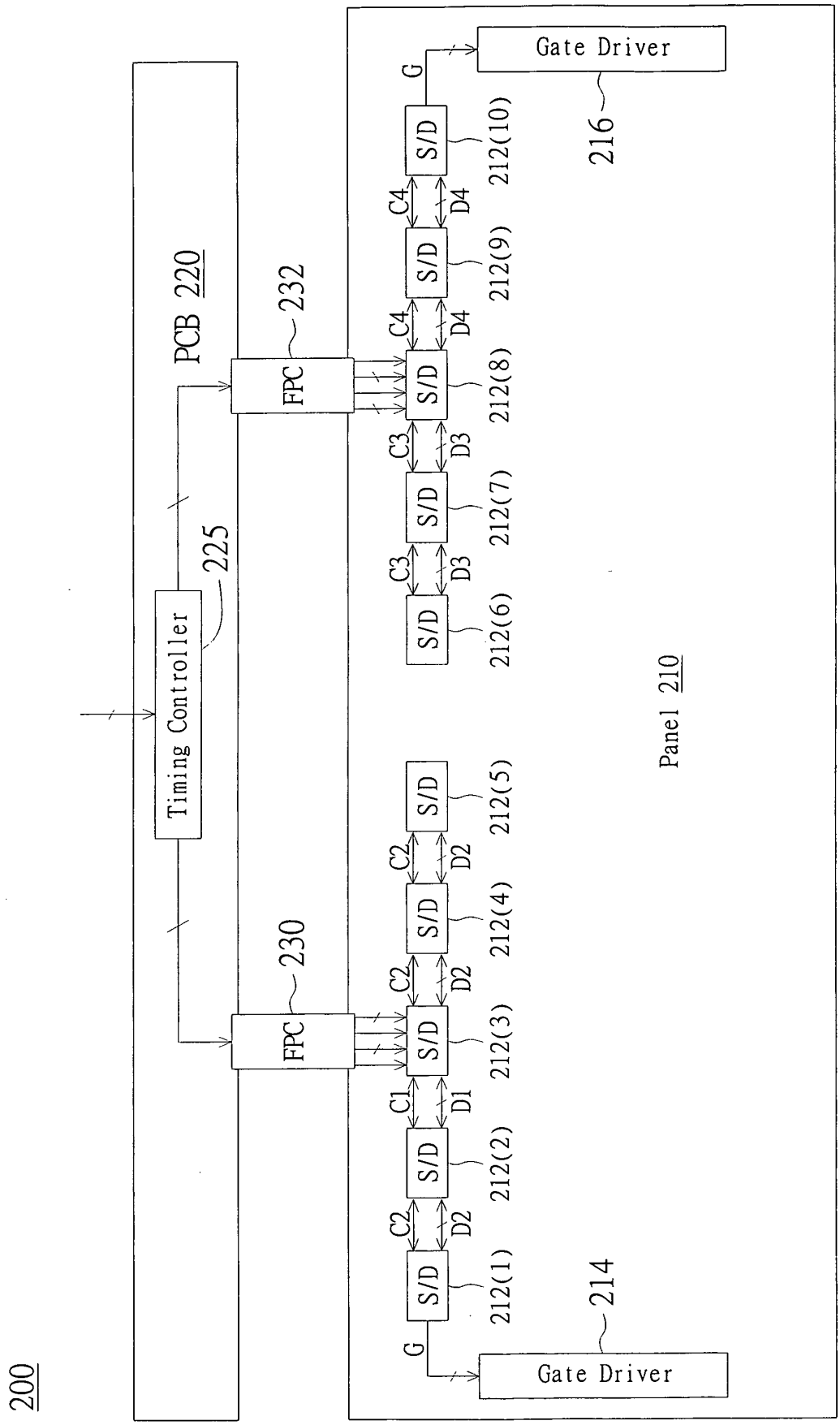

200
PCB 220
Timing Controller
225
FPC
230
FPC
232
Gate Driver
216
Gate Driver
214
Panel 210
S/D
212(1)
212(2)
212(3)
212(4)
212(5)
212(6)
212(7)
212(8)
212(9)
212(10)
G
C1
C2
C3
C4
D1
D2
D3
D4

FIG. 2B

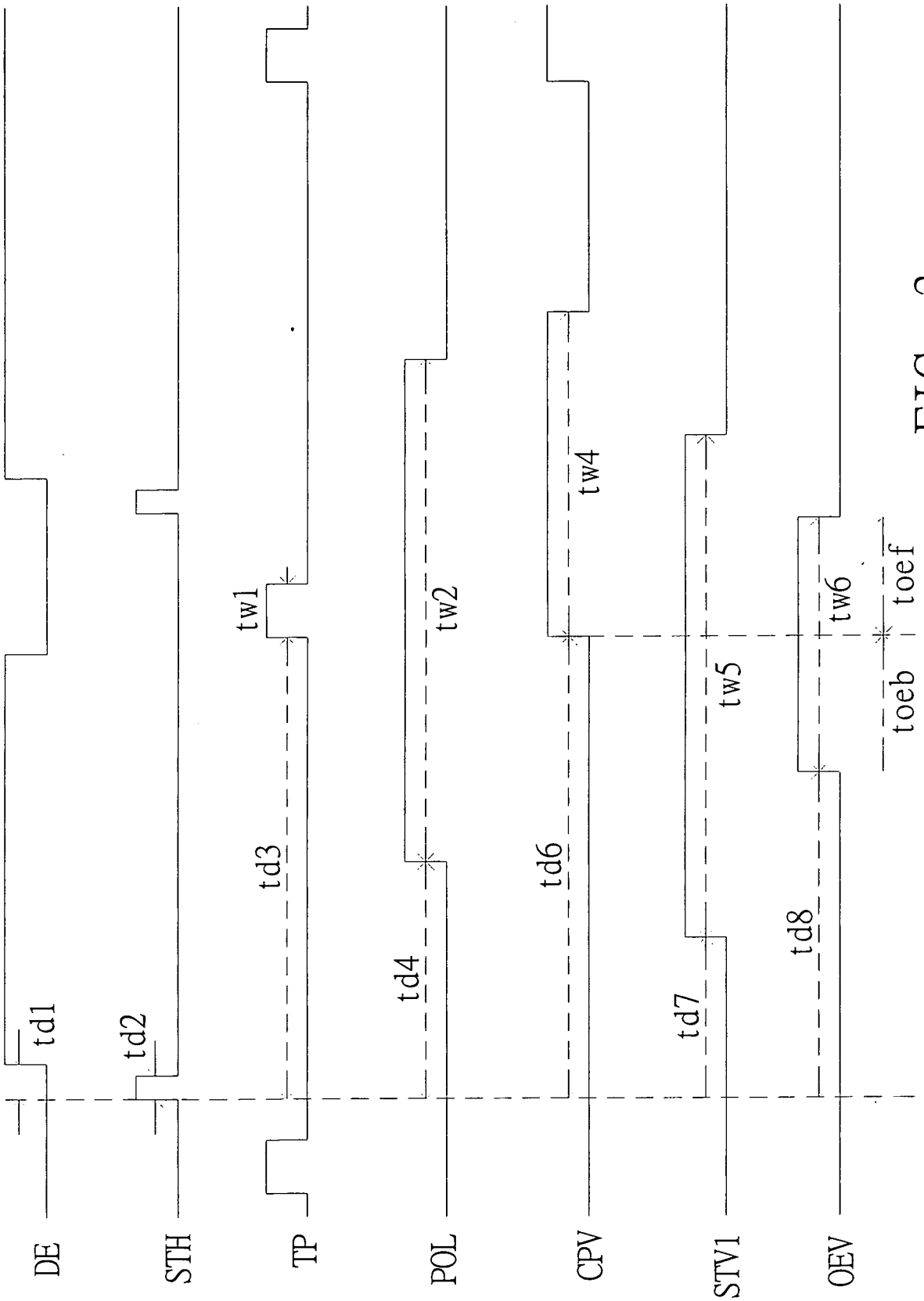

DE
STH
TP
POL
CPV
STV1
OEV
td1
td2
td3
td4
td6
td7
td8
tw1
tw2
tw4
tw5
tw6
toeb
toef

FIG. 3

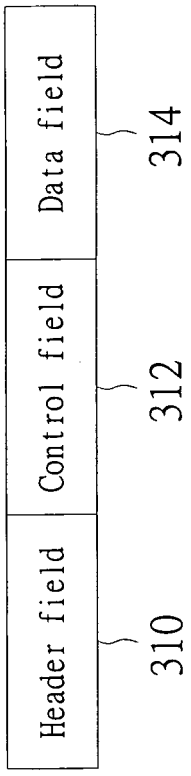



FIG. 4

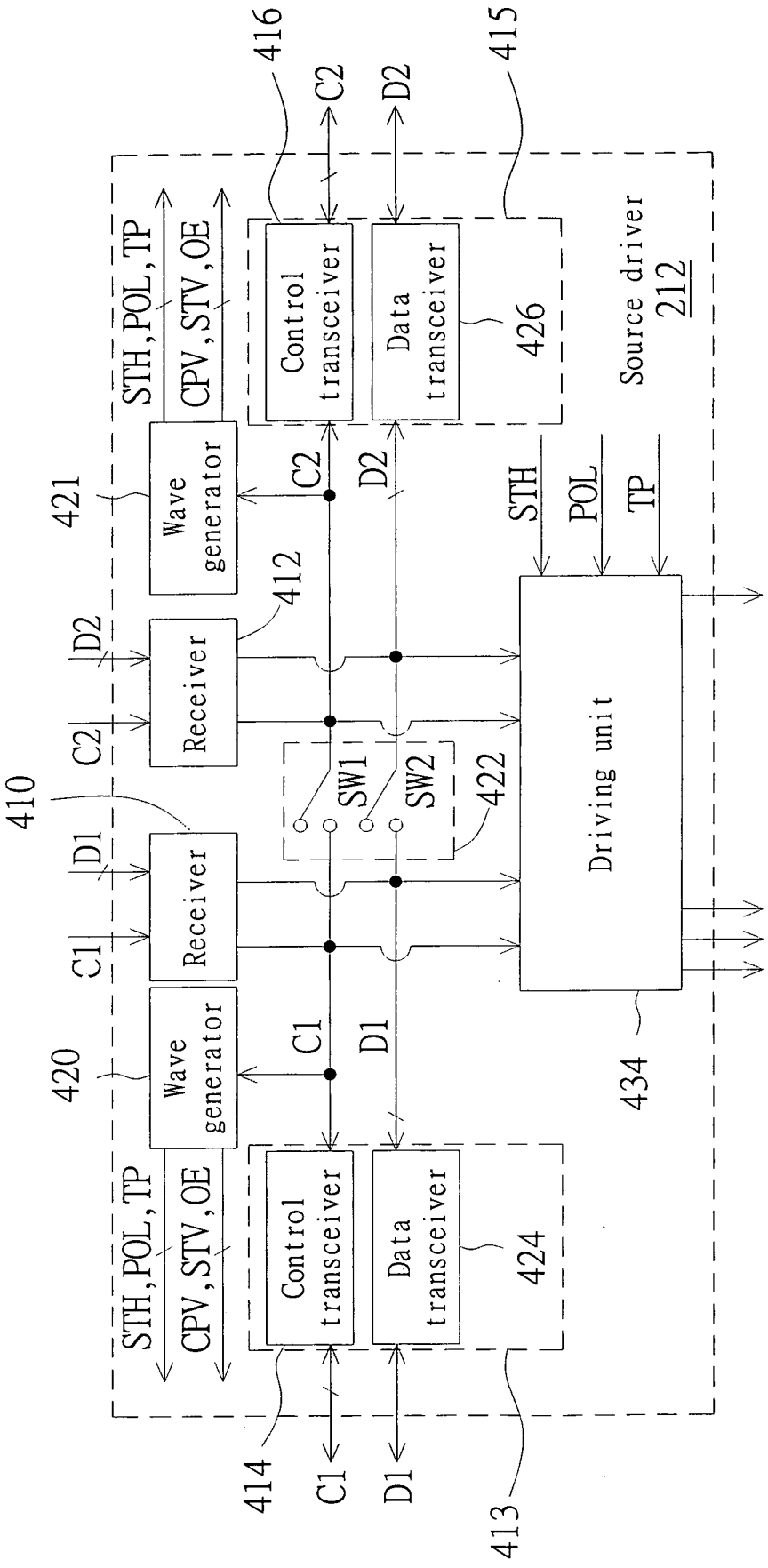

Source driver
212
Control transceiver
Data transceiver
426
424
Wave generator
Receiver
Receiver
Wave generator
Driving unit
SW1
SW2
422
410
412
421
420
434
415
416
414
413
STH, POL, TP
CPV, STV, OE
STH, POL, TP
CPV, STV, OE
C2
D2
C1
D1
STH
POL
TP

FIG. 5A

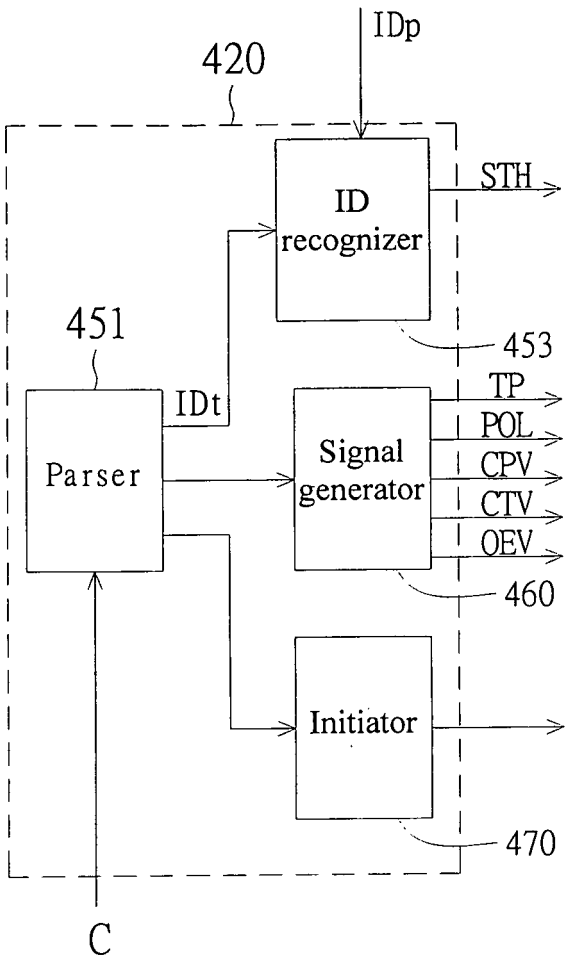

IDp
420
ID
recognizer
STH
451
453
IDt
TP
POL
CPV
CTV
OEV
Parser
Signal
generator
460
Initiator
470
C

FIG. 5B

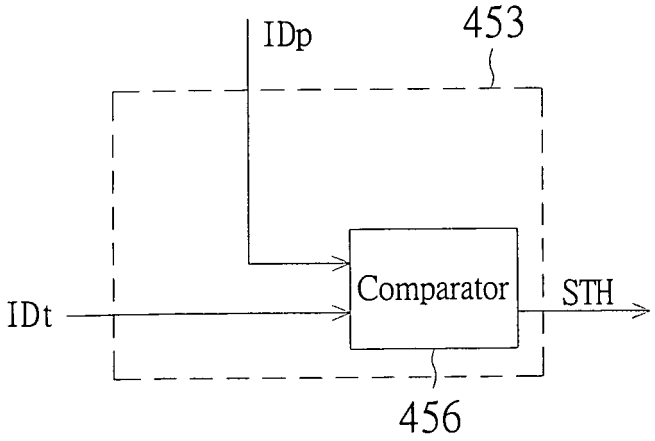

IDp
453
Comparator
IDt
STH
456

FIG. 5C

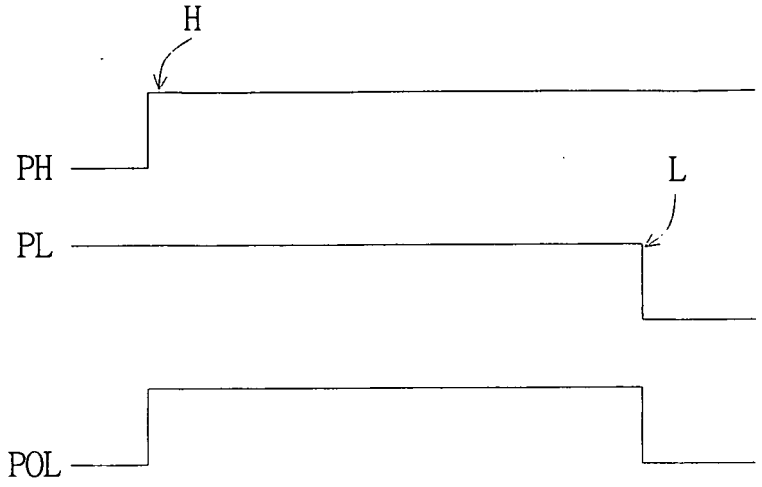



FIG. 5D

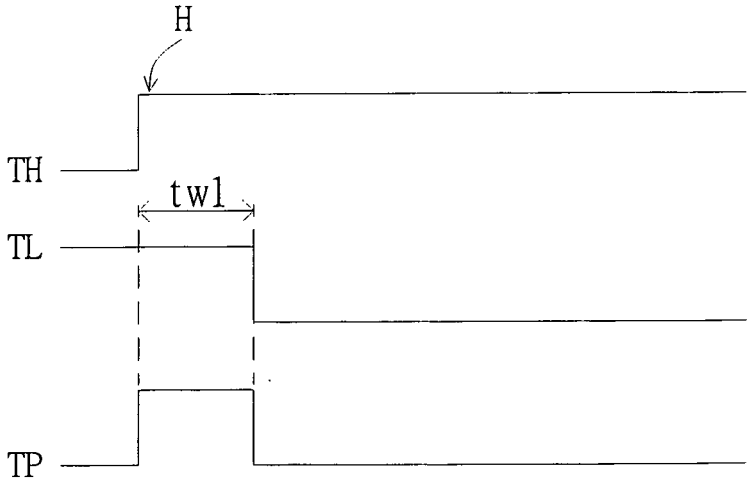



FIG. 5E

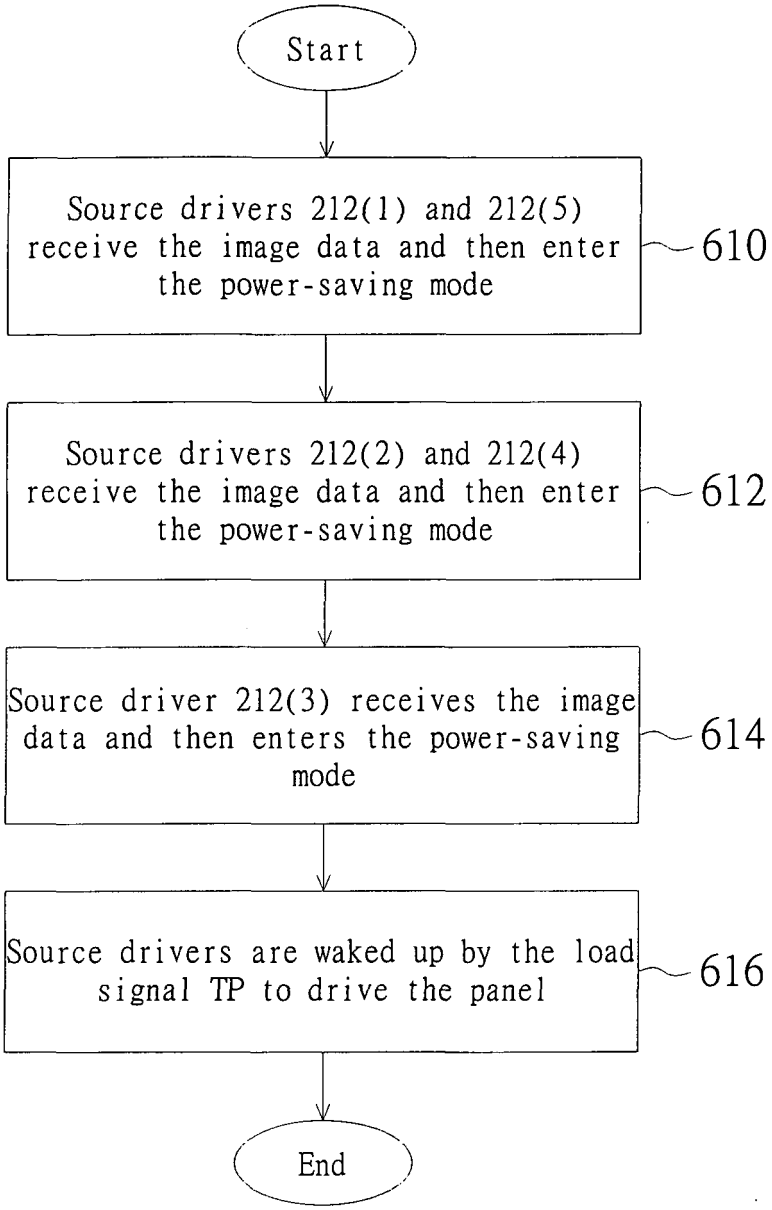

Start
Source drivers 212(1) and 212(5) receive the image data and then enter the power-saving mode
610
Source drivers 212(2) and 212(4) receive the image data and then enter the power-saving mode
612
Source driver 212(3) receives the image data and then enters the power-saving mode
614
Source drivers are waked up by the load signal TP to drive the panel
616
End

FIG. 6A

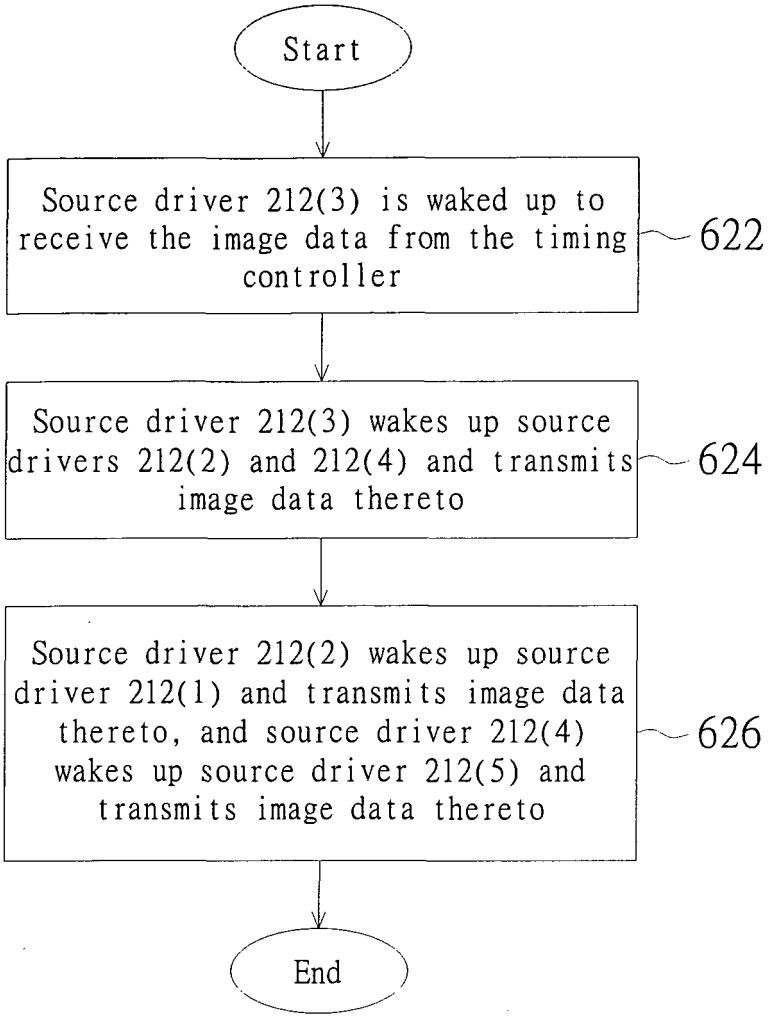

Start
Source driver 212(3) is waked up to receive the image data from the timing controller
622
Source driver 212(3) wakes up source drivers 212(2) and 212(4) and transmits image data thereto
624
Source driver 212(2) wakes up source driver 212(1) and transmits image data thereto, and source driver 212(4) wakes up source driver 212(5) and transmits image data thereto
626
End

FIG. 6B

## REFERENCES CITED IN THE DESCRIPTION

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