(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 1 750 205 B1

(12) **EUROPEAN PATENT SPECIFICATION**

(45) Date of publication and mention of the grant of the patent:
11.06.2008 Bulletin 2008/24

(51) Int Cl.:
G06F 13/42 *(2006.01)*

(21) Application number: **06251866.7**

(22) Date of filing: **03.04.2006**

(54) **Flexible width data protocol**

Datenprotokoll mit flexibler Breite

Protocole pour largeur de données sélectif

(84) Designated Contracting States:
DE GB

(30) Priority: **11.07.2005 US 698149 P**
13.03.2006 US 374663

(43) Date of publication of application:
07.02.2007 Bulletin 2007/06

(73) Proprietor: **VIA Technologies, Inc.**
Hsin-Tien City
Taipei Hsien 231 (TW)

(72) Inventor: **Gaskins, Darius D.**
Austin, Texas 78750 (US)

(74) Representative: **O'Connell, David Christopher**
HASELTINE LAKE,
Redcliff Quay
120 Redcliff Street
Bristol BS1 6HU (GB)

(56) References cited:
WO-A-01/48621 **US-A1- 2003 088 799**

EP 1 750 205 B1

Printed by Jouve, 75001 PARIS (FR)

Description

FIELD OF THE INVENTION

[0001] The present invention relates to processor data buses, and more particularly to a flexible width data protocol which solves the problem of large package and unreasonable power requirements for a present day microprocessor where a significant amount of pins and power are devoted to the data bus interface of the microprocessor.

DESCRIPTION OF THE RELATED ART

[0002] In a present day microprocessor, such as an x86-compatible microprocessor, transactions (i.e., read and write transactions) to/from memory are accomplished over a system bus. These transactions include a request phase and a data (i.e., response) phase. During the request phase, an address for a transaction along with the transaction type are provided over an address signal group. The address signal group typically includes an address bus, a set of corresponding address strobe signals, and a request bus. During the data phase, data corresponding to the transaction is transferred over a data signal group. The data signal group typically includes a data bus, a set of corresponding data strobe signals, a response bus (indicating the type of response), and bus control signals. In one particular conventional configuration, the data signal group includes about 72 or so signals which must be provided on pins of a package for the microprocessor die. Many conventional configurations support "quad-pumped" transactions in which an entire cache line (e.g., eight quadwords for a 64-byte cache line) is transferred across the bus in just a few cycles (e.g., two clock cycles) of a bus or system clock. During the quad-pumped transactions for the conventional microprocessor, most of the signals of the data signal group are asserted multiple times during each clock cycle, consuming a considerable amount of power.

[0003] The present inventor has noted that the conventional data signal group configuration is problematic in certain application areas where package size and/or power are constrained. It is therefore desirable to provide a mechanism whereby the number of data signal group pins and commensurate power requirements are reduced, but where the data transfer functionality is retained. Furthermore, to accommodate varying application areas, it is desirable to provide a mechanism whereby a data transferring capability can be configured in either a full-width data bus mode as described above or in a new half-width data bus mode, as will be described herein.

[0004] WO 01/48621 discloses a microprocessor that is capable of full-width transactions that are quad-pumped, double pumped or that use the common clock signalling mode.

[0005] US 2003/0088799 discloses regulating power consumption and component temperature with regard to communication between only two interconnected devices.

SUMMARY OF THE INVENTION

[0006] Aspects of the present invention may be found in the appendent independent claims 1 and 6, to which reference should now be made. Embodiments of the present invention may be found in the appendent dependent claims.

BRIEF DESCRIPTION OF THE DRAWINGS

[0007] The benefits, features, and advantages of the present invention will become better understood with regard to the following description, and accompanying drawings where:

[0008] FIG. 1 is a simplified block diagram of a conventional microprocessor interface system;

[0009] FIG. 2 is a timing diagram showing the interaction of the signals within the data signal group described with reference to the conventional microprocessor interface system of FIG. 1 for performing the data phase of a bus transaction;

[0010] FIG. 3 is a timing diagram illustrating a data phase of a half-width quad-pumped transaction using a half-width data bus implemented according to an embodiment of the present invention;

[0011] FIG. 4 is a diagram of a table illustrating how the data bus signals of a half-width quad-pumped data bus according to an embodiment of the present invention are mapped during a data phase to data bytes within a 64-byte cache line;

[0012] FIG. 5 is a simplified block diagram of a microprocessor interface system including a system bus with data signal group signals for a half-width quad-pumped data bus according to an embodiment of the present invention; and

[0013] FIG. 6 is a block diagram of data bus configuration logic which may be used to implement the data bus configuration logic of FIG. 5 according to an exemplary embodiment of the present invention.

DETAILED DESCRIPTION

[0014] The following description is presented to enable one of ordinary skill in the art to make and use the present invention as provided within the context of a particular application and its requirements. Various modifications to the preferred embodiment will, however, be apparent to one skilled in the art, and the general principles defined herein may be applied to other embodiments. Therefore, the present invention is not intended to be limited to the particular embodiments shown and described herein, but is to be accorded the widest scope consistent with the principles and novel features herein disclosed.

[0015] The present inventor has noted that the con-

ventional data signal group configuration is problematic in certain application areas where package size and/or power are constrained. He has therefore developed a flexible width data protocol which solves the problem of large package and unreasonable power requirements for a present day microprocessor where a significant amount of pins and power are devoted to the microprocessor's data bus interface, as will be further described below with respect to FIGS 1-6.

[0016] FIG. 1 is a simplified block diagram of a conventional microprocessor interface system 100. The microprocessor interface system 100 includes a microprocessor 101 and a bus agent 103 interfaced with a system bus 105. The bus agent 103 represents any number of different types of bus agents as known to those skilled in the art, such as a memory controller, a host/PCI (Peripheral Component Interconnect) bridge, chipset, etc. The system bus 105 includes the signals for performing data transactions, including a bidirectional address bus A, a bidirectional data bus DATA, and multiple control signals. In the illustrated embodiment, the A bus has 33 signals shown as A[35:3] and the DATA bus has 64 signals shown as DATA[63:0], although it is understood that the address and data buses may have any suitable number of signals depending upon the particular configuration and architecture. One skilled in the art will appreciate that the least significant address signals (A[2:0]) are not required to allow for transfer of data with quadword granularity, which is the present state of the art.

[0017] The control signals include a differential clock bus BCLK[1:0], a bidirectional address strobe bus ADSTB[1:0] (indicating validity of the addresses on the A bus), a bidirectional request bus REQ[4:0] specifying the type of transaction requested (e.g., memory code read, memory data read, memory line write, memory quadword write with byte enables), a pair of data strobe buses DSTBP[3:0] and DSTBN[3:0], a bidirectional data bus busy signal DBSY (asserted by the entity that is providing data on the DATA bus), a data ready signal DRDY (asserted by either the device providing data during all clock cycles that data is transferred over the DATA bus), and a response bus RS[2:0] which provides the type of transaction response (e.g., no data, normal data, implicit writeback) that is being completed over the DATA bus. In the illustrated embodiment, the RS bus has 3 signals shown as RS[2:0] and is asserted by the bus agent 103.

[0018] The signals shown for the conventional microprocessor interface system 100 are provided in virtually all present day microprocessors with minor variation. Some processors multiplex addresses and data over the same signal group and thus provide control signals to indicate whether data or addresses are present. Other microprocessors utilize different address or data bus widths or control signals alternatively named. Still further, addresses and/or data may be multiplexed over a smaller bus size than those illustrated by the conventional microprocessor interface system 100. What is important to note is that substantially all processors provide signals for communication with bus agents to indicate what type of transaction is requested, the parameters of that transaction, and to transmit/receive the data.

[0019] In a present day microprocessor, including the microprocessor 101, data can be transferred on a cache line basis (e.g., eight quadwords for a 64-byte cache line) according to a "quad-pumped" configuration. When transferring an entire cache line, two cycles of the bus clock signals BCLK[1:0] are used to transfer the eight associated quadwords in a cache line. Accordingly, four quadwords are transferred during each cycle of the bus clock BCLK[1:0], thus accounting for the descriptor "quad-pumped." During this type of data transfer, the signals of the data strobe buses DSTBP[3:0], DSTBN[3:0] are provided to indicate the validity of various quadword beats on the data bus so that 4 beats are transferred during a single bus clock (each "beat" including the 64 bits of the DATA bus).

[0020] FIG. 2 is a timing diagram showing the interaction of the signals within the data signal group described with reference to the conventional microprocessor interface system 100 for performing the data phase of a bus transaction. Operation of such transactions and corresponding signals as named herein in an x86-compatible microprocessor are described in numerous references, one of which is the book "The Unabridged Pentium® 4 IA32 Processor Genealogy, 1st Edition," by Tom Shanley. For clarity, assertion of the control signals is shown as a logic low level, although one skilled in the art will appreciate that assertion can as well be indicated by a logic high level. Cycles of the differential bus clock BCLK[1:0] are shown across the top of the timing diagram, in which BCLK[1] is shown using a dashed line and which toggles with opposite polarity as the BCLK[0] signal.

[0021] As noted above, the current state of the art provides for a 64-bit data bus DATA[63:0] that supports transfer during the data phase of a 64-byte cache line over two cycles of the bus clock BCLK[1:0]. The transfer of eight bytes over the 64-bit data bus is known as a beat and 4 beats 1-4, 5-8 are transferred during each cycle of the bus clock BCLK[1:0]. In an x86-compatible configuration, the data bus signal group is divided into four subgroups. Subgroup 0 includes DATA[15:0], DSTBP0, and DSTBN0; subgroup 1 includes DATA[31:16], DSTBP1, and DSTBN1; subgroup 2 includes DATA[47:32], DSTBP2, and DSTBN2; and subgroup 3 includes DATA [63:48], DSTBP3, and DSTBN3. The falling edges of DSTBP0 are used to indicate validity of words 1, 3, 5, and 7 on DATA[15:0], and the falling edges of DSTBN0 are used to indicate validity of words 2, 4, 6, and 8 on DATA[15:0]. The falling edges of DSTBP1 are used to indicate validity of words 1, 3, 5, and 7 on DATA[31:16], and the falling edges of DSTBN1 are used to indicate validity of words 2, 4, 6, and 8 on DATA[31:16]. The falling edges of DSTBP2 are used to indicate validity of words 1, 3, 5, and 7 on DATA[47:32], and the falling edges of DSTBN2 are used to indicate validity of words 2, 4, 6,

and 8 on DATA[47:32]. The falling edges of DSTBP3 are used to indicate validity of words 1, 3, 5, and 7 on DATA [63:48], and the falling edges of DSTBN3 are used to indicate validity of words 2, 4, 6, and 8 on DATA[63:48].

[0022] The data signal group configuration used by the conventional microprocessor interface system 100 described above is problematic in certain application areas where package size and/or power is constrained. More particularly, the data signal group including signals DATA [63:0], DSTBP[3:0], and DSTBN[3:0] of the conventional microprocessor interface system 100 includes 72 signals which must be provided on pins of a package for the microprocessor die. Furthermore, every time one of these signals is driven to the system 105 bus, power is consumed. It is therefore desirable to provide a mechanism whereby the number of data signal group pins and commensurate power requirements are reduced, but where the data transfer functionality is retained. Furthermore, to accommodate varying application areas, it is desirable to provide a mechanism whereby a data transferring capability can be configured in either a full-width data bus mode as described above or in a new half width data bus mode, as will be described below.

[0023] The present invention provides for a new type of data signal group, which includes a half-width quad-pumped data bus, and which requires roughly half (e.g., 36) of the data signal group signals described above with reference to a full-width quad-pumped data bus, and which requires roughly half of the power of a the full-width data bus. In one embodiment, the microprocessor and one or more bus agents may be implemented with a reduced number of data signal group pins to reduce package size and to reduce power consumption. In another embodiment, the microprocessor and one or more bus agents may each be implemented with a full-width data bus according to the conventional configuration, in which the microprocessor operates in either in the full-width data bus mode using the full-width data bus or the half-width data bus mode using the half-width data bus including only a subset of the data signal group pins to reduce power. For embodiments in which both half-width and full-width data bus modes are supported, mode switching may be performed during operation or negotiated by the devices coupled to the system bus during initialization (e.g., power-on or reset). Mode switching during operation may employ an additional signal on the system bus to switch between modes. Alternatively, an existing signal on the system bus may be employed for mode switching purposes.

[0024] FIG. 3 is a timing diagram illustrating a data phase of a half-width quad-pumped transaction using a half-width data bus implemented according to an embodiment of the present invention. A half-width quad-pumped data bus according to an embodiment of the present invention employs a reduced-size data signal group including data signals DATA[31:0] and four data strobe signals DSTBP[1:0] and DSTBN[1:0]. As shown by the timing diagram of FIG. 3, the data phase of the transaction still includes four beats that are driven out to the DATA bus during a single cycle of BCLK[1:0], but each of the beats consists of a transfer of a doubleword rather than a quadword. Thus, to transfer a 64-byte cache line, 16 beats A, B, C, D, E, F, G, H, I, J, K, L, M, N, O, and P (A-P) are used and the entire transfer takes 4 clock cycles rather than two clock cycles.

[0025] In an x86-compatible embodiment, the data bus signal group according to an embodiment of the present invention is divided into two subgroups. Subgroup 0 includes signals DATA[15:0], DSTBP0, and DSTBN0 and subgroup 1 includes signals DATA[31:16], DSTBP1, and DSTBN1. The falling edges of the DSTBP0 signal are used to indicate validity of words on the DATA [15:0] signals for beats A, C, E, G, I, K, M, and O. The falling edges of the DSTBN0 signal are used to indicate validity of words on the DATA[15:0] signals for beats B, D, F, H, J, L, N, and P. The falling edges of the DSTBP1 signal are used to indicate validity of words on the DATA[31:16] signals for beats A, C, E, G, I, K, M, and O. The falling edges of the DSTBN1 signal are used to indicate validity of words on the DATA[31:16] signals for beats B, D, F, H, J, L, N, and P.

[0026] FIG. 4 is a diagram of a table 400 illustrating how the data bus signals DATA[31:0] of a half-width quad-pumped data bus according to an embodiment of the present invention are mapped during a data phase to data bytes within a 64-byte cache line. In table 400, the 16 beats A-P are listed versus BCLK cycles and corresponding cache line bytes transferred on the data signals DATA[31:0]. For example, during the first cycle of BCLK, or cycle 0, cache line bytes 3:0, 7:4, 11:8, and 15:12 are transferred during beats A, B, C, and D, respectively. One skilled in the art will appreciate that other mapping configurations are contemplated as well by the present invention and that the example of table 400 is provided to teach how data is transferred over the illustrated half-width data bus.

[0027] FIG. 5 is a simplified block diagram of a microprocessor interface system 500 including a system bus 505 with data signal group signals for a half-width quad-pumped data bus according to an embodiment of the present invention. The microprocessor interface system 500 includes a microprocessor 501 and a bus agent 503 interfaced with a system bus 505, in which the bus agent 503 represents any number of different types of bus agents as previously described for the bus agent 103. The A, ADSTB, REQ, DATA, DSTBP, DSTBN and RS buses along with the DBSY, DRDY and BCLK[1:0] signals are included. The A, ADSTB, REQ and RS buses along with the DBSY and DRDY signals operate in substantially the same manner as described above with reference to the conventional microprocessor interface system 100. In addition, the microprocessor 501 includes data bus configuration logic 507 which interfaces the DATA bus and the data strobe signals DSTBP[1:0] and DSTBN[1:0] to enable half-width quad-pumped data transactions as described with reference to FIGs 3 and 4. And

the bus agent 503 includes data bus configuration logic 509 which also interfaces the DATA bus and the data strobe signals DSTBP[1:0] and DSTBN[1:0] to enable half-width quad-pumped data transactions. In particular, the data phase for a 64-byte transfer over the half-width data bus includes beats A-P over four cycles of BCLK[1:0] as previously described. Data strobe signals DSTBP[1:0] and DSTBN[1:0] are employed to latch associated data during the four cycles of BCLK[1:0] as shown in FIG. 3.

[0028] In an alternative embodiment, the microprocessor 501 and/or the bus agent 503 include a full set of data signal group signals, e.g., the DATA[63:0] and the data strobe signals DSTBP[3:0] and DSTBN[3:0], and the data bus configuration logic 507 and 509 enable a half-width quad-pumped mode in which roughly half of the data signal group signals are employed to perform half-width quad-pumped data transactions as described with reference to FIGs 3 and 4.

[0029] FIG. 6 is a block diagram of data bus configuration logic 601 which may be used to implement the data bus configuration logic 507 and/or the data bus configuration logic 509 according to an exemplary embodiment of the present invention. The data bus configuration logic 601 includes at least one input to which a half-width data bus configuration enable signal HWDB is provided. The data bus configuration logic 601 operates with all of the inputs/outputs of a full-width quad-pumped data signal group. Responsive to the state of HWDB, a corresponding data bus protocol is enabled via full-width protocol logic 603 (which employs all of the data bus signals shown in accordance with that shown in FIGs 1 and 2) or half-width protocol logic 605 (which employs a subset of the data bus signals as described with reference to FIGs 3-5). In operation, if HWDB is asserted, then a transaction data phase operates over the half-width quad-pumped data signal group as described with reference to FIGs 3-5. If HWDB is not asserted, then a transaction data phase operates over the full-width quad-pumped data signal group as described with reference to the microprocessor interface system 100 described in FIGs 1-2.

[0030] One skilled in the art will appreciate that signals may be shared with other signals and may be mapped differently than described herein. In one embodiment, the data bus configuration logic 601 (and/or 507/509) comprises logic, circuits, and/or microcode. In another embodiment, the data bus configuration logic 601 (and/or 507/509) receives HWDB responsive to a fuse that is blown during fabrication to establish a specific data bus configuration. Other embodiments contemplate read-only memory, write-once memory, and the like. A further embodiment provides for communication with one or more bus agents 503 when a RESET signal (not shown) or other signal on the microprocessor 501 is held asserted or otherwise is placed in a non-architectural state. The communication between the bus agent(s) 503 and the microprocessor 501 is accomplished over signals employed for half-width quad-pumped operation. The communication establishes the capability of the bus agent(s) 503 to execute in half-width quad-pumped mode. Responsive to the communication, the data bus configuration logic 601 (and/or 507/509) enables either full-width or half-width functionality.

[0031] A half-width data bus configuration system according to an embodiment of the present invention is particularly advantageous for embedded applications. One advantage is that a half-width data bus configuration system according to an embodiment of the present invention allows for approximately a 50 percent reduction in the number of pins required to provide for a present day data signal group. In addition, a half-width data bus configuration system according to an embodiment of the present invention provides for a configurable reduction in power requirements by reducing the number of data bus signals. Furthermore, a half-width data bus configuration system according to an embodiment of the present invention allows a system designer to cut memory requirements in half for applications where memory requirements are less than that provided for by existing memory components.

[0032] Although the present invention has been described in considerable detail with reference to certain preferred versions thereof, other versions and variations are possible and contemplated. Those skilled in the art should appreciate that they can readily use the disclosed conception and specific embodiments as a basis for designing or modifying other structures for carrying out the same purposes of the present invention without departing from the scope of the invention as defined by the appended claims.

Claims

1. A microprocessor (501), comprising:

a system clock pin receiving a bus clock signal (BCLK[1:0]);

a plurality of data signal group pins; and

data bus configuration logic (507), comprising:

half-width protocol logic (605), responsive to an enable signal, and configured to perform a half-width data transaction on said plurality of data signal group pins in which a doubleword is transferred for each of four beats during each of four consecutive cycles of said bus clock signal (BCLK[1:0]), when enabled;

full-width protocol logic (603), responsive to the enable signal, and configured to perform a full-width data transaction on said plurality of data signal group pins in which a quadword is transferred for each of four beats during each of two consecutive cycles of said bus clock signal (BCLK[1:0]) when enabled; and

wherein the microprocessor (501) is configured to communicate with one or more bus agents over said plurality of data signal group pins to establish the capability of said one or more bus agents to execute said half-width transaction or said full-width transaction, and wherein said data bus configuration logic (507) enables either said full-width transaction or said half-width transaction for corresponding transaction data phases accordingly.

2. The microprocessor (501) of claim 1, wherein said plurality of data signal group pins comprises a plurality of data strobe pins.

3. The microprocessor (501) of claim 2, wherein said plurality of data strobe pins comprise first and second data strobe pins for latching first and third doublewords and third and fourth data strobe pins for latching second and fourth doublewords during each of said four consecutive cycles of said bus clock signal.

4. The microprocessor (501) of claim 1, wherein said plurality of data signal group pins comprises first and second data portions and wherein each said doubleword is divided between said first and second data portions.

5. The microprocessor (501) of claim 4, wherein said plurality of data signal group pins comprises first and second data strobe signals which latch data on said first data portion and third and fourth data strobe signals which latch data on said second data portion.

6. A method of performing a half-width data transaction on a system bus (505), comprising:

communicating with one or more bus agents over a first data portion and a second data portion of the system bus to establish the capability of the one or more bus agents to execute the half-width data transaction or a full-width data transaction;
responsive to said communicating, enabling either the full-width data transaction or the half-width data transaction for corresponding transaction data phases;
executing a first half-width data transaction for a particular bus agent that is capable of the half-width data transaction, said executing comprising:

asserting a doubleword of data for each of four beats on the system bus (505) during each of four consecutive cycles of a bus clock (BCLK[1:0]); and
asserting at least one data strobe for each beat.

7. The method of claim 6, wherein said executing further comprises:

asserting a first pair of data strobes to latch first and third doublewords during each bus clock cycle; and
asserting a second pair of data strobes to latch second and fourth doublewords during each bus clock cycle.

8. The method of claim 7, wherein:

said asserting a first pair of data strobes to latch first and third doublewords during each bus clock cycle comprises asserting a first data strobe to latch first and third words on the first data portion of the system bus (505) and asserting a second data strobe to latch second and fourth words on the first data portion; and
wherein said asserting a second pair of data strobes to latch second and fourth doublewords during each bus clock cycle comprises asserting a third data strobe to latch first and third words on the second data portion of the system bus (505) and asserting a fourth data strobe to latch second and fourth words on the second data portion.

9. The method of claim 6, wherein said asserting a doubleword of data for each of four beats on the system bus (505) during each of four consecutive cycles of a bus clock (BCLK[1:0]) comprises asserting a data word on each of the first and second data portions of the system bus (505).

Patentansprüche

1. Mikroprozessor (501), umfassend:

einen Systemtakt-Anschlussstift, der ein Bustaktsignal (BCLK[1:0]) empfängt;
eine Anzahl Datensignalgruppen-Anschlussstifte; und
eine Datenbus-Konfigurationslogik (507), umfassend:

eine Halbbreiten-Protokolllogik (605), die auf ein Freigabesignal anspricht und dafür ausgelegt ist, eine Halbbreiten-Datentransaktion auf der Anzahl Datensignalgruppen-Anschlussstifte vorzunehmen, worin ein Doppelwort für jeden von vier Beats während eines jeden Zyklus von vier aufeinander folgenden Zyklen des Bustaktsignals (BCLK[1:0]) übertragen wird, wenn eine Freigabe vorliegt;
eine Vollbreiten-Protokolllogik (603), die

auf das Freigabesignal anspricht und dafür ausgelegt ist, eine Vollbreiten-Datentransaktion auf der Anzahl Datensignalgruppen-Anschlussstifte vorzunehmen, worin ein Vierfachwort für jeden von vier Beats während eines jeden Zyklus von zwei aufeinander folgenden Zyklen des Bustaktsignals (BCLK[1:0]) übertragen wird, wenn eine Freigabe vorliegt;

wobei der Mikroprozessor (501) dafür konfiguriert ist, mit einem oder mehreren Busagenten über die Anzahl Datensignalgruppen-Anschlussstifte zu kommunizieren, um die Fähigkeit des einen oder der mehreren Busagenten herzustellen, die Halbbreitentransaktion oder die Vollbreitentransaktion auszuführen, und die Datenbus-Konfigurationslogik (507) entweder die Vollbreitentransaktion oder die Halbbreitentransaktion für zugehörige Transaktionsdatenphasen entsprechend ermöglicht.

2. Mikroprozessor (501) nach Anspruch 1, worin die Anzahl Datensignalgruppen-Anschlussstifte eine Anzahl Datenimpulsstifte enthält.

3. Mikroprozessor (501) nach Anspruch 2, worin die Anzahl Datenimpulsstifte einen ersten und einen zweiten Datenimpulsstift umfasst, die dem Zwischenspeichern erster und dritter Doppelwörter dienen, und einen dritten und einen vierten Datenimpulsstift, die dem Zwischenspeichern zweiter und vierter Doppelwörter dienen, und zwar während eines jeden Zyklus der vier aufeinander folgenden Zyklen des Bustaktsignals.

4. Mikroprozessor (501) nach Anspruch 1, worin die Anzahl Datensignalgruppen-Anschlussstifte erste und zweite Datenabschnitte umfasst, und worin jedes Doppelwort auf den ersten und den zweiten Datenabschnitt aufgeteilt wird.

5. Mikroprozessor (501) nach Anspruch 4, worin die Anzahl Datensignalgruppen-Anschlussstifte erste und zweite Datenimpulssignale umfasst, die Daten auf den ersten Datenabschnitt zwischenspeichern, und dritte und vierte Datenimpulssignale, die Daten auf den zweiten Datenabschnitt zwischenspeichern.

6. Verfahren zum Ausführen einer Halbbreiten-Datentransaktion auf einem Systembus (505), umfassend:

das Kommunizieren mit einem oder mehreren Busagenten über einen ersten Datenabschnitt und einen zweiten Datenabschnitt des Systembusses, um die Fähigkeit des einen oder der mehreren Busagenten herzustellen, die Halbbreiten-Datentransaktion oder eine Vollbreiten-Datentransaktion auszuführen;
abhängig von der Kommunikation das Freigeben entweder der Vollbreiten-Datentransaktion oder der Halbbreiten-Datentransaktion für zugehörige Transaktionsdatenphasen;
das Ausführen einer ersten Halbbreiten-Datentransaktion für einen bestimmten Busagenten, der in der Lage ist, die Halbbreiten-Datentransaktion vorzunehmen, wobei das Ausführen umfasst:

das Zuweisen eines Doppelworts an Daten für jeden von vier Beats auf dem Systembus (505) während eines jeden Zyklus von vier aufeinander folgenden Zyklen eines Bustakts (BCLK[1:0]); und
das Zuweisen mindestens eines Datenimpulses für jeden Beat.

7. Verfahren nach Anspruch 6, worin das Ausführen zudem umfasst:

das Zuweisen eines ersten Paars Datenimpulse zum Zwischenspeichern erster und dritter Doppelwörter während eines jeden Bustaktzyklus; und
das Zuweisen eines zweiten Paars Datenimpulse zum Zwischenspeichern zweiter und vierter Doppelwörter während eines jeden Bustaktzyklus.

8. Verfahren nach Anspruch 7, worin:

das Zuweisen eines ersten Paars Datenimpulse zum Zwischenspeichern erster und dritter Doppelwörter während eines jeden Bustaktzyklus das Zuweisen eines ersten Datenimpulses zum Zwischenspeichern erster und dritter Wörter auf dem ersten Datenabschnitt des Systembusses (505) und das Zuweisen eines zweiten Datenimpulses zum Zwischenspeichern zweiter und vierter Wörter auf dem ersten Datenabschnitt umfasst; und
das Zuweisen eines zweiten Paars Datenimpulse zum Zwischenspeichern zweiter und vierter Doppelwörter während eines jeden Bustaktzyklus das Zuweisen eines dritten Datenimpulses zum Zwischenspeichern erster und dritter Wörter auf dem zweiten Datenabschnitt des Systembusses (505) und das Zuweisen eines vierten Datenimpulses zum Zwischenspeichern zweiter und vierter Wörter auf dem zweiten Datenabschnitt umfasst.

9. Verfahren nach Anspruch 6, worin das Zuweisen eines Doppelworts an Daten für jeden Beat von vier Beats auf dem Systembus (505) während eines jeden Zyklus von vier aufeinander folgenden Zyklen

eines Bustakts (BCLK[1:0]) das Zuweisen eines Datenworts sowohl an den ersten als auch den zweiten Datenabschnitt des Systembusses (505) umfasst.

Revendications

1. Microprocesseur (501), comportant:

une broche d'horloge de système recevant un signal d'horloge de bus (BCLK [1:0]) ;
une pluralité de broches de groupes de signaux de données ; et
une logique de configuration de bus de données (507), comportant:

une logique de protocole en demi-largeur (605), sensible à un signal d'activation, et configurée pour mettre en oeuvre une transaction de données en demi-largeur sur ladite pluralité de broches de groupes de signaux de données dans laquelle un double mot est transféré pour chacun de quatre battements au cours de chacun de quatre cycles consécutifs dudit signal d'horloge de bus (BCLK [1:0]), lorsqu'activé ;
une logique de protocole en pleine largeur (603), sensible au signal d'activation, et configurée pour mettre en oeuvre une transaction de données pleine largeur sur ladite pluralité de broches de groupes de signaux de données dans laquelle un quadruple mot est transféré pour chacun de quatre battements au cours de chacun de deux cycles consécutifs dudit signal d'horloge de bus (BCLK [1:0]), lorsque activé ; et

dans lequel le microprocesseur (501) est configuré pour communiquer avec un ou plusieurs agents de bus sur ladite pluralité de broches de groupes de signaux de données pour établir la capacité dudit un ou desdits plusieurs agents de bus à exécuter ladite transaction en demi-largeur ou ladite transaction pleine largeur, et dans lequel ladite logique de configuration de bus de données (507) active ladite transaction pleine largeur ou ladite transaction en demi-largeur pour des phases de données de transaction correspondantes, de manière pertinente.

2. Microprocesseur (501) selon la revendication 1, dans lequel ladite pluralité de broches de groupes de signaux de données comporte une pluralité de broches d'échantillonnage de données.

3. Microprocesseur (501) selon la revendication 2, dans lequel ladite pluralité de broches d'échantillonnage de données comporte des première et deuxième broches d'échantillonnage de données pour verrouiller des premier et troisième doubles mots et des troisième et quatrième broches d'échantillonnage de données pour verrouiller des deuxième et quatrième doubles mots au cours de chacun de quatre cycles consécutifs dudit signal d'horloge de bus.

4. Microprocesseur (501) selon la revendication 1, dans lequel ladite pluralité de broches de groupes de signaux de données comporte des première et seconde parties de données et dans lequel chaque dit double mot est réparti entre lesdites première et seconde parties de données.

5. Microprocesseur (501) selon la revendication 4, dans lequel ladite pluralité de broches de groupes de signaux de données comporte des premier et deuxième signaux d'échantillonnage de données qui verrouillent des données sur ladite première partie de données et des troisième et quatrième signaux d'échantillonnage de données qui verrouillent des données sur ladite seconde partie de données.

6. Procédé pour mettre en oeuvre une transaction de données en demi-largeur sur un système de bus (505), comportant les étapes consistant à :

communiquer avec un ou plusieurs agents de bus sur une première partie de données et une seconde partie de données du bus de système pour établir la capacité dudit un ou desdits plusieurs agents de bus à exécuter la transaction de données en demi-largeur ou une transaction de données pleine largeur ;
en réponse à ladite communication, activer la transaction pleine largeur ou la transaction en demi-largeur pour des phases de données de transaction correspondantes ;
exécuter une première transaction de données en demi-largeur pour un agent de bus particulier qui est capable de mettre en oeuvre la transaction de données en demi-largeur, ladite exécution comportant les étapes consistant à :

affirmer un double mot de données pour chacun de quatre battements sur le bus de système (505) au cours de chacun de quatre cycles consécutifs d'une horloge de bus (BCLK [1:0]) ; et
affirmer au moins un échantillonnage de données pour chaque battement.

7. Procédé selon la revendication 6, dans lequel ladite exécution comporte en outre les étapes consistant à :

affirmer une première paire d'échantillonnages de données pour verrouiller des premier et troi-

sième doubles mots au cours de chaque cycle d'horloge de bus ; et
affirmer une seconde paire d'échantillonnages de données pour verrouiller des deuxième et quatrième double mots au cours de chaque cycle d'horloge de bus.

8. Procédé selon la revendication 7, dans lequel :

ladite affirmation d'une première paire d'échantillonnages de données pour verrouiller des premier et troisième doubles mots au cours de chaque cycle d'horloge de bus comporte l'étape consistant à affirmer un premier échantillonnage de données pour verrouiller des premier et troisième mots sur la première partie de données du bus de système (505) et l'étape consistant à affirmer un deuxième échantillonnage de données pour verrouiller des deuxième et quatrième mots sur la première partie de données ; et
dans lequel ladite affirmation d'une seconde paire d'échantillonnages de données pour verrouiller des deuxième et quatrième doubles mots au cours de chaque cycle d'horloge de bus comporte l'étape consistant à affirmer un troisième échantillonnage de données pour verrouiller des premier et troisième mots sur la seconde partie de données du bus de système (505) et l'étape consistant à affirmer un quatrième échantillonnage de données pour verrouiller des deuxième et quatrième mots sur la seconde partie de données.

9. Procédé selon la revendication 6, dans lequel ladite affirmation d'un double mot de données pour chacun de quatre battements sur le bus de système (505) au cours de chacun de quatre cycles consécutifs d'une horloge de bus (BCLK [1:0]) comporte l'étape consistant à affirmer un mot de données sur chacune des première et seconde parties de données du bus de système (505).

MICROPROCESSOR SIGNALS FOR BUS TRANSACTIONS

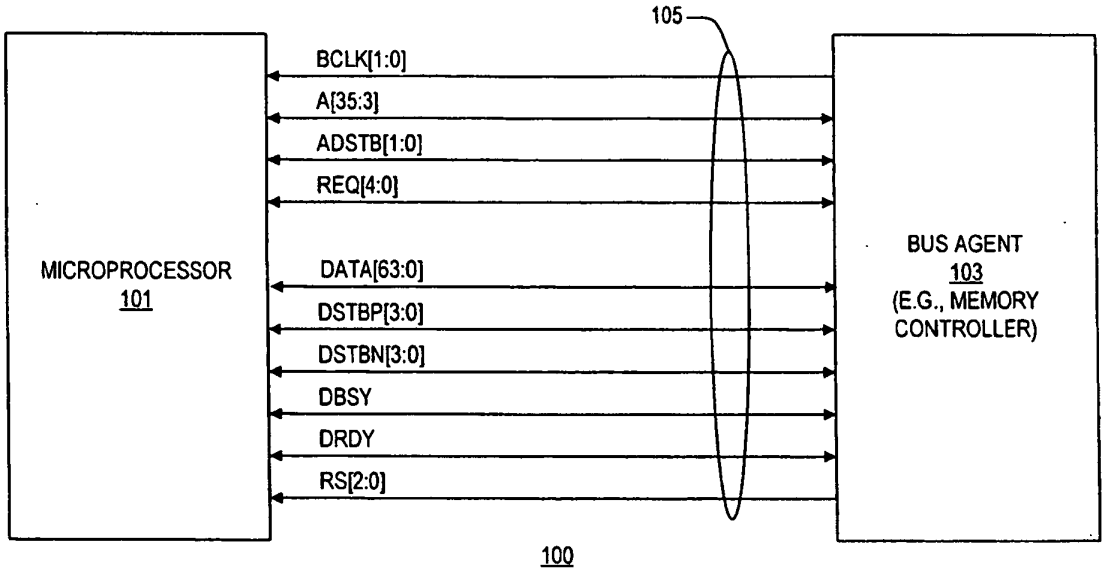
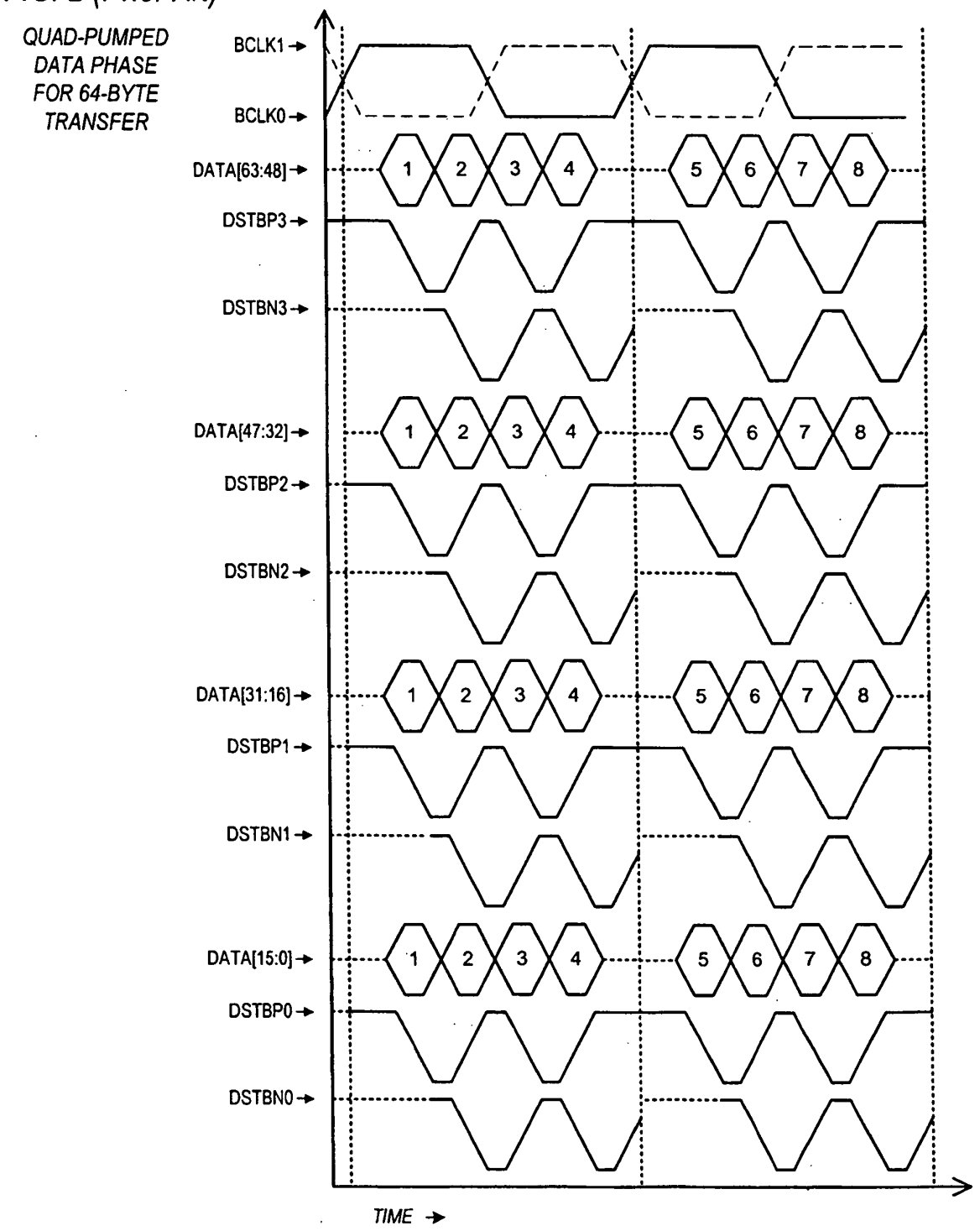


FIG. 1 (Prior Art)

FIG. 2 (Prior Art)



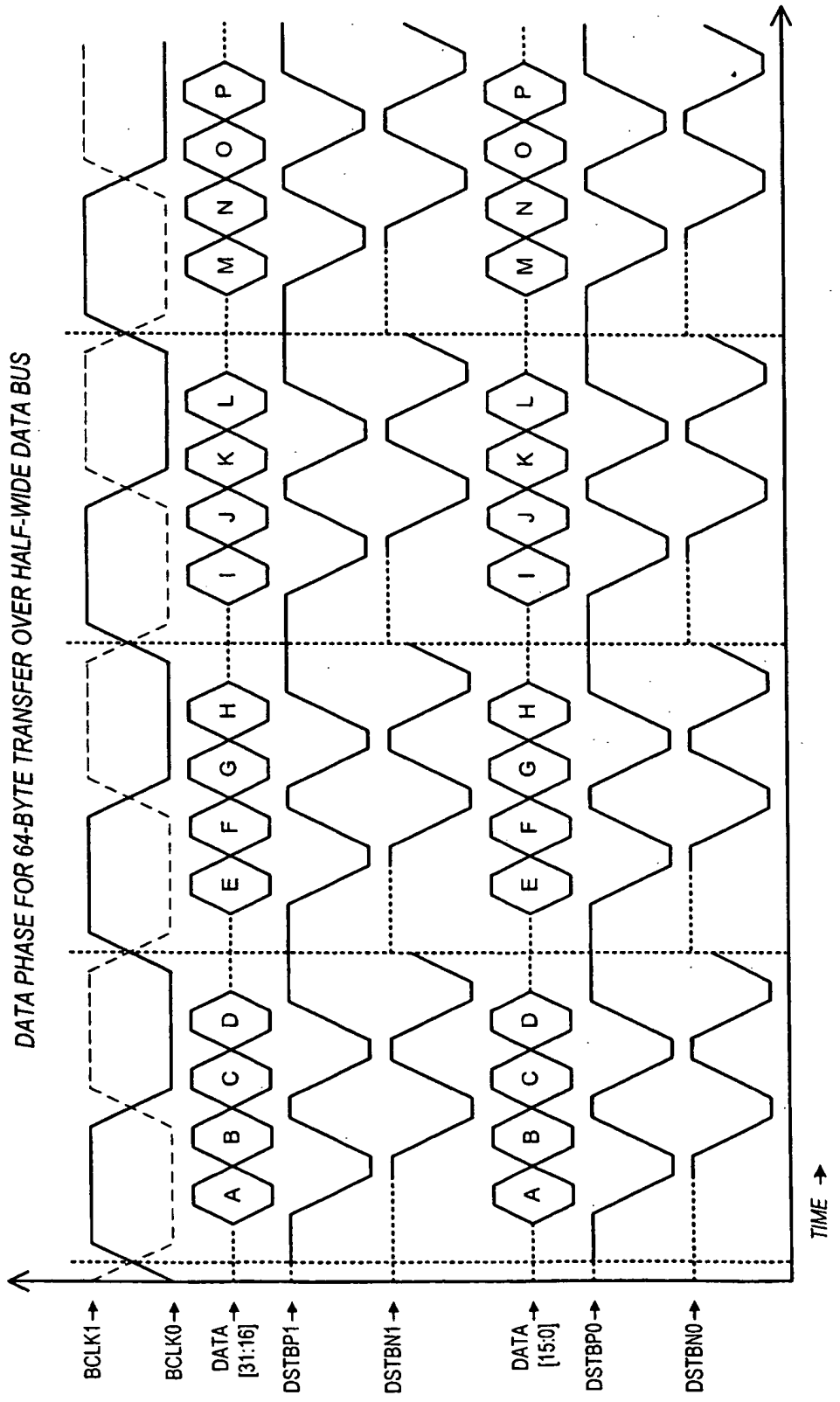

DATA PHASE FOR 64-BYTE TRANSFER OVER HALF-WIDE DATA BUS
BCLK1
BCLK0
DATA [31:16]
DSTBP1
DSTBN1
DATA [15:0]
DSTBP0
DSTBN0
TIME
A
B
C
D
E
F
G
H
I
J
K
L
M
N
O
P

FIG. 3

EXEMPLARY BYTE ORDERING FOR 64-BYTE TRANSFER OVER HALF-WIDE DATA BUS

105

BEAT	BCLK	CACHE LINE BYTES TRANSFERRED OVER DATA[31:0]
A	0	3:0
B	0	7:4
C	0	11:8
D	0	15:12
E	1	19:16
F	1	23:20
G	1	27:24
H	1	31:28
I	2	35:32
J	2	39:36
K	2	43:40
L	2	47:44
M	3	51:48
N	3	55:52
O	3	59:56
P	3	63:60

FIG. 4

MICROPROCESSOR SIGNALS FOR FLEXIBLE WIDTH DATA BUS

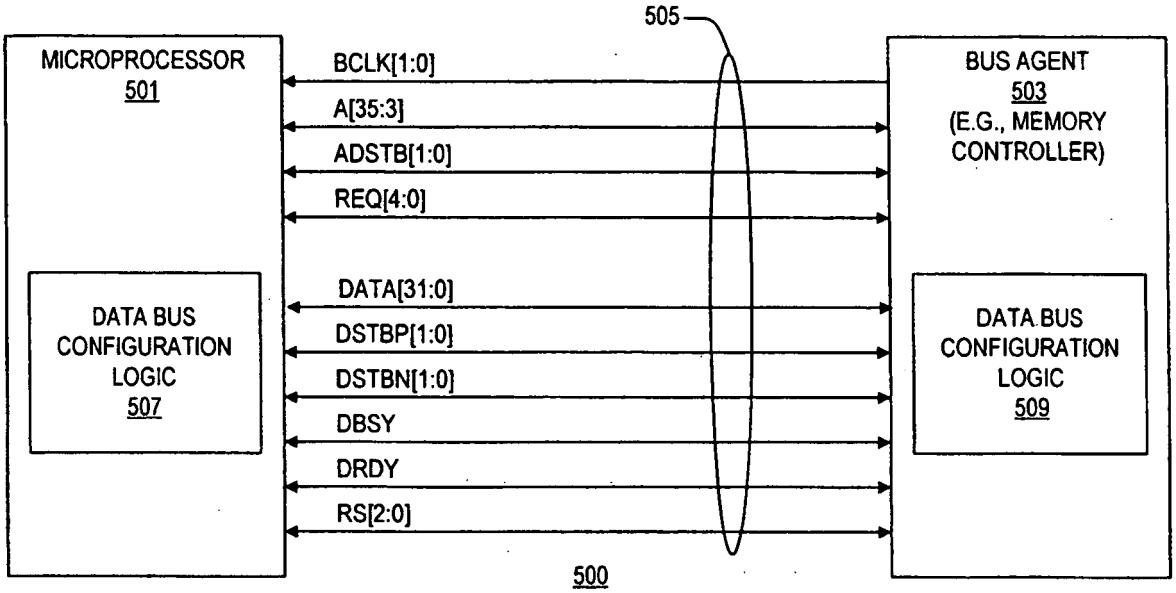


FIG. 5

CONFIGURATION LOGIC

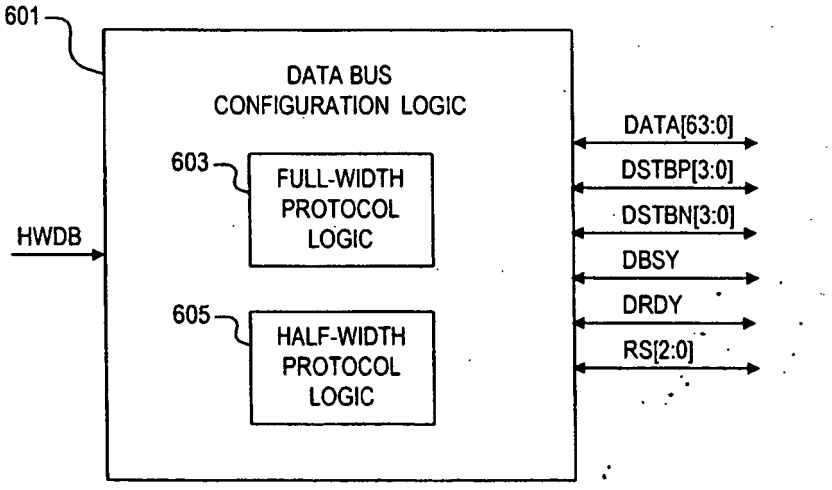


FIG. 6

REFERENCES CITED IN THE DESCRIPTION

This list of references cited by the applicant is for the reader's convenience only. It does not form part of the European patent document. Even though great care has been taken in compiling the references, errors or omissions cannot be excluded and the EPO disclaims all liability in this regard.

Patent documents cited in the description

- WO 0148621 A **[0004]**
- US 20030088799 A **[0005]**