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(54) **Chip-to-chip communication system**

(57) The invention relates to a chip-to-chip communication system (10) of the type comprising at least a transmitter TX (11) and a receiver RX (12), inserted between a first and a second voltage references (Vdd, GND) and connected to respective transmitter and receiver clock terminal wherein respective transmitter and receiver clock signals (CP, G) are applied, the transmitter TX (11) having an input terminal (TXin) receiving an input data (D) and an output terminal (TXout) connected to an input terminal (RXin) of the receiver RX (12) at a connection block (15), the receiver RX (12) having an output terminal (RXout) issuing an output signal (Q).

Advantageously according to the invention:
- the transmitter TX (11) comprises at least a precharge and an evaluation blocks (18, 19) connected to each other and to the transmitter clock terminal (CP);
- the receiver RX (12) comprises at least a precharge block (25) connected to the receiver clock terminal (G)

the precharge blocks (18, 25) precharging the output terminal (TXout) of the transmitter TX (11) and the input terminal (RXin) of the receiver RX (12), respectively, to a value corresponding to a first voltage reference (Vcc) during a low phase of the transmitter clock signal (CP).

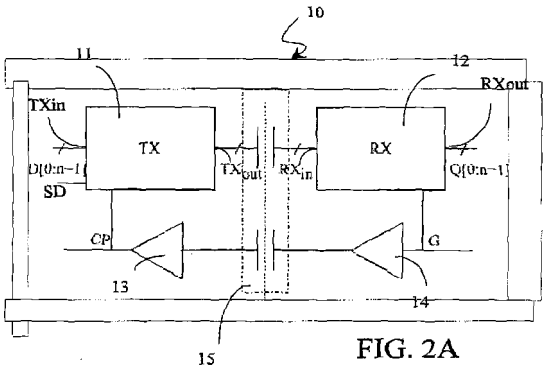

FIG. 2A

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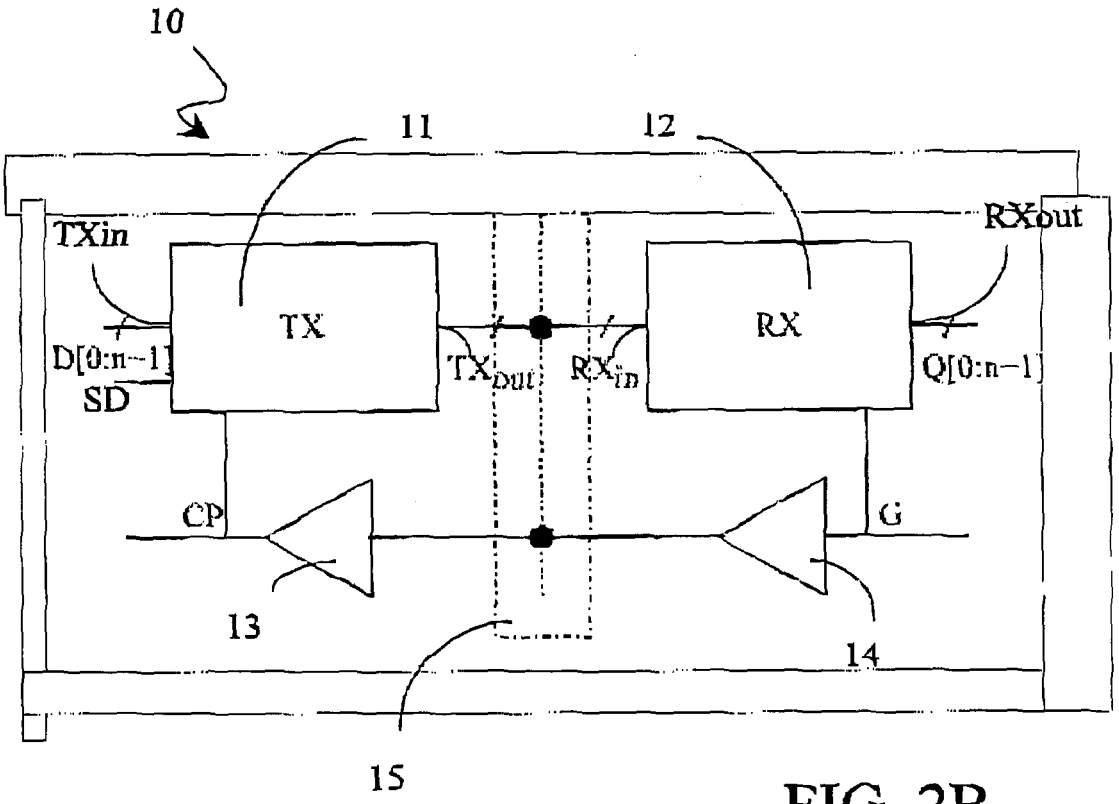

FIG. 2B