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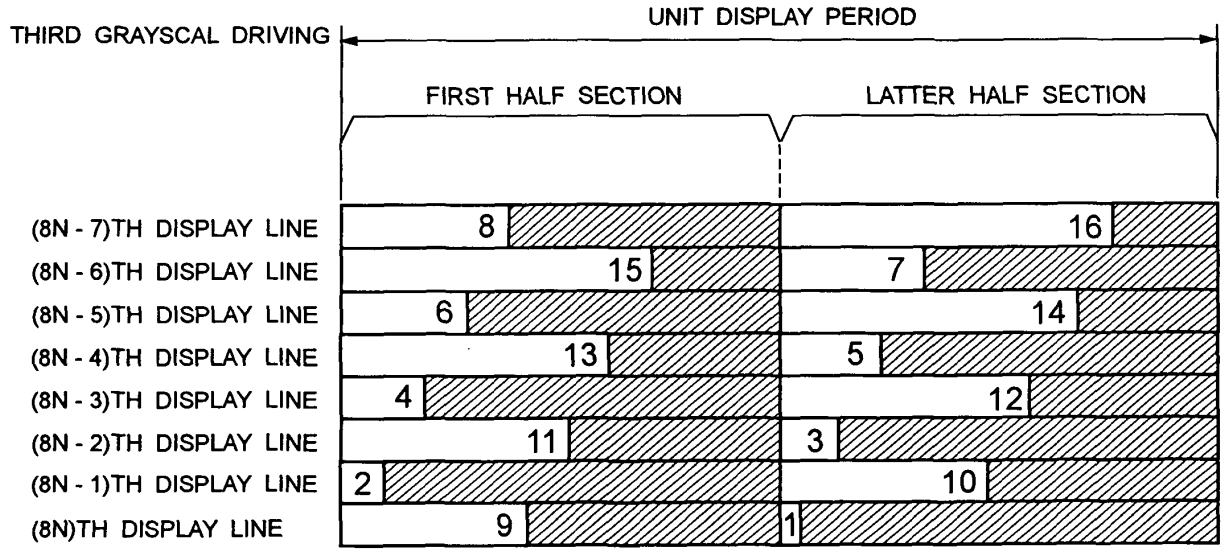
(54) Method for driving display panel

(57) A method for driving a display panel having capability to provide good image display with suppressed flickers and dither patterns respectively assigns brightness weight values to a plurality of successive display lines belonging to each of display line groups. An emission period within a unit display period of one pixel cell belonging to one display line differs from that of another pixel cell belonging to another display line based on this brightness weight values. In this instance, the emission operation of the pixel cell during this emission period is separated into a first half section and a latter half section within a unit display period. Further, relationship of the length of an emission period in the first half section to that in the latter half section is reversed between one discharge cell belonging to one display line and another discharge cell belonging to another display line among the same display line group.

FIG. 8



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Description

BACKGROUND OF THE INVENTION

1. Field of the Invention

[0001] The present invention relates to a method for driving a matrix display type display panel.

2. Description of the Related Art

[0002] Recently a plasma display panel (hereafter referred to as PDP) having a plurality of discharge cells arranged in a matrix pattern draws attention as a two-dimensional image display panel. On the other hand, a subfield method which displays an image corresponding to an input video signal on a PDP has been known. According to the subfield method, a display period of one field is divided into a plurality of subfields, and each of the discharge cells is selectively discharged for emission in each subfield in accordance with a brightness level indicated by the input video signal. By this operation, intermediate brightness corresponding to an overall emission period within one field period is visually recognized.

[0003] Fig. 1 shows an example of an emission drive sequence based on the subfield method (see for example Japanese Patent Application Laid-Open No. 2000-227778, Fig. 14).

[0004] In the emission drive sequence shown in Fig. 1, one field period is divided into 14 subfields, i.e., subfields SF1 to SF14. Only in the first subfield SF1 among the subfields SF1 to SF14, all the discharge cells of the PDP are initialized into light ON mode (Rc). Further, in each of the subfields SF1 to SF14, a discharge cell is set to light OFF mode depending on the input video signal (Wc), and only a display cell set to light ON mode is discharged for emission during a period assigned to this subfield (Ic).

[0005] Fig. 2 shows an example of an emission drive pattern within one field period of one discharge cell, which is driven based on such emission drive sequence (see for example Japanese Patent Application Laid-Open No. 2000-227778, Fig. 27).

[0006] According to the emission pattern in Fig. 2, a discharge cell which has been initialized to the light ON mode in the first subfield SF1 is selectively erase-discharged in one of the subfields SF1 to SF14 so as to set to light OFF mode as shown by black dots. A discharge cell which is once set to light OFF mode maintains its light OFF mode until the subfield SF14 at the very end. In other words, until being set to light OFF mode, a discharge cell is continuously discharged for emission in subfields shown by white circles from the first subfield SF1. Since each of the 15 types of emission patterns shown in Fig. 2 has a different total emission period in one field period, 15 types of intermediate brightness can be represented. In short, (N + 1) grayscales (N is the number of subfields) of intermediate brightness display is possible.

[0007] In this method, however, the number of subfields into which one field is divided is limited, and therefore the number of grayscales may become insufficient. To compensate the insufficiency of the number of grayscales, multi-grayscale processing, such as error diffusion and dither processing, is performed for the input video signal.

[0008] In error diffusion processing, the input video signal is converted into, for example, 8-bit pixel data for each pixel where the significant 6 bits thereof are recognized as the display data and the remaining insignificant 2 bits are recognized as error data. Error data corresponding to the peripheral pixels are respectively weighted and then added to each other so as to incorporate into the display data concerned. By this operation, the brightness of the insignificant 2 bits in an original pixel is artificially represented by the peripheral pixels, and therefore the grayscale representation of the brightness equivalent to the 8 bits of pixel data becomes possible by 6 bits of display data. Dither processing is then performed on the 6 bits of error diffusion-processed pixel data acquired by the above-described error diffusion processing. In the dither processing, a plurality of adjacent pixels are regarded as one pixel unit, and different dither coefficients are respectively assigned and added to the pixels in this one pixel unit where each of the pixels corresponds to the error diffusion-processed pixel data. By adding the dither coefficients, brightness equivalent to 8 bits can be represented only by the significant 4 bits of the dither-added pixel data in terms of one pixel unit. Accordingly, the significant 4 bits of the dither-added pixel data are extracted as the multi-grayscale pixel data Ds, and those data are respectively assigned to the 15 types of emission patterns, as shown in Fig. 2.

[0009] However, when dither coefficients are regularly added to the pixel data by dither processing, a pseudo-pattern called a dither pattern, which is not related to the input video signal, may be visually recognized, which deteriorates image quality.

[0010] Further, when the emission drive pattern shown in Fig. 2 is carried out, the switching from emission sustaining status to light OFF status is once or less within one field period, and therefore the switching frequency is the same as the vertical synchronizing frequency which determines one field display period. Therefore if a PAL type television signal, of which vertical synchronizing frequency is only 50 [Hz], is supplied as the input video signal, flickers tend to be outstanding.

SUMMARY OF THE INVENTION

[0011] The present invention is provided to solve the foregoing problems, and an object of the present invention is to provide a method for driving a display panel which allows good image display where flickers and dither patterns are suppressed.

[0012] According to a first aspect of the invention, there

is provided a method for driving a display panel having a plurality of display lines each provided with a plurality of pixel cells, said pixel cells are driven by a plurality of subfields within each unit display period, said method comprising: a drive step for respectively assigning different brightness weight values to a series of M (M is an integer 2 or higher) display lines belonging to each of display line groups, and for emitting said pixel cells based on said brightness weight values such that an emission period of a pixel cell belonging to one display line differs from that of another pixel cell belonging to another display line among said M display lines, wherein said drive step comprises a first half drive step for executing emission of a first period out of said emission period in a first half section of said unit display period, and a latter half drive step for executing emission of a remaining second period out of said emission period in a latter half section of said unit display period, and relationship of a length of said first period to a length of said second period is reversed between one pixel cell belonging to one display line and another pixel cell belonging to another display line among said display line group.

[0013] According to a second aspect of the invention, there is provided a method for driving a display panel having a plurality of display lines each provided with a plurality of pixel cells, said display panel is driven to display grayscale by a plurality of subfields in each unit display period in accordance with an input video signal, the method comprising: emitting one pixel cell belonging to one display line by P subfields (P is an integer) continuously placed in a first half section of said unit display period and by Q subfields (Q is an integer less than P) continuously placed in a latter half section of said unit display period, and emitting another pixel cell belonging to another display line adjacent to said one display line by Q subfields continuously placed in the first half section of said unit display period and by P subfields continuously placed in the latter half section of said unit display period, when the Kth grayscale display is performed, and emitting one pixel cell belonging to said one display line by said P subfields similara to said Kth grayscale display in the first half section of said unit display period, and by said Q subfields similar to said Kth grayscale display in the latter half section of said unit display period and by L subsequent subfields, and emitting said another pixel cell belonging to said another display line adjacent to said one display line by said P subfields similar to said Kth grayscale display and L subsequent subfields in the first half section of said unit display period, and by said P subfields similar to said Kth grayscale display, when (K+1)th grayscale is displayed.

BRIEF DESCRIPTION OF THE DRAWINGS

[0014]

Fig. 1 is a diagram showing an example of an emission drive sequence based on the subfield method;

Fig. 2 is a diagram showing an example of an emission drive pattern in one field period of one discharge cell which is driven based on the emission drive sequence shown in Fig. 1;

Fig. 3 is a diagram showing a configuration of a plasma display device for driving a plasma display panel based on a driving method according to the present invention;

Fig. 4 is a data conversion table in a drive data conversion circuit 3 shown in Fig. 3;

Fig. 5 is a diagram showing an example of an emission drive sequence;

Fig. 6 is a diagram showing an emission drive pattern based on the emission drive sequence shown in Fig. 5;

Fig. 7 is a diagram showing a brightness level represented by a first to sixth grayscale drive for each display line; and

Fig. 8 is a diagram showing an emission pattern in a unit display period by a third grayscale drive for each display line.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0015] A method for driving a display panel according to the present invention respectively assigns brightness weight values to a plurality of successive display lines belonging to each of display line groups. An emission period within a unit display period of one pixel cell belonging to one display line differs from that of another pixel cell belonging to another display line based on this brightness weight values. In this instance, the emission operation of the pixel cell during this emission period is separated into a first half section and a latter half section within a unit display period. Further, relationship of the length of an emission period in the first half section to that in the latter half section is reversed between one discharge cell belonging to one display line and another discharge cell belonging to another display line among the same display line group. According to this method, frequency to change the status of the discharge cell from light ON status to light OFF status is twice per a unit display period. Accordingly, a good display with suppressed flickers can be performed even if an input video signal with low vertical synchronizing frequency such as PAL type television signal is supplied. Further, emission patterns of a series of 8 display lines change in a unit display period in a manner different from the line dither pattern corresponding to the brightness weight values fixedly assigned to the 8 display lines, and therefore the generation of a line dither pattern can be suppressed.

[0016] Embodiments of the present invention will be hereinafter described with reference to the drawings.

[0017] Fig. 3 is a diagram showing a schematic configuration of a plasma display device for driving a plasma display panel according to the method of the present invention.

[0018] In Fig. 3, the PDP 100 as a plasma display panel has column electrodes D1 to Dm extending in the vertical direction, and row electrodes X1 to Xn and row electrodes Y1 to Yn extending in the horizontal direction of the two dimensional display screen. The row electrodes X1 to Xn and row electrodes Y1 to Yn are alternately arranged one by one. A pair of row electrodes X and Y, which are adjacent to each other, serve display of one display line in the PDP 100. Specifically, the PDP 100 has a first display line including row electrodes X1 and Y1, a second display line including row electrodes X2 and Y2, ... and an n-th display line including row electrodes Xn and Yn. A discharge space is provided between these first to n-th display lines and the column electrodes D1 to Dm so as to seal discharge gas therebetween, and a plurality of discharge cells each corresponding to a pixel are respectively formed at intersections between the row electrodes and the column electrodes including the discharge space. The PDP 100 thus has ($n \times m$) discharge cells $G_{(1, 1)}$ to $G_{(n, m)}$ which are arranged in a matrix pattern.

[0019] A pixel data conversion circuit 1 converts an input video signal into pixel data PD of, for example, 8 bits which represents a brightness level of a pixel, and supplies the pixel data PD to a multi-grayscale processing circuit 2. It should be noted that the input video signal mentioned above is obtained after gamma correction on a source video signal corresponding to the image to be displayed.

[0020] The multi-grayscale processing circuit 2 includes a line dither offset value generation circuit 21, adder 22 and insignificant bit round-off circuit 23.

[0021] The line dither offset value generation circuit 21 first generates 8 line dither offset values LD respectively having the values of, for example, 0 through 7 such that these values respectively correspond to the following 8 display line sets, which are formed by dividing a first to n-th display lines of the PDP 100 in a manner that each of the sets is provided with a plurality of display lines of every eighth display line:

(8N-7)th display line set having {1st, 9th, 17th, ... (n-7)th display line},
(8N-6)th display line set having (2nd, 10th, 18th, ... (n-6)th display line),
(8N-5)th display line set having {3rd, 11th, 19th, ... (n-5)th display line},
(8N-4)th display line set having {4th, 12th, 20th, ... (n-4)th display line},
(8N-3)th display line set having {5th, 13th, 21th, ... (n-3)th display line},
(8N-2)th display line set having {6th, 14th, 22th, ... (n-2)th display line},
(8N-1)th display line set having (7th, 15th, 23th, ... (n-1)th display line}, and
(8N)th display line set having {8th, 16th, 24th, ... nth display line},

where N denotes natural numbers of (1/8)·n and smaller.

[0022] The line dither offset value generation circuit 21 then supplies the line dither offset value LD to the adder 22 such that the line dither offset value LD corresponds to the display line which includes the discharge cell of the pixel data PD supplied from the pixel data conversion circuit 1.

[0023] The adder 22 supplies the line offset added pixel data LF, which is obtained by addition of the line dither offset value LD with the pixel data PD, to an insignificant bit round-off circuit 23. The insignificant bit round-off circuit 23 rounds off the insignificant 3 bits of the line offset added pixel data LF, and supplies the remaining significant 3 bits to a drive data conversion circuit 3 as multi-grayscale pixel data MD.

[0024] The drive data conversion circuit 3 converts the 3 bit multi-grayscale pixel data MD to 6 bit pixel drive data GD in accordance with a data conversion table shown in Fig. 4, and supplies it to a memory 4.

[0025] The memory 4 sequentially receives and stores the pixel drive data GD of each pixel. Upon completion of the writing of pixel drive data $GD_{1, 1}$ to $GD_{n, m}$ of one image frame (n rows $\times$ m columns), the memory 4 separates each of the pixel drive data $GD_{1, 1}$ to $GD_{n, m}$ into bit digits, and reads one display line at a time. The memory 4 reads pixel drive data bits of the one display line (m bits), and supplies them to a column electrode drive circuit 5 as the pixel drive data bits DB1 to DB(m).

[0026] The drive control circuit 6 generates various timing signals for grayscale driving the PDP 100 in accordance with the emission drive sequence shown in Fig. 5, and supplies them to the column electrode drive circuit 5, row electrode Y drive circuit 7 and row electrode X drive circuit 8 respectively. Each of the column electrode drive circuit 5, row electrode Y drive circuit 7 and row electrode X drive circuit 8 generates various drive pulses (not shown) for driving the PDP 100 as described below in response to a timing signal supplied from the drive control circuit 6, and applies them to the column electrodes D1 to Dm, row electrodes X1 to Xn and row electrodes Y1 to Yn of the PDP 100.

[0027] In the emission drive sequence shown in Fig. 5, the following six subfields SF0 to SF5 are used so as to represent the various brightness levels for displaying one frame or one field of image in six levels.

[0028] The subfield SF0 determines whether the lowest brightness level 0 is represented or a higher brightness level is represented. The subfield SF0 is comprised of a low-level subfield $SF0_a$ placed in the beginning of the first half section of a unit display period, i.e., one frame or one field display period, and a low-level subfield $SF0_b$ placed in the beginning of the latter half section thereof, as shown in Fig. 5. In each of the low-level subfields $SF0_a$ and $SF0_b$, the drive control circuit 6 executes a reset step R for initializing all the discharge cells to light ON mode status, where a predetermined amount of wall charges are formed, and an address step W0 for selectively erase-discharging discharge cells depending on the pixel drive data GD from the first to n-th display lines of the PDP

100 in a manner that each display line is erase-discharged at a time.

[0029] The subfield SF1 serves to provide emission with higher brightness level than the lowest brightness level 0 by only one level. The subfield SF1 is comprised of 8 low-level subfields $SF1_{a1}$ to $SF1_{a4}$ and $SF1_{b1}$ to $SF1_{b4}$, as shown in Fig. 5, so as to differentiate a brightness level of emission of one discharge cell belonging to one display line from that of another discharge cell belonging to another display line among 8 display lines of each display line group. In this case, as shown in Fig. 5, 4 low-level subfields $SF1_{a1}$ to $SF1_{a4}$, out of these 8 low-level subfields, are placed after the low-level subfield $SF0_a$ in the first half section of the unit display period, and the remaining low-level subfields $SF1_{b1}$ to $SF1_{b4}$ are placed after the low-level subfield $SF0_b$ in the latter half section of the unit display period. In the low-level subfield $SF1_{a1}$, the drive control circuit 6 sequentially executes the sustain step I for repeatedly sustain-discharging the display cells which are set to light ON mode, during a period extending over 2, and the address step W7 for selectively erase-discharging only the discharge cells placed in the (8N-1)th display line in accordance with the pixel drive data GD. In the low-level subfield $SF1_{a2}$, the drive control circuit 6 sequentially executes the sustain step I for repeatedly sustain-discharging the discharge cells which are set to light ON mode, during a period extending over 2, and the address step W5 for selectively erase-discharging only the discharge cells placed in the (8N-3)th display line in accordance with the pixel drive data GD. In the low-level subfield $SF1_{a3}$, the drive control circuit 6 sequentially executes the sustain step I for repeatedly sustain-discharging the discharge cells which are set to light ON mode, during a period extending over 2, and the address step W3 for selectively erase-discharging only the discharge cells placed in the (8N-5)th display line in accordance with the pixel drive data GD. In the low-level subfield $SF1_{a4}$, the drive control circuit 6 sequentially executes the sustain step I for repeatedly sustain-discharging the discharge cells which are set to light ON mode, during a period extending over 2, and the address step W1 for selectively erase-discharging only the discharge cells placed in the (8N-7)th display line in accordance with the pixel drive data GD. In the low-level subfield $SF1_{b1}$, the drive control circuit 6 sequentially executes the sustain step I for repeatedly sustain-discharging the discharge cells which are set to light ON mode, during a period extending over 1, and the address step W8 for selectively erase-discharging only the discharge cells placed in the (8N)th display line in accordance with the pixel drive data GD. In the low-level subfield $SF1_{b2}$, the drive control circuit 6 sequentially executes the sustain step I for repeatedly sustain-discharging the discharge cells which are set to light ON mode, during a period extending over 2, and the address step W6 for selectively erase-discharging only the discharge cells placed in the (8N-2)th display line in accordance with the pixel drive data GD. In the low-level subfield $SF1_{b3}$, the drive control circuit 6 sequentially executes the sustain step I for repeatedly sustain-discharging the discharge cells which are set to light ON mode, during a period extending over 2, and the address step W4 for selectively erase-discharging only the discharge cells placed in the (8N-4)th display line in accordance with the pixel drive data GD. In the low-level subfield $SF1_{b4}$, the drive control circuit 6 sequentially executes the sustain step I for repeatedly sustain-discharging the discharge cells which are set to light ON mode, during a period extending over 2, and the address step W2 for selectively erase-discharging only the discharge cells placed in the (8N-6)th display line in accordance with the pixel drive data GD.

[0030] The subfield SF2 serves to provide emission with higher brightness level than the subfield SF1 by only one level. The subfield SF2 is comprised of 8 low-level subfields $SF2_{a1}$ to $SF2_{a4}$ and $SF2_{b1}$ to $SF2_{b4}$, as shown in Fig. 5, so as to differentiate a brightness level of emission of one discharge cell belonging to one display line from that of another discharge cell belonging to another display line among 8 display lines of each display line group. In this case, as Fig. 5 shows, 4 low-level subfields $SF2_{a1}$ to $SF2_{a4}$, out of these 8 low-level subfields, are placed after the low-level subfield $SF1_{a4}$ in the first half section of the unit display period, and the remaining low-level subfields $SF2_{b1}$ to $SF2_{b4}$ are placed after the low-level subfield $SF1_{b4}$ in the latter half section of the unit display period. In the low-level subfield $SF2_{a1}$, the drive control circuit 6 sequentially executes the sustain step I for repeatedly sustain-discharging the discharge cells which are set to light ON mode, during a period extending over 1, and the address step W8 for selectively erase-discharging only the discharge cells placed in the (8N)th display line in accordance with the pixel drive data GD. In the low-level subfield $SF2_{a2}$, the drive control circuit 6 sequentially executes the sustain step I for repeatedly sustain-discharging the discharge cells which are set to light ON mode, during a period extending over 2, and the address step W6 for selectively erase-discharging only the discharge cells placed in the (8N-2)th display line in accordance with the pixel drive data GD. In the low-level subfield $SF2_{a3}$, the drive control circuit 6 sequentially executes the sustain step I for repeatedly sustain-discharging the discharge cells which are set to light ON mode, during a period extending over 2, and the address step W4 for selectively erase-discharging only the discharge cells placed in the (8N-4)th display line in accordance with the pixel drive data GD. In the low-level subfield $SF2_{a4}$, the drive control circuit 6 sequentially executes the sustain step I for repeatedly sustain-discharging the discharge cells which are set to light ON mode, during a period extending over 2, and the address step W2 for selectively erase-discharging only the discharge cells placed in the (8N-6)th display line in accordance with the pixel drive data GD. In the low-level subfield $SF2_{b1}$, the drive control circuit 6 sequentially executes the sustain step I for repeatedly sustain-discharging the discharge cells which are set to light ON mode, during a period

extending over 3, and the address step W7 for selectively erase-discharging only the discharge cells placed in the (8N-1)th display line in accordance with the pixel drive data GD. In the low-level subfield $SF2_{b2}$, the drive control circuit 6 sequentially executes the sustain step I for repeatedly sustain-discharging the discharge cells which are set to light ON mode, during a period extending over 2, and the address step W5 for selectively erase-discharging only the discharge cells placed in the (8N-3)th display line in accordance with the pixel drive data GD. In the low-level subfield $SF2_{b3}$, the drive control circuit 6 sequentially executes the sustain step I for repeatedly sustain-discharging the discharge cells which are set to light ON mode, during a period extending over 2, and the address steps W3 for selectively erase-discharging only the discharge cells placed in the (8N-5)th display line according to the pixel data GD. In the low-level subfield $SF2_{b4}$, the drive control circuit 6 sequentially executes the sustain step I for repeatedly sustain-discharging the discharge cells which are set to light ON mode, during a period extending over 2, and the address step W1 for selectively erase-discharging only the discharge cells placed in the (8N-7)th display line in accordance with the pixel drive data GD.

[0031] The subfield SF3 serves to provide emission with higher brightness than the subfield SF2 by only one level. The subfield SF3 is comprised of 8 low-level subfields $SF3_{a1}$ to $SF3_{a4}$ and $SF3_{b1}$ to $SF3_{b4}$, as shown in Fig. 5, so as to differentiate a brightness level of emission of one discharge cell belonging to one display line from that of another discharge cell belonging to another display line among 8 display lines of each display line group. In this case, as Fig. 5 shows, 4 low-level subfields $SF3_{a1}$ to $SF3_{a4}$, out of these 8 low-level subfields, are placed after the low-level subfield $SF2_{a4}$ in the first half section of the unit display period, and the remaining low-level subfields $SF3_{b1}$ to $SF3_{b4}$ are placed after the low-level subfield $SF2_{b4}$ in the latter half section of the unit display period. In the low-level subfield $SF3_{a1}$, the drive control circuit 6 sequentially executes the sustain step I for repeatedly sustain-discharging the discharge cells which are set to light ON mode, during a period extending over 5, and the address step W7 for selectively erase-discharging only the discharge cells placed in the (8N-1)th display line in accordance with the pixel drive data GD. In the low-level subfield $SF3_{a2}$, the drive control circuit 6 sequentially executes the sustain step I for repeatedly sustain-discharging the discharge cells which are set to light ON mode, during a period extending over 4, and the address step W5 for selectively erase-discharging only the discharge cells placed in the (8N-3)th display line in accordance with the pixel drive data GD. In the low-level subfield $SF3_{a3}$, the drive control circuit 6 sequentially executes the sustain step I for repeatedly sustain-discharging the discharge cells which are set to light ON mode, during a period extending over 4, and the address step W3 for selectively erase-discharging only the discharge cells placed in the (8N-5)th display line in accordance with the pixel drive data GD. In the low-level subfield $SF3_{a4}$, the drive control circuit 6 sequentially executes the sustain step I for repeatedly sustain-discharging the discharge cells which are set to light ON mode, during a period extending over 4, and the address step W1 for selectively erase-discharging only the discharge cells placed in the (8N-7)th display line in accordance with the pixel drive data GD. In the low-level subfield $SF3_{b1}$, the drive control circuit 6 sequentially executes the sustain step I for repeatedly sustain-discharging the discharge cells which are set to light ON mode, during a period extending over 2, and the address step W8 for selectively erase-discharging only the discharge cells placed in the (8N)th display line in accordance with the pixel drive data GD. In the low-level subfield $SF3_{b2}$, the drive control circuit 6 sequentially executes the sustain step I for repeatedly sustain-discharging the discharge cells which are set to light ON mode, during a period extending over 4, and the address step W6 for selectively erase-discharging only the discharge cells placed in the (8N-2)th display line in accordance with the pixel drive data GD. In the low-level subfield $SF3_{b3}$, the drive control circuit 6 sequentially executes the sustain step I for repeatedly sustain-discharging the discharge cells which are set to light ON mode, during a period extending over 4, and the address step W4 for selectively erase-discharging only the discharge cells placed in the (8N-4)th display line in accordance with the pixel drive data GD. In the low-level subfield $SF3_{b4}$, the drive control circuit 6 sequentially executes the sustain step I for repeatedly sustain-discharging the discharge cells which are set to light ON mode, during a period extending over 4, and the address step W2 for selectively erase-discharging only the discharge cells placed in the (8N-6)th display line in accordance with the pixel drive data GD.

[0032] The subfield SF4 serves to provide emission with higher brightness level than the subfield SF3 by only one level. The subfield SF4 is comprised of 8 low-level subfields $SF4_{a1}$ to $SF4_{a4}$ and $SF4_{b1}$ to SFb_{4b}, as shown in Fig. 5, so as to differentiate a brightness level of emission of one discharge cell belonging to one display line from that of another discharge cell belonging to another display line among 8 display lines of each display line group. In this case, as Fig. 5 shows, 4 low-level subfields $SF4_{a1}$ to $SF4_{a4}$, out of these 8 low-level subfields, are placed after the low-level subfield $SF3_{a4}$ in the first half section of the unit display period, and the remaining low-level subfields $SF4_{b1}$ to $SF4_{b4}$ are placed after the low-level subfield $SF3_{b4}$ in the latter half section of the unit display period. In the low-level subfield $SF4_{a1}$, the drive control circuit 6 sequentially executes the sustain step I for repeatedly sustain-discharging the discharge cells which are set to light ON mode, during a period extending over 2, and the address step W8 for selectively erase-discharging only the discharge cells placed in the (8N)th display line in accordance with the pixel drive data GD. In the low-level subfield $SF4_{a2}$, the drive control circuit 6 sequentially executes the sustain step I for repeatedly

sustain-discharging the discharge cells which are set to light ON mode, during a period extending over 4, and the address step W6 for selectively erase-discharging only the discharge cells placed in the (8N-2)th display line in accordance with the pixel drive data GD. In the low-level subfield $SF4_{a3}$, the drive control circuit 6 sequentially executes the sustain step I for repeatedly sustain-discharging the discharge cells which are set to light ON mode, during a period extending over 4, and the address step W4 for selectively erase-discharging only the discharge cells placed in the (8N-4)th display line in accordance with the pixel drive data GD. In the low-level subfield $SF4_{a4}$, the drive control circuit 6 sequentially executes the sustain step I for repeatedly sustain-discharging the discharge cells which are set to light ON mode, during a period extending over 4, and the address step W2 for selectively erase-discharging only the discharge cells placed in the (8N-6)th display line in accordance with the pixel drive data GD. In the low-level subfield $SF4_{b1}$, the drive control circuit 6 sequentially executes the sustain step I for repeatedly sustain-discharging the discharge cells which are set to light ON mode, during a period extending over 6, and the address step W7 for selectively erase-discharging only the discharge cells placed in the (8N-1)th display line in accordance with the pixel drive data GD. In the low-level subfield $SF4_{b2}$, the drive control circuit 6 sequentially executes the sustain step I for repeatedly sustain-discharging the discharge cells which are set to light ON mode, during a period extending over 4, and the address step W5 for selectively erase-discharging only the discharge cells placed in the (8N-3)th display line in accordance with the pixel drive data GD. In the low-level subfield $SF4_{b3}$, the drive control circuit 6 sequentially executes the sustain step I for repeatedly sustain-discharging the discharge cells which are set to light ON mode, during a period extending over 4, and the address step W3 for selectively erase-discharging only the discharge cells placed in the (8N-5)th display line in accordance with the pixel drive data GD. In the low-level subfield $SF4_{b4}$, the drive control circuit 6 executes the sustain step I for repeatedly sustain-discharging the discharge cells which are set to light On mode during a period extending over 4.

[0033] The subfield SF5 serves to provide emission with higher brightness level than the subfield SF4 by only one level, and is placed only at the very end of the first half section of the unit display period. In the subfield SF5, the drive control circuit 6 executes the sustain step I for repeatedly sustain-discharging the discharge cells which are set to light ON mode during a period extending over 2.

[0034] Fig. 6 is a diagram showing an emission drive pattern based on the emission drive sequence shown in Fig. 5 and the pixel drive data GD.

[0035] First, according to the pixel drive data GD of [110000] indicating lowest brightness, the following emission display is performed in accordance with the first grayscale drive. Specifically, the column electrode drive circuit 5, row electrode Y drive circuit 7, row electrode X drive circuit 8 and drive control circuit 6 (hereafter called drive section) erase-discharge the discharge cells (indicated by black dots) in the address step W0 in the low-level subfields $SF0_a$ and $SF0_b$, as shown in Fig. 6, in accordance with the pixel drive data GD of [110000], and set the discharge cells to light OFF mode. According to the driving shown in Fig. 5, the chances to shift discharge cells to light ON mode in the unit display period are only the reset steps R in low-level subfields $SF0_a$ and $SF0_b$. Therefore, in the case of the first grayscale drive in accordance with the pixel drive data GD of [110000], all discharge cells maintain light OFF mode throughout the unit display period, and display with brightness level 0 is performed.

[0036] According to the pixel drive data GD of [011000] indicating higher brightness than the above-described [110000] by only one level, the following emission display is performed in accordance with the second grayscale drive.

[0037] Specifically, for the discharge cells belonging to the (8N-7)th display line, the drive section generates erase-discharge only in the low-level subfield $SF1_{a4}$ (indicated by a double circle) for the first half section and $SF0_b$ (indicated by a black dot) in the latter half section within the unit display period. Therefore in this case, the discharge cells belonging to the (8N-7)th display line continuously perform sustain-discharge for emission in $SF1_{a1}$ to $SF1_{a4}$ (indicated by white circles and a double circle) which extend from initialization to light ON mode in the first low-level subfield $SF0_a$ until generation of erase-discharge in $SF1_{a4}$. By this operation, the brightness level 8 corresponding to the overall length of the sustain-discharge for emission throughout the low-level subfields $SF1_{a1}$ to $SF1_{a4}$ is represented. For the discharge cells belonging to the (8N-6)th display line, the drive section generates erase-discharge in the low-level subfield $SF0_a$ (indicated by a black dot) for the first half section and $SF1_{b4}$ (indicated by a double circle) in the latter half section within the unit display period. Therefore in this case, the discharge cells belonging to the (8N-6)th display line continuously perform sustain-discharge for emission in $SF1_{b1}$ to $SF1_{b4}$ (indicated by white circles and double circle) which extend from initialization to light ON mode in the low-level subfield $SF0_b$ until generation of erase-discharge in $SF1_{b4}$ in the latter half section of the unit display period. By this operation, the brightness level 7 corresponding to the overall length of the sustain-discharge for emission throughout the low-level subfields $SF1_{b1}$ to $SF1_{b4}$ is represented. For the discharge cells belonging to the (8N-5)th display line, the drive section generates erase-discharge in the low-level subfield $SF1_{a3}$ (indicated by a double circle) for the first half section and $SF0_b$ (indicated by a black dot) in the latter half section within the unit display period. Therefore in this case, the discharge cells belonging to the (8N-5)th display line continuously perform sustain-discharge for emission in $SF1_{a1}$ to $SF1_{a3}$ (indicated by white circles and a double circle) which extend from initialization to

light ON mode in the first low-level subfield SFO_a until generation of erase-discharge in $SF1_{a3}$. By this operation, the brightness level 6 corresponding to the overall length of the sustain-discharge for emission throughout the low-level subfields $SF1_{a1}$ to $SF1_{a3}$ is represented. For the discharge cells belonging to the (8N-4)th display line, the drive section generates erase-discharge in the low-level subfield SFO_a (indicated by a black dot) for the first half section and $SF1_{b3}$ (indicated by a double circle) in the latter half section within the unit display period. Therefore in this case, the discharge cells belonging to the (8N-4)th display line continuously perform sustain-discharge for emission in $SF1_{b1}$ to $SF1_{b3}$ (indicated by white circles and a double circle) which extend from initialization to light ON mode in the low-level subfield $SF0_b$ until generation of erase-discharge in $SF1_{b3}$ in the latter half section of the unit display period. By this operation, the brightness level 5 corresponding to the overall length of the sustain-discharge for emission throughout the low-level subfields $SF1_{b1}$ to $SF1_{b3}$ is represented. For the discharge cells belonging to the (8N-3)th display line, the drive section generates erase-discharge in the low-level subfield $SF1_{a2}$ (indicated by a double circle) for the first half section and $SF0_b$ (indicated by a black dot) in the latter half section within the unit display period. Therefore in this case, the discharge cells belonging to the (8N-3)th display line continuously perform sustain-discharge for emission in $SF1_{a1}$ and $SF1_{a2}$ (indicated by a white circle and a double circle) which extend from initialization to light ON mode in the first low-level subfield $SF0_a$ until generation of erase-discharge in $SF1_{a2}$. By this operation, the brightness level 4 corresponding to the overall length of the sustain-discharge for emission throughout the low-level subfields $SF1_{a1}$ and $SF1_{a2}$ is represented. For the discharge cells belonging to the (8N-2)th display line, the drive section generates erase-discharge in the low-level subfield $SF0_a$ (indicated by a black dot) for the first half section and $SF1_{b2}$ (indicated by a double circle) in the latter half section within the unit display period. Therefore in this case, the discharge cells belonging to the (8N-2)th display line continuously perform sustain-discharge for emission in $SF1_{b1}$ and $SF1_{b2}$ (indicated by a white circle and a double circle) which extend from initialization to light ON mode in the low-level subfield $SF0_b$ until generation of erase-discharge in $SF1_{b2}$ in the latter half section of the unit display period. By this operation, the brightness level 3 corresponding to the overall length of the sustain-discharge for emission throughout the low-level subfields $SF1_{b1}$ and $SF1_{b2}$ is represented. For the discharge cells belonging to the (8N-1)th display line, the drive section generates erase-discharge in the low-level subfield $SF1_{a1}$ (indicated by a double circle) for the first half section and $SF0_b$ (indicated by a black dot) in the latter half section within the unit display period. Therefore in this case, the discharge cells belonging to the (8N-1)th display line perform sustain-discharge emissions in the low-level subfield $SF1_{a1}$ (indicated by a double circle). By this operation, the brightness level 2 corresponding to the overall length of the sustain-discharge for emission in the low-level subfield $SF1_{a1}$ is represented. For the discharge cells belonging to the (8N)th display line, the drive section generates erase-discharge in the low-level subfield $SF0_a$ (indicated by a black dot) for the first half section and SFl_{b1} (indicated by a double circle) in the latter half section within the unit display period. Therefore in this case, the discharge cells belonging to the (8N)th display line perform sustain-discharge emissions only in the low-level subfield $SF1_{b1}$ in the latter half section of the unit display period. By this operation, the brightness level 1 corresponding to the overall length of the sustain-discharge for emission in the low-level subfield $SF1_{b1}$ is represented.

[0038] According to the pixel drive data GD of [001100] indicating higher brightness than the above-described [011000] by only one level, the following emission display is performed in accordance with the third grayscale drive described below.

[0039] Specifically, for the discharge cells belonging to the (8N-7)th display line, the drive section generates erase-discharge only in the low-level subfield $SF1_{a4}$ (indicated by a double circle) for the first half section and low-level subfield $SF2_{b4}$ (indicated by a double circle) in the latter half section within the unit display period. Therefore in this case, the discharge cells belonging to the (8N-7)th display line continuously perform sustain-discharge emissions in $SF1_{a1}$ to $SF1_{a4}$ (indicated by white circles and a double circle) for the first half section and $SF1_{b1}$ to $SF2_{b4}$ (indicated by white circles and a double circle) in the latter half section within the unit display period. By this operation, the brightness level 24 corresponding to the overall length of the sustain-discharge for emission throughout the low-level subfields $SF1_{a1}$ to $SF1_{a4}$ and $SF1_{b1}$ to $SF2_{b4}$ is represented. For the discharge cells belonging to the (8N-6)th display line, the drive section generates erase-discharge only in the low-level subfield $SF2_{a4}$ (indicated by a double circle) for the first half section and low-level subfield $SF1_{b4}$ (indicated by a double circle) in the latter half section within the unit display period. Therefore in this case, the discharge cells belonging to the (8N-6)th display line continuously perform sustain-discharge for emission in $SF1_{a1}$ to $SF2_{a4}$ (indicated by white circles and a double circle) for the first half section and $SF1_{b1}$ to $SF1_{b4}$ (indicated by white circles and a double circle) in the latter half section within the unit display period. By this operation, the brightness level 22 corresponding to the overall length of sustain-discharge for emission throughout the low-level subfields $SF1_{a1}$ to $SF2_{a4}$ and $SF1_{b1}$ to $SF1_{b4}$ is represented. For the discharge cells belonging to the (8N-5)th display line, the drive section generates erase-discharge only in the low-level subfields $SF1_{a3}$ (indicated by a double circle) for the first half section and low-level subfield $SF2_{b3}$ (indicated by a double circle) in the latter half section within the unit display period. Therefore in this case, the discharge cells belonging to the (8N-5)th display line continuously perform sustain-discharge for emission in

$SF1_{a1}$ to $SF1_{a3}$ (indicated by white circles and a double circle) for the first half section and $SF1_{b1}$ to $SF2_{b3}$ (indicated by white circles and a double circle) in the latter half section within the unit display period. By this operation, the brightness level 20 corresponding to the overall length of the sustain-discharge for emission throughout the low-level subfields $SF1_{a1}$ to $SF1_{a3}$ and $SF1_{b1}$ to $SF2_{b3}$ is represented. For the discharge cells belonging to the (8N-4)th display line, the drive section generates erase-discharge only in the low-level subfield $SF2_{a3}$ (indicated by a double circle) for the first half section and low-level subfield $SF1_{b3}$ (indicated by a double circle) in the latter half section within the unit display period. Therefore in this case, the discharge cells belonging to the (8N-4)th display line continuously perform sustain-discharge for emission in $SF1_{a1}$ to $SF2_{a3}$ (indicated by white circles and a double circle) for the first half section and $SF1_{b1}$ to $SF1_{b3}$ (indicated by white circles and a double circle) in the latter half section within the unit display period. By this operation, the brightness level 18 corresponding to the overall length of sustain-discharge for emission throughout the low-level subfields $SF1_{a1}$ to $SF2_{a3}$ and $SF1_{b1}$ to $SF1_{b3}$ is represented. For the discharge cells belonging to the (8N-3)th display line, the drive section generates erase-discharge only in the low-level subfield $SF1_{a2}$ (indicated by a double circle) for the first half section and low-level subfield $SF2_{b2}$ (indicated by a double circle) in the latter half section within the unit display period. Therefore in this case, the discharge cells belonging to the (8N-3)th display line continuously perform sustain-discharge for emission in $SF1_{a1}$ and $SF1_{a2}$ (indicated by a white circle and a double circle) for the first half section and $SF1_{b1}$ to $SF2_{b2}$ (indicated by white circles and a double circle) in the latter half section within the unit display period. By this operation, the brightness level 16 corresponding to the overall length of sustain-discharge for emission throughout the low-level subfields $SF1_{a1}$ and $SF1_{a2}$, and $SF1_{b1}$ to $SF2_{b2}$ is represented. For the discharge cells belonging to the (8N-2)th display line, the drive section generates erase-discharge only in the low-level subfield $SF2_{a2}$ (indicated by a double circle) for the first half section and low-level subfield $SF1_{b2}$ (indicated by a double circle) in the latter half section within the unit display period. Therefore in this case, the discharge cells belonging to the (8N-2)th display line continuously performs sustain-discharge emissions in each of $SF1_{b1}$ to $SF2_{a2}$ (indicated by white circles and a double circle) for the first half section and $SF1_{b1}$ and $SF1_{b2}$ (indicated by a white circle and a double circle) in the latter half section within the unit display period. By this operation, the brightness level 14 corresponding to the overall length of the sustain-discharge for emission throughout the low-level subfields $SF1_{a1}$ to $SF2_{a2}$ and $SF1_{b1}$ and $SF1_{b2}$ is represented. For the discharge cells belonging to the (8N-1)th display line, the drive section generates erase-discharge only in the low-level subfield $SF1_{a1}$ (indicated by a double circle) for the first half section and low-level subfield $SF2_{b1}$ (indicated by a double circle) in the latter half section within the unit display period. Therefore in this case, the discharge cells belonging to the (8N-1)th display line continuously perform sustain-discharge for emission in $SF1_{a1}$ (indicated by a double circle) for the first half section and $SF1_{b1}$ to $SF2_{b1}$ (indicated by white circles and a double circle) in the latter half section within the unit display period. By this operation, the brightness level 12 corresponding to the overall length of the sustain-discharge for emission throughout the low-level subfields $SF1_{a1}$ and $SF1_{b1}$ to $SF2_{b1}$ is represented. For the discharge cells belonging to the (8N)th display line, the drive section generates erase-discharge only in the low-level subfield $SF2_{a1}$ (indicated by a double circle) for the first half section and low-level subfield $SF1_{b1}$ (indicated by a double circle) in the latter half section within the unit display period. Therefore in this case, the discharge cells belonging to the (8N)th display line continuously perform sustain-discharge for emission in $SF1_{a1}$ to $SF2_{a1}$ (indicated by white circles and a double circle) for the first half section and $SF1_{b1}$ in the latter half section within the unit display period. By this operation, the brightness level 10 corresponding to the overall length of sustain-discharge for emission throughout the low-level subfields $SF1_{a1}$ to $SF2_{a1}$ and $SF1_{b1}$ is represented.

[0040] Accordance to the pixel drive data GD of [000110] indicating higher brightness than the above-described [001100] by only one level, the following emission display is performed in accordance with the fourth gray-scale drive described below.

[0041] Specifically, for the discharge cells belonging to the (8N-7)th display line, the drive section generates erase-discharge only in the low-level subfield $SF3_{a4}$ (indicated by a double circle) for the first half section and low-level subfield $SF2_{b4}$ (indicated by a double circle) in the latter half section within the unit display period. Therefore in this case, the discharge cells belonging to the (8N-7)th display line continuously perform sustain-discharge for emission in $SF1_{a1}$ to $SF3_{a4}$ (indicated by white circles and a double circle) for the first half section and $SF1_{b1}$ to $SF2_{b4}$ (indicated by white circles and a double circle) in the latter half section within the unit display period. By this operation, the brightness level 48 corresponding to the overall length of the sustain-discharge for emission throughout the low-level subfields $SF1_{a1}$ to $SF3_{a4}$ and $SF1_{b1}$ to $SF2_{b4}$ is represented. For the discharge cells belonging to the (8N-6)th display line, the drive section generates erase-discharge only in the low-level subfield $SF2_{a4}$ (indicated by a double circle) for the first half section and low-level subfield $SF3_{b4}$ (indicated by a double circle) in the latter half section within the unit display period. Therefore in this case, the discharge cells belonging to the (8N-6)th display line continuously perform sustain-discharge for emission in $SF1_{a1}$ to $SF2_{a4}$ (indicated by white circles and a double circle) for the first half section and $SF1_{b1}$ to $SF3_{b4}$ (indicated by white circles and a double circle) in the latter half section within the unit display period. By this operation, the brightness level 45 corresponding to the overall length of sustain-discharge

for emission throughout the low-level subfields $SF1_{a1}$ to $SF2_{a4}$ and $SF1_{b1}$ to $SF3_{b4}$ is represented. For the discharge cells belonging to the (8N-5)th display line, the drive section generates erase-discharge only in the low-level subfield $SF3_{a3}$ (indicated by a double circle) for the first half section and low-level subfield $SF2_{b3}$ (indicated by a double circle) in the latter half section within the unit display period. Therefore in this case, the discharge cells belonging to the (8N-5)th display line continuously perform sustain-discharge for emission in $SF1_{a1}$ to $SF3_{a3}$ (indicated by white circles and a double circle) for the first half section and $SF1_{b1}$ to $SF2_{b3}$ (indicated by white circles and a double circle) in the latter half section within the unit display period. By this operation, the brightness level 42 corresponding to the overall length of the sustain-discharge for emission throughout the low-level subfields $SF1_{a1}$ to $SF3_{a3}$ and $SF1_{b1}$ to $SF2_{b3}$ is represented. For the discharge cells belonging to the (8N-4)th display line, the drive section generates erase-discharge only in the low-level subfield $SF2_{a3}$ (indicated by a double circle) for the first half section and low-level subfield $SF3_{b3}$ (indicated by a double circle) in the latter half section within the unit display period. Therefore in this case, the discharge cells belonging to the (8N-4)th display line continuously perform sustain-discharge for emission in $SF1_{a1}$ to $SF2_{a3}$ (indicated by white circles and a double circle) for the first half section and $SF1_{b1}$ to $SF3_{b3}$ (indicated by white circles and a double circle) in the latter half section within the unit display period. By this operation, the brightness level 39 corresponding to the overall length of sustain-discharge for emission throughout the low-level subfields $SF1_{a1}$ to $SF2_{a3}$ and $SF1_{b1}$ to $SF3_{b3}$ is represented. For the discharge cells belonging to the (8N-3)th display line, the drive section generates erase-discharge only in the low-level subfield $SF3_{a2}$ (indicated by a double circle) for the first half section and low-level subfield $SF2_{b2}$ (indicated by a double circle) in the latter half section within the unit display period. Therefore in this case, the discharge cells belonging to the (8N-3)th display line continuously perform sustain-discharge for emission in $SF1_{a1}$ to $SF3_{a2}$ (indicated by white circles and a double circle) for the first half section and $SF1_{b1}$ to $SF2_{b2}$ (indicated by white circles and a double circle) in the latter half section within the unit display period. By this operation, the brightness level 36 corresponding to the overall length of the sustain-discharge for emission throughout the low-level subfields $SF1_{a1}$ to $SF3_{a2}$ and $SF1_{b1}$ to $SF2_{b2}$ is represented. For the discharge cells belonging to the (8N-2)th display line, the drive section generates erase-discharge only in the low-level subfield $SF2_{a2}$ (indicated by a double circle) for the first half section and low-level subfield $SF3_{b2}$ (indicated by a double circle) in the latter half section within the unit display period. Therefore in this case, the discharge cells belonging to the (8N-2)th display line continuously perform sustain-discharge for emission in the $SF1_{a1}$ to $SF2_{a2}$ (indicated by white circles and a double circle) for the first half section and $SF1_{b1}$ to $SF3_{b2}$ (indicated by white circles and a double circle) in the latter half section within the unit display period. By this operation, the brightness level 33 corresponding to the overall length of sustain-discharge for emission throughout the low-level subfields $SF1_{a1}$ to $SF2_{a2}$ and $SF1_{b1}$ to $SF3_{b2}$ is represented. For the discharge cells belonging to the (8N-1)th display line, the drive section generates erase-discharge only in the low-level subfield $SF3_{a1}$ (indicated by a double circle) for the first half section and low-level subfield $SF2_{b1}$ (indicated by a double circle) in the latter half section within the unit display period. Therefore in this case, the discharge cells belonging to the (8N-1)th display line continuously perform sustain-discharge for emission in $SF1_{a1}$ to $SF3_{a1}$ (indicated by white circles and a double circle) for the first half section and $SF1_{b1}$ to $SF2_{b1}$ (indicated by white circles and a double circle) in the latter half section within the unit display period. By this operation, the brightness level 30 corresponding to the overall length of sustain-discharge for emission throughout the low-level subfields $SF1_{a1}$ to $SF3_{a1}$ and $SF1_{b1}$ to $SF2_{b1}$ is represented. For the discharge cells belonging to the (8N)th display line, the drive section generates erase-discharge only in the low-level subfield $SF2_{a1}$ (indicated by a double circle) for the first half section and low-level subfield $SF3_{b1}$ (indicated by a double circle) for the later half section in the unit display period. Therefore in this case, the discharge cells belonging to the (8N)th display line continuously perform sustain-discharge for emission in $SF1_{a1}$ to $SF2_{a1}$ (indicated by white circles and a double circle) for the first half section and $SF1_{b1}$ to $SF3_{b1}$ (indicated by white circles and a double circle) in the latter half section within the unit display period. By this operation, the brightness level 27 corresponding to the overall length of the sustain-discharge for emission throughout the low-level subfields $SF1_{a1}$ to $SF2_{a1}$ and $SF1_{b1}$ to $SF3_{b1}$ is represented.

[0042] According to the pixel drive data GD of [000011] indicating higher brightness than the above-described [000110] by only one level, the following emission display is performed in accordance with the fifth grayscale drive described below.

[0043] Specifically, for the discharge cells belonging to the (8N-7)th display line, the drive section generates erase-discharge only in the low-level subfield $SF3_{a4}$ (indicated by a double circle) for the first half section in the unit display period. Therefore in this case, the discharge cells belonging to the (8N-7)th display line continuously perform sustain-discharge for emission in $SF1_{a1}$ to $SF3_{a4}$ (indicated by white circles and a double circle) for the first half section and whole low-level subfields $SF1_{b1}$ to $SF4_{b4}$ (indicated by white circles) in the latter half section within the unit display period. By this operation, the brightness level 80 corresponding to the overall length of the sustain-discharge for emission throughout the low-level subfields $SF1_{a1}$ to $SF3_{a4}$ and $SF1_{b1}$ to $SF4_{b4}$ is represented. For the discharge cells belonging to the (8N-6)th display line, the drive section generates erase-discharge only in the low-level subfield $SF4_{a4}$ (indicated by a double circle) for the first half section and low-level

subfield $SF3_{b4}$ (indicated by a double circle) in the latter half section within the unit display period. Therefore in this case, the discharge cells belonging to the (8N-6)th display line continuously perform sustain-discharge for emission in $SF1_{a1}$ to $SF4_{a4}$ (indicated by white circles and a double circle) for the first half section and $SF1_{b1}$ to $SF3_{b4}$ (indicated by white circles and a double circle) in the latter half section within the unit display period. By this operation, brightness level 76 corresponding to the overall length of the sustain-discharge for emission is represented. For the discharge cells belonging to the (8N-5)th display line, the drive section generates erase-discharge only in the low-level subfield $SF3_{a3}$ (indicated by a double circle) for the first half section and the low-level subfield $SF4_{b3}$ (indicated by a double circle) for the latter section in the unit display period. Therefore in this case, the discharge cells belonging to the (8N-5)th display line continuously perform sustain-discharge for emission in $SF1_{a1}$ to $SF3_{a3}$ (indicated by white circles and a double circle) for the first half section and $SF1_{b1}$ to $SF4_{b3}$ (indicated by white circles and a double circle) in the latter half section within the unit display period. By this operation, the brightness level 72 corresponding to the overall length of the sustain-discharge for emission is represented. For the discharge cells belonging to the (8N-4)th display line, the drive section generates erase-discharge only in the low-level subfield $SF4_{a3}$ (indicated by a double circle) for the first half section and low-level subfield $SF3_{b3}$ (indicated by a double circle) in the latter half section within the unit display period. Therefore in this case, the discharge cells belonging to the (8N-4)th display line continuously perform sustain-discharge for emission in $SF1_{a1}$ to $SF4_{a3}$ (indicated by white circles and a double circle) for the first half section and $SF1_{b1}$ to $SF3_{b3}$ (indicated by white circles and a double circle) in the latter half section within the unit display period. By this operation, the brightness level 68 corresponding to the overall length of the sustain-discharge for emission is represented. For the discharge cells belonging to the (8N-3)th display line, the drive section generates erase-discharge only in the low-level subfield $SF3_{a2}$ (indicated by a double circle) for the first half section and the low-level subfield $SF4_{b2}$ (indicated by a double circle) in the latter half section within the unit display period. Therefore in this case, the discharge cells belonging to the (8N-3)th display line continuously perform sustain-discharge for emission in $SF1_{a1}$ to $SF3_{a2}$ (indicated by white circles and a double circle) for the first half section and $SF1_{b1}$ to $SF4_{b2}$ (indicated by white circles and a double circle) in the latter half section within the unit display period. By this operation, the brightness level 64 corresponding to the overall length of the sustain-discharge for emission is represented. For the discharge cells belonging to the (8N-2)th display line, the drive section generates erase-discharge only in the low-level subfield $SF4_{a2}$ (indicated by a double circle) for the first half section and low-level subfield $SF3_{b2}$ (indicated by a double circle) in the latter half section within the unit display period. Therefore in this case, the discharge cells belonging to the (8N-2)th display line continuously perform sustain-discharge for emission in $SF1_{a1}$ to $SF4_{a2}$ (indicated by white circles and a double circle) for the first half section and $SF1_{b1}$ to $SF3_{b2}$ (indicated by white circles and a double circle) in the latter half section within the unit display period. By this operation, the brightness level 60 corresponding to the overall length of the sustain-discharge for emission is represented. For the discharge cells belonging to the (8N-1)th display line, the drive section generates erase-discharge only in the low-level subfield $SF3_{a1}$ (indicated by a double circle) for the first half section and low-level subfield $SF4_{b1}$ (indicated by a double circle) in the latter half section within the unit display period. Therefore in this case, the discharge cells belonging to the (8N-1)th display line continuously perform sustain-discharge for emission in $SF1_{a1}$ to $SF3_{a1}$ (indicated by white circles and a double circle) for the first half section and $SF1_{b1}$ to $SF4_{b1}$ (indicated by white circles and a double circle) in the latter half section within the unit display period. By this operation, the brightness level 56 corresponding to the overall length of the sustain-discharge for emission is represented. For the discharge cells belonging to the (8N)th display line, the drive section generates erase-discharge only in the low-level subfield $SF4_{a1}$ (indicated by a double circle) for the first half section and low-level subfield $SF3_{b1}$ (indicated by a double circle) in the latter half section within the unit display period. Therefore in this case, the discharge cells belonging to the (8N)th display line continuously perform sustain-discharge for emission in $SF1_{a1}$ to $SF4_{a1}$ (indicated by white circles and a double circle) for the first half section and $SF1_{b1}$ and $SF3_{b1}$ (indicated by white circles and a double circle) in the latter half section within the unit display period. By this operation, the brightness level 52 corresponding to the overall length of the sustain-discharge for emission is represented.

[0044] In short, when the Kth grayscale display (K denotes integers 3 and 4) is performed for a discharge cell belonging to one display line, sustain-discharge for emission is performed by P subfields continuously placed in the first half section of the unit display period and by Q (Q < P) subfields continuously placed in the latter half section thereof. On the other hand, when the Kth grayscale display is performed for another discharge cell belonging to another display line adjacent to the above-described one display line, sustain-discharge for emission is performed by Q subfields continuously placed in the first half section of the unit display period and by P subfields continuously placed in the latter half section thereof. Further, when the (K+1)th grayscale display is performed for a discharge cell belonging to the above mentioned one display line, sustain-discharge for emission is performed by these M subfields similar to the above-described Kth grayscale display in the first half section of the unit display period, and by these Q subfields similar to the above-described Kth grayscale display and by L subsequent subfields in the latter half sec-

tion thereof. Whereas, for another discharge cell belonging to another display line adjacent to the above-described one display line, emission is performed by these Q subfields similar to the above-described Kth grayscale display and by L subsequent subfields in the first half section of the unit display period, and by these P subfields similar to the above-described Kth grayscale display in the latter half section thereof.

[0045] In other words, the number of subfields providing sustain-discharge for emission corresponding to the emission brightness in the first half section of the unit display period and the number of subfields providing sustain-discharge for emission corresponding to emission brightness in the latter half section thereof are switched or reversed between adjacent display lines.

[0046] According to the pixel drive data GD of [000000] indicating the highest brightness, an emission display is performed as described below in accordance with the sixth grayscale drive so as to represent the highest brightness.

[0047] Specifically, the drive section in this case does not generate an erase-discharge at all on the discharge cells during the unit display period, and therefore sustain-discharge for emission are continuously performed throughout the low-level subfields from $SF1_{a1}$ to SF5 and from $SF1_{b1}$ to $SF4_{b4}$. By this operation, the highest brightness level 96 corresponding to the overall length of sustain-discharge for emission throughout the subfields is represented.

[0048] As described above, the plasma display device shown in Fig. 3 performs the following line dither processing. Specifically, different line dither offset values LD are respectively assigned to a series of 8 display lines, that is:

(8N-7)th display line,
(8N-6)th display line,
(8N-5)th display line,
(8N-4)th display line,
(8N-3)th display line,
(8N-2)th display line,
(8N-1)th display line, and
(8N)th display line,

which are included in each of the display line groups. Then each of the pixel data PD is added with the line dither offset value LD in a manner that a line dither offset value LD to be added corresponds to a display line including a discharge cell of such pixel data PD. Then different brightness weight values are respectively assigned to the series of 8 display lines. Accordingly, as shown in Fig. 7, the discharge cells respectively belonging to these 8 display lines are emitted at different brightness levels (hereafter referred to as line dither processing) in each grayscale (first to sixth grayscale).

[0049] Specifically, in the second grayscale drive representing brightness with only one level higher than the first grayscale representing the lowest brightness, the following emission is performed as shown in Fig. 7:

discharge cells belonging to the (8N-7)th display line have brightness level 8,
discharge cells belonging to the (8N-6)th display line have brightness level 7,
discharge cells belonging to the (8N-5)th display line have brightness level 6,
discharge cells belonging to the (8N-4)th display line have brightness level 5,
discharge cells belonging to the (8N-3)th display line: brightness level 4,
discharge cells belonging to the (8N-2)th display line have brightness level 3,
discharge cells belonging to the (8N-1)th display line have brightness level 2, and
discharge cells belonging to the (8N)th display line have brightness level 1.

[0050] In the third grayscale drive representing brightness with only one level higher than the second grayscale, the following emission is performed as shown in Fig. 7:

discharge cells belonging to the (8N-7)th display line have brightness level 24,
discharge cells belonging to the (8N-6)th display line have brightness level 22,
discharge cells belonging to the (8N-5)th display line have brightness level 20,
discharge cells belonging to the (8N-4)th display line have brightness level 18,
discharge cells belonging to the (8N-3)th display line have brightness level 16,
discharge cells belonging to the (8N-2)th display line have brightness level 14,
discharge cells belonging to the (8N-1)th display line have brightness level 12, and
discharge cells belonging to the (8N)th display line have brightness level 10.

[0051] In the fourth grayscale drive representing brightness with only one level higher than the third grayscale, the following emission is performed as shown in Fig. 7:

discharge cells belonging to the (8N-7)th display line have brightness level 48,
discharge cells belonging to the (8N-6)th display line have brightness level 45,
discharge cells belonging to the (8N-5)th display line have brightness level 42,
discharge cells belonging to the (8N-4)th display line have brightness level 39,
discharge cells belonging to the (8N-3)th display line have brightness level 36,
discharge cells belonging to the (8N-2)th display line have brightness level 33,
discharge cells belonging to the (8N-1)th display line have brightness level 30, and

discharge cells belonging to the (8N)th display line have brightness level 27.

[0052] In the fifth grayscale drive representing brightness with only one level higher than the fourth grayscale, the following emission is performed as shown in Fig. 7:

discharge cells belonging to the (8N-7)th display line have brightness level 80,
discharge cells belonging to the (8N-6)th display line have brightness level 76,
discharge cells belonging to the (8N-5)th display line have brightness level 72,
discharge cells belonging to the (8N-4)th display line have brightness level 68,
discharge cells belonging to the (8N-3)th display line have brightness level 64,
discharge cells belonging to the (8N-2)th display line have brightness level 60,
discharge cells belonging to the (8N-1)th display line have brightness level 56, and
discharge cells belonging to the (8N)th display line have brightness level 52.

[0053] By this line dither processing, the number of grayscales visually recognized is increased.

[0054] When the discharge cell is sustain-discharged for emission in continuous subfields in the line dither processing, such sustain-discharge is executed separately in the subfield group ($SF0_a$, $SF1_{a1}$ to $SF1_{a4}$, $SF2_{a1}$ to $SF2_{a4}$, $SF3_{a1}$ to $SF3_{a4}$, $SF4_{a1}$ to $SF4_{a4}$, SF5) in the first half section of the unit display period, and in the subfield group ($SF0_b$, $SF1_{b1}$ to $SF1_{b4}$, $SF2_{b1}$ to $SF2_{b4}$, $SF3_{b1}$ to $SF3_{b4}$, $SF4_{b1}$ to $SF4_{b4}$) in the latter half section thereof, as shown in Fig. 5 and Fig. 6.

[0055] Therefore this line dither processing has two chances in the third to fifth grayscale drive to change the status of the discharge cell from light ON status to light OFF status within the unit display period (indicated by a double circle) as shown in Fig. 6. In other words, since the frequency of the discharge cell switching from light ON status to light OFF status is twice as much as the vertical synchronizing frequency, a good display with suppressed flickers can be performed even if an input video signal with low vertical synchronizing frequency such as PAL type television signal is supplied.

[0056] Further in this line dither processing, as shown in Fig. 6, sustain-discharge for emission is performed in both of the first half section and the latter half section of the unit display period for every grayscale in a manner that an emission period of one discharge cell belonging to one discharge line differs from that of another discharge cell belonging to another discharge line among a series of 8 discharge lines. In this case, relationship of the length of an emission period in the first half section to that in the latter half section is reversed between one discharge cell belonging to an even numbered display line and another discharge cell belonging to an odd numbered display line.

[0057] For example, as seen in the third grayscale driving case shown in Fig. 6, for a discharge cell in the (8N-7)th display line which is an odd numbered display line, sustain-discharge for emission with an emission period extending over 24 is performed separately by an emission period extending over 8 in the first half section and an emission period extending over 16 in the latter half section as shown in Fig. 8. For a discharge cell on the (8N-6)th display line which is an even numbered display line, sustain-discharge emission with an emission period extending over 22 is performed separately by an emission period extending over 15 in the first half section and an emission period extending over 7 in the latter half section, as shown in Fig. 8. For a discharge cell in the (8N-5)th display line which is an odd numbered display line, the sustain-discharge emission with an emission period extending over 20 is performed separately by an emission period extending over 6 in the first half section and an emission period extending over 14 in the latter half section, as shown in Fig. 8. For discharge cells in the (8N-4)th display line which is an even numbered display line, sustain-discharge emission with an emission period extending over 18 is performed separately by an emission period extending over 13 in the first half section and an emission period extending over 5 in the latter half section, as shown in Fig. 8. For discharge cells in the (8N-3)th display line which is an odd numbered display line, the sustain-discharge emission with an emission period extending over 16 is performed separately by an emission period extending over 4 in the first half section and an emission period extending over 12 in the latter half section, as shown in Fig. 8. For a discharge cell in the (8N-2)th display line which is an even numbered display line, sustain-discharge emission with an emission period extending over 14 is performed separately by an emission period extending over 11 in the first half section and an emission period extending over 3 in the latter half section, as shown in Fig. 8. For a discharge cell in the (8N-1)th display line which is an odd numbered display line, sustain-discharge emission with an emission period extending over 12 is performed separately by an emission period extending over 2 in the first half section and an emission period extending over 10 in the latter half section, as shown in Fig. 8. For a discharge cell in the (8N)th display line which is an even numbered display line, sustain-discharge emission with an emission period extending over 10 is performed separately by an emission period extending over 9 in the first half section and an emission period extending over 1 in the latter half section, as shown in Fig. 8.

[0058] In other words, in the case of the line dither processing, when the continuous sustain-discharge for emission of the discharge cell is separated into the first half section and latter half section within the unit display period, relationship of the length of an emission period in the first half section to that in the latter half section is reversed between one discharge cell belonging to one

display line and another discharge cell belonging to adjacent display line among a display line group.

[0059] Therefore emission patterns of a series of 8 display lines, which are different from the line dither pattern corresponding to the brightness weight value fixedly assigned to the 8 display lines, differs to each other within a unit display period, and therefore the generation of a line dither pattern can be suppressed.

[0060] As a consequence, according to the plasma display device shown in Fig. 1, a good image display with suppressed line dither patterns and flickers can be performed even if an input video signal with a low vertical synchronizing frequency is supplied.

[0061] In the above embodiment, as shown in Fig. 6, the relationship of the length of the emission period in the first half section to that in the and latter half section within the unit display period is reversed between one discharge cell belonging to an even numbered display line and another discharge cell belonging to an odd numbered display line, however above relationship may be reversed in a different manner. For example, the relationship of the length of the emission period in the first half section to that in the latter half section within the unit display period may be reversed between adjacent display line units each having paired or tripled display lines, where such relationship are the same among display lines within each display line unit.

[0062] In short, a series of display lines may by arranged in a manner that one adjacent display line pair has such feature that relationship of the length of the emission period in the first half section to that in the latter half section within the unit display period is reversed between such adjacent display lines, whereas another adjacent display line pair has such feature that relationship of the length of the emission period in the first half section to that in the latter half section within the unit display period is the same between such adjacent display lines.

[0063] This application is based on a Japanese patent application No. 2005-259095 which is herein incorporated by reference.

Claims

1. A method for driving a display panel having a plurality of display lines each provided with a plurality of pixel cells, said pixel cells are driven by a plurality of subfields within each unit display period, said method comprising:

   a drive step for respectively assigning different brightness weight values to a series of M (M is an integer of 2 or higher) display lines belonging to each of display line groups, and for emitting said pixel cells based on said brightness weight values such that an emission period of a pixel cell belonging to one display line differs from that of another pixel cell belonging to another display line among said M display lines,

   wherein said drive step comprises a first half drive step for executing emission of a first period out of said emission period in a first half section of said unit display period, and a latter half drive step for executing emission of a remaining second period out of said emission period in a latter half section of said unit display period, and

   relationship of a length of said first period to a length of said second period is reversed between one pixel cell belonging to one display line and another pixel cell belonging to another display line among said display line group.

2. The method for driving a display panel according to Claim 1, wherein said first half drive step includes a first half address step in said first half section for sequentially selecting every Mth of said display lines arranged in said display panel, and for setting a pixel cell belonging to said selected display line to a drive mode in accordance with pixel data of an input video signal, and an emission step for emitting only a pixel cell of light ON mode immediately before said first half address step for a period corresponding to a predetermined weighted value, and

   said latter half drive step includes a latter half address step in said latter half section for sequentially selecting every Mth of said display lines arranged in said display panel, and for setting a pixel cell belonging to said selected display line to a drive mode in accordance with pixel data of an input video signal, and an emission step for emitting only a pixel cell of light ON mode immediately before said latter address steps for a period corresponding to a predetermined weighted value.

3. The method for driving a display panel according to Claim 2, wherein said first half address step and said emission step are repeated M1 times within said first half drive step, and said first half address step and said emission step are repeated M2 times within said latter half drive step, where M1 plus M2 equals M.

4. A method for driving a display panel having a plurality of display lines each provided with a plurality of pixel cells, said display panel is driven to display grayscale by a plurality of subfields in each unit display period in accordance with an input video signal, the method comprising:

   emitting one pixel cell belonging to one display line by P subfields (P is an integer) continuously placed in a first half section of said unit display period and by Q subfields (Q is an integer less than P) continuously placed in a latter half section of said unit display period, and emitting another pixel cell belonging to another display line adjacent to said one display line by Q subfields

continuously placed in the first half section of said unit display period and by P subfields continuously placed in the latter half section of said unit display period, when the Kth grayscale display is performed, and

emitting one pixel cell belonging to said one display line by said P subfields similar to said Kth grayscale display in the first half section of said unit display period, and by said Q subfields similar to said Kth grayscale display in the latter half section of said unit display period and by L subsequent subfields, and emitting said another pixel cell belonging to said another display line adjacent to said one display line by said P subfields similar to said Kth grayscale display and L subsequent subfields in the first half section of said unit display period, and by said P subfields similar to said Kth grayscale display, when (K+1)th grayscale is displayed.

5. The method for driving a display panel according to Claim 4, wherein said display lines are divided into display line groups each including a series of T display lines (T is an integer of 2 or higher), and different brightness weighting values are respectively assigned to said series of T display lines.

6. The method for driving a display panel according to Claim 4, wherein in the first half section and latter half section within said unit display period, all of said pixel cells are initialized to light ON mode in a subfield placed at the beginning of said first half section and latter half section and then each of said pixel cells is repeatedly emitted in a subsequent subfield for a period corresponding to a brightness weighted value of said subsequent subfield until said pixel cell is shifted to light OFF mode.

7. The method for driving a display panel according to Claim 6, wherein as brightness level to be represented in a pixel cell becomes higher, the number of subfields increases which perform continuous emission of a pixel cell from the beginning of said first half section and said latter half section.

FIG. 1

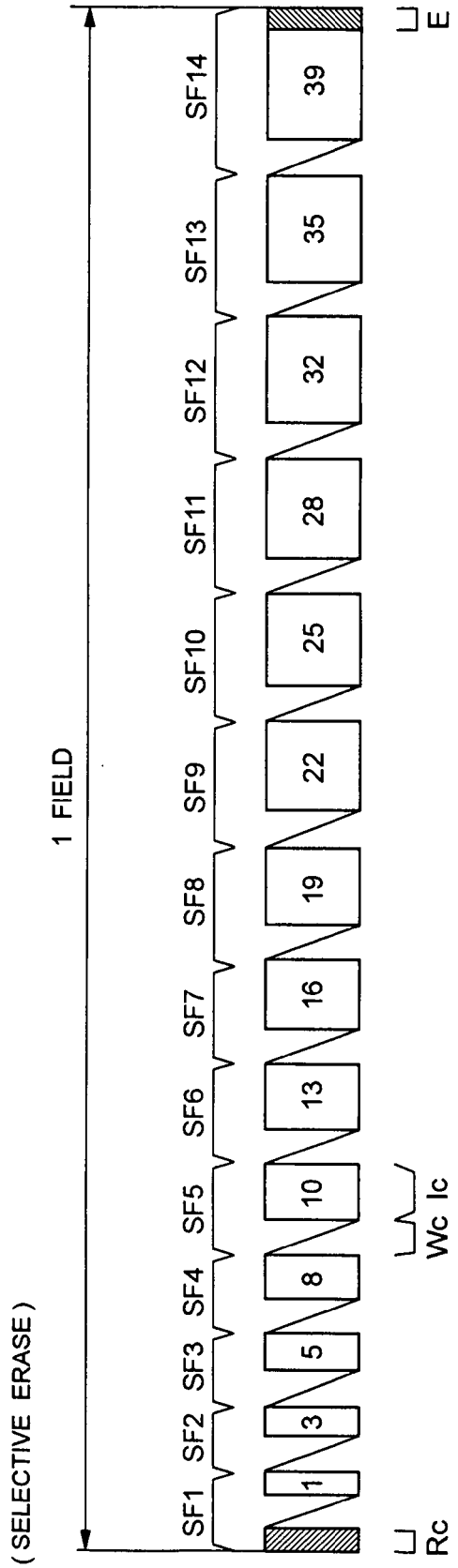

1 FIELD
(SELECTIVE ERASE)
SF1
SF2
SF3
SF4
SF5
SF6
SF7
SF8
SF9
SF10
SF11
SF12
SF13
SF14
1
3
5
8
10
13
16
19
22
25
28
32
35
39
Rc
Wc
Ic
E

FIG. 2

(SELECTIVE ERASE)

Ds	HD														EMISSION DRIVE PATTERN IN ONE FIELD														EMISSION BRIGHTNESS
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	SF 1	SF 2	SF 3	SF 4	SF 5	SF 6	SF 7	SF 8	SF 9	SF 10	SF 11	SF 12	SF 13	SF 14	
0000	1	0	0	0	0	0	0	0	0	0	0	0	0	0	●														0
0001	0	1	0	0	0	0	0	0	0	0	0	0	0	0	○	●													1
0010	0	0	1	0	0	0	0	0	0	0	0	0	0	0	○	○	●												4
0011	0	0	0	1	0	0	0	0	0	0	0	0	0	0	○	○	○	●											9
0100	0	0	0	0	1	0	0	0	0	0	0	0	0	0	○	○	○	○	●										17
0101	0	0	0	0	0	1	0	0	0	0	0	0	0	0	○	○	○	○	○	●									27
0110	0	0	0	0	0	0	1	0	0	0	0	0	0	0	○	○	○	○	○	○	●								40
0111	0	0	0	0	0	0	0	1	0	0	0	0	0	0	○	○	○	○	○	○	○	●							56
1000	0	0	0	0	0	0	0	0	1	0	0	0	0	0	○	○	○	○	○	○	○	○	●						75
1001	0	0	0	0	0	0	0	0	0	1	0	0	0	0	○	○	○	○	○	○	○	○	○	●					97
1010	0	0	0	0	0	0	0	0	0	0	1	0	0	0	○	○	○	○	○	○	○	○	○	○	●				122
1011	0	0	0	0	0	0	0	0	0	0	0	1	0	0	○	○	○	○	○	○	○	○	○	○	○	●			150
1100	0	0	0	0	0	0	0	0	0	0	0	0	1	0	○	○	○	○	○	○	○	○	○	○	○	○	●		182
1101	0	0	0	0	0	0	0	0	0	0	0	0	0	1	○	○	○	○	○	○	○	○	○	○	○	○	○	●	217
1110	0	0	0	0	0	0	0	0	0	0	0	0	0	0	○	○	○	○	○	○	○	○	○	○	○	○	○	○	256

BLACK DOT : SELECTIVE ERASE DISCHARGE
WHITE CIRCLE : EMISSION

FIG. 3

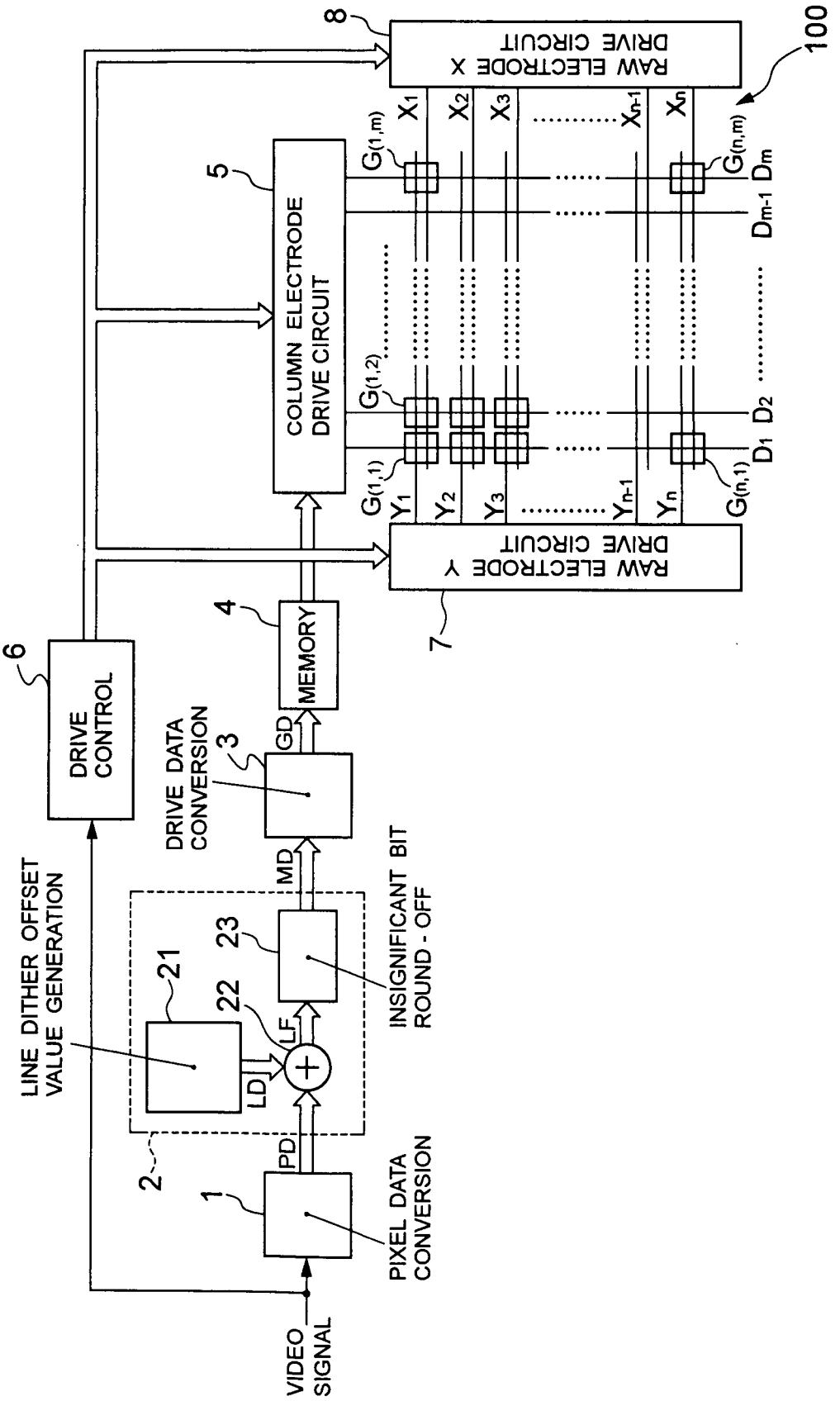

8
RAW ELECTRODE X DRIVE CIRCUIT
100
5
COLUMN ELECTRODE DRIVE CIRCUIT
RAW ELECTRODE Y DRIVE CIRCUIT
7
4
MEMORY
6
DRIVE CONTROL
DRIVE DATA CONVERSION
3
GD
MD
LINE DITHER OFFSET VALUE GENERATION
INSIGNIFICANT BIT ROUND - OFF
21
22
23
LF
LD
2
1
PD
PIXEL DATA CONVERSION
VIDEO SIGNAL
X1
X2
X3
Xn-1
Xn
Y1
Y2
Y3
Yn-1
Yn
G(1,m)
G(n,m)
G(1,2)
G(1,1)
G(n,1)
Dm
Dm-1
D2
D1

FIG. 4

DATA CONVERSION TABLE						
MD	GD					
	1	2	3	4	5	6
000	1	1	0	0	0	0
001	0	1	1	0	0	0
010	0	0	1	1	0	0
011	0	0	0	1	1	0
100	0	0	0	0	1	1
101	0	0	0	0	0	0

FIG. 5

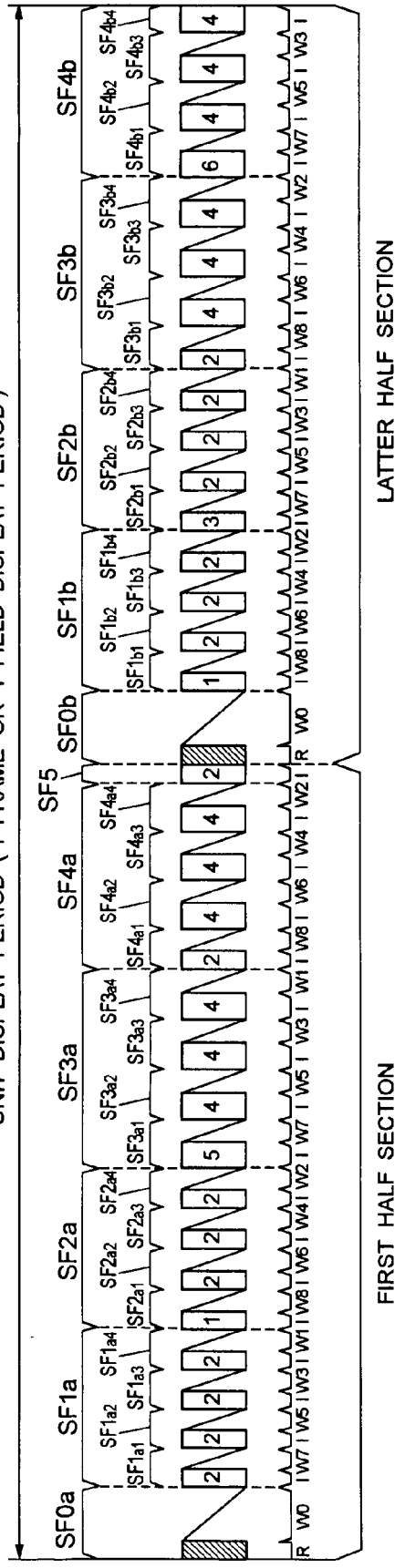

UNIT DISPLAY PERIOD (1 FRAME OR 1 FIELD DISPLAY PERIOD)
SF0a
SF1a
SF2a
SF3a
SF4a
SF5
SF0b
SF1b
SF2b
SF3b
SF4b
FIRST HALF SECTION
LATTER HALF SECTION

FIG. 6

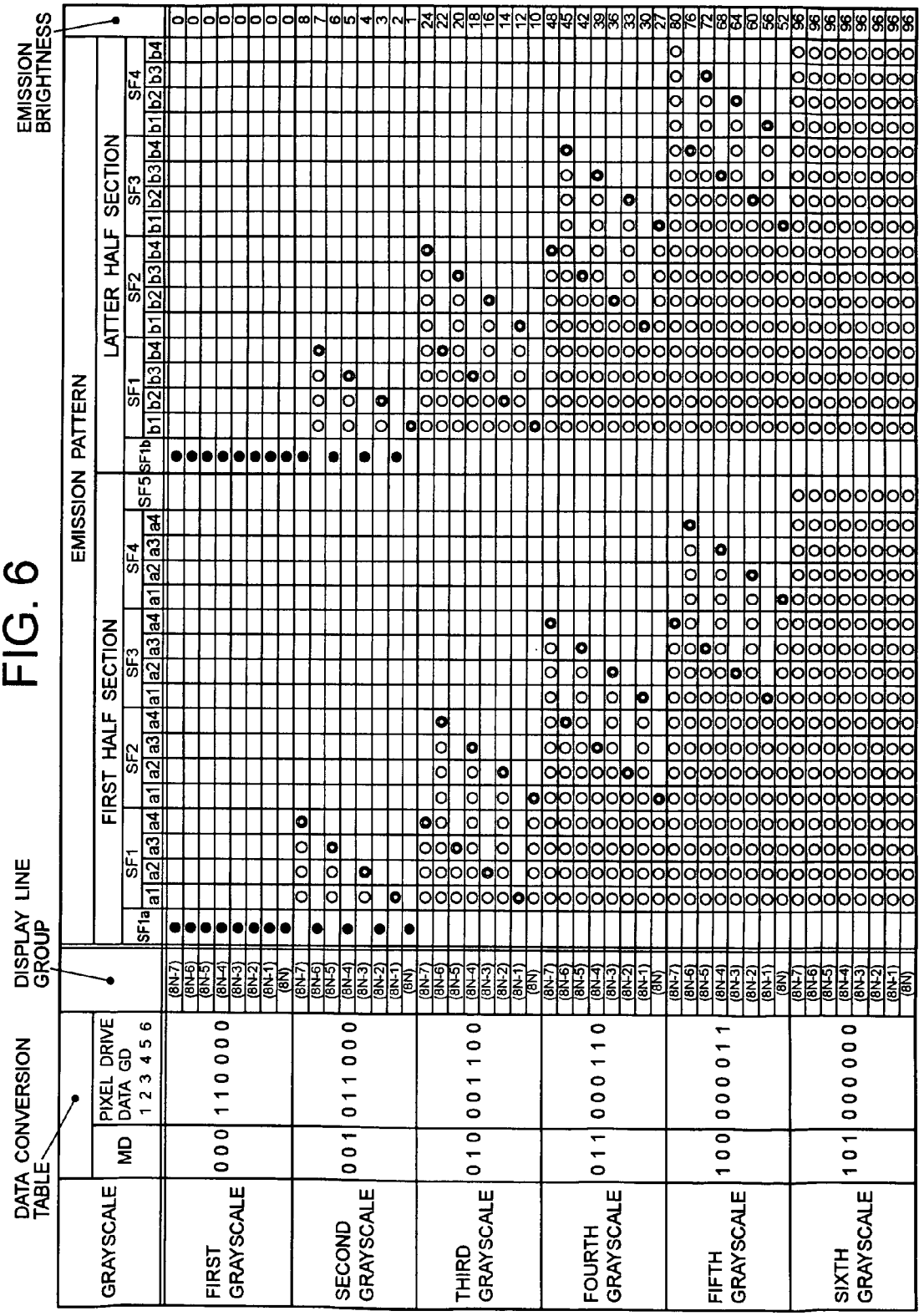
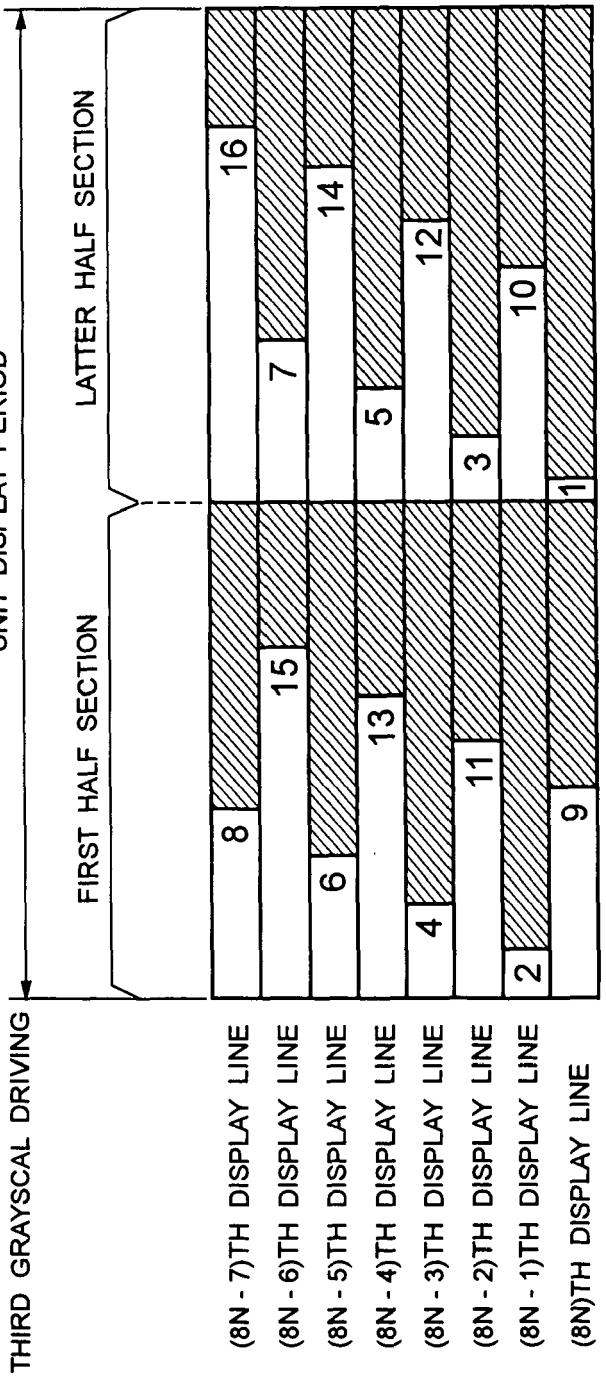

DATA CONVERSION TABLE
DISPLAY LINE GROUP
EMISSION BRIGHTNESS
GRAYSCALE
MD
PIXEL DRIVE DATA GD 1 2 3 4 5 6
EMISSION PATTERN
FIRST HALF SECTION
LATTER HALF SECTION
SF1
SF2
SF3
SF4
SF5
SF1a
SF1b
a1 a2 a3 a4
b1 b2 b3 b4
FIRST GRAYSCALE
SECOND GRAYSCALE
THIRD GRAYSCALE
FOURTH GRAYSCALE
FIFTH GRAYSCALE
SIXTH GRAYSCALE
● SELECTIVE ERASE
○ SUSTAIN DISCHARGE EMISSION
⊕ SELECTIVE ERASE + SUSTAIN DISCHARGE EMISSION

FIG. 7


FIRST GRAYSCALE
SECOND GRAYSCALE
THIRD GRAYSCALE
FOURTH GRAYSCALE
FIFTH GRAYSCALE
SIXTH GRAYSCALE
(8N - 7)TH DISPLAY LINE
(8N - 6)TH DISPLAY LINE
(8N - 5)TH DISPLAY LINE
(8N - 4)TH DISPLAY LINE
(8N - 3)TH DISPLAY LINE
(8N - 2)TH DISPLAY LINE
(8N - 1)TH DISPLAY LINE
(8N)TH DISPLAY LINE
0
1
2
3
4
5
6
7
8
10
12
14
16
18
20
22
24
27
30
33
36
39
42
45
48
52
56
60
64
68
72
76
80
96

FIG. 8


THIRD GRAYSCAL DRIVING
UNIT DISPLAY PERIOD
FIRST HALF SECTION
LATTER HALF SECTION
(8N - 7)TH DISPLAY LINE
(8N - 6)TH DISPLAY LINE
(8N - 5)TH DISPLAY LINE
(8N - 4)TH DISPLAY LINE
(8N - 3)TH DISPLAY LINE
(8N - 2)TH DISPLAY LINE
(8N - 1)TH DISPLAY LINE
(8N)TH DISPLAY LINE
8
15
6
13
4
11
2
9
16
7
14
5
12
3
10
1

REFERENCES CITED IN THE DESCRIPTION

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Patent documents cited in the description

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- JP 2005259095 A **[0063]**