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(54) **Systems and methods for generating reference voltages**

(57) Systems and methods for generating reference voltages are provided. A representative system comprises a resistor circuit (32); a first switch (SW1) coupled between a first end of the resistor circuit (C) and first power source (Vss); a second switch (SW2) coupled between the first end of the resistor circuit (C) and a second power source (Vcc); a third switch (SW3) coupled to a second end of the resistor circuit (D); a fourth switch (SW4) coupled to the second end of the resistor circuit (D); a first resistor (R1) coupled between the first end of the resistor circuit and the first switch; a second resistor (R2) coupled between the first end of the resistor circuit and the second switch; a third resistor (R3) coupled between the second end of the resistor circuit and the third switch; a fourth resistor (R4) coupled between the second end of the resistor circuit and the fourth switch; and a control circuit (34) for controlling the switches.

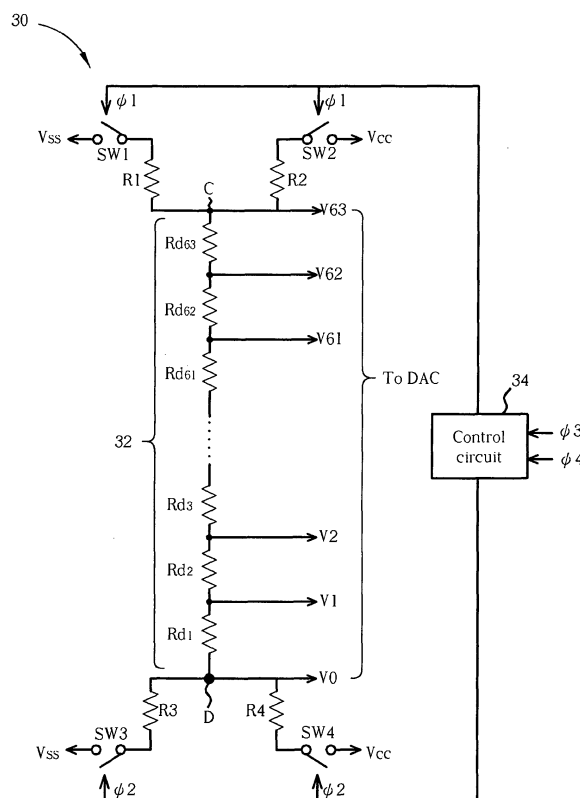


Fig. 3

Description

Background of the Invention

1. Field of the Invention

[0001] The present invention relates to electrical circuitry and, in particular, to systems and methods for generating reference voltages.

2. Description of the Prior Art

[0002] Active matrix liquid crystal displays (AMLCDs) are currently the leading flat-panel display technology. An AMLCD comprises a grid (or matrix) of picture elements (pixels). Thousands or millions of these pixels are used together to create an image on such a display. In a thin film transistor (TFT) panel design, TFT technology is used to build a tiny transistor switch and capacitor for each pixel in the AMLCD panel. TFTs act as switches to individually turn each pixel "on" (light) or "off" (dark). Besides the normal display mode in which an image is represented with full gradation, a display usually has several power-saving modes. For example, a display can have an n-gradation mode (where n is an integer smaller than the number of levels in full gradation) in which an image is represented with fewer gradations, a partial display mode in which only a portion of the display is used to represent an image, and/or a standby mode in which the display is turned off temporarily until being activated again.

[0003] Integrating driving (reference voltage generating) circuits into display panels using TFT technology can largely reduce display module cost. In order to have precise analog voltage control and to simplify circuit structures in the integrated reference voltage generating circuits, a conventional resistor string (R-string) approach is adopted for providing different voltages. Fig. 1 shows a prior art reference voltage generating circuit 10 disclosed in U.S. Patent No. 6,839,043 to Nakajima, which is incorporated herein by reference. The reference voltage generating circuit 10 includes switch circuits 41 and 42, dividing resistors R1-R7, and switches SW15 and SW16. The switch circuits 41 and 42 include switches SW11, SW12 and switches SW13, SW14, respectively. The switches SW11-SW14 couple output terminals A and B of the R-string to a positive power supply Vcc and a power supply Vss, which has a lower voltage level with respect to the positive power supply Vcc. The power supplies Vcc and Vss operate at fixed periods in opposite phases for row inversion driving methodology. The dividing resistors R1 to R7 are connected in series between output terminals A and B of the R-string, with switches SW15 and SW16 interposed therebetween, respectively. Voltages V0, V7, and V1-V6 obtained by voltage division by the R-string are outputted to a digital-analog-converter (DAC).

[0004] Reference is made to Fig. 2 for a timing chart

illustrating the operation of the reference voltage generating circuit 10. In the reference voltage generating circuit 10 of Fig. 1, the reference voltages V0 and V7 are both produced by connecting node A to the positive power supply Vcc and node B to the power supply Vss in a first driving period, and by connecting node B to the positive power supply Vcc and node A to the power supply Vss in a second driving period. Each such driving period alternates in a fixed interval based on control pulses $\phi 1$ and $\phi 2$, as shown in the timing chart of Fig. 2. Meanwhile, the reference voltages V1-V6 for intermediate gradations are produced by voltage division through the dividing resistors R1 to R7. During power-saving modes, the switches SW15 and SW16 are opened (switched off) to stop the supply of current to the dividing resistors R1-R7 based on control pulse $\phi 3$. As a result, since no current flows through the dividing resistors R1-R7 and power consumption by the dividing resistors R1 to R7 is eliminated, a reduction of the power consumption can be anticipated. Although the voltage levels of V1 and V6 are represented with flat lines of zero voltage in Fig. 2 during power saving modes, the prior art reference voltage generating circuit 10 actually produces floating voltages when the R-string is disconnected from power supplies Vcc and Vss.

[0005] The prior art reference voltage generating circuit 10 has two perceived major drawbacks. First, the switches SW15 and SW16 are used to disconnect the R-string from the power sources Vcc and Vss during power-saving modes. In contrast to metal-oxide semiconductor field-effect transistors (MOSFETs), which are made on silicon wafers and use bulk-silicon as an active layer, a TFT is a transistor the active, current-carrying layer of which is a thin film (usually a film of polysilicon). Thus, the resistance of a TFT is usually much larger than that of a MOSFET. In order to achieve fast turn-on time and small voltage drop across switches for the reference voltage generating circuit 10, the switches SW15 and SW16 typically are large enough to exhibit low turn-on resistance. As a result, the reference voltage generating circuit 10 occupies a large amount of space. Second, since the R-string is disconnected from the power sources Vcc and Vss, the release voltage generating circuit 10 exhibits floating voltage levels that are outputted to the DAC during power-saving modes. This tends to result in the DAC operation being non-stable and can result in more power consumption.

Summary of the Invention

[0006] Systems and methods for generating reference voltages are provided.

[0007] An embodiment of such a system comprises an integrated reference voltage generating circuit comprising a resistor circuit comprising a plurality of resistors coupled in series, a first switch coupled between a first end of the resistor circuit and a first power source, a second switch coupled between the first end of the resistor

circuit and a second power source, a third switch coupled to a second end of the resistor circuit, a fourth switch coupled to the second end of the resistor circuit, a first resistor coupled between the first end of the resistor circuit and the first switch, a second resistor coupled between the first end of the resistor circuit and the second switch, a third resistor coupled between the second end of the resistor circuit and the third switch, a fourth resistor coupled between the second end of the resistor circuit and the fourth switch, and a control circuit for controlling the first, second, third, and fourth switches.

[0008] Another embodiment of a system comprises an integrated reference voltage generating circuit, a multiplexer for selecting from input data obtained in different operating modes as output data of the system, a digital-to-analog controller coupled to the multiplexer and the integrated reference voltage generating circuit for processing input data of an image displayed with full gradation, and a control circuit for sending signals to the integrated reference voltage generating circuit and the multiplexer based on an operating mode of the system.

[0009] An embodiment of a method for generating reference voltages comprises providing a resistor circuit comprising a plurality of resistors coupled in series, coupling first and second ends of the resistor circuit to a same power source when displaying an image with reduced power, and coupling the first end of the resistor circuit to a first power source and the second end of the resistor circuit to a second power source when displaying an image with full gradation. These and other objectives of the present invention will no doubt become obvious to those of ordinary skill in the art after reading the following detailed description of the preferred embodiment that is illustrated in the various figures and drawings.

Brief Description of the Drawings

[0010]

Fig. 1 shows a prior art reference voltage generating circuit.

Fig. 2 is a timing chart illustrating the operation of the reference voltage generating circuit in Fig. 1.

Fig. 3 shows an embodiment of an integrated reference voltage generating circuit.

Fig. 4 is a timing chart illustrating the operation of the integrated reference voltage generating circuit in Fig. 3.

Fig. 5 shows an equivalent circuit of a prior art pixel.

Fig. 6 shows a graph illustrating the charge-injection effect.

Fig. 7 shows an integrated reference voltage generating circuit according to a second embodiment of the present invention.

Fig. 8 is a functional block diagram of an embodiment of a display system incorporating an embodiment of an integrated reference voltage generating circuit.

Detailed Description

[0011] Systems and methods for generating reference voltages are provided. Some embodiments can potentially reduce power consumption and/or compensate for charge injection effect. As such, some embodiments may be well suited for use in display systems, such as panel displays.

[0012] In this regard, reference is made to Fig. 3 which depicts an embodiment of an integrated reference voltage generating circuit 30. The integrated reference voltage generating circuit 30 includes a resistor circuit 32, switches SW1-SW4, resistors R1-R4, voltage sources Vcc and Vss, and a control circuit 34. The power sources Vcc provide higher voltages than the power sources Vss. The resistor circuit 32 includes a plurality of dividing resistors Rd1-Rd63 coupled in series. The switch SW1 is coupled between node C of the resistor circuit 32 and the power source Vss, the switch SW2 is coupled between node C of the resistor circuit 32 and the power source Vcc, the switch SW3 is coupled between node D of the resistor circuit 32 and the power source Vss, and the switch SW4 is coupled between node D of the resistor circuit 32 and the power source Vcc. The resistor R1 is coupled between node C of the resistor circuit 32 and the switch SW1, the resistor R2 is coupled between node C of the resistor circuit 32 and the switch SW2, the resistor R3 is coupled between node D of the resistor circuit 32 and the switch SW3, and the resistor R4 is coupled between node D of the resistor circuit 32 and the switch SW4. The integrated reference voltage generating circuit 30 provides reference voltages by voltage division of the resistor circuit 32.

In the embodiment shown in Fig. 3, the integrated reference voltage generating circuit 30 provides reference voltages V0-V63 between two adjacent dividing resistors of the resistor circuit 32. The switches SW1-SW4 are turned on or off based on signals generated by the control circuit 34. The switches SW1-SW4 can be made of transistors of different doping types. For example, the switches SW1 and SW3 can be N-type transistors, and the switches SW2 and SW4 can be P-type transistors, or vice versa. If the switches SW1 and SW3 are N-type transistors and the switches SW2 and SW4 are P-type transistors, the switches SW1 and SW3 are turned on (closed circuit) and the switches SW2 and SW4 are turned off (open circuit) when receiving a control signal of "1" (high voltage level), and the switches SW1 and SW3 are turned off and the switches SW2 and SW4 are turned on when receiving a control signal of "0" (low voltage level).

[0013] With reference to Fig. 4, the operation of the integrated reference voltage generating circuit 30 will be described. In Fig. 4, $\phi 1$ - $\phi 4$ represent control pulses, each with two states: high and low. For ease of explanation, only reference voltages V0, V1, V62 and V63 are shown for illustrating the operation of the integrated reference voltage generating circuit 30 during the normal mode and the power saving modes. To prevent electroplating of ion

impurity and image retention of the liquid crystal (LC) material, the polarity of the LC cell voltage is reversed on alternative intervals. The reference voltage V0 and V63 are both produced by coupling node C of the resistor circuit 32 to the power supply Vcc and node D of the resistor circuit 32 to the power supply Vss in a first driving period, and by coupling node C of the resistor circuit 32 to the power supply Vss and node D of the resistor circuit 32 to the power supply Vcc in a second driving period. Each such driving period alternates in a fixed interval based on control pulses $\phi 1$ and $\phi 2$, as shown in a timing chart of Fig. 4. In the normal display mode, the control circuit 34 provides a control pulse $\phi 4$ of alternating high and low levels at the fixed interval and a control pulse $\phi 3$ of high level, and therefore generates control pulses $\phi 1$ and $\phi 2$ for the switches SW1-SW4, as shown in Fig. 4. In the first driving interval, the resistor circuit 32 is coupled to power sources Vcc and Vss through the switches SW4 and SW1, respectively. In the second driving interval, the resistor circuit 32 is coupled to power sources Vcc and Vss through the switches SW2 and SW3, respectively. Intermediate reference voltages V1-V62 are generated by voltage division by the dividing resistors Rd1-Rd63 of the resistor circuit 32.

[0014] During the power-saving mode, the control pulse $\phi 3$ switches to low level and the control pulse $\phi 4$ remains unchanged as in the normal mode, thereby generating the control signals $\phi 1$ and $\phi 2$ each having a high level. Consequently, the switches SW2 and SW4 are turned off, disconnecting the resistor circuit 32 from the power source Vcc. At the same time, the switches SW1 and SW3 are turned on, coupling the resistor circuit 32 to the power source Vss. Therefore, during the power-saving mode, no current flows through the resistor circuit 32 and the power consumption from the driving resistors can be reduced. Although no current flows through the resistor circuit 32, both ends of the resistor circuit 32 are still coupled to Vss during the power-saving mode. In contrast to floating voltages of the prior art reference voltage generating circuit 10, the voltage of the entire resistor circuit 32 is fixed to Vss during the power saving mode thereby shutting down DAC operation in a stable way. Therefore, the integrated reference voltage generating circuit 30 can reduce power consumption without occupying large circuit space and without influencing the stability of the DAC during power-saving mode.

[0015] Fig. 5 is a diagram showing an equivalent circuit of a pixel 50. The pixel 50 includes a TFT for turning on and off the pixel 50, a storage capacitor Cst for data storage, and a liquid crystal capacitor Clc representing the capacitance of the liquid crystal material. Data sent to the pixel 50 is stored in the capacitors Cst and Clc. The parasitic capacitance of the pixel 50 is represented by a parasitic capacitor Cgd. A signal from a gate line turns on the TFT, allowing data sent from a data line to be stored in the capacitors Cst and Clc. Usually reference voltages generated by an integrated reference voltage generating circuit are sent to a DAC, which in turn selects

a voltage from the reference voltages and sends the selected voltage to the data line.

[0016] The charge-injection effect is a phenomenon of level change caused by stray capacitance represented by the parasitic capacitor Cgd. In this regard, Fig. 6 is a diagram illustrating the charge-injection effect. In Fig. 6, Vgate represents the voltage sent to the gate line, Vpixel (dashed line) represents the ideal voltage obtained across the capacitors Cst and Clc if a voltage of Vp is sent to the data line and Vpixel' represents the actual voltage obtained across the capacitors Cst and Clc if a voltage of Vp is sent to the data line. Due to charge-injection effect, Vpixel' differs from Vpixel

in that it suffers a voltage drop ΔVp , potentially causing loss of data stored in the capacitors Cst and Clc. The voltage drop ΔVp is represented as follows:

$$\Delta Vp = \Delta Vg \times \frac{Cgd}{Cgd + Clc + Cs}$$

[0017] Embodiments of an integrated reference voltage generating circuit, such as circuit 30, can potentially compensate for the charge-injection effect using the resistors R1- R4. Based on capacitance of the capacitors Cst, Clc and Cgd, the voltage drop ΔVp can be calculated. Through the resistors R1-R4, different voltages can therefore be provided at both ends of the resistor circuit 32 for compensating for the voltage drop ΔVp . The resistance of the resistors R1-R4 depends on the value of ΔVp . In the integrated reference voltage generating circuit 30 of the present invention, the resistors R1 and R4 have the same resistance, and the resistors R2 and R3 have the same resistance.

[0018] Fig. 7 is another embodiment of an integrated reference voltage generating circuit 70. The integrated reference voltage generating circuit 70 includes a resistor circuit 32, switches SW1-SW4, resistors R1-R4, voltage sources Vcc and Vss, and a control circuit 34. The power sources Vcc provide higher voltages than the power sources Vss. The resistor circuit 32 includes a plurality of dividing resistors Rd1-Rd63 coupled in series. Notably, the integrated reference voltage generating circuit 70 differs from the prior art voltage generating circuit 10, at least in one respect, in that it includes resistors R1-R4 for compensating for the charge-injection effect.

[0019] Fig. 8 is a schematic diagram of an embodiment of a display system 80 incorporating embodiments of integrated reference voltage generating circuit. The display system 80 of Fig. 8 includes MUX devices 81 and 82, a buffer 83, a control circuit 84, a timing controller 85, a DAC 87 and a reference generating circuit 89. The reference generating circuit 89 could be configured as the integrated reference generating circuits 30 and 70 shown in Fig. 3 and 7, for example, for providing reference voltages to the DAC 87. Based on signals sent from the con-

trol circuit 84, the MUX device 81 selects from partial display mode input data, 8-color mode input data or normal mode input data as output data. When operating in normal mode, the reference generating circuit 89 performs voltage division and provides the DAC 87 a plurality of reference voltages. The MUX device 81 then selects the normal mode input data having been processed by the DAC 87 and the buffer 83 as the output data. When operating in power-saving modes, such as partial display mode and 8-color mode, the resistor circuit adopted in the reference generating circuit 89 either has both ends coupled to a power source (such as when using the integrated reference generating circuits 30) or disconnected from a power source (such as when using the integrated reference generating circuits 70). The MUX device 81 then selects the partial display mode input data or the 8-color mode input data as the output data.

[0020] Integrated reference voltage generating circuits can potentially occupy less circuit space than prior art structures.

[0021] Those skilled in the art will readily observe that numerous modifications and alterations of the device and method may be made while retaining the teachings of the invention. Accordingly, the above disclosure should be construed as limited only by the metes and bounds of the appended claims.

Claims

1. A system for generating reference voltages comprising:

an integrated reference voltage generating circuit comprising:

a resistor circuit comprising a plurality of resistors coupled in series;
a first switch coupled between a first end of the resistor circuit and a first power source;
a second switch coupled between the first end of the resistor circuit and a second power source;
a third switch coupled to a second end of the resistor circuit;
a fourth switch coupled to the second end of the resistor circuit;
a first resistor coupled between the first end of the resistor circuit and the first switch;
a second resistor coupled between the first end of the resistor circuit and the second switch;
a third resistor coupled between the second end of the resistor circuit and the third switch;
a fourth resistor coupled between the second end of the resistor circuit and the fourth switch; and

a control circuit for controlling the first, second, third, and fourth switches.

2. The system of claim 1 further comprising the first and second sources; and wherein the first and the second power sources are voltage sources, the first power source having a voltage level lower than that of the second power source.

3. The system of claim 1 further comprising the first and second power sources; and wherein the first power source is a positive voltage source and the second power source is a negative voltage source.

4. The system of claim 1 further comprising the first and second power sources; and wherein the third switch is coupled to the first power source.

5. The system of claim 1 further comprising the first and second power sources; and wherein the fourth switch is coupled to the second power source.

6. The system of claim 2 further comprising a first power source and a second power source; and wherein the third switch is coupled to a first voltage source and the fourth switch is coupled to a second voltage source, wherein a voltage difference between the first and second voltage sources is the same as a voltage difference between the first and second power sources.

7. The system of claim 1 wherein the first and third switches are N-type transistors and the second and the fourth switches are P-type transistors.

8. The system of claim 1 further comprising:

a fifth switch having a first end coupled to the first end of the resistor circuit, and a second end coupled to the first and second resistors; and
a sixth switch having a first end coupled to the second end of the resistor circuit, and a second end coupled to the third and fourth resistors.

9. A system for generating reference voltages comprising:

an integrated reference voltage generating circuit comprising:

a resistor circuit comprising a plurality of resistors coupled in series;
a first switch coupled between a first end of the resistor circuit and a first power source;
a second switch coupled between the first end of the resistor circuit and a second power source;
a third switch coupled to a second end of

- the resistor circuit;
 a fourth switch coupled to the second end of the resistor circuit;
 a first resistor coupled between the first end of the resistor circuit and the first switch;
 a second resistor coupled between the first end of the resistor circuit and the second switch;
 a third resistor coupled between the second end of the resistor circuit and the third switch;
 a fourth resistor coupled between the second end of the resistor circuit and the fourth switch;
 a control circuit for controlling the first, second, third, and fourth switches; a multiplexer for selecting from input data obtained in different operating modes as output data of the system;
- a digital-to-analog controller coupled to the multiplexer and the integrated reference voltage generating circuit for processing input data of an image displayed with full gradation; and
 a control circuit for sending signals to the integrated reference voltage generating circuit and the multiplexer based on an operating mode of the system, wherein the system is operative to display images.
10. The system of claim 9 wherein the multiplexer selects from input data displayed with full gradation, in a partial display mode or in an 8-color mode as output data of the system.
 11. The system of claim 9 further comprising a buffer coupled between the digital-to-analog controller and the multiplexer.
 12. The system of claim 11 further comprising a timing controller coupled between the buffer, the control circuit and the integrated reference voltage generating circuit.
 13. The system of claim 9, wherein the system comprises a pixel display device and the reference voltage generator circuit is incorporated therein.
 14. The system of claim 13, wherein the pixel display is an active matrix liquid crystal display.
 15. A method for generating reference voltages comprising:

providing a resistor circuit comprising a plurality of resistors coupled in series; coupling first and second ends of the resistor circuit to a same power source when displaying an image with
 - reduced power; and
 coupling the first end of the resistor circuit to a first power source and the second end of the resistor circuit to a second power source when displaying an image with full gradation.
 16. The method of claim 15 wherein coupling first and second ends comprises coupling the first and second ends of the resistor circuit to a negative voltage source when displaying an image with reduced power.
 17. The method of claim 15 wherein coupling the first end comprises coupling the first end of the resistor circuit to a positive voltage source and the second end of the resistor circuit to a negative voltage when displaying an image with full gradation.
 18. The method of claim 15 wherein coupling the first end comprises coupling the first end of the resistor circuit to the first power source through a first resistor and the second end of the resistor circuit to the second power source through a second resistor when displaying an image with full gradation for compensating for a charge-injection effect.
 19. The method of claim 18 wherein coupling the first end comprises coupling the first end of the resistor circuit to a positive voltage source through the first resistor and the second end of the resistor circuit to a negative voltage through the second resistor when displaying an image with full gradation.
 20. The method of claim 15 further comprising providing a voltage established between two adjacent resistors of the resistor circuit to a digital-to-analog controller.

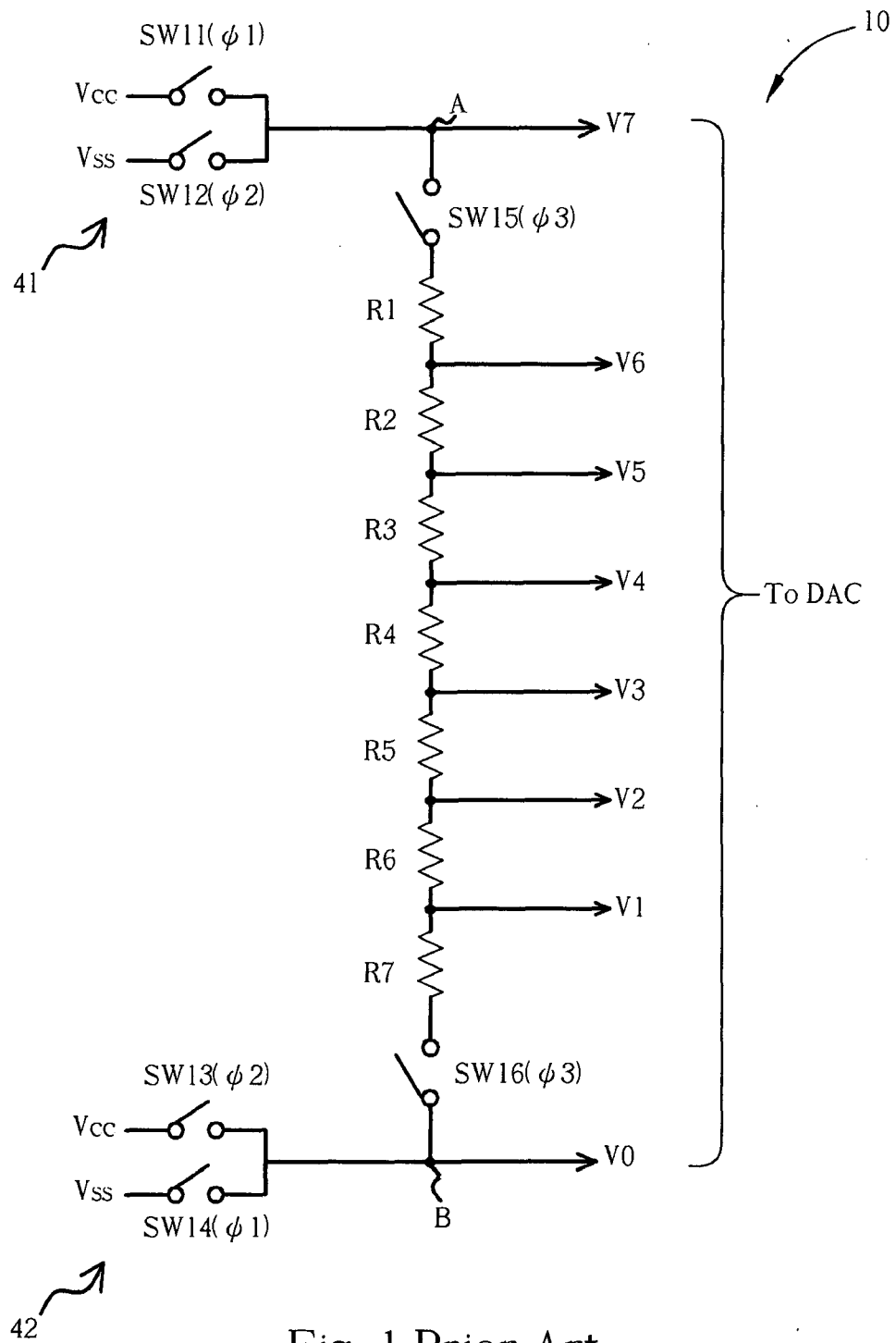


Fig. 1 Prior Art

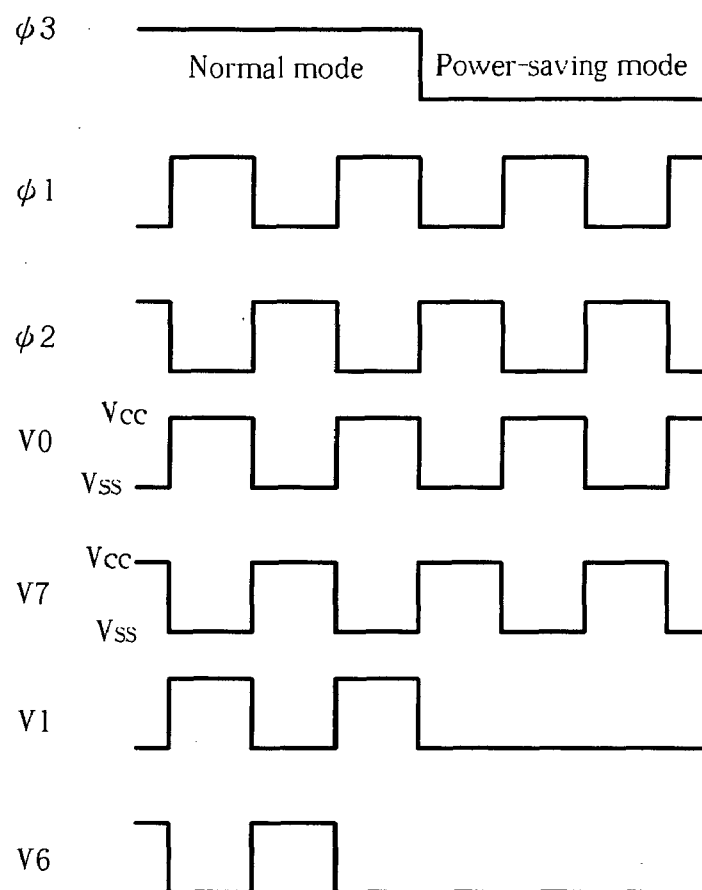


Fig. 2 Prior Art

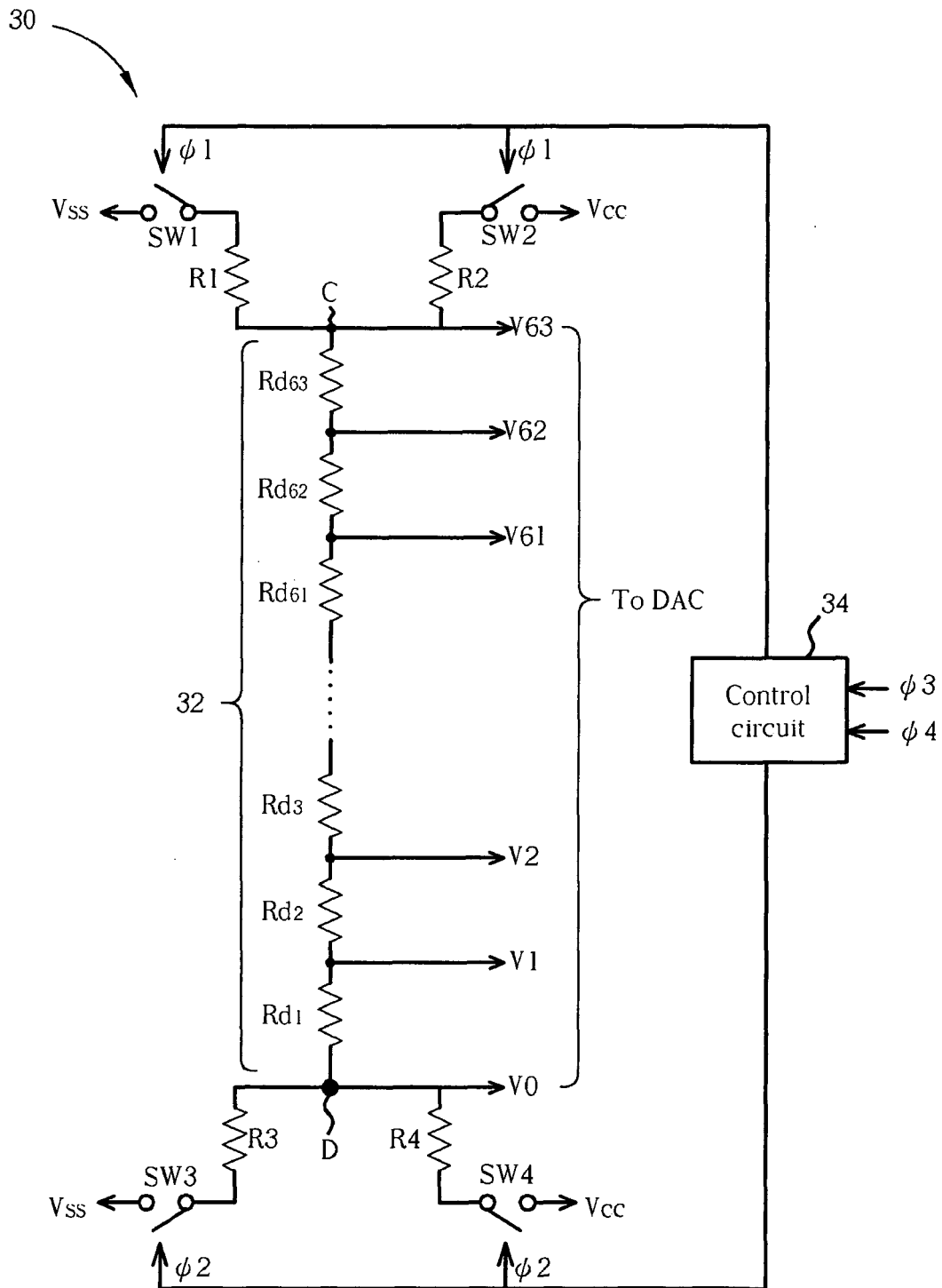


Fig. 3

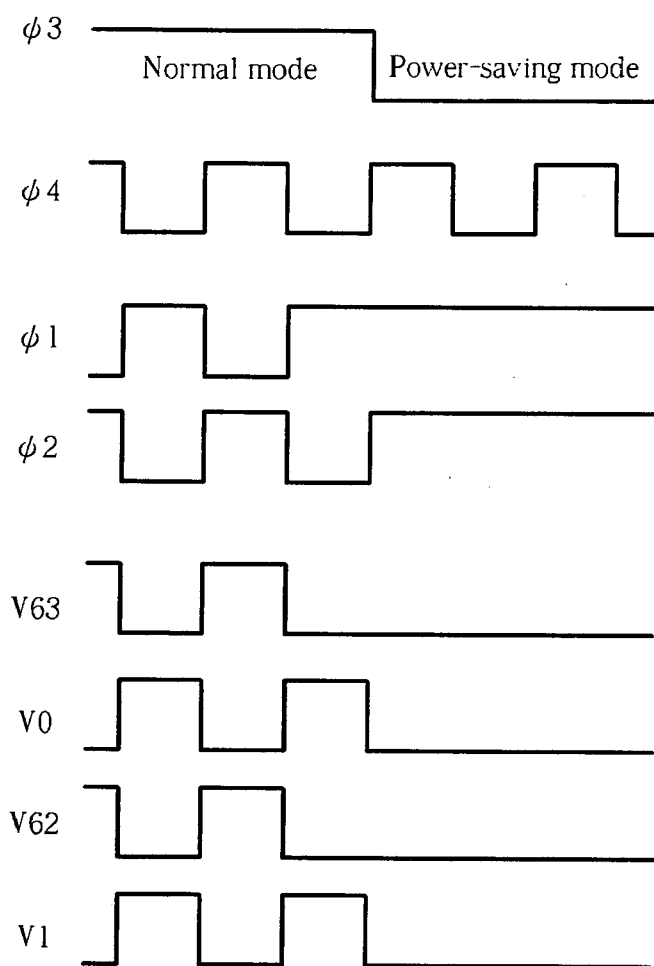


Fig. 4

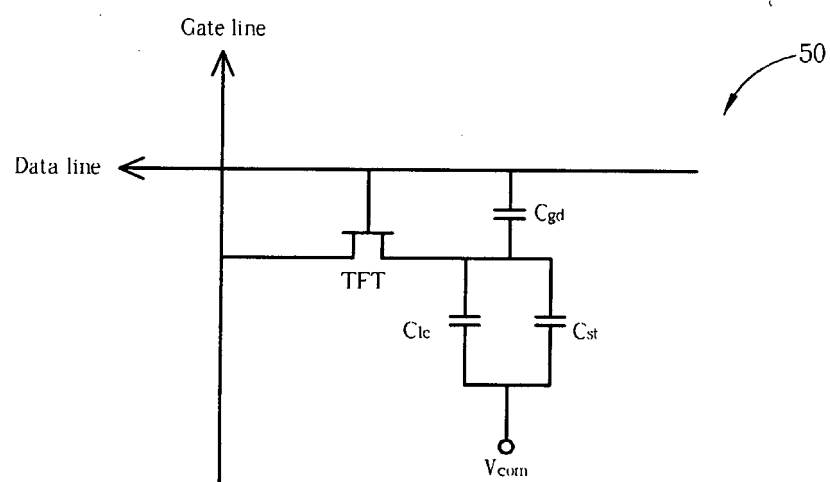


Fig. 5 Prior Art

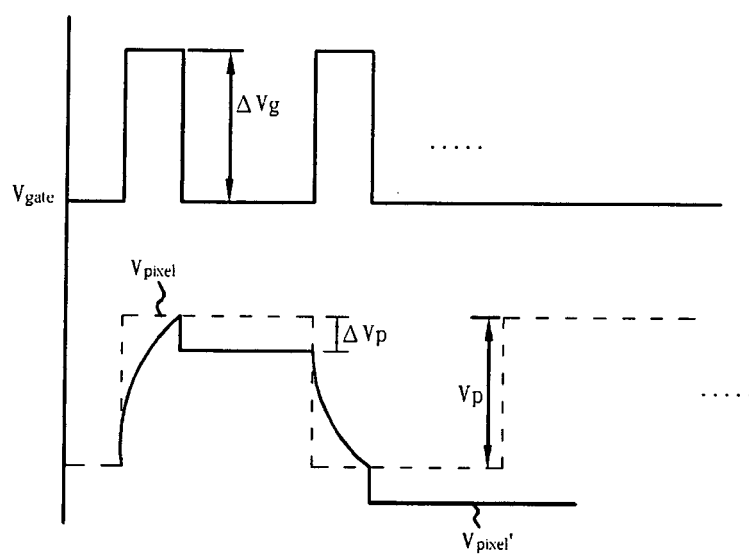


Fig. 6 Prior Art

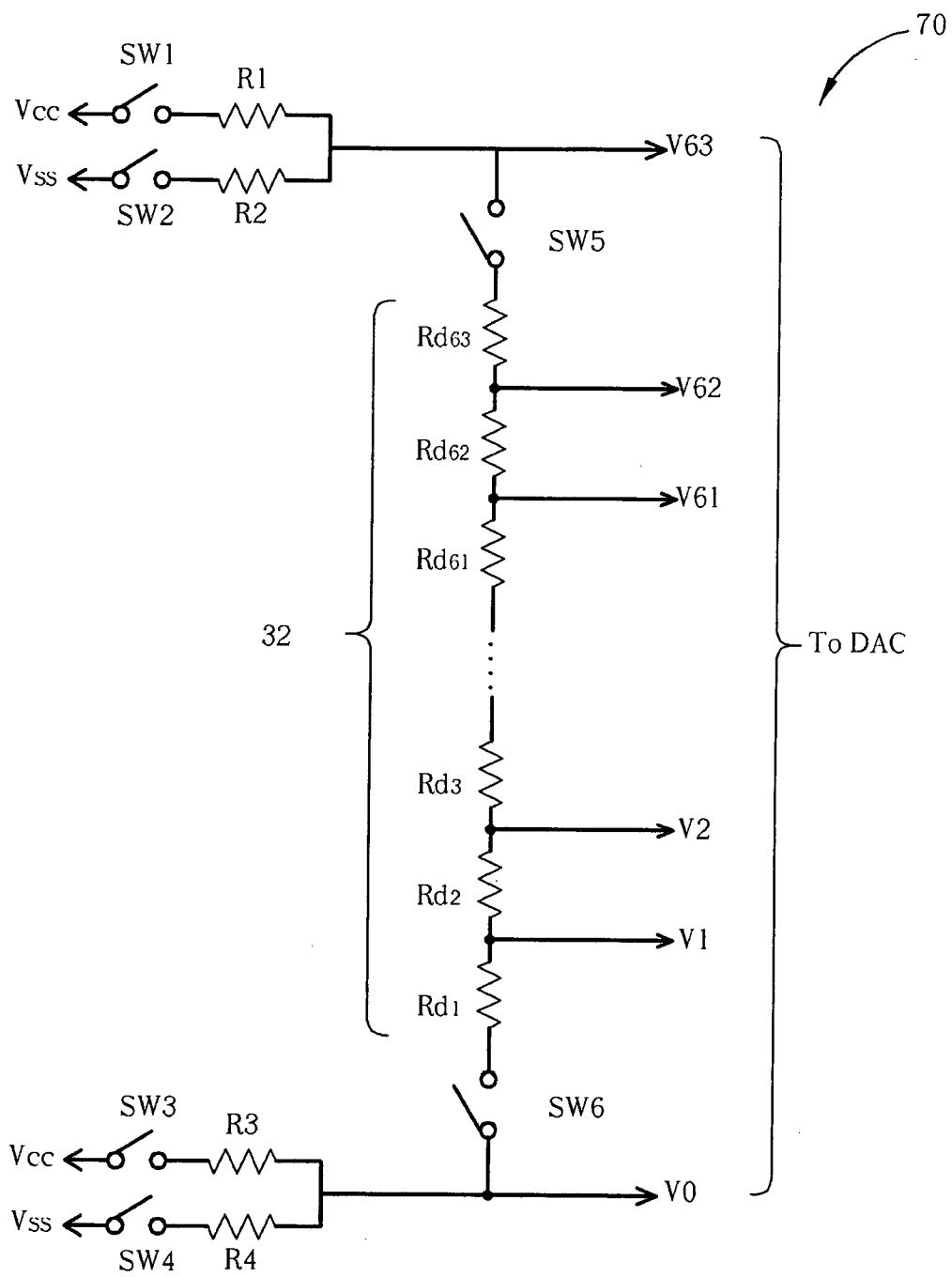


Fig. 7

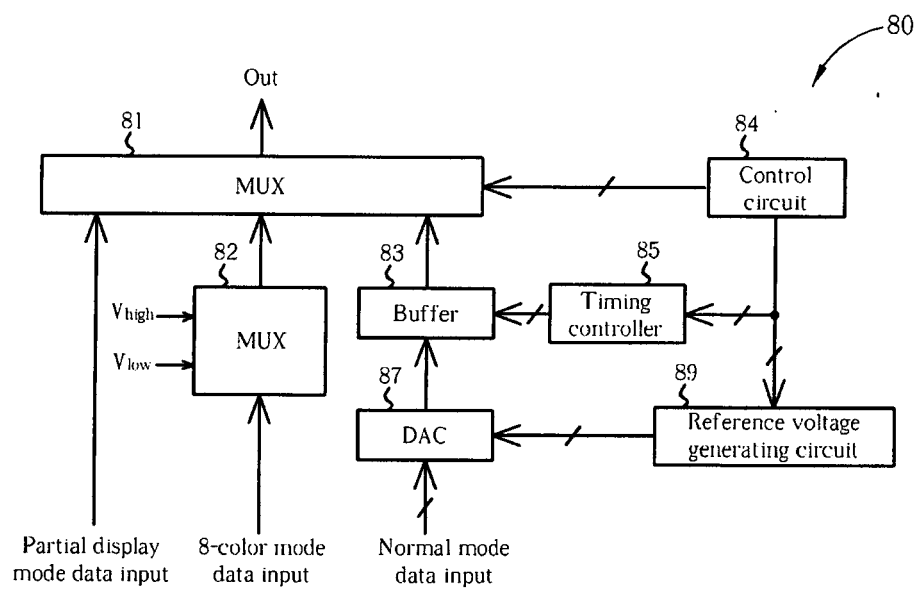


Fig. 8



European Patent
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EUROPEAN SEARCH REPORT

Application Number
EP 05 01 9572

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Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (IPC)
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The present search report has been drawn up for all claims			
Place of search The Hague		Date of completion of the search 11 January 2006	Examiner Fanning, C
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EPO FORM 1503 03 82 (P04C01)

**ANNEX TO THE EUROPEAN SEARCH REPORT
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EP 05 01 9572

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