



(11) **EP 1 794 952 B1**

(12) **EUROPEAN PATENT SPECIFICATION**

(45) Date of publication and mention  
of the grant of the patent:  
**14.07.2010 Bulletin 2010/28**

(21) Application number: **05798761.2**

(22) Date of filing: **27.09.2005**

(51) Int Cl.:  
**H04L 12/56** <sup>(2006.01)</sup>

(86) International application number:  
**PCT/US2005/034758**

(87) International publication number:  
**WO 2006/039319 (13.04.2006 Gazette 2006/15)**

(54) **HIGH SPEED FIBRE CHANNEL SWITCH ELEMENT**

HOCHGESCHWINDIGKEITS-FASERKANALSCHALTELEMENT

ELEMENT DE COMMUTATION POUR CANAL FIBRE GRANDE VITESSE

(84) Designated Contracting States:  
**AT BE BG CH CY CZ DE DK EE ES FI FR GB GR  
HU IE IS IT LI LT LU LV MC NL PL PT RO SE SI  
SK TR**

(30) Priority: **01.10.2004 US 956501**

(43) Date of publication of application:  
**13.06.2007 Bulletin 2007/24**

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## Description

### BACKGROUND

#### 1. Field of the Invention

**[0001]** The present invention relates to Fibre Channel networks, and more particularly to a Fibre Channel switch element that can operate at a high speed.

#### 2. Background of the Invention

**[0002]** Fibre Channel is a set of American National Standard Institute (ANSI) standards, which provide a serial transmission protocol for storage and network protocols such as HIPPI, SCSI, IP, ATM and others. Fibre Channel provides an input/output interface to meet the requirements of both Channel and network users.

**[0003]** Fibre Channel supports three different topologies: point-to-point, arbitrated loop and Fibre Channel fabric. The point-to-point topology attaches two devices directly. The arbitrated loop topology attaches devices in a loop. The Fibre Channel fabric topology attaches host systems directly to a fabric, which are then connected to multiple devices. The Fibre Channel fabric topology allows several media types to be interconnected.

**[0004]** In Fibre Channel, a path is established between two nodes where the path's primary task is to transport data from one point to another at high speed with low latency, performing only simple error detection in hardware.

**[0005]** Fibre Channel fabric devices include a node port or "N\_Port" that manages fabric connections. The N\_port establishes a connection to a fabric element (e.g., a switch) having a fabric port or "F\_port". Fabric elements include the intelligence to handle routing, error detection, recovery, and similar management functions.

**[0006]** A Fibre Channel switch is a multi-port device where each port manages a simple point-to-point connection between itself and its attached system. Each port can be attached to a server, peripheral, I/O subsystem, bridge, hub, router, or even another switch. A switch receives messages from one port and automatically routes it to another port. Multiple calls or data transfers happen concurrently through the multi-port Fibre Channel switch.

**[0007]** Fibre Channel switches use memory buffers to hold frames received and sent across a network. Associated with these buffers are credits, which are the number of frames that a buffer can hold per fabric port.

**[0008]** Current Fibre Channel standards define switch port/link operations to occur at 1 gigabit per second ("G"), 2G, 4G and 10G. However, as bandwidth increases a need for 20G, 40G or higher port/link operation will occur. Conventional standards and Fibre Channel switches do not provide Fibre Channel switches that can operate at such high speeds.

**[0009]** Therefore, there is a need for a Fibre Channel switch whose ports can be selected to operate at high

speeds, for example, at 10G, 20G or 40G.

**[0010]** Curt Ridgeway: "20GFC-40GFC Using 4-lane XAUI's" T11/03-069VO.PDF, [online] 2 March 2002, pages 1-9, XP002358728 LSI LOGIC and Curtis A. Ridgeway: "Design considerations for 10-Gbit Fibre Channel" COMSDESIGN, [Online] 14 April 2003, pages 1-3, XP 002358 727 disclose a Fibre Channel element.

### SUMMARY OF THE PRESENT INTENTION

**[0011]** In one aspect of the present invention, there is provided a Fibre Channel switch element, comprising: a port for receiving and transmitting Fibre Channel frames; a control port for generating a rate select signal that is used for selecting an operating speed for the port; and a rate select module that selects an operating speed for the port based on the select signal from the control port; wherein the port operates at least at a rate of 10 gigabits per second ("G").

**[0012]** Also, a cut status is provided for cut-through routing between ports operating at different speed. Plural transmit and receive lines are used for port operation at a rate equal to or higher than 10G.

**[0013]** In another aspect of the present invention, there is provided a Fibre Channel network, comprising: a Fibre

**[0014]** Channel switch element having a port for receiving and transmitting Fibre Channel frames; a control port for generating a rate select signal that is used for selecting an operating speed for the port; and a rate select module that selects an operating speed for the port based on the select signal from the control port; wherein the port operates at least at a rate of 10 gigabits per second ("G").

**[0015]** This brief summary has been provided so that the nature of the invention may be understood quickly. A more complete understanding of the invention can be obtained by reference to the following detailed description of the preferred embodiments thereof concerning the attached drawings.

### BRIEF DESCRIPTION OF THE DRAWINGS

**[0016]** The foregoing features and other features of the present invention will now be described with reference to the drawings of a preferred embodiment. In the drawings, the same components have the same reference numerals. The illustrated embodiment is intended to illustrate, but not to limit the invention. The drawings include the following Figures:

Figure 1A shows an example of a Fibre Channel network;

Figure 1B shows an example of a Fibre Channel switch element, according to one aspect of the present invention;

Figure 1C shows a block diagram of a 20-channel switch chassis, according to one aspect of the present invention;

Figure 1D shows a block diagram of a Fibre Channel switch element with sixteen GL\_Ports and four XG ports, according to one aspect of the present invention;

Figure 2 shows a block diagram of a Fibre Channel switch with a rate select module, according to one aspect of the present invention; and

Figure 3 shows a table for cut-through routing, according to one aspect of the present invention.

## DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

### **[0017]** Definitions:

The following definitions are provided as they are typically (but not exclusively) used in the Fibre Channel environment, implementing the various adaptive aspects of the present invention.

"E\_Port": A fabric expansion port that attaches to another Interconnect port to create an Inter-Switch Link.

"F\_Port": A port to which non-loop N\_Ports are attached to a fabric and does not include FL\_ports.

"Fibre Channel ANSI Standard": The standard describes the physical interface, transmission and signaling protocol of a high performance serial link for support of other high level protocols associated with IPI, SCSI, IP, ATM and others.

"Fabric": The structure or organization of a group of switches, target and host devices (NL\_Port, N\_ports etc.).

"N-Port": A direct fabric attached port, for example, a disk drive or a HBA.

"NL\_Port": A L\_Port that can perform the function of a N\_Port.

"Port": A general reference to N. Sub.-- Port or F.Sub.--Port.

"Port": A general reference to N. Sub.-- Port or F.Sub.--Port.

"Switch": A fabric element conforming to the Fibre Channel Switch standards.

**[0018]** To facilitate an understanding of the preferred embodiment, the general architecture and operation of a Fibre Channel switch system/element will be described. The specific architecture and operation of the preferred embodiment will then be described with reference to the general architecture.

### Fibre Channel System

**[0019]** Figure 1A is a block diagram of a Fibre Channel system 100 implementing the methods and systems in accordance with the adaptive aspects of the present invention. System 100 includes plural devices that are interconnected. Each device includes one or more ports, classified as node ports (N\_Ports), fabric ports (F\_Ports),

and expansion ports (E\_Ports). Node ports may be located in a node device, e.g. server 103, disk array 105 and storage device 104. Fabric ports are located in fabric devices such as switch 101 and 102. Arbitrated loop 106 may be operationally coupled to switch 101 using arbitrated loop ports (FL\_Ports).

**[0020]** The devices of Figure 1A are operationally coupled via "links" or "paths". A path may be established between two N\_ports, e.g. between server 103 and storage 104. A packet-switched path may be established using multiple links, e.g. an N\_Port in server 103 may establish a path with disk array 105 through switch 102.

### SWITCH ELEMENT

**[0021]** Figure 1B is a block diagram of a 20-port ASIC fabric element according to one aspect of the present invention. Figure 1B provides the general architecture of a 20-channel switch chassis using the 20-port fabric element. Fabric element includes ASIC 20 with non-blocking Fibre Channel class 2 (connectionless, acknowledged) and class 3 (connectionless, unacknowledged) service between any ports. It is noteworthy that ASIC 20 may also be designed for class 1 (connection-oriented) service, within the scope and operation of the present invention as described herein.

**[0022]** The fabric element of the present invention is presently implemented as a single CMOS ASIC, and for this reason the term "fabric element" and ASIC are used interchangeably to refer to the preferred embodiments in this specification. Although Figure 1B shows 20 ports, the present invention is not limited to any particular number of ports.

**[0023]** ASIC 20 has 20 ports numbered in Figure 1B as GL0 through GL19. These ports are generic to common Fibre Channel port types, for example, F\_Port, FL\_Port and E-Port. In other words, depending upon what it is attached to, each GL port can function as any type of port. Also, the GL port may function as a special port useful in fabric element linking, as described below.

**[0024]** For illustration purposes only, all GL ports are drawn on the same side of ASIC 20 in Figure 1B. However, the ports may be located on both sides of ASIC 20 as shown in other figures. This does not imply any difference in port or ASIC design. Actual physical layout of the ports will depend on the physical layout of the ASIC.

**[0025]** Each port GL0-GL19 has transmit and receive connections to switch crossbar 50. One connection is through receive buffer 52, which functions to receive and temporarily hold a frame during a routing operation. The other connection is through a transmit buffer 54.

**[0026]** Switch crossbar 50 includes a number of switch crossbars for handling specific types of data and data flow control information. For illustration purposes only, switch crossbar 50 is shown as a single crossbar. Switch crossbar 50 is a connectionless crossbar (packet switch) of known conventional design, sized to connect 21 x 21 paths. This is to accommodate 20 GL ports plus a port

for connection to a fabric controller, which may be external to ASIC 20.

**[0027]** In the preferred embodiments of switch chassis described herein, the fabric controller is a firmware-programmed microprocessor, also referred to as the input/output processor ("IOP"). IOP 66 is shown in Figure 1C as a part of a switch chassis utilizing one or more of ASIC 20. As seen in Figure 1B, bi-directional connection to IOP 66 is routed through port 67, which connects internally to a control bus 60. Transmit buffer 56, receive buffer 58, control register 62 and Status register 64 connect to bus 60. Transmit buffer 56 and receive buffer 58 connect the internal connectionless switch crossbar 50 to IOP 66 so that it can source or sink frames.

**[0028]** Control register 62 receives and holds control information from IOP 66, so that IOP 66 can change characteristics or operating configuration of ASIC 20 by placing certain control words in register 62. IOP 66 can read status of ASIC 20 by monitoring various codes that are placed in status register 64 by monitoring circuits (not shown).

**[0029]** Figure 1C shows a 20-channel switch chassis S2 using ASIC 20 and IOP 66. S2 will also include other elements, for example, a power supply (not shown). The 20 GL\_Ports correspond to channel C0-C19. Each GL\_Port has a serial/deserializer (SERDES) designated as S0-S19. Ideally, the SERDES functions are implemented on ASIC 20 for efficiency, but may alternatively be external to each GL\_Port. The SERDES converts parallel data into a serial data stream for transmission and converts received serial data into parallel data. The 8 bit to 10 bit encoding enables the SERDES to generate a clock signal from the received data stream.

**[0030]** Each GL\_Port may have an optical-electric converter, designated as OE0-OE19 connected with its SERDES through serial lines, for providing fibre optic input/output connections, as is well known in the high performance switch design. The converters connect to switch channels C0-C19. It is noteworthy that the ports can connect through copper paths or other means instead of optical-electric converters.

**[0031]** Figure 1D shows a block diagram of ASIC 20 with sixteen GL ports and four high-speed port control modules designated as XG0-XG3 (for example, 10G, 20G or 40G). ASIC 20 include a control port 62A that is coupled to IOP 66 through a PCI connection 66A.

**[0032]** Details of how switch 20 is operated is provided in US patent application Serial Number 10/894,587, filed on July 20, 2004.

**[0033]** Figure 2 shows another block diagram of switch element 20, according to one aspect of the present invention. Switch element 20 has receive and transmit pipelines 202A that operate in the manner described in the aforementioned patent application using plural data buffers 203.

**[0034]** A rate select module 202 is provided that selects a particular speed for a port based on a select speed signal 201 that is generated from the common port 62A.

Firmware for switch element 20 may be used to generate signal 201. Module 202 provides the appropriate clock and configuration signals for a 10G, 20G, 40G or port/link operation at any rate.

**[0035]** A port can negotiate with another port to operate at 10G/20G/40G or any other rate. A port may operate at 10G, 20G, 40G, 10G and 20G, 20G and 40G or any other combination. The negotiation process may be similar to that described in the FC-FS Fibre Channel standard. The 'RF' primitive may be used to replace the 'NOS' primitive, as discussed in FC-FS.

**[0036]** SERDES 204, 205, 206 and 207 converts parallel 10 bit characters into a serial stream on the transmit side (i.e. data to the network) and converts data received by switch element 20 into 10-bit characters. SERDES 204-207 recover clock information from data that is received by a port.

**[0037]** In one aspect of the present invention, for a 20G operation, 4 serial streams (i.e., four transmit and four receive lanes) (as shown in Figure 2 with SERDES 204-207) at 6.375G may be used. Each lane encodes/decodes a byte of data using 8B/10B code. The 20G ports may be connected through passive copper, actively driven copper or optical at the same or different wavelengths (one wavelength for each lane) paths (not shown).

**[0038]** For a 40G operation, 4 serial streams each at 12.75G may be used. Each lane encodes/decodes a byte of data using 8B/10B code. The four lanes are synchronized and aligned, as described in the aforementioned patent application.

**[0039]** It is noteworthy that the invention is not limited to any particular number of serial streams; for example, a single stream may be used to operate a port at 20G/40G or any other rate. Also, the serial streams may operate at the same optical wavelength or different wavelengths; one for each serial stream.

**[0040]** SERDES 204-207 clock rates are manipulated to facilitate higher speed operation. Currently the XAUI interface supports 10G operation using four transmit and four receive lanes; each lane encoding data with an 8B/10B code for differential serial transmission and operating at 3.1875 GigaBaud. To operate at higher speeds, a full rate will be at 12.75 GigaBaud, half rate will be at 6.375 GigaBaud. The full rate, half and quarter rates are selected by module 202, based on signal 201.

#### Cut-Through Routing at Higher Speeds:

**[0041]** "Cut" bits are a status signal sent from receive to transmit buffers to keep the transmit buffer running as quickly as possible by either guaranteeing that the transmit port either does not run out of data or by allowing the transmit port to re-arbitrate its tags to select a frame source that has the "cut" bit set. The use of cut bits at lower rates (i.e., 1G, 2G, 4G and 10G) is described in the aforementioned patent application. The Cut Bits may be expanded to include 20G, 40G or higher transfer rates.

**[0042]** To reduce latency, a frame is released from a receive buffer, after a certain threshold value is reached. However, if the receive buffer slots become almost full with other frames, then new incoming frames wait for the end of frame ("EOF"). This reduces contention time on shared resources that may occur if the receive buffer is tied up for "cut" through routing.

**[0043]** There are different conditions on cut status depending on what kind of port the Receive Buffer resides in (for example, 10G/20G/40G or any other speed). The selection of cut status also depends on the type of port the Transmit Port resides in. Table I in Figure 3, shows how some cut through frame length calculations are performed depending upon port transfer rates.

**[0044]** In one aspect of the present invention, a port can be configured to operate at different rates. High bandwidth operation is permitted for better performance.

**[0045]** Although the present invention has been described with reference to specific embodiments, these embodiments are illustrative only and not limiting. Many other applications and embodiments of the present invention will be apparent in light of this disclosure and the following claims.

## Claims

### 1. A Fibre Channel switch element, comprising:

a port (GL0-GL19) for receiving and transmitting fibre channel frames; **characterized by** a control port (62A) for generating a speed select signal (201) that is used for selecting an operating speed for the port; and a rate select module (202) that is adapted to select an operating speed for the port based on the speed select signal from the control port; wherein the port is adapted to operate at least at a rate of 10 gigabits per second ("G").

2. The Fibre Channel switch element of Claim 1, wherein the port is adapted to operate at 20G.

3. The Fibre Channel switch element of Claim 1, wherein the port is adapted to operate at 40G.

4. The Fibre Channel switch element of Claim 1, wherein the port includes a receive buffer (58) to store a received Fibre Channel frame, the element being operative to send a status signal to a transmit segment of the port after a certain portion of the Fibre Channel frame has been received, where the portion of the Fibre Channel frame depends on an operating speed of the port.

5. The Fibre Channel switch element of Claim 1, comprising a plurality of transmit and receive lanes (SERDES 204-207) usable when the port operates at least

at a 10G rate.

6. The Fibre Channel switch element of Claim 7, wherein each of the plurality of lanes are operative at 6.375 GigaBaud when the port operates at a 20G rate.

7. The Fibre Channel switch element of Claim 7, wherein, when the port is operative at a 40G rate, each of the plurality of lanes operates at 12.75 Gigabaud.

8. A Fibre Channel network, comprising a Fibre Channel switch element as claimed in any preceding claim.

## Patentansprüche

### 1. Faserkanalschaltelement, umfassend:

einen Port (GLO-GL19) zum Empfangen und Senden von Faserkanalrahmen; **gekennzeichnet durch:**

einen Steuerport (62A) zum Generieren eines Signals (201 für Geschwindigkeitswahl, das zum Auswählen einer Betriebsgeschwindigkeit für den Port benutzt wird; und

ein Modul (202) für Bitratenwahl, das angepasst ist, eine Betriebsgeschwindigkeit für den Port, beruhend auf dem Signal für Geschwindigkeitswahl vom Steuerport, zu selektieren; wobei der Port angepasst ist, mit zumindest einer Rate von 10 Gigabits pro Sekunde ("G") zu arbeiten.

2. Faserkanalschaltelement nach Anspruch 1, wobei der Port angepasst ist, mit 20G zu arbeiten.

3. Faserkanalschaltelement nach Anspruch 1, wobei der Port angepasst ist, mit 40G zu arbeiten.

4. Faserkanalschaltelement nach Anspruch 1, wobei der Port einen Empfangspuffer (58) umfasst, um einen empfangenen Faserkanalrahmen zu speichern, wobei das Element betriebsfähig ist, ein Statussignal zu einem Sendesegment des Ports zu senden, nach dem ein gewisser Teil des Faserkanalrahmens empfangen worden ist, wo der Teil des Faserkanalrahmens von einer Betriebsgeschwindigkeit des Ports abhängt.

5. Faserkanalschaltelement nach Anspruch 1, das eine Mehrheit von Sende- und Empfangs-Lanes (SERDES 204-207) umfasst, die verwendbar sind, wenn der Port zumindest mit einer Rate von 10G arbeitet.

6. Faserkanalschaltelement nach Anspruch 7, wobei jede der Mehrheit von Lanes mit 6,375 Gigabaud betriebsfähig ist, wenn der Port mit einer Rate von 20G arbeitet.

7. Faserkanalschaltelement nach Anspruch 7, wobei, wenn der Port mit einer Rate von 40G betriebsfähig ist, jede der Mehrheit von Lanes mit 12,75 Gigabaud arbeitet.
8. Faserkanalnetzwerk, das ein Faserkanalschattelement, wie in einem beliebigen vorhergehenden Anspruch beansprucht, umfasst.

revendication 7, dans lequel, quand le port fonctionne à un débit de 40G, chacune de la pluralité de voies fonctionne à 12,75 Giga-Bauds.

- 5 8. Réseau Fibre Channel, comprenant un élément de commutation Fibre Channel selon l'une quelconque des revendications précédentes.

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## Revendications

1. Élément de Commutation de Fibre Channel, comprenant:

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un port (GL0-GL19) pour recevoir et transmettre des trames Fibre Channel ; **caractérisé par** un port de commande (62A) pour générer un signal de sélection de vitesse (201) qui sert à sélectionner une vitesse opérationnelle du port ; et un module de sélection de débit (202) qui est adapté pour sélectionner une vitesse opérationnelle du port en fonction du signal de sélection de vitesse provenant du port de commande ; le port étant adapté pour fonctionner à au moins un débit de 10 gigabits par seconde ("G").

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2. Élément de commutation de Fibre Channel selon la revendication 1, dans lequel le port est adapté pour fonctionner à 20G.

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3. Élément de commutation de Fibre Channel selon la revendication 1, dans lequel le port est adapté pour fonctionner à 40G.

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4. Élément de commutation de Fibre Channel selon la revendication 1, dans lequel le port inclut un tampon de réception (58) pour mémoriser une trame Fibre Channel reçue, l'élément fonctionnant pour envoyer un signal d'état à un segment de transmission du port après qu'une certaine partie de la trame Fibre Channel a été reçue, la partie de la trame Fibre Channel dépendant d'une vitesse opérationnelle du port.

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5. Élément de commutation de Fibre Channel selon la revendication 1, comprenant une pluralité de voies d'émission et de réception (SERDES 204-207) utilisables quand le port fonctionne au moins à un débit de 10G.

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6. Élément de commutation de Fibre Channel selon la revendication 7, dans lequel chacune de la pluralité de voies fonctionne à 6,375 Giga-Bauds quand le port fonctionne à un débit de 20G.

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7. Élément de commutation de Fibre Channel selon la

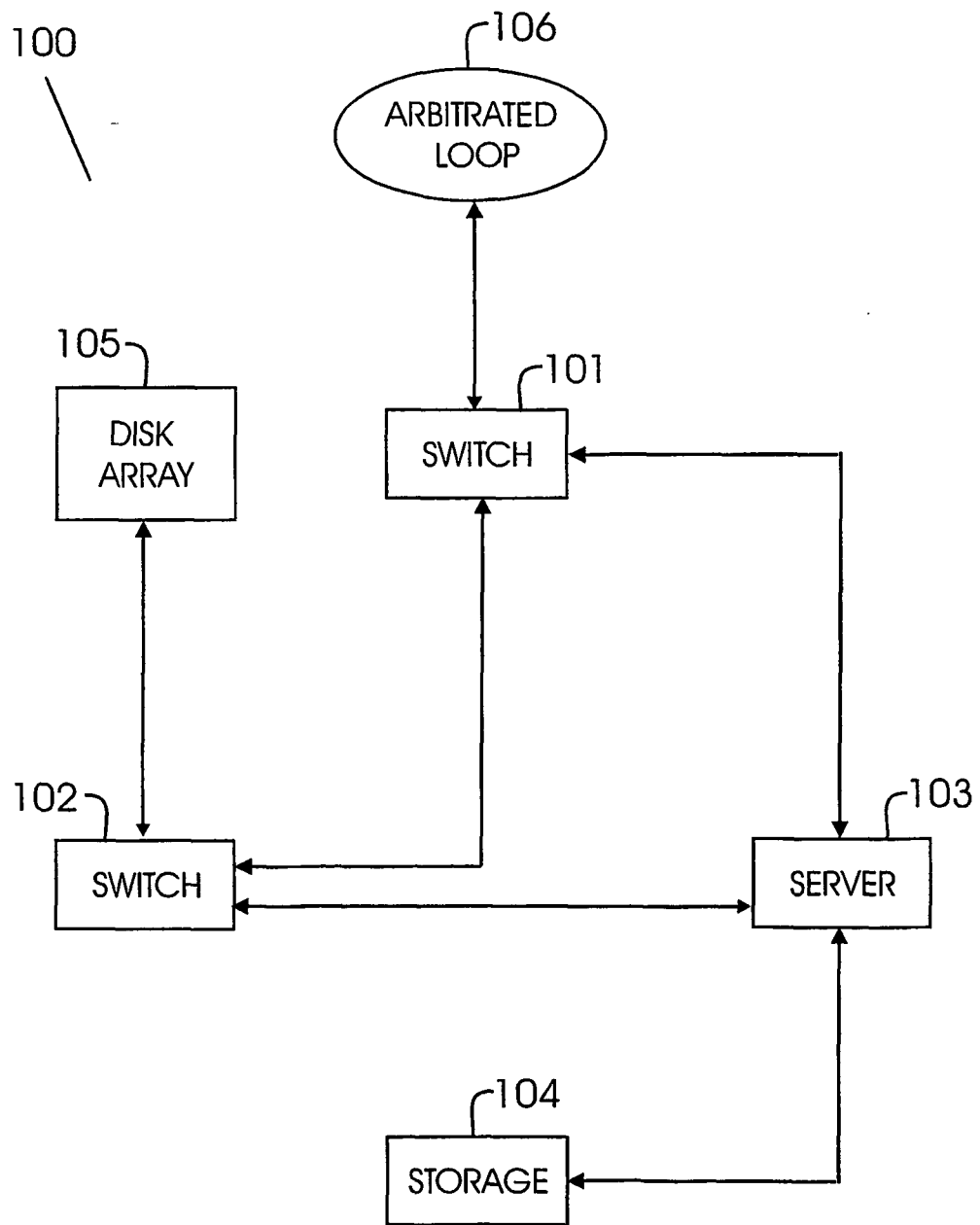


FIGURE 1A

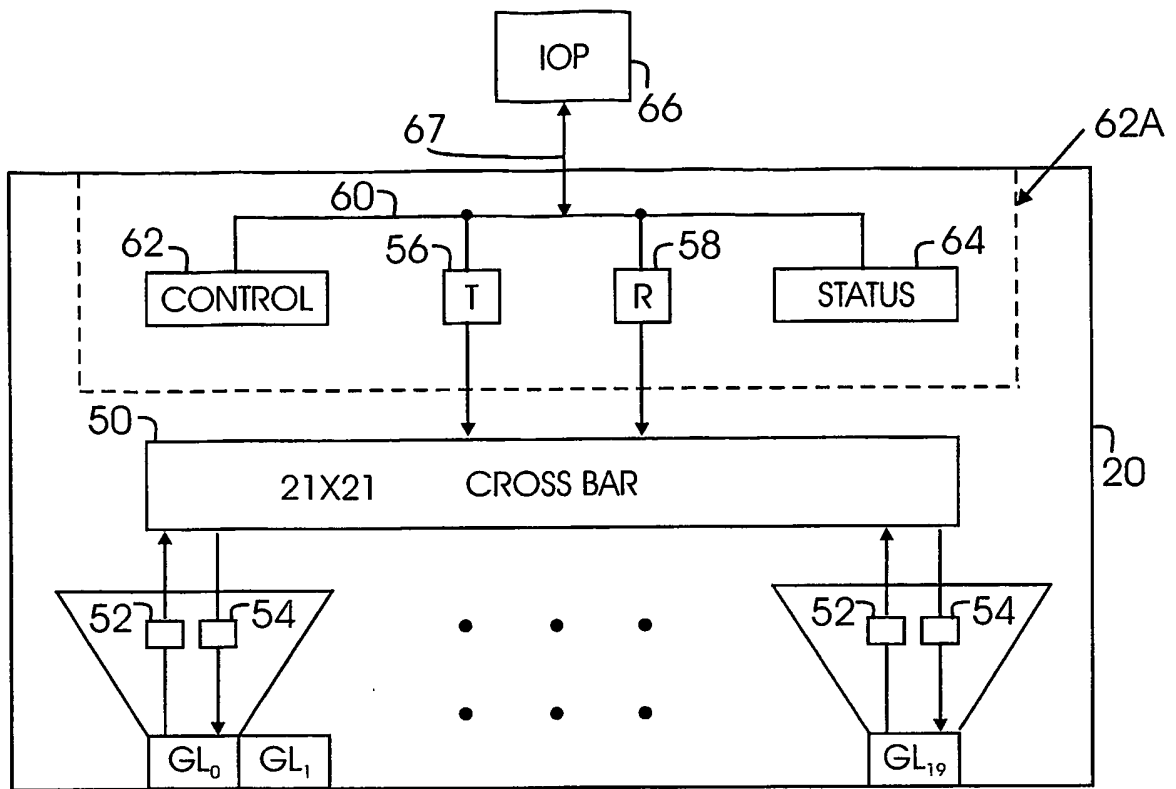


FIGURE 1B

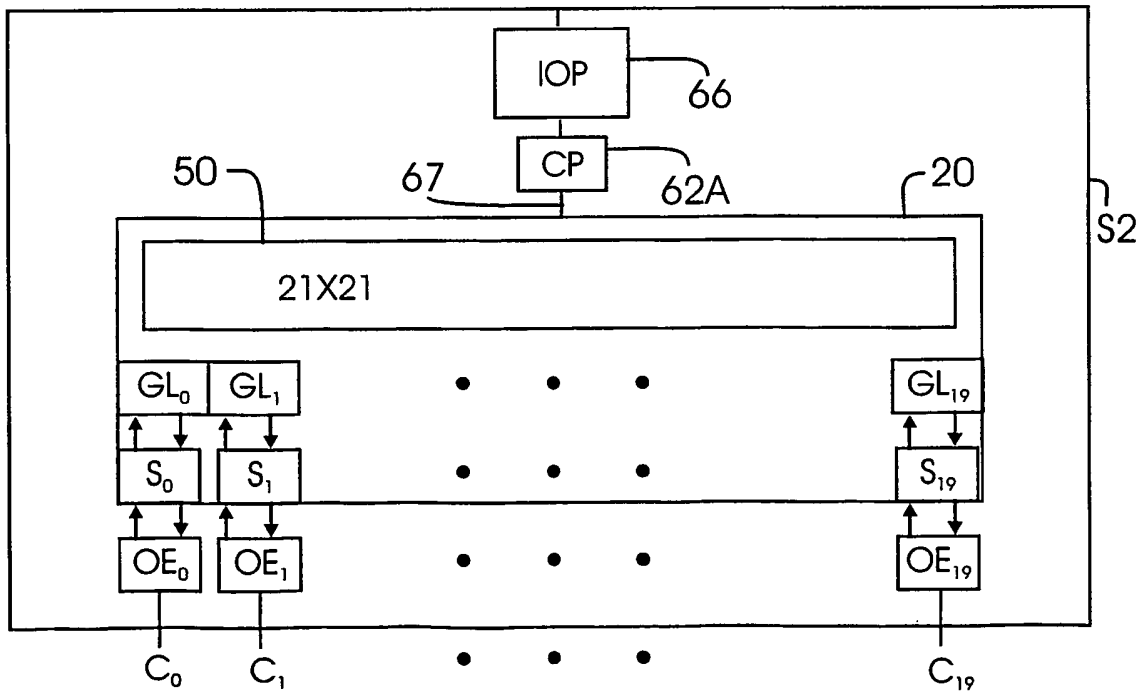


FIGURE 1C



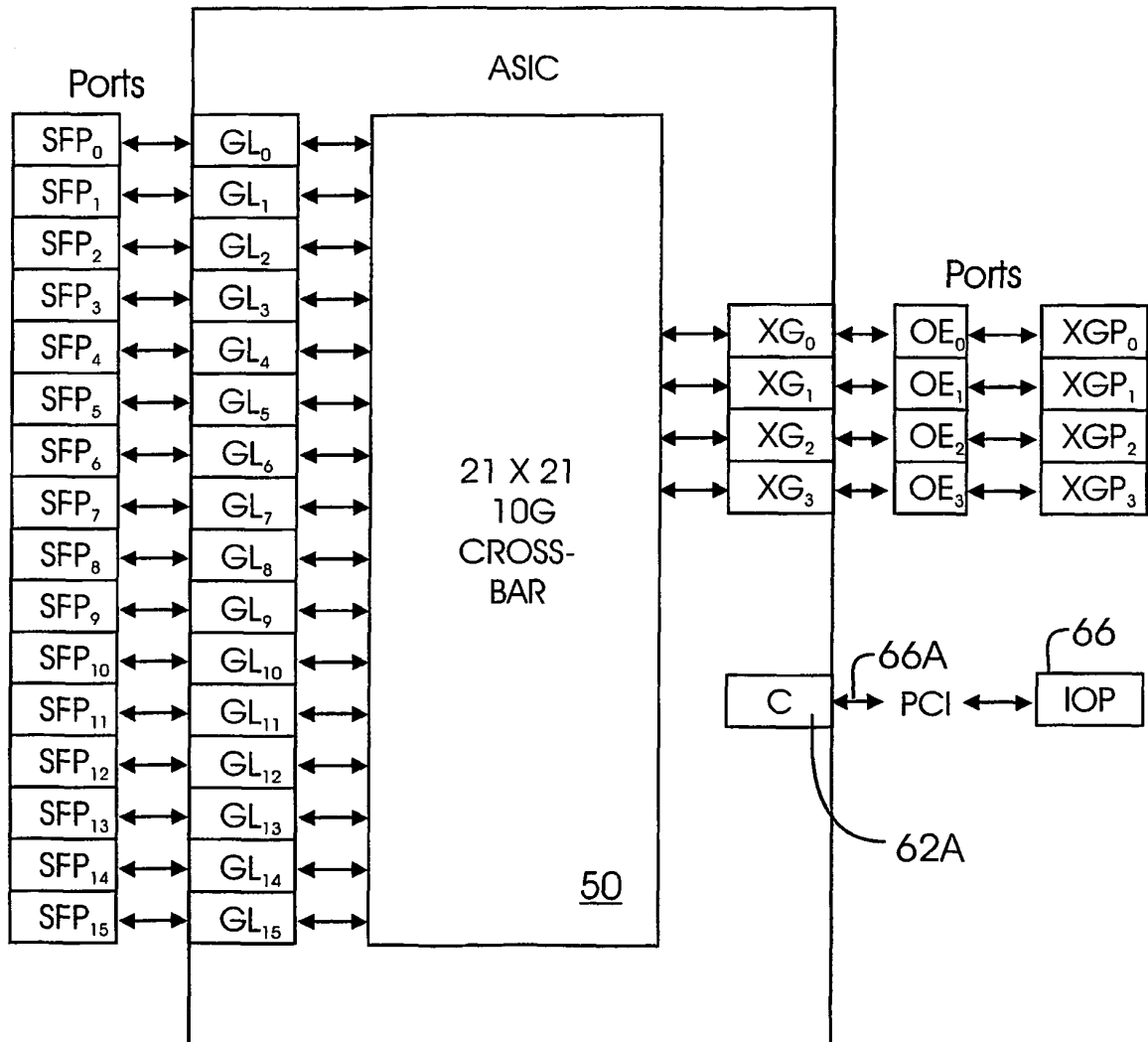


FIGURE 1D

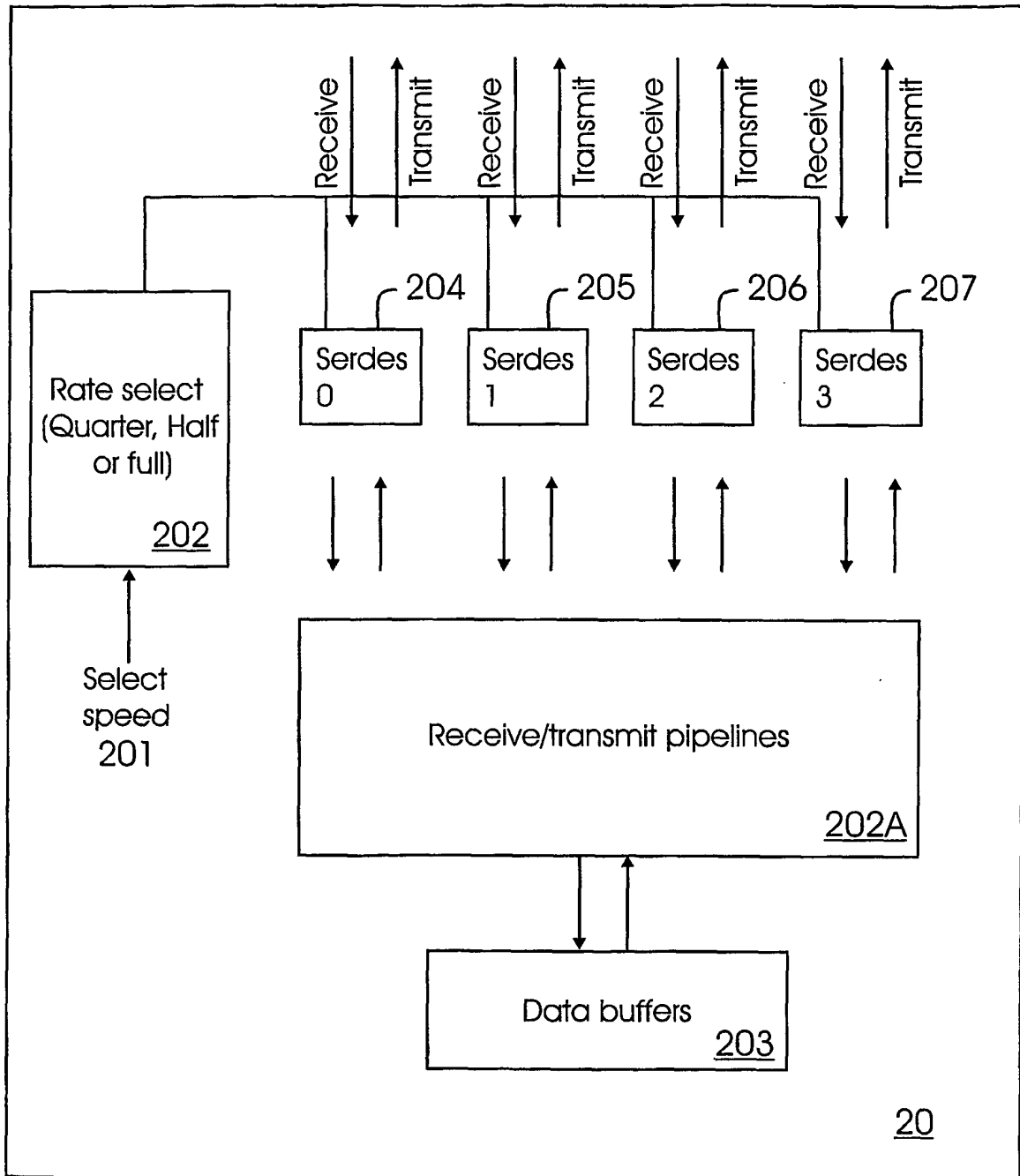


FIGURE 2

| Amount of max Length Frame Received | RPORT RX_Rate = 10G |         |                 |         | RPORT RX_Rate = 20G |         |                 |         | RPORT RX_Rate = 40G |         |                 |         |
|-------------------------------------|---------------------|---------|-----------------|---------|---------------------|---------|-----------------|---------|---------------------|---------|-----------------|---------|
|                                     | > 1 Slot Empty      |         | <= 1 Slot Empty |         | > 1 Slot Empty      |         | <= 1 Slot Empty |         | > 1 Slot Empty      |         | <= 1 Slot Empty |         |
|                                     | 40G Cut             | 20G Cut | 40G Cut         | 20G Cut | 40G Cut             | 20G Cut | 40G Cut         | 20G Cut | 40G Cut             | 20G Cut | 40G Cut         | 20G Cut |
| 0/0 < rcvd < 1/2                    | 0                   | 0       | 0               | 0       | 0                   | 1       | 0               | 0       | 1                   | 1       | 0               | 0       |
| 1/2 < rcvd < 3/4                    | 0                   | 1       | 0               | 0       | 1                   | 1       | 0               | 0       | 1                   | 1       | 0               | 0       |
| 3/4 < rcvd < EOF                    | 1                   | 1       | 0               | 0       | 1                   | 1       | 0               | 0       | 1                   | 1       | 0               | 0       |
| EOF Received                        | 1                   | 1       | 1               | 1       | 1                   | 1       | 1               | 1       | 1                   | 1       | 1               | 1       |

FIGURE 3

## REFERENCES CITED IN THE DESCRIPTION

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