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(54) A METHOD AND CIRCUIT FOR ACQUIRING AN ASYNCHRONOUSLY DE-MAP CLOCK

VERFAHREN UND SCHALTUNG ZUM BILDEN EINES ASYNCHRONEN DEMAPPING-TAKTES

PROCEDE ET CIRCUIT POUR L'ACQUISITION D'UNE HORLOGE DE DEMAPPAGE ASYNCHRONE

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(56) References cited:
EP-A- 1 343 261 **WO-A-99/27669**
WO-A1-03/079591 **CN-A- 1 511 400**
US-A1- 2005 074 032

- **XU D.: 'THE EXTRACTION OF 2 MBIT/S SIGNAL FROM STM-1 AND DESYNCHRONIZING' STUDY ON OPTICAL COMMUNICATIONS June 2000, pages 46 - 48, 60, XP008095060**

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Description

Field of the Invention

[0001] The present invention relates to the field of optical network, particularly to a method and a circuit for obtaining an asynchronous demapping clock.

Background of the Invention

[0002] With the increasing utilization of synchronous digital hierarchy (SDH) networks, there is a demand for transmitting the OTN (Optical Transport Network) connection signal ODUk (Optical Channel Data Unit k) in SDH network. In addition, in consideration of the coexistence of OTN and SDH networks, it is also necessary to provide a method of mapping ODUk signal into C-4-Xv (C-4 plus the overhead constitutes the STM-N data) in the form of client data and to transmitting it in a virtual concatenation mode.

[0003] ITU-T G.707 standard defines a method of mapping an ODUk signal into a C-4-Xv signal asynchronously, so that the ODUk connection signal may be transmitted in SDH network in VC-4 virtual concatenation mode, that is, ODU1 is mapped into C-4-17C, while ODU2 is mapped into C-4-68v. Fig.1 shows an actual mapping structure from ODU1 to C-4-17c, wherein D represents payload, R represents fixed padding data, and C represents adjustment opportunity in which CCCCC=00000 indicates that S is a payload, while CCCCC=11111 indicates that S is padding data.

[0004] Taking the ODU1 as an example, when ODU1 data are demapped and recovered, an asynchronous clock for ODU1 has to be recovered from C-4-17c. The asynchronous mapping and demapping processes will inevitably result in a great deal of mapping and combination jittering. It is known from the definition in G.8251 that OTN services have strict requirements regarding jittering. As a result, a clock recovery scheme is required to filter off the jittering so as to ensure, the clock performance.

[0005] An existing implementation to filter off jittering and ensure the performance of clock is shown in Fig.2, in which a writing control module generates a gapped clock in accordance with the actual data and the corresponding clock signal, removes the overhead and padding bits from STM-N (Synchronous Transport Module Level N), and writes the actual ODU1 data into an FIFO (Fist In First Out) queue. In addition, the gapped clock is input into a phase lock loop (PLL) constituted by the serially connected phase discriminator (PD), low pass filter (LPF), and voltage controlled oscillator (VCO). The PLL performs a phase locking to the gapped clock to obtain the current ODU1 clock, i.e., the demapping clock signal.

[0006] The detailed procedure of the above described phase locking is: the PD produces a phase difference between the gapped clock and the ODU1 clock fed back by the VCO, in which the phase difference reflects the current difference between the data written into the FIFO and the data read out from the FIFO. In order to balance between the data written into FIFO and the data read from FIFO, the PD sends the phase difference into the LPF for low pass filtering so as to produce a corresponding signal. This signal is sent to the VCO as the control signal for adjusting ODU1 clock frequency output from the VCO, so as to control the ODU1 clock output from VCO to keep track of the gapped clock, thereby balancing the ODU1 clock with the gapped clock.

[0007] Since there are not only fixed bits of padding data but also asynchronous data rate adjusting and controlling bits, as well as a great deal of overhead, in STM-N, it is difficult to suppress jittering in an actually output ODU clock by only utilizing one PLL to adjust ODU1 clock directly, and thus it is difficult to meet the requirement for OTN jittering in G.8251

[0008] WO 99/27669 A1 discloses a method of transferring data signals as well as a method and an apparatus for desynchronizing plesiochronous digital hierarchy (PDH) signals. In the method and apparatus for desynchronizing the PDH signals which have been transferred via a synchronous digital hierarchy (SDH) network in which pointer adjustments may occur, the pointer adjustments are compensated in the desynchronization with a temporary frequency deviation in a clock signal regenerated on the basis of the received PDH signals.

[0009] EP 1 343 261 A1 discloses a plesiochronous demultiplexer for extracting and desynchronizing a tributary signal from a multiplex signal at its original data rate, which has a buffer memory for temporarily storing tributary data bits, an adjustable oscillator for generating a read clock, and a comparator for comparing read or write timing rates to generate a control signal to adjust the oscillator.

[0010] US 2005/0074032 A1 disclosed a transparent sub-wavelength network comprising an arrangement that allows transmission of client signals with higher clock fidelity, which is achieved by developing a phase offset measure at an ingress node, communicating it to the egress node, and recovering the client's clock from the received data and from the received phase-offset information.

Summary of the Invention

[0011] The embodiments of the present invention are to provide a method and a circuit for obtaining asynchronous demapping clock, by which a low-jittering and high-performance demapping clock signal may be obtained, thereby ensuring a high-performance data demapping.

[0012] The embodiments of the present invention provide the following technical solutions:

[0013] An embodiment of the present invention provides a method of obtaining asynchronous demapping clock, including:

obtaining a smoothed clock signal with evenly distributed gaps in accordance with data to be demapped and a corresponding clock signal;

performing phase locking to the smoothed clock signal with evenly distributed gaps in accordance with a signal reflecting writing and reading conditions of data of a First In First Out (FIFO), to obtain a clock signal required for demapping.

[0014] The step of obtaining a clock signal with evenly distributed gaps includes:

smoothing the corresponding clock signal with a predefined scheduling pattern, and obtaining the clock signal with evenly distributed gaps, wherein the scheduling pattern is obtained through calculation in accordance with the data to be demapped.

[0015] The step of performing phase locking may include:

writing the data to be demapped into the FIFO based on the clock signal with evenly distributed gaps;

performing phase locking in accordance with positions of reading and writing pointers of the FIFO to obtain the required Optical Channel Data Unit (ODU) clock signal.

[0016] Alternatively, the step of performing phase locking may include:

performing phase discrimination, low pass filtering, and voltage-controlled oscillation for the clock signal with evenly distributed gaps, and obtaining the required Optical Channel Data Unit (ODU) clock signal.

[0017] An embodiment of the present invention provides a circuit for generating an asynchronous demapping clock, which includes:

a smoothing control module, which is adapted to obtain and output a clock signal with evenly distributed gaps in accordance with data to be mapped and a corresponding clock signal, wherein obtaining a clock signal with evenly distributed gaps comprises smoothing the corresponding clock signal with a predefined scheduling pattern, and obtaining the clock signal with evenly distributed gaps, and the scheduling pattern is obtained through calculation in accordance with the data to be demapped;
a phase locking module, which is adapted to perform phase locking to the clock signal with evenly distributed gaps input from the smoothing control module in accordance.with a signal reflecting writing and reading conditions of data of a FIFO so as to obtain the demapping clock.

[0018] In this circuit, the phase locking module may include a phase discriminator, a low-pass filter, and a voltage controlled oscillator, the signal reflecting writing and reading conditions of data of the FIFO is processed by the phase discriminator, the low-pass filter, and the voltage controlled oscillator in turn so as to obtain the asynchronous demapping clock.

[0019] Alternatively, the phase locking module may include a phase discriminator, a low-pass filter, a reverse control sub-module, a Digital/Analogue (D/A) conversion sub-module, and a voltage controlled oscillator, the signal reflecting writing and reading conditions of data of the FIFO is processed by the phase discriminator, the low-pass filter, the reverse control sub-module, the D/A conversion sub-module, and the voltage controlled oscillator in turn so as to obtain the asynchronous demapping clock.

[0020] Alternatively, the phase locking module may include a phase discriminator, a low-pass filter, a reverse control sub-module, and a direct digital synthesis module; the signal reflecting writing and reading conditions of data of the FIFO is processed by the phase discriminator, the low-pass filter, the reverse control sub-module, and the direct digital synthesis module in turn so as to obtain the asynchronous demapping clock. An embodiment of the present invention provides an asynchronous demapping circuit, which, in addition to the above described circuit for generating an asynchronous demapping clock, further includes:

a writing control module, which is adapted to receive data to be demapped and a corresponding clock signals, and output a gapped clock as the writing clock of a primary FIFO;

a primary FIFO, which is adapted to receive the data to be demapped which are written into the FIFO in accordance with the gapped clock output from the writing control module and control the reading of data from the primary FIFO by utilizing the clock signal with evenly distributed gaps output from the smoothing control module as a reading clock;

a secondary FIFO, which is adapted to receive the data output from the primary FIFO, in which the clock signal with evenly distributed gaps output from the smoothing control module is utilized as a writing clock, the secondary FIFO is connected to the phase locking module, and is adapted to send positions of writing and reading pointers of the secondary FIFO to the phase locking module, so as to enable the phase locking module to perform phase locking in accordance with the positions of writing and reading pointers, to obtain a reading clock for the secondary FIFO and control the reading of demapped data from the secondary FIFO.

[0021] An embodiment of the present invention provides an asynchronous demapping circuit, which, in addition to the above described circuit for generating an asynchronous demapping clock, further includes:

a writing control module, which is adapted to receive the data to be demapped and a corresponding clock signal, and output a gapped clock as a writing clock for a FIFO;

the FIFO, which is adapted to receive the data to be demapped which are written into the FIFO in accordance with the gapped clock from the writing control module and control the reading of demapped data from the FIFO by utilizing the demapping clock output from the phase locking module as a reading clock.

[0022] As can be seen from the above description, with the method of the present invention, a low-jittering ODU clock signal may be recovered from the SDH, thereby a high-performance demapped ODU data may be obtained from the asynchronous demapping process in OTN.

[0023] The method for clock generation provided in the embodiments of the present invention is applicable to a variety of asynchronous demapping processes in OTN and can obtain high-performance clock signals.

[0024] In summary, the method according to the embodiments of the present invention can effectively filter off the jittering created during asynchronous mapping/demapping processes and thus ensure a high-performance clock output. Furthermore, the method is applicable to not only mapping from OTN to SDH but also other asynchronous demapping processes, e.g., mapping from SDH to OTN.

Brief Description of the Drawings

[0025]

Fig.1 is a structural representation of the mapping from ODU1 to C-4-17c;

Fig.2 is a schematic diagram of an asynchronous demapping circuit in the prior art;

Fig.3 is a schematic diagram of a first asynchronous demapping circuit according to an embodiment of the present invention;

Fig.4 is a schematic diagram illustrating the principle for generating clock by a writing control module;

Fig.5 is a schematic diagram of a second asynchronous demapping circuit according to an embodiment of the present invention;

Fig.6 is a schematic diagram illustrating the principle of the ODU clock generating module as shown in Fig.5;

Fig.7 is a schematic diagram of the clock signals as shown in Fig.5.

Detailed Description of the Embodiments

[0026] The following description takes ODU1 data as an example since the demapping procedures for various ODU data are similar.

[0027] The embodiments of the present invention are directed to smooth a clock signal in accordance with the characteristics of the data to be processed so as to obtain a smooth clock signal; then, a phase locking is performed in accordance with a signal that reflects the writing and reading conditions of data of an FIFO, in order to obtain a low-jittering clock signal.

[0028] In particular, a method of obtaining asynchronous demapping clock according to an embodiment of the present invention includes:

[0029] First, the data to be demapped and the corresponding clock signal are processed to obtain a smoothed clock with even gaps;

[0030] Specifically, a predefined scheduling pattern may be utilized to smooth the corresponding clock signal to obtain a smoothed clock with even gaps. The scheduling pattern is obtained through calculation in accordance with the characteristics of the data to be demapped.

[0031] Next, a phase locking is performed in accordance with a signal that reflects the writing and reading conditions of data of the FIFO, to obtain the clock signal required for demapping. Particularly, the phase locking can be implemented by using either of the following two approaches:

(1) The data to be demapped is written into the FIFO based on the smoothed clock, and then a phase locking is performed in accordance with the positions of the writing and reading pointers of the FIFO to obtain the required ODU (Optical channel Data Unit) clock signal;

(2) A phase locking is performed for the smoothed clock to obtain the required ODU clock signal.

[0032] Other embodiments of the present invention will be detailed below.

[0033] In an embodiment, a circuit for obtaining an asynchronous demapping clock includes:

a smoothing control module, which receives the data to be demapped and the corresponding clock signal, and is adapted to obtain and output a smoothed clock with even gaps in accordance with the data to be demapped and the corresponding clock signal;

a phase locking module, which is connected to the output of the smoothing control module, and is adapted to perform a phase locking for the smoothed clock to obtain the demapping clock. Particularly, the phase locking processing includes phase discrimination and low pass filtering, etc..

[0034] An asynchronous demapping circuit for the data to be demapped based on the above described circuit for obtaining an asynchronous demapping clock is shown in Fig.3. The asynchronous demapping circuit includes a writing control module, a smoothing control module, a phase locking module, and an FIFO, wherein:

[0035] The writing control module is adapted to receive the data to be demapped and the corresponding clock signal, and output a gapped clock to the FIFO as the writing clock of the FIFO.

[0036] The smoothing control module is adapted to smooth the corresponding clock signal of the data to be demapped to obtain a smoothed clock with even gaps and send the smoothed clock to the phase locking module.

[0037] The phase locking module, i.e., the ODU1 clock generating module as shown in fig.3, includes a phase discriminator PD, a low-pass filter LPF, and a voltage controlled oscillator VCO. The phase locking module is adapted to perform a phase locking for the smoothed clock and obtain an asynchronous demapping clock.

[0038] The FIFO is adapted to receive the data to be demapped which are written into the FIFO in accordance with the gapped clock CLK output from the writing control module. The FIFO also utilizes the demapping clock, i.e., ODU1 clock, output from the phase locking module as the reading clock to control the reading of the demapped data output from the FIFO.

[0039] In addition, the embodiments of the present invention also provide another asynchronous demapping circuit based on the above described circuit for obtaining an asynchronous demapping clock, as shown in fig.5. This asynchronous demapping circuit includes: a writing control module, a smoothing control module, a primary FIFO1, a secondary FIFO2, and an ODU1 clock generating module (i.e., a phase locking module). The connection relationship between the modules and the functions of the modules will be described in detail below.

(1) The writing control module

[0040] The writing control module is adapted to generate a gapped clock CLKb in accordance with an STM-N clock and the actual data (i.e., the STM-N data as shown in Fig. 5) through the following procedures: first, the overhead in STM-N data is stripped off, that is, a gap is generated in the clock at the position of overhead, so as to produce a C-4-17c clock. Next, a gap is generated in the clock at the position of the padding bits on the basis of the C-4-17c clock, that is, the padding bits in C-4-17c are removed, so as to produce a clock CLKb, as shown in Fig.4; then, the actual data is written into the primary FIFO 1 under the control of the clock CLKb.

(2) The smoothing control module

[0041] The smoothing control module is adapted to produce a gapped clock CLKa in accordance with the STM-N clock and the actual data to control the rate for reading data from the primary FIFO 1; the clock CLKa is a clock signal with evenly distributed gaps, i.e., a smoothed clock;

[0042] Depending on the actual structure for mapping ODU1 to C-4-17c, the clock CLKa may be a gapped clock of 155MHz, then the data DATAa output from the primary FIFO 1 have a 17-bit width. The CLKa may also be a clock of any other frequency. For the frequency of 155MHz, a 6.4ns jittering will occur whenever a clock gap is produced. Therefore, the higher the clock frequency is, the smaller the clock jittering per gap will be.

[0043] The smoothing control module may utilize a predefined scheduling pattern to achieve an even distribution of clock gaps. The calculation method for the corresponding scheduling pattern in the case of a 17-bit data width and a 155MHz clock frequency will be described below:

[0044] As shown in Fig.1, a frame includes 9 subframes, each of the subframes includes 5 blocks, each block is used as a scheduling cycle, therefore:

1 scheduling cycle = $(270 \times 8)/5=432$ cycles of 155M;

[0045] The payloads to be read in 1 scheduling cycle = $17 \times 51D$ or $17 \times 51D+1D$ bytes.

[0046] Thus, without the "S" byte, the number of payloads (17 bits) to be read in 1 scheduling cycle = $(17\times51D)/17=408$. That is, for a block with $17\times51D$ payloads with the "S" byte omitted, a scheduling pattern 408 can be used. In that way, the writing into primary FIFO1 and the reading from FIFO1 may be balanced.

[0047] Taking the "S" byte into account, for blocks in which the "S" byte is valid, a scheduling pattern 409 may be used. In that case, the writing into FIFO1 and the reading from FIFO1 may be balanced, as long as there are 17 blocks in which the "S" bytes are valid, in which 8 blocks employ the scheduling pattern 409 and the other 9 blocks employ the scheduling pattern 408.

[0048] Therefore, by choosing between the two scheduling patterns <432, 408> and <432, 409>, the CLKa may smooth the clock gaps. <432, 308> indicates that 408 cycles of 432 cycles are valid, in other words, there are 432-408=24 clock gaps.

[0049] The distribution of gaps in <432, 408> and <432, 409> patterns can be determined based on the principle of even gap distribution. For example, in the case of <432, 408> pattern, there are 408 valid cycles in 432 cycles of 155M and altogether 24 gaps. If the gaps are distributed evenly, i.e., 432/24=18, the scheduling pattern can be designed as 24 consecutive cycles of <18, 17>. For each <18, 17> cycle, the gap can be in the 9th cycle. In the case of <432, 409> pattern, the pattern can be designed as 12 cycles of <18, 17>, then 1 cycle of <18, 18>, and consequently 11 cycles of <18, 17>, with 23 gaps altogether.

[0050] Thus, a smoothed clock with even gaps may be obtained by use of the smoothing control module.

(3) the ODU1 clock generating module (i.e., the phase locking module)

[0051] As shown in Fig.6, the ODU1 clock generating module mainly includes a phase discriminator PD, a low-pass filter LPF, a reverse control sub-module, Digital to Analog conversion sub-module D/A, and a Voltage-Controlled Oscillator VCO. The phase discriminator reads the positions of writing and reading pointers of the secondary FIFO2 to obtain the difference in pointer positions. The difference in pointer positions is the actual remaining amount of data, which is referred to as A. The remaining amount of data A reflects the difference between current data input into FIFO2 and the current data output from FIFO2, i.e., the phase difference between clock CLKa and ODU1 clock. The LPF sub-module performs a digital low-pass filtering for each obtained A (A1, A2, A3, ...), and sends the filtered result B to the reverse control sub-module;

[0052] Firstly, the reverse control sub-module sends a mean value to the D/A conversion sub-module to control the output from the VCO. Next, the reverse control sub-module compares each obtained B (B1, B2, B3, ...). If the value of B is increasing, it means that the frequency of ODU1 clock output from the VCO is lower than that of CLKa. Thus, the data sent to the D/A conversion sub-module needs to be increased, so as to increase the frequency of ODU1 clock output from the VCO. Otherwise, the data.sent to the D/A conversion sub-module needs to be decreased, so as to decrease the frequency of ODU1 clock output from the VCO. The above procedure may be repeated so as to balance the ODU1 clock output from VCO with the CLKa.

[0053] The time relationships between the clock signals CLKb, CLKa, and ODU1 obtained through the method according to the embodiments of the invention are shown in Fig.7. In Fig.7, the characteristics of the clock signals are also illustrated. In addition, it can be seen that, with.the method according to the embodiments of the invention, a desired clock signal with low-jittering and high-performance may be produced.

[0054] In addition, in the embodiments of the present invention, a Direct Digital Synthesis (DDS) module may be used instead of the D/A conversion sub-module and VCO sub-module, to produce the ODU1 clock of corresponding frequency in accordance with the data input.

[0055] In conclusion, with the method according to the embodiments of the present invention, jittering created during asynchronous mapping/demapping process may be filtered off effectively, and a high-performance clock output may be guaranteed. Furthermore, the method according to the embodiments of the present invention is applicable to not only mapping from OTN to SDH but also other asynchronous demapping processes, for example, mapping from SDH to OTN, thereby improving the data demapping performance effectively.

[0056] While the present invention has been described with respect to the embodiments described above, it is to be understood that the protection scope of the present invention should not be limited to those specific embodiments. Those skilled in the art can easily make variations or replacements to the embodiments, without departing from the technical scope disclosed in the present invention. Any of such variations or replacements shall fall into the protection scope of the present invention. Therefore, the protection scope of the present invention shall be defined by the following claims.

Claims

1. A method of obtaining asynchronous demapping clock (ODU1 clock), comprising:

   obtaining a clock signal (CLKa) with evenly distributed gaps in accordance with data (STM-N data) to be demapped and a corresponding clock signal (STM-N clock), comprising smoothing the corresponding clock signal (STN-M clock) with a predefined scheduling pattern, and obtaining the clock signal (CLKa) with evenly distributed gaps, wherein the scheduling pattern is obtained through calculation in accordance with the data (STN-M data) to be demapped; and performing phase locking to the clock signal (CLKa) with evenly distributed gaps in accordance with a signal deflecting writing and reading conditions of data of a First In First Out (FIFO), to obtain a clock signal (ODU1 clock) required for demapping.

2. The method according to any one of claims 1, wherein performing phase locking comprises:

   writing the data (STN-M data) to be demapped into the First In First Out (FIFO), based on the clock signal (CLKa) with evenly distributed gaps; performing phase locking in accordance with positions of reading and writing pointers of the First In First Out (FIFO) to obtain the a required Optical Channel Data Unit clock signal (ODU1 clock).

3. The method according to any one of claims 1, wherein performing phase locking comprises:

   performing phase discrimination, low pass filtering, and voltage-controlled oscillation for the clock signal (CLKa) with evenly distributed gaps, and obtaining the required Optical Channel Data Unit clock signal (ODU1 clock).

4. A circuit for generating an asynchronous demapping

clock (ODU1 clock), comprising:

a smoothing control module, which is adapted to obtain and output a clock signal (CLKa) with evenly distributed gaps in accordance with data (STM-N data) to be mapped and a corresponding clock signal (STM-N clock), wherein obtaining a clock signal (CLKa) with evenly distributed gaps comprises smoothing the corresponding clock signal (STN-M clock) with a predefined scheduling pattern, and obtaining the clock signal (CLKa) with evenly distributed gaps, and the scheduling pattern is obtained through calculation in accordance with the data (STN-M data) to be demapped; and
a phase locking module, which is adapted to perform phase locking to the clock signal (CLKa) with evenly distributed gaps input from the smoothing control module in accordance with a signal reflecting writing and reading conditions of data of a First In First Out (FIFO) so as to obtain a demapping clock (ODU1 clock).

5. The circuit according to claim 4, wherein the phase locking module comprises a phase discriminator (PD), a low-pass filter (LPF), and a voltage controlled oscillator (VCO), the signal reflecting writing and reading conditions of data of the First In First Out (FIFO) is processed by the phase discriminator (PD), the low-pass filter (LPF), and the voltage controlled oscillator (VCO) in turn so as to obtain the asynchronous demapping clock (ODU1 clock).

6. The circuit according to claim 4, wherein the phase locking module comprises a phase discriminator (PD), a low-pass filter (LPF), a reverse control sub-module, a Digital/Analogue conversion sub-module (D/A), and a voltage controlled oscillator (VCO), the signal reflecting writing and reading conditions of data of the First In First Out (FIFO) is processed by the phase discriminator (PD), the low-pass filter (LPF), the reverse control sub-module, the Digital/Analogue conversion sub-module(D/A), and the voltage controlled oscillator (VCO) in turn so as to obtain the asynchronous demapping clock (ODU1 clock).

7. The circuit according to claim 4, wherein the phase locking module comprises a phase discriminator (PD), a low-pass filter (LPF), a reverse control sub-module, and a direct digital synthesis module; the signal reflecting writing and reading conditions of data of the First In First Out (FIFO) is processed by the phase discriminator (PD), the low-pass filter (LPF), the reverse control sub-module, and the direct digital synthesis module in turn so as to obtain the asynchronous demapping clock (ODU1 clock).

8. An asynchronous demapping circuit comprising the circuit according to any one of claims 4-7, wherein the asynchronous demapping circuit further comprises:

a writing control module, which is adapted to receive data (STM-N data) to be demapped and corresponding clock signal (STM-N clock), and output a gapped clock (CLKb) as a writing clock of a primary FIFO (FIFO1);
the primary FIFO (FIFO1), which is adapted to receive the data (STM-N data) to be demapped which are written into the primary FIFO (FIFO1) in accordance with the gapped clock (CLKb) output from the writing control module and control the reading of data from the primary FIFO (FIFO1) by utilizing the clock signal (CLKa) with evenly distributed gaps output from the smoothing control module as a reading clock;
the secondary FIFO (FIFO2), which is adapted to receive the data (DATAa) output from the primary FIFO(FIFO1), wherein the clock signal (CLKa) with evenly distributed gaps output from the smoothing control module is utilized as a writing clock of the secondary FIFO (FIFO2), the secondary FIFO (FIFO2) is connected to a phase locking module, and is adapted to send positions of writing and reading pointers of the secondary FIFO (FIFO2) to the phase locking module, so as to enable the phase locking module to perform phase locking in accordance with the positions of writing and reading pointers, to obtain a reading clock (ODU1 clock) for the secondary FIFO (FIFO2) to control the reading of demapped data from the secondary FIFO (FIFO2).

9. An asynchronous demapping circuit comprising the circuit according to any one of claims 4-7, wherein the asynchronous demapping circuit further comprises:

a writing control module, which is adapted to receive the data (STM-N data) to be demapped and a corresponding clock signal (STM-N clock), and output a gapped clock (CLK) as a writing clock for the First In First Out (FIFO);
the First In First Out (FIFO), which is adapted to receive the data (STM-N data) to be demapped which are written into the First In First Out (FIFO) in accordance with the gapped clock (CLK) from the writing control module and control the reading of demapped data (ODU1 data) from the First In First Out (FIFO) by utilizing the demapping clock (ODU1 clock) output from the phase locking module as a reading clock of the First In First Out (FIFO).

Patentansprüche

1. Verfahren zum Erhalten eines asynchronen Demapping-Taktes (ODU1 clock), umfassend:

   Erhalten eines Taktsignals (CLKa) mit gleichmäßig verteilten Abständen entsprechend den zu demappenden Daten (STM-N data) und einem entsprechenden Taktsignal (STM-N clock), umfassend das Glätten des entsprechenden Taktsignals (STN-M clock) mit einem vordefinierten Scheduling-Muster, und Erhalten des Taktsignals (CLKa) mit gleichmäßig verteilten Abständen, wobei das Scheduling-Muster durch Berechnung entsprechend der zu demappenden Daten (STN-M data) erhalten wird; und
   Durchführen einer Phasenverriegelung mit dem Taktsignal (CLKa) mit gleichmäßig verteilten Abständen entsprechend einem Signal, das Schreib- und Lesebedingungen von Daten eines First-In-First-Out-Speichers (FIFO) widerspiegelt, um ein Taktsignal (ODU1 clock) zu erhalten, das für das Demapping benötigt wird.

2. Verfahren nach Anspruch 1, wobei die Durchführung der Phasenverriegelung umfasst:

   Schreiben der zu demappenden Daten (STN-M data) in den First-In-First-Out-Speicher (FIFO) basierend auf dem Taktsignal (CLKa) mit gleichmäßig verteilten Abständen;
   Durchführen der Phasenverriegelung entsprechend der Positionen von Lese- und Schreibzeigern des First-In-First-Out-Speichers (FIFO), um das erforderliche Taktsignal (ODU1 clock) einer Dateneinheit eines optischen Kanals zu erhalten.

3. Verfahren nach Anspruch 1, wobei die Durchführung der Phasenverriegelung umfasst:

   Durchführen einer Phasen-Unterscheidung, Tiefpassfilterung und spannungsgesteuerten Oszillation für das Taktsignal (CLKa) mit gleichmäßig verteilten Abständen und Erhalten des erforderlichen Taktsignals der Dateneinheit eines optischen Kanals (ODU1 clock).

4. Schaltkreis zum Erzeugen eines asynchronen Demapping-Taktes (ODU1 clock), umfassend:

   ein Glättungs-Steuerungs-Modul, das angepasst ist, ein Taktsignal (CLKa) mit gleichmäßig verteilten Abständen entsprechend den zu mappenden Daten (STM-N data) und einem entsprechenden Taktsignal (STM-N clock) zu erhalten und auszugeben, wobei das Erhalten eines Taktsignals (CLKa) mit gleichmäßig verteilten Abständen es umfasst, das entsprechende Taktsignal (STN-M clock) mit einem vordefinierten Scheduling-Muster zu glätten und das Taktsignal (CLKa) mit gleichmäßig verteilten Abständen zu erhalten, und das Scheduling-Muster wird durch Berechnung entsprechend der zu demappenden Daten (STN-M data) erhalten; und
   ein Phasenverriegelungs-Modul, das angepasst ist, die Phasenverriegelung auf das Taktsignal (CLKa) mit gleichmäßig verteilten Abständen, das vom Glättungs-Steuerungs-Modul eingegeben wird, entsprechend einem Signal durchzuführen, das Schreib- und Lesebedingungen von Daten eines First-In-First-Out-Speichers (FIFO) widerspiegelt, um einen Demapping-Takt (ODU1 clock) zu erhalten.

5. Schaltkreis nach Anspruch 4, wobei das Phasenverriegelungs-Modul einen Phasen-Diskriminator (PD), ein Tiefpassfilter (LPF) und einen spannungsgesteuerten Oszillator (VCO) enthält, wobei das Signal, das Schreib- und Lesebedingungen von Daten des First-In-First-Out-Speichers (FIFO) widerspiegelt, der Reihe nach vom Phasen-Diskriminator (PD), vom Tiefpassfilter (LPF) und dem spannungsgesteuerten Oszillator (VCO) verarbeitet wird, um den asynchronen Demapping-Takt (ODU1 clock) zu erhalten.

6. Schaltkreis nach Anspruch 4, wobei das Phasenverriegelungs-Modul einen Phasen-Diskriminator (PD), ein Tiefpassfilter (LPF), ein Rückwärts-Steuerungs-Untermodul, ein Digital-/Analog-Wandlungs-Untermodul (D/A) und einen spannungsgesteuerten Oszillator (VCO) enthält, wobei das Signal, das Schreib- und Lesebedingungen von Daten des First-In-First-Out-Speichers (FIFO) widerspiegelt, der Reihe nach vom Phasen-Diskriminator (PD), vom Tiefpassfilter (LPF), vom Rückwärts-Steuerungs-Untermodul, vom Digital-/Analog-Wandlungs-Untermodul (D/A) und vom spannungsgesteuerten Oszillator (VCO) verarbeitet wird, um den asynchronen Demapping-Takt (ODU1 clock) zu erhalten.

7. Schaltkreis nach Anspruch 4, wobei das Phasenverriegelungs-Modul einen Phasen-Diskriminator (PD), ein Tiefpassfilter (LPF), ein Rückwärts-Steuerungs-Untermodul und ein Modul zur direkten Digital-Synthese enthält, wobei das Signal, das Schreib- und Lesebedingungen von Daten des First-In-First-Out-Speichers (FIFO) widerspiegelt, der Reihe nach vom Phasen-Diskriminator (PD), vom Tiefpassfilter (LPF), vom Rückwärts-Steuerungs-Untermodul und vom Modul zur direkten Digital-Synthese verarbeitet wird, um den asynchronen Demapping-Takt (ODU1 clock) zu erhalten.

8. Asynchroner Demapping-Schaltkreis, der den

Schaltkreis nach einem beliebigen der Ansprüche 4-7 enthält, wobei der asynchrone Demapping-Schaltkreis ferner umfasst:

ein Schreib-Steuerungs-Modul, das angepasst ist, zu demappende Daten (STM-N data) und das entsprechende Taktsignal (STM-N clock) zu empfangen und einen Takt mit Abständen (CLKb) als Schreibtakt eines primären FIFO-Speichers (FIFO1) auszugeben;
den primären FIFO-Speicher (FIFO1), der angepasst ist, die zu demappenden Daten (STM-N data) zu empfangen, die entsprechend dem Takt mit Abständen (CLKb), der vom Schreib-Steuerungs-Modul ausgegeben wird, in den primären FIFO-Speicher (FIFO1) geschrieben werden, und das Lesen der Daten aus dem primären FIFO-Speicher (FIFO1) zu steuern, indem das Taktsignal (CLKa) mit gleichmäßig verteilten Abständen, das vom Glättungs-Steuerungs-Modul ausgegeben wird, als Lesetakt benutzt wird;
den sekundären FIFO-Speicher (FIFO2), der angepasst ist, die vom primären FIFO-Speicher (FIFO1) ausgegebenen Daten (DATAa) zu empfangen, wobei das Taktsignal (CLKa) mit gleichmäßig verteilten Abständen, das vom Glättungs-Steuerungs-Modul ausgegeben wird, als Schreibtakt des sekundären FIFO-Speicher (FIFO2) benutzt wird, wobei der sekundäre FIFO-Speicher (FIFO2) mit einem Phasenverriegelungs-Modul verbunden und angepasst ist, Positionen von Schreib- und Lese-Zeigern des sekundären FIFO-Speicher (FIFO2) zum Phasenverriegelungs-Modul zu senden, um das Phasenverriegelungs-Modul in die Lage zu versetzen, eine Phasenverriegelung entsprechend der Positionen von Schreib-und Lese-Zeigern durchzuführen, um einen Lesetakt (ODU1clock) für den sekundären FIFO-Speicher (FIFO2) zu erhalten, um das Lesen von Daten, deren Demapping durchgeführt wurde, aus dem sekundären FIFO-Speicher (FIFO2) zu steuern.

9. Asynchroner Demapping-Schaltkreis, der den Schaltkreis nach einem beliebigen der Ansprüche 4-7 enthält, wobei der asynchrone Demapping-Schaltkreis ferner umfasst:

ein Schreib-Steuerungs-Modul, das angepasst ist, zu demappende Daten (STM-N data) und ein entsprechendes Taktsignal (STM-N clock) zu empfangen und einen Takt mit Abständen (CLK) als Schreibtakt für den First-In-First-Out-Speicher (FIFO) auszugeben;
den First-In-First-Out-Speicher (FIFO), der angepasst ist, die zu demappenden Daten (STM-N data) zu empfangen, die entsprechend dem Takt mit Abständen (CLK) vom Schreib-Steuerungs-Modul in den First-In-First-Out-Speicher (FIFO) geschrieben werden, und das Lesen der Daten, deren Demapping durchgeführt wurde (ODU1 data), aus dem First-In-First-Out-Speicher (FIFO) zu steuern, indem der Demapping-Takt (ODU1 clock), der vom Phasenverriegelungs-Modul ausgegeben wird, als Lesetakt des First-In-First-Out-Speichers (FIFO) benutzt wird.

Revendications

1. Méthode pour l’acquisition d’une horloge de démappage asynchrone (ODU1 clock), comprenant :

l’acquisition d’un signal d’horloge (CLKa) avec des intervalles uniformément répartis en conformité avec des données (STM-N data) devant être démappées et un signal d’horloge (STM-N clock) correspondant, comprenant le lissage du signal d’horloge (STN-M clock) afférent selon un modèle de programmation prédéfini, et l’acquisition du signal d’horloge (CLKa) avec des intervalles uniformément répartis, dans laquelle le modèle de programmation est obtenu par calcul conformément aux données (STN-M data) devant être démappées ; et
l’exécution du verrouillage de phase avec le signal d’horloge (CLKa) avec des intervalles uniformément répartis en conformité avec un signal reflétant les conditions d’écriture et de lecture des données d’un premier-entré-premier-sorti (FIFO) pour acquérir un signal d’horloge (ODU1 clock) requis pour le démappage.

2. Méthode selon l’une quelconque des revendications 1, dans laquelle l’exécution du verrouillage de phase comprend :

l’écriture des données (STN-M data) devant être démappées dans le premier-entré-premier-sorti (FIFO) sur la base du signal d’horloge (CLKa) avec des intervalles uniformément répartis ;
l’exécution du verrouillage de phase conformément aux positions des pointeurs de lecture et d’écriture du premier-entré-premier-sorti (FIFO) pour acquérir le signal d’horloge (ODU1 clock) d’unité de données de canal optique.

3. Méthode selon l’une quelconque des revendications 1, dans laquelle l’exécution du verrouillage de phase comprend :

l’exécution de la discrimination de phase, du filtrage passe-bas et de l’oscillation commandée en tension pour le signal d'horloge (CLKa) avec des intervalles uniformément répartis et l'acquisition du signal d'horloge d'unité de données de canal optique (ODU1 clock).

4. Circuit pour la génération d'une horloge de démappage asynchrone (ODU1 clock), comprenant :

un module de commande de lissage, lequel est adapté pour acquérir et délivrer un signal d'horloge (CLKa) avec des intervalles uniformément répartis sur la base des données (STM-N data) devant être mappées et un signal d'horloge correspondant (STM-N clock), dans lequel l'acquisition d'un signal d'horloge (CLKa) avec des intervalles uniformément répartis comprend le lissage du signal d'horloge correspondant (STN-M clock) avec un modèle de programmation prédéfini et l'acquisition du signal d'horloge (CLKa) avec des intervalles uniformément répartis, et le modèle de programmation est obtenu par calcul sur la base des données (STN-M data) devant être démappées ; et

un module de verrouillage de phase, lequel est adapté pour exécuter le verrouillage de phase sur le signal d'horloge (CLKa) avec des intervalles uniformément répartis entré à partir du module de commande de lissage suivant un signal reflétant les conditions d'écriture et de lecture des données d'un premier-entré-premier-sortie (FIFO) de manière à acquérir une horloge de démappage (ODU1 clock).

5. Circuit selon la revendication 4, dans lequel le module de verrouillage de phase comprend un discriminateur de phase (PD), un filtre passe-bas (LPF) et un oscillateur commandé en tension (VCO), le signal reflétant les conditions d'écriture et de lecture des données du premier-entré-premier-sortie (FIFO) est traité à tour de rôle par le discriminateur de phase (PD), le filtre passe-bas (LPF) et l'oscillateur commandé en tension (VCO) de manière à acquérir l'horloge de démappage asynchrone (ODU1 clock).

6. Circuit selon la revendication 4, dans lequel le module de verrouillage de phase comprend un discriminateur de phase (PD), un filtre passe-bas (LPF), un sous-module de commande réversible, un sous-module de conversion numérique-analogique (D/A) et un oscillateur commandé en tension (VCO), le signal reflétant les conditions d'écriture et de lecture des données du premier-entré-premier-sortie (FIFO) est traité à tour de rôle par le discriminateur de phase (PD), le filtre passe-bas (LPF), le sous-module de commande réversible, le sous-module de conversion numérique-analogique (D/A) et l'oscillateur commandé en tension (VCO) de manière à acquérir l'horloge de démappage asynchrone (ODU1 clock).

7. Circuit selon la revendication 4, dans lequel le module de verrouillage de phase comprend un discriminateur de phase (PD), un filtre passe-bas (LPF), un sous-module de commande réversible et un module de synthèse numérique directe ; le signal reflétant les conditions d'écriture et de lecture des données du premier-entré-premier-sortie (FIFO) est traité à tour de rôle par le discriminateur de phase (PD), le filtre passe-bas (LPF), le sous-module de commande réversible et le module de synthèse numérique directe de manière à acquérir l'horloge de démappage asynchrone (ODU1 clock).

8. Circuit de démappage asynchrone comprenant le circuit selon l'une quelconque des revendications 4 à 7, dans lequel le circuit de démappage asynchrone comprend en outre :

un module de commande d'écriture, lequel est adapté pour recevoir les données (STM-N data) devant être démappées et le signal d'horloge (STM-N clock) correspondant, et délivrer une horloge sans chevauchement (CLKb) comme horloge d'écriture d'un premier-entré-premier-sorti (FIFO) primaire (FIFO1) ;

le FIFO primaire (FIFO1), lequel est adapté pour recevoir les données (STM-N data) devant être démappées, lesquelles sont écrites dans le FIFO primaire (FIFO1) conformément à l'horloge sans chevauchement (CLKb) délivrée par le module de commande d'écriture et commandent la lecture des données à partir du FIFO primaire (FIFO1) en utilisant le signal d'horloge (CLKa) avec des intervalles uniformément repartis délivré par le module de commande de lissage comme une horloge de lecture ;

le FIFO secondaire (FIFO2), lequel est adapté pour recevoir les données (DATAa) délivrées par le FIFO primaire (FIFO1), sachant que le signal d'horloge (CLKa) avec intervalles uniformément répartis délivré par le module de commande de lissage est utilisé comme horloge d'écriture du FIFO secondaire (FIFO2), ledit FIFO secondaire (FIFO2) est connecté à un module de verrouillage de phase et il est adapté pour envoyer les positions des pointeurs d'écriture et lecture du FIFO secondaire (FIFO2) au module de verrouillage de phase de manière à permettre au module de verrouillage de phase d'exécuter le verrouillage de phase conformément aux positions des pointeurs d'écriture et de lecture, d'acquérir une horloge de lecture (horloge ODU1) pour le FIFO secondaire (FIFO2) pour commander la lecture des données démappées à partir du FIFO secondaire (FIFO2).

9. Circuit de démappage asynchrone comprenant le circuit selon l'une quelconque des revendications 4 à 7, dans lequel le circuit de démappage asynchrone comprend en outre :

un module de commande d'écriture, lequel est adapté pour recevoir les données (STM-N data) devant être démappées et le signal d'horloge (STM-N clock) correspondant, et délivrer une horloge sans chevauchement (CLK) comme horloge d'écriture pour le premier-entré-premier-sorti (FIFO) ;
le premier-entré-premier-sorti (FIFO), lequel est adapté pour recevoir les données (STM-N data) devant être démappées, lesquelles sont écrites dans le premier-entré-premier-sorti (FIFO) conformément à l'horloge sans chevauchement (CLK) à partir du module de commande d'écriture et commandent la lecture des données démappées (ODU1 data) à partir du premier-entré-premier-sorti (FIFO) en utilisant l'horloge de démappage (ODU1 clock) délivrée par le module de verrouillage de phase comme une horloge de lecture du premier-entré-premier-sorti (FIFO).

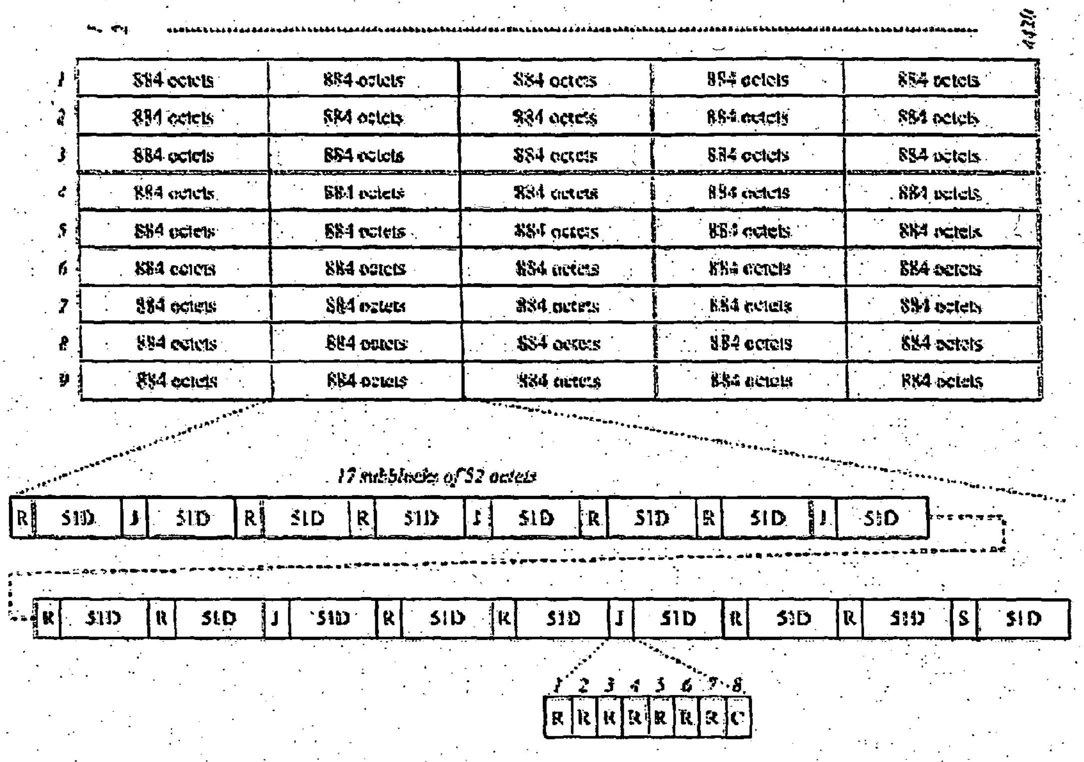
884 octets
17 subblocks of 52 octets
R
51D
J
S
C
1 2 3 4 5 6 7 8

Fig. 1

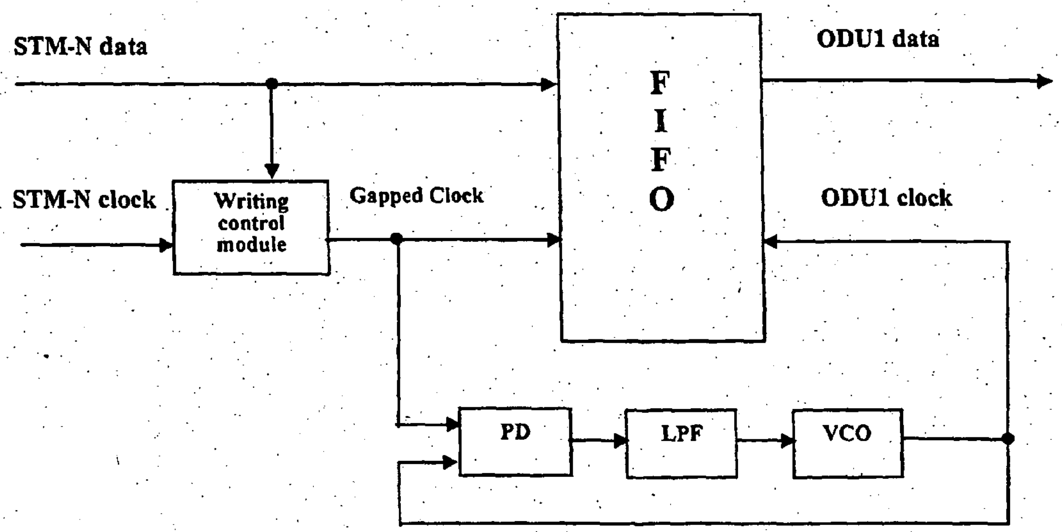
STM-N data
STM-N clock
Writing control module
Gapped Clock
FIFO
ODU1 data
ODU1 clock
PD
LPF
VCO

Fig. 2

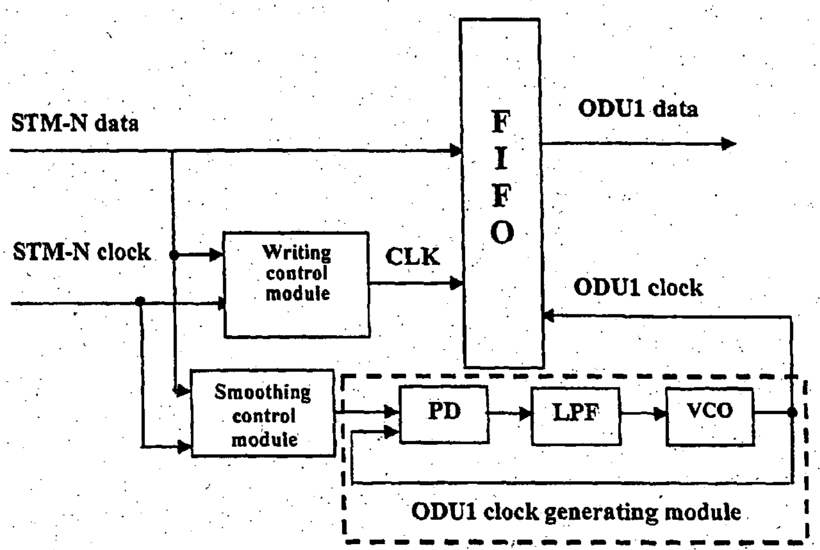
STM-N data
FIFO
ODU1 data
STM-N clock
Writing control module
CLK
ODU1 clock
Smoothing control module
PD
LPF
VCO
ODU1 clock generating module

Fig. 3

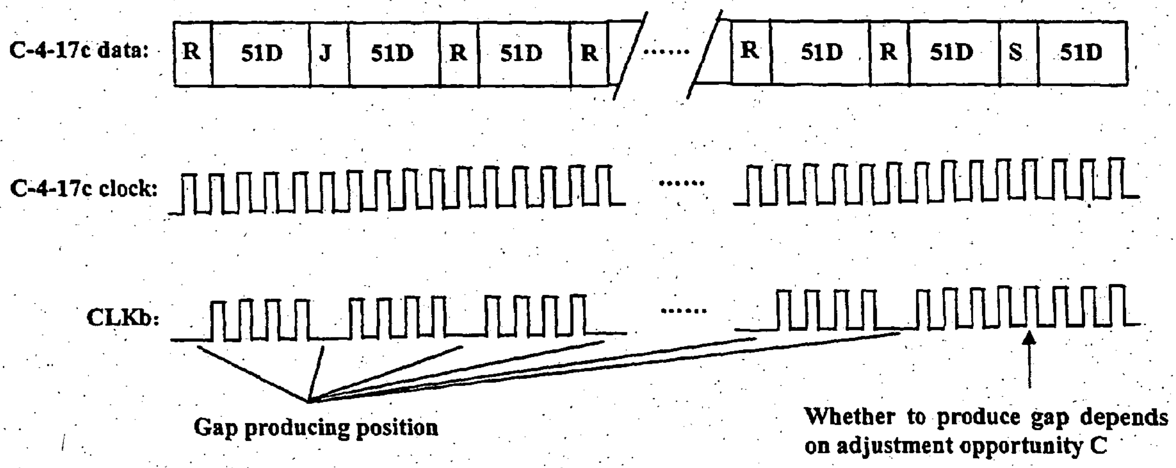
C-4-17c data:
R
51D
J
51D
R
51D
R
......
R
51D
R
51D
S
51D
C-4-17c clock:
CLKb:
Gap producing position
Whether to produce gap depends on adjustment opportunity C

Fig. 4

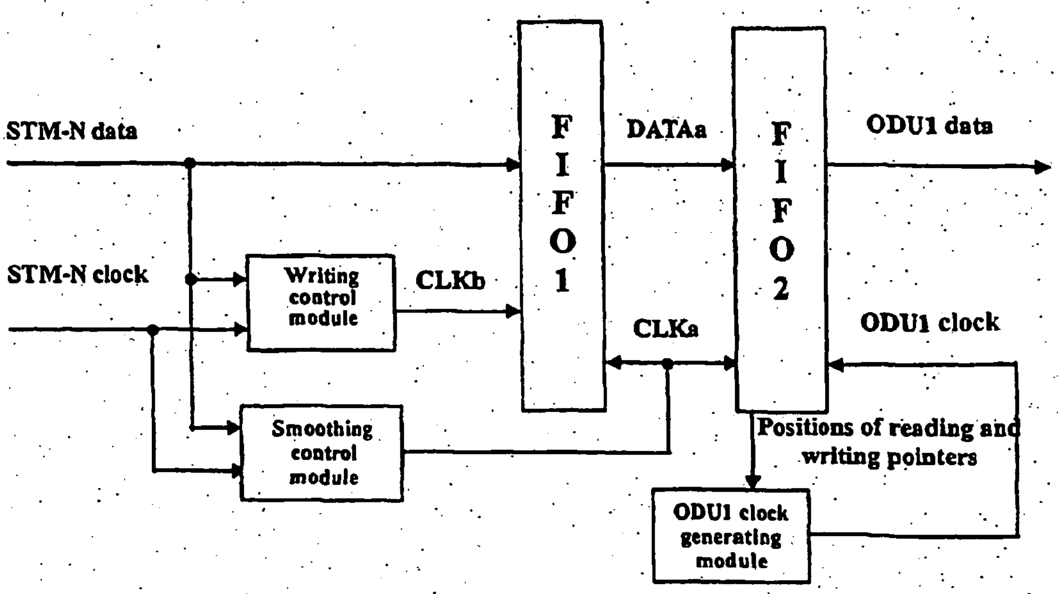
STM-N data
STM-N clock
Writing control module
CLKb
FIFO 1
DATAa
CLKa
FIFO 2
ODU1 data
ODU1 clock
Smoothing control module
Positions of reading and writing pointers
ODU1 clock generating module

Fig. 5

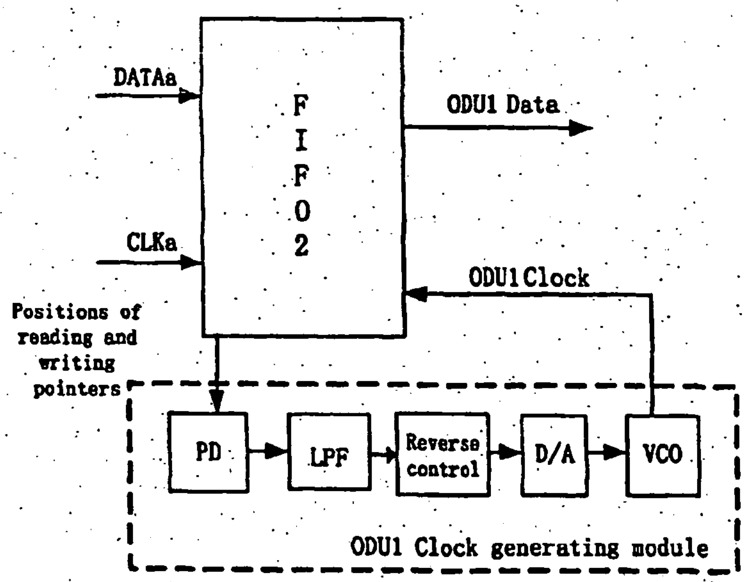
DATAa
CLKa
FIFO 2
ODU1 Data
ODU1 Clock
Positions of reading and writing pointers
PD
LPF
Reverse control
D/A
VCO
ODU1 Clock generating module

Fig. 6

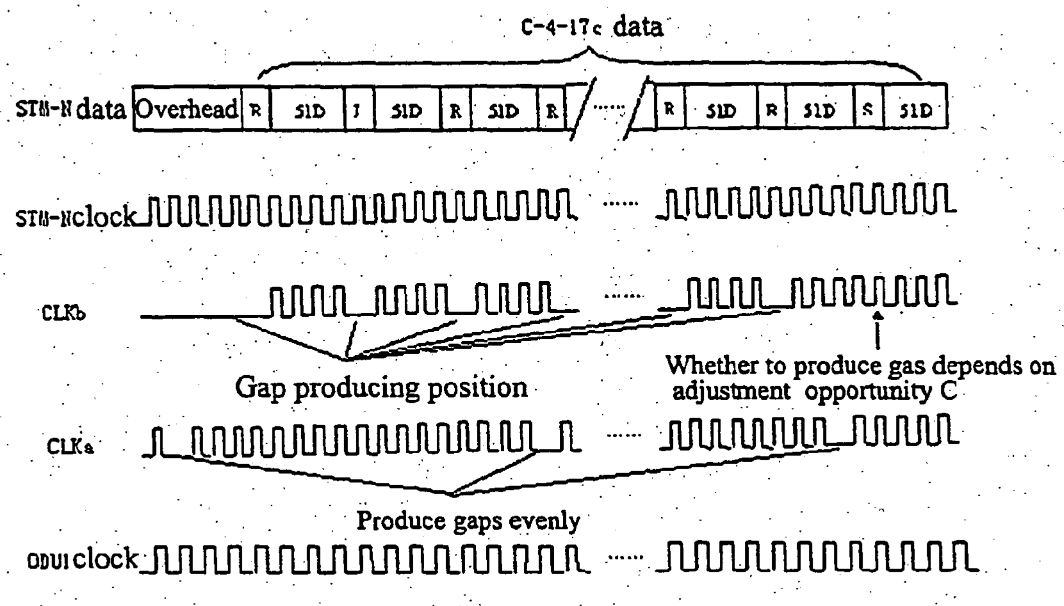
C-4-17c data
STM-N data
Overhead
R
51D
J
51D
R
51D
R
R
51D
R
51D
S
51D
STM-N clock
CLKb
Gap producing position
Whether to produce gas depends on adjustment opportunity C
CLKa
Produce gaps evenly
ODU1 clock

Fig. 7

REFERENCES CITED IN THE DESCRIPTION

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Patent documents cited in the description

- WO 9927669 A1 **[0008]**
- EP 1343261 A1 **[0009]**
- US 20050074032 A1 **[0010]**