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(54) **System and method of providing driving voltages to an RGBW display panel**

(57) A representative system comprises a data driver with a reference voltage generation circuit that is operative to provide reference voltages according to a white component signal (W) extracted from three color input signals (R,G,B), and a digital-to-analog (D/A) conversion unit that is operative to generate driving voltages according to the reference voltages, the three color input signals and the white component signal.

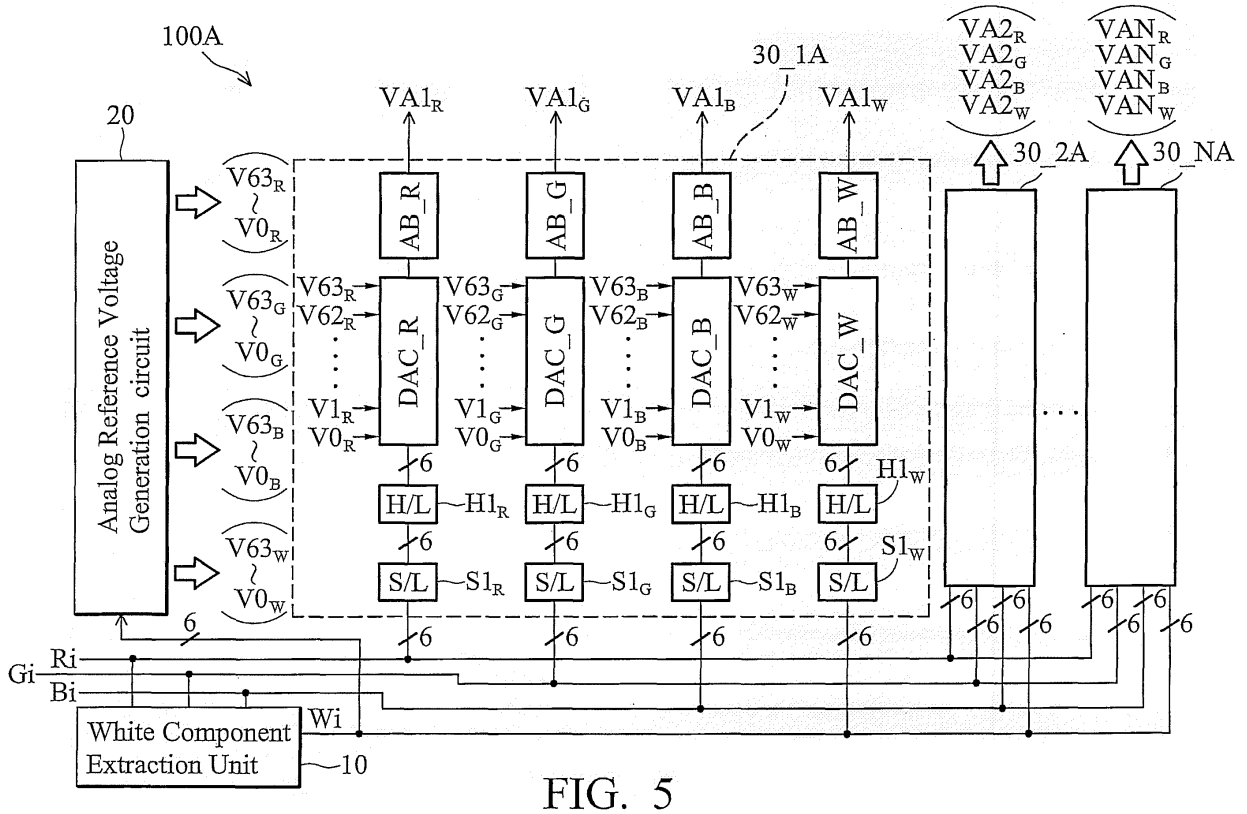

FIG. 5

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Description

BACKGROUND

[0001] The invention relates to panel displays, and more particularly, to systems and methods for providing driving voltages to RGBW display panels.

[0002] Color image display devices are well known and are based upon a variety of technologies such as cathode ray tubes, liquid crystal modulators and solid-state light emitters such as Organic Light Emitting Diodes (OLEDs). In a common OLED color image display device, a pixel includes red, green and blue colored subpixels. These light emitting colored subpixels define a color gamut, and by additively combining the illumination from each of these three subpixels, i.e. with the integrative capabilities of the human visual system, a wide variety of colors can be achieved. OLEDs may be used to generate color directly using organic materials to emit energy in desired portions of the electromagnetic spectrum, or alternatively, broadband emitting (apparently white) OLEDs may be attenuated with color filters to achieve red, green and blue output.

[0003] Images and data displayed on a color display device are typically stored and/or transmitted in three channels, that is, having these signals corresponding to a standard (e.g. RGB). It is also important to recognize that data typically is sampled to assume a particular spatial arrangement of light emitting elements. In an OLED display device, these light emitting elements are typically arranged side by side on a plane. Therefore, if incoming data is sampled for display on a color display device, the data will also be resampled for display on an OLED display having four subpixels per pixel rather than the three subpixels used in a three channel display device.

[0004] In this regard, Fig. 1A shows a conventional OLED subpixel driving circuit structure, and Fig. 1B shows RGBW subpixel arrangements of a conventional display panel. As shown in Fig. 1A, the subpixel is driven by the current 11 through the driving transistor T1. The driving transistor T1 outputs the current 11 according to the voltage V1.

[0005] Fig. 1C shows a conventional digital signal processing (DSP) structure for driving RGBW subpixels. As shown in Fig. 1C, RGB digital signals are sampled and held and output to a Gamma linear control unit. The Gamma linear control unit adjusts RGB digital signals for Gamma linearity and outputs to the conversion unit. The conversion unit converts the adjusted RGB digital signals to RGBW digital signals and outputs to a Gamma compensation unit. The Gamma compensation unit executes a Gamma compensation of the RGBW digital signals from the conversion unit for Gamma correction and outputs to a RGBW driver. The RGBW driver converts the RGBW digital signals to RGBW analog signals to drive corresponding RGBW subpixels.

[0006] Fig. 2A shows the relationship between the luminance of the OLED subpixel and the current I1. As shown, there is a linear relationship between the luminance of the OLED subpixel and the current I1. Fig. 2B shows the relationship between the current I1 of the driving transistor T1 and the voltage V1 to be non-linear. Fig. 2C shows the relationship between luminance of the OLED subpixel and observable brightness (gamma). Fig. 2D shows the relationship between observable brightness and voltage V1 applied to the driving transistor T1.

[0007] Thus, a gamma correction is required to compensate the non-linear relationship.

[0008] Conventionally, RGB data is converted to RGBW data through digital data processing (DSP). However, due to different optical characteristics (gamma correction) for each RGBW color, DSP typically requires a complicated algorithm to execute such conversion. Further, it may be difficult to obtain a precise analog output corresponding to the gamma correction for each color after using the complicated conversion algorithm.

[0009] For example, Fig. 3 shows a conventional method for converting RGB data to RGBW data. As shown in Fig. 3, the Min(R,G,B) is assumed to be W data, and R'G'B' data (driving the display device) can be obtained by removing the W component from the R,G,B components respectively. Fig. 4 shows another conventional method for converting RGB data to RGBW data. As shown in Fig. 4, the Min(R,G,B) is assumed to be W data, and the W component is converted to W' data in accordance with a characteristic of α*W, where α<1. The R'G'B' data are obtained by removing the W' component from the RGB components respectively. However, these two simple methods typically cannot precisely provide gamma correction for each color because of the non-linear relationship between driving voltage and observable brightness.

SUMMARY

[0010] Systems and method for providing driving voltages of RGBW display panels are disclosed. An exemplary embodiment of such a system comprises a data driver with a reference voltage generation circuit providing reference voltages according to a white component signal (W) extracted from three color input signals (R,G, B), and a digital-to-analog (D/A) conversion unit to generate driving voltages according to the reference voltages, the three color input signals and the white component signal.

[0011] An exemplary embodiment of a method for providing driving voltages of a RGBW display panel, comprises generating reference voltages according to a white component signal (W) extracted from three color input signals (R,G,B); and generating driving voltages according to the reference voltages, the three color input signals and the white component signal.

DESCRIPTION OF THE DRAWINGS

[0012] The invention can be more fully understood by

the subsequent detailed description and examples with reference made to the accompanying drawings, wherein:

Fig. 1A shows a conventional OLED subpixel driving circuit structure;
Fig. 1B shows RGBW pixel arrangements of conventional display panel;
Fig. 1C shows a conventional digital signal processing (DSP) structure for driving RGBW pixels;
Fig. 2A shows the relationship between the luminance of OLED and current;
Fig. 2B shows the relationship between current through the control transistor and driving voltage thereof;
Fig. 2C shows the relationship between luminance of the OLED and observable brightness;
Fig. 2D shows the relationship between observable brightness and driving voltage of driving transistor;
Fig. 3 shows a conventional method for converting RGB data to RGBW data;
Fig. 4 shows another conventional method for converting RGB data to RGBW data;
Fig. 5 shows an embodiment of a data driver;
Figs. 6A~6D show embodiments of a voltage generator;
Fig. 7 shows another embodiment of a data driver;
Figs. 8-1 and 8-2 show another embodiment of a data driver;
Fig. 9 is a schematic diagram of an embodiment of a display; and
Fig. 10 is a schematic diagram of an embodiment of an electronic device employing the display panel shown in Fig. 9.

DETAILED DESCRIPTION

[0013] Systems for providing driving voltages to display panels will now be described with reference to several exemplary embodiments. In this regard, an embodiment of a system providing driving voltages to an RGBW display panel is depicted in Fig. 5. As shown in Fig. 5, data driver 100A comprises a white component extraction unit 10, an analog reference voltage generation circuit 20 and N digital-to-analog (D/A) conversion units 30_1A~30_NA.

[0014] The white component extraction unit 10 extracts a white component signal Wi from three color input signals Ri, Gi and Bi. For example, three color input signals Ri, Gi and Bi can be 6 bit digital data, and the white component extraction unit 10 can be a minimum value detector. If color input signals R1, G1 and B1 are 110111, 010111 and 000111 respectively, the white component signal W1 can be 000111. Alternately, white component extraction unit 10 can output a suppressed white component signal W1 of 000011 according to the color input signal R1, G1 and B1.

[0015] Alternately, the white component signal Wi can be obtained by executing an AND logic operation to the three color input signals Ri, Gi and Bi. For example, when the color input signals R1, G1 and B1 are 110111, 010111 and 000111 respectively, the white component signal W1 can be 000111.

[0016] Conversely, the white component signal Wi can be obtained by executing an AND logic operation to M bits of the three color input signals Ri, Gi, Bi, and 0 < M < 6. For example, when M=2, a suppressed white component signal W1 of 000011 can be obtained according to the color input signal R1, G1 and B1.

[0017] The analog reference voltage generation circuit 20 generates four sets of reference voltages $V0_R$~$V63_R$, $V0_G$~$V63_G$, $V0_B$~$V63_B$ and $V0_W$~$V63_W$ for color input signal Ri, Gi and Bi and the white component signal Wi respectively, the reference voltages $V0_R$~$V63_R$, $V0_G$~$V63_G$ and $V0_B$~$V63_B$ are generated according to the white component signal Wi.

[0018] The D/A conversion units 30_1A~30_NA receive the reference voltages $V0_R$~$V63_R$, $V0_G$~$V63_G$, $V0_B$~$V63_B$ and $V0_W$~$V63_W$ from the analog reference voltage generation circuit 20 to generate corresponding driving voltages $VA1_R$~VAN_R, $VA1_G$~VAN_G, $VA1_B$~VAN_B and $VA1_W$~VAN_W according to the three color input signals Ri, Gi and Bi and the white component signal Wi. For example, the D/A conversion unit 30_1A receives the reference voltages $V0_R$~$V63_R$, $V0_G$~$V63_G$, $V0_B$~$V63_B$ and $V0_W$~$V63_W$ and generates corresponding driving voltages $VA1_R$, $VA1_G$, $VA1_B$ and $VA1_W$ according to the three color input signals R1, G1 and B1 and the white component signal W1 during a first period. The D/A conversion unit 30_2A receives the reference voltages $V0_R$~$V63_R$, $V0_G$~$V63_G$, $V0_B$~$V63_B$ and $V0_W$~$V63_W$ and generates corresponding driving voltages $VA2_R$, $VA2_G$, $VA2_B$ and $VA2_W$ according to the three color input signals R2, G2 and B2 and the white component signal W2 during a second period, and so on. Namely, all D/A conversion units 30_1A~30_NA employ the same type of analog reference voltage circuit which can generate different reference voltages $V0_R$~$V63_R$, $V0_G$~$V63_G$, $V0_B$~$V63_B$ and $V0_W$~$V63_W$ according to different white component signals Wi during different periods.

[0019] The D/A conversion units 30_1A~30_NA each comprise four sampling latches $S1_R$~$S1_W$, four holding latches $H1_R$~$H1_W$, four D/A converters DAC_R~DAC_W and four analog buffers AB_R~AB_W. The sampling latches $S1_R$~$S1_W$ sample the color input signals Ri, Gi and Bi and the white component signal Wi at one time. The holding latches $H1_R$~$H1_W$ hold the color input signals Ri, Gi and Bi and the white component signal Wi sampled by the sampling latches $S1_R$~$S1_W$. The D/A converters DAC_R~DAC_W convert the held color input signals Ri, Gi and Bi and the held white component signal Wi to corresponding analog voltages $VA1_R$~$VA1_W$ according to the reference voltages $V0_R$~$V63_R$, $V0_G$~$V63_G$, $V0_B$~$V63_B$ and $V0_W$~$V63_W$, and output the corresponding driving voltages $VA1_R$~$VA1_W$ through the analog buff-

ers AB_R~AB_W. Operation and structure of the D/A conversion units 30_2A~30_NA are similar to those of the D/A conversion unit 30_1A. In this embodiment, the data diver 100A can output four corresponding voltages to drive four data lines at one time.

[0020] The analog reference voltage generation circuit 20 comprises four voltage generators 22R, 22G, 22B and 22W shown in Figs. 6A~6D to generate reference voltages $V0_R$~$V63_R$, $V0_G$~$V63_G$, $V0_B$~$V63_B$ and $V0_W$~$V63_W$. As shown in Fig. 6A, the voltage generator 22R generates the reference voltages $V0_R$~$V63_R$ to D/A converters DAC_R of the D/A conversion units 30_1A~30_NA according to the white component signal Wi. The voltage generator 22R comprises two de-multiplexers 211 and 212 and two series-connected resistor strings 231 and 232. The resistor string 231 comprises resistors $R0_{R"}$~$R62_{R"}$ connected in series, and the resistor string 232 comprises resistors $R0_R$~$R64_R$ for red color grey level gamma correction. The de-multiplexer 211 selectively outputs a first power voltage VerfH to one node of the resistor string 231 according to the white component signals Wi, and the de-multiplexer 212 selectively outputs a second power voltage VrefL to one node of the resistor string 232 according to the white component signals Wi. The first power voltage VrefH exceeds the second power voltage VrefL, the resistors $R0_{R"}$ and $R0_R$ are the same, the resistors $R1_{R"}$ and $R1_R$ are the same, the resistors $R2_{R"}$ and $R2_R$ are the same, and so on.

[0021] For example, if the white component signal Wi extracted from the three color input signals Ri, Gi and Bi is 000000, the power voltage VrefL is forced to the node N0 of the resistor string 232, and the power voltage VrefH is forced to the node N3 of the resistor string 231. Alternately, if the white component signal Wi extracted from the three color input signals Ri, Gi and Bi is 000001, the power voltage VrefL is forced to the node N1 of the resistor string 232, and the power voltage VrefH is forced to the node N4 of the resistor string 231. Accordingly, the voltage level of the reference voltage $V0_R$~$V63_R$ for the red input signal Ri can be lowered by a first voltage drop.

[0022] Alternately, if the white component signal Wi extracted from the three color input signals Ri, Gi and Bi is 000010, the power voltage VrefL is forced to the node N2 of the resistor string 232, and the power voltage VrefH is forced to the node N5 of the resistor string 231. Accordingly, the voltage level of the reference voltage $V0_R$~$V63_R$ for the red input signal Ri can be lowered by a second voltage drop exceeding the first voltage drop. Thus, the voltage level of the reference voltage $V0_R$~$V63_R$ for the red input signal Ri can be adjusted based on the white component signal Wi.

[0023] As shown in Fig. 6B, the voltage generator 22G generates the reference voltages $V0_G$~$V63_G$ to D/A converters DAC_G of the D/A conversion units 30_1A~30_NA according to the white component signal Wi. The voltage generator 22R comprises two de-multiplexers 213 and 214 and two series-connected resistor strings 233 and 234. The resistor string 233 comprises resistors $R0_{G"}$~$R62_{G"}$ connected in series, and the resistor string 234 comprises resistors $R0_G$~$R64_G$ for green color grey level gamma correction. The de-multiplexer 213 selectively outputs the first power voltage VrefH to one node of the resistor string 233, and the de-multiplexer 214 selectively outputs the second power voltage VrefL to one node of the resistor string 234. The resistors $R0_{G"}$ and $R0_G$ are the same, the resistors $R1_{G"}$ and $R1_G$ are the same, the resistors $R2_{G"}$ and $R2_G$ are the same, and so on.

[0024] As shown in Fig. 6C, the voltage generator 22B generates the reference voltages $V0_B$~$V63_B$ to D/A converters DAC_B of the D/A conversion units 30_1A~30_NA according to the white component signal Wi. The voltage generator 22B comprises two de-multiplexers 215 and 216 and two series-connected resistor strings 235 and 236. The resistor string 235 comprises resistors $R0_{B"}$~$R62_{B"}$ connected in series, and the resistor string 236 comprises resistors $R0_B$~$R64_B$ for blue color grey level gamma correction. The de-multiplexer 215 selectively outputs the first power voltage VrefH to one node of the resistor string 235, and the de-multiplexer 216 selectively outputs the second power voltage VrefL to one node of the resistor string 236. The resistors $R0_{B"}$ and $R0_B$ are the same, the resistors $R1_{B"}$ and $R1_B$ are the same, the resistors $R2_{B"}$ and $R2_B$ are the same, and so on. Operation of the voltage generator 22G and 22B is similar to that of the voltage generator 22R., . The resistors $R0_R$~$R64_R$, $R0_G$~$R64_G$ and $R0_B$~$R62_B$ can be different from others, depending on design.

[0025] As shown in Fig. 6D, the voltage generator 22W comprises a resistor string 237 comprising a plurality of resistors $R0_W$~$R63_W$ connected in series for white color grey level gamma correction. The power voltages VrefH and VrefL are forced to two ends of the resistor string 237, such that the reference voltages $V0_W$~$V63_W$ are generated according to difference resistances of the resistors $R0_W$~$R63_W$.

[0026] In this embodiment , the voltage level of the reference voltages V0R~V63R, V0G~V63G and V0B~V63B for three color input signals Ri, Gi and Bi can be adjusted based on the white component signal Wi. The lower voltage level of the reference voltages $V0_R$~$V63_R$, $V0_G$~$V63_G$ and $V0_B$~$V63_B$, the lower driving voltage $VA1_R$~VAN_R, $VA1_G$~VAN_G and $VA1_B$~VAN_B generated by D/A conversion units 30_1A~30_NA. Namely, the voltage level of the driving voltages $VA1_R$~VAN_R, $VA1_G$~VAN_G and $VA1_B$~VAN_B generated by D/A conversion units 30_1A~30_NA can be adjusted according to the extracted white component signal Wi. When N-type transistors are used as driving devices of pixels, the RGB brightness of the subpixels on a display device is lowered as the driving voltage decreases based on the white component signal Wi. In some embodiments, when P-type transistors are used as driving devices of pixels, the RGB brightness of the pixels on a display device is lowered as the driving voltage increases based on the white component signal Wi. Thus, gamma

correction for RGBW brightness can be accurately controlled.

[0027] Alternately, in some embodiments, the de-multiplexers 211, 213 and 215 selectively output the second power voltage VrefL to one node of the resistor string 231, 233 and 235, and the de-multiplexer 212, 214 and 216 selectively output the first power voltage VrefH to one node of the resistor string 232, 234 and 236.

[0028] Fig. 7 shows another embodiment of a data driver. As shown, the data driver 100B is similar to the data driver 100A shown in Fig. 5, with the exception of analog sampling and holding latches ASH_R~ASH_W coupled between the analog buffers AB_R~AB_W and the D/A converters DAC_R~DAC_W in each D/A conversion unit 30_1B~30_NB. Description of the same structure shown in Fig. 5 is omitted for simplification. In the data driver 100B, the driving voltages $VA1_R$~VAN_R, $VA1_G$~VAN_G, $VA1_B$~VAN_B and $VA1_W$~VAN_W generated by the D/A conversion units 30_1B~30_NB during different periods can be sampled and held by the analog sampling and holding latches ASH_R~ASH_W. Thus, the data driver 100B can output the corresponding voltages to drive one row of data lines in one time.

[0029] Figs. 8-1 and 8-2 show another embodiment of a data driver. As shown, the data driver 100C is similar to the data driver 100A shown in Fig. 5, with the exception of N analog reference voltage generation circuits 20_1~20_N coupled to the D/A conversion units 30_1C~30_NC. Description of the same structure shown in Fig. 7 is omitted for simplification. In the data driver 100C, the N analog reference voltage generation circuits 20_1~20_N each correspond to one of the D/A conversion units 30_1C~30_NC. For example, the analog reference voltage generation circuit 20_1 corresponds to the D/A conversion unit 30_1C, the analog reference voltage generation circuit 20_2 corresponds to the D/A conversion unit 30_2C, and so on. The color input signals Ri, Gi, Bi and the extracted white component signal Wi are sampled by the sampling latches $S1_R$~$S1_W$ and held by the holding latches $H1_R$~$H1_W$ in the D/A conversion units 30_1C~30_NC during each period. For example, the color input signals R1, G1, B1 and the extracted white component signal W1 are sampled and held in the D/A conversion units 30_1C during a first period, the color input signals R2, G2, B2 and the extracted white component signal W2 are sampled and held in the D/A conversion units 30_2C during a second period, and so on.

[0030] All held color input signals Ri, Gi, Bi and the white component signal Wi can be output to the corresponding D/A converters DAC_R~DAC_W and the corresponding analog reference voltage circuit at one time. For example, the white component signal W1 is output to analog reference voltage generation circuit 20_1, such that the reference voltages $V0_R$~$V63_R$, $V0_G$~$V63_G$, $V0_B$~$V63_B$ and $V0_W$~$V63_W$ are output to the D/A converters DAC_R~DAC_W. Accordingly, the D/A converters DAC_R~DAC_W receive the reference voltages $V0_R$~$V63_R$, $V0_G$~$V63_G$, $V0_B$~$V63_B$ and $V0_W$~$V63_W$ and generate the driving voltage $VA1_R$~$VA1_W$ according to the three color input signals R1, G1, B1 and W1. Similarly, the D/A conversion units 30_2C~30_NC generate the driving voltages $VA2_R$~VAN_R, $VA2_G$~VAN_G and $VA2_B$~VAN_B at the same time. Namely, the data driver 100C can output the corresponding voltages to drive one row of data lines in one time.

[0031] Fig. 9 is a schematic diagram of another embodiment of a system, in this case a display panel, for providing driving voltages. As shown in Fig. 9, the display device 300 comprises a data driver such as data drvier100A/100B/100C, a pixel array 200 and a gate driver 210. The pixel array 200 comprises RGBW color pixels arranged in matrix, a plurality of data lines and a plurality of scan lines. The data driver generates analog driving voltages to the pixel array 200, and the gate driver 210 provides scan signals to the pixel array 200 such that the scan lines are asserted or de-asserted. The pixel array 200 generates color images according to the analog driving voltages from the data driver. While the display panel can be an organic light emitting panel, an electroluminescent panel or a liquid crystal display panel for example, various other technologies can be used in other embodiments.

[0032] Fig. 10 schematically shows an embodiment of yet another system, in this case an electronic device for providing driving voltages. In particular, electronic device 600 employs a display panel such as display panel 600 shown in Fig. 9. The electronic device 600 may be a device such as a PDA, notebook computer, digital camera, tablet computer, cellular phone or a display monitor device, for example.

[0033] Generally, the electronic device 600 comprises a housing 500, a display panel 300 and a DC/DC converter 400, although it is to be understood that various other components can be included, such components not shown or described here for ease of illustration and description. In operation, the DC/DC converter 400 powers the display panel 300 so that the display panel 300 can display color images.

[0034] While the invention has been described by way of example and in terms of preferred embodiment, it is to be understood that the invention is not limited thereto. To the contrary, it is intended to cover various modifications and similar arrangements (as would be apparent to those skilled in the art). Therefore, the scope of the appended claims should be accorded the broadest interpretation so as to encompass all such modifications and similar arrangements.

Claims

1. A system for displaying image, comprising:

a data driver comprising:

a reference voltage generation circuit oper-

ative to provide reference voltages according to a white component signal (W) extracted from three color input signals (R,G,B); and

a digital-to-analog (D/A) conversion unit operative to generate driving voltages according to the reference voltages, the three color input signals and the white component signal.

2. The system as claimed in claim 1, further comprising a white component extraction unit operative to extract the white component signal (W) from the three color input signals (R,G,B).

3. The system as claimed in claim 1, wherein the reference voltage generation circuit comprises first, second, third and fourth voltage generators, in which the first to third voltage generators are operative to generate the first to third sets of reference voltages according to the white component signal, and the fourth voltage generator is operative to generate the fourth set of reference voltage.

4. The system as claimed in claim 3, wherein the digital-to-analog conversion unit comprises first, second, third and fourth (D/A) converters operative to generate the driving voltages according to the first to fourth sets of reference voltages, the three color input signals and the white component signal.

5. The system as claimed in claim 4, wherein the digital-to-analog conversion unit further comprises a plurality of digital holding units coupled to the (D/A) converters and operative to hold the three color input signals and the white component signal.

6. The system as claimed in claim 4, wherein the digital-to-analog conversion unit further comprises a plurality of analog holding units operative to hold the driving voltages from the (D/A) converters.

7. The system as claimed in claim 1, further comprising a display panel comprising four color (R,G,B,W) pixels operative to generate color images according to the driving voltages.

8. The system as claimed in claim 3, wherein the first to third voltage generators each comprise:

first and second resistor strings connected in series, each comprising a plurality of resistors and nodes;

first de-multiplexers coupled between the first resistor and a first power voltage; and

a second de-multiplexer coupled between the second resistor string and a second power voltage, wherein, according to the white component signal, the first de-multiplexer selectively forces the first power voltage to one node of the first resistor string and the second de-multiplexer selectively forces the second power voltage to one node of the second resistor string, such that first to third sets of reference voltages are regulatable.

9. The system as claimed in claim 8, wherein the fourth voltage generator comprises a third resistor string coupled between the first power voltage and the second power voltage.

10. The system as claimed in claim 8, wherein the first and second resistor strings of the first, the second and the third voltage generators exhibit different resistances.

11. The system as claimed in claim 7, wherein the display panel is a liquid crystal display panel.

12. The system as claimed in claim 7, wherein the display panel is an electroluminescent panel.

13. The system as claimed in claim 7, wherein the display panel is an organic light emitting panel.

14. The system as claimed in claim 1, wherein the system is implemented as a PDA, a display monitor, a digital camera, a notebook computer, a tablet computer or a cellular phone.

15. A method for providing driving voltages of a system for displaying images, comprising:

generating reference voltages according to a white component signal (W) extracted from three color input signals (R,G,B); and

generating driving voltages according to the reference voltages, the three color input signals and the white component signal.

16. The method as claimed in claim 15, further comprising extracting the white component signal (W) from the three color input signals (R,G,B).

17. The method as claimed in claim 16, wherein the reference voltages comprise first, second and third sets of reference voltages corresponding to the three color input signals respectively according to the white component signal, and a fourth set of reference voltages corresponding to the white component signal.

18. The method as claimed in claim 17, wherein the driving voltage is generated according to the first to fourth sets of reference voltages, the three color input signals and the white component signal.

19. The method as claimed in claim 15, further comprising holding the white component signal (W) and the three color input signals (R,G,B) before generating the driving voltages.

20. The method as claimed in claim 16, wherein the white component signal (W) and the three color input signals (R,G,B) each is a digital data comprising N bits, and the white component signal (W) is obtained by executing an AND logic operation to the three color input signals (R,G,B).

21. The method as claimed in claim 16, wherein the white component signal (W) and the three color input signals (R,G,B) each is a digital data comprising N bits, and the white component signal (W) is obtained by executing an AND logic operation to M bits of the three color input signals (R,G,B), and $0 < M < N$.

22. The method as claimed in claim 15, further comprising holding the generated driving voltage.

23. The method as claimed in claim 15, wherein the system comprises a display device and the display device is an organic light emitting device, a liquid crystal display device or an electroluminescent device.

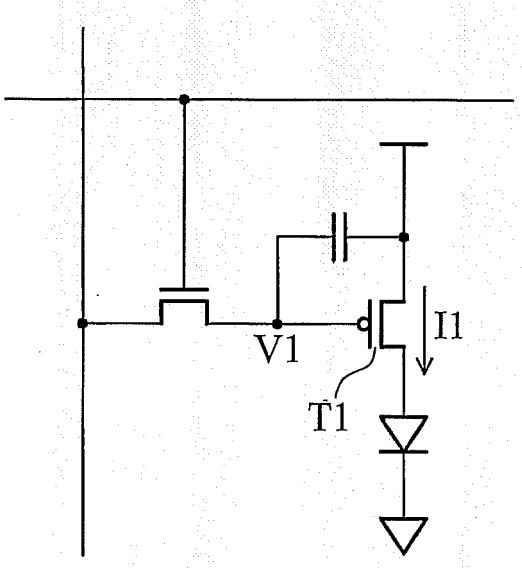

FIG. 1A (RELATED ART)

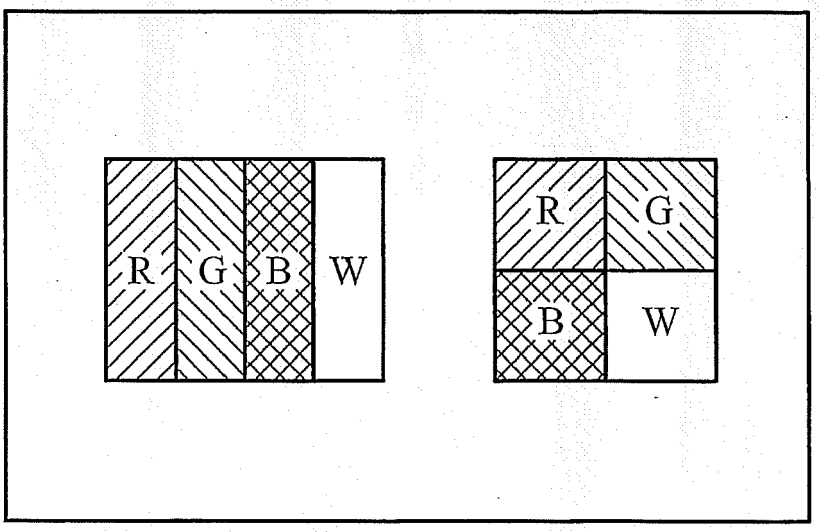

FIG. 1B (RELATED ART)

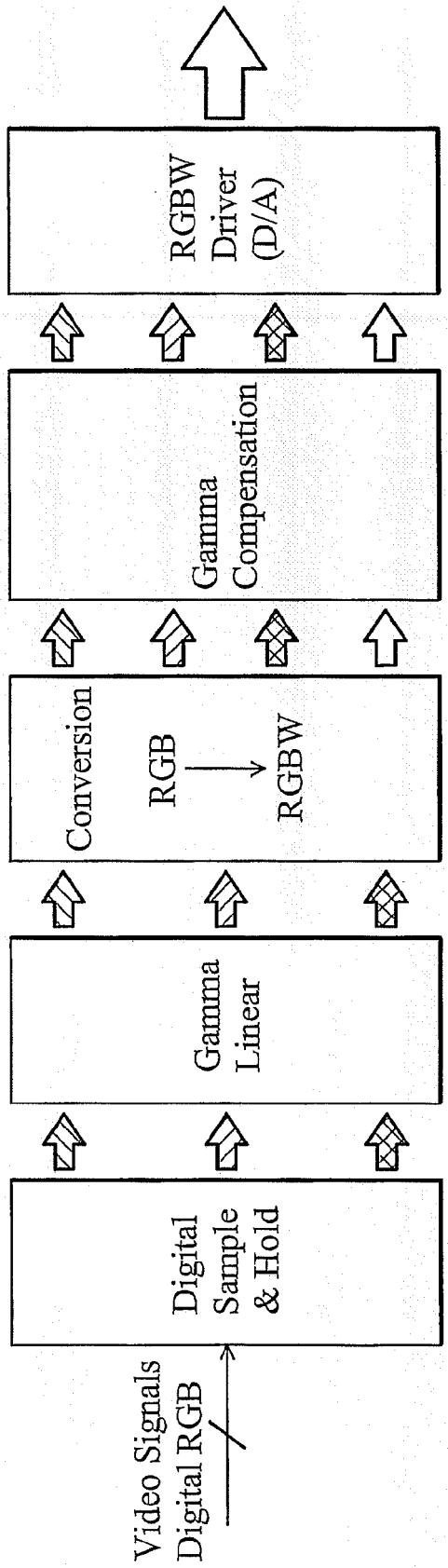

FIG. 1C (RELATED ART)

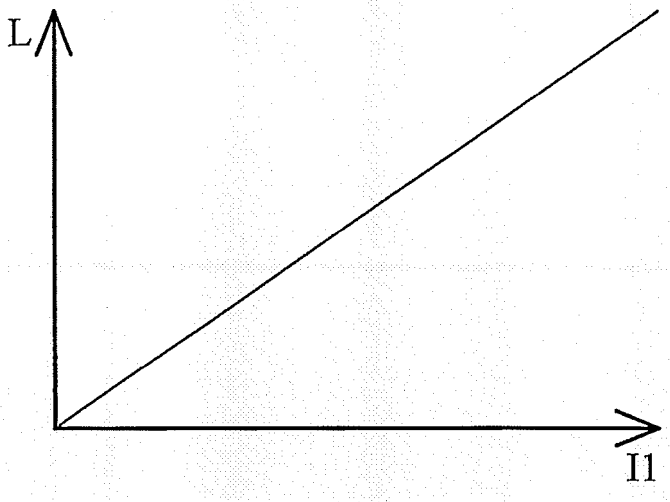

FIG. 2A (RELATED ART)

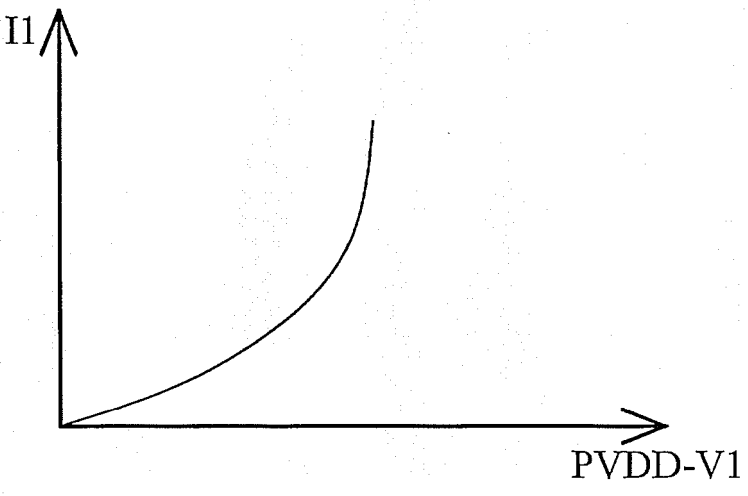

FIG. 2B (RELATED ART)

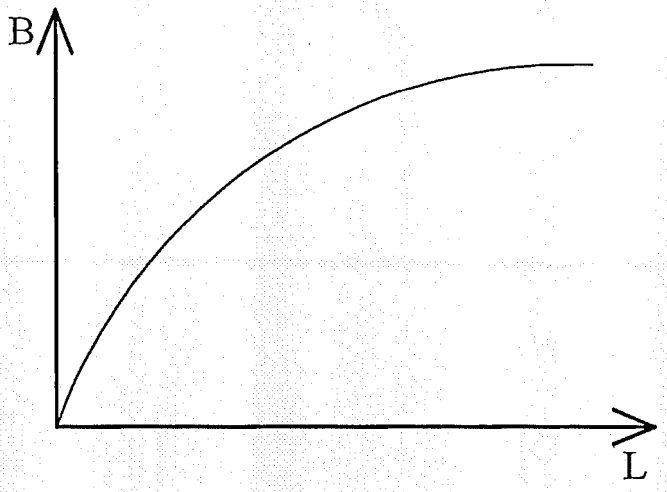

FIG. 2C (RELATED ART)

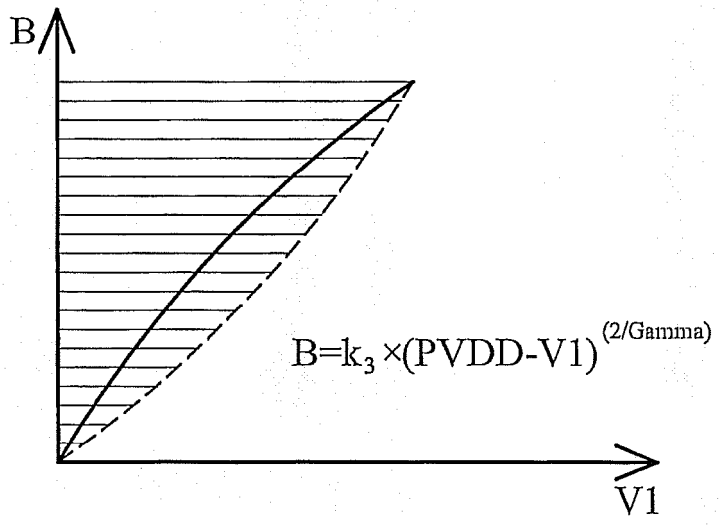

FIG. 2D (RELATED ART)

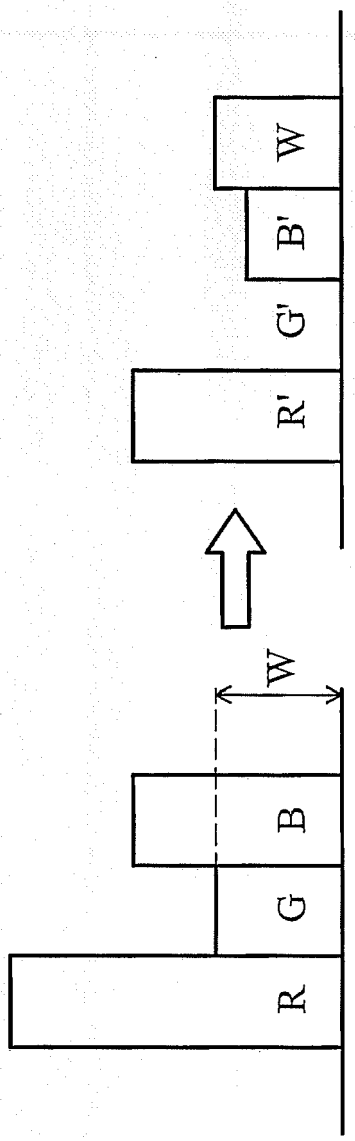

FIG. 3 (RELATED ART)

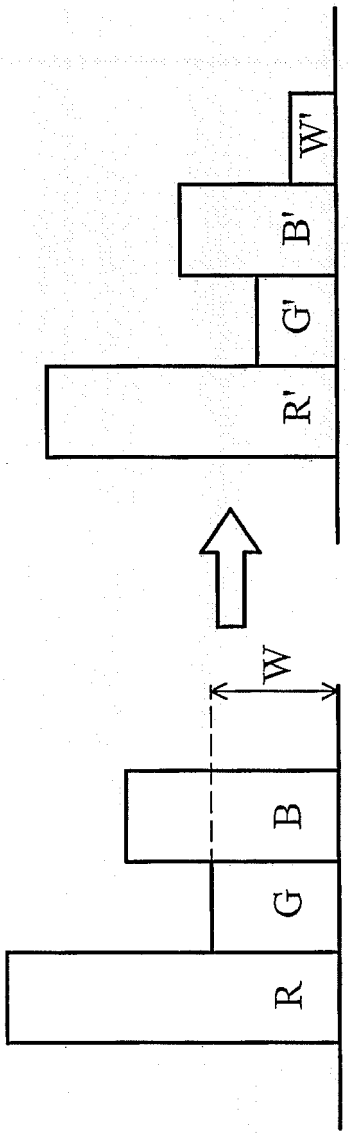

FIG. 4 (RELATED ART)

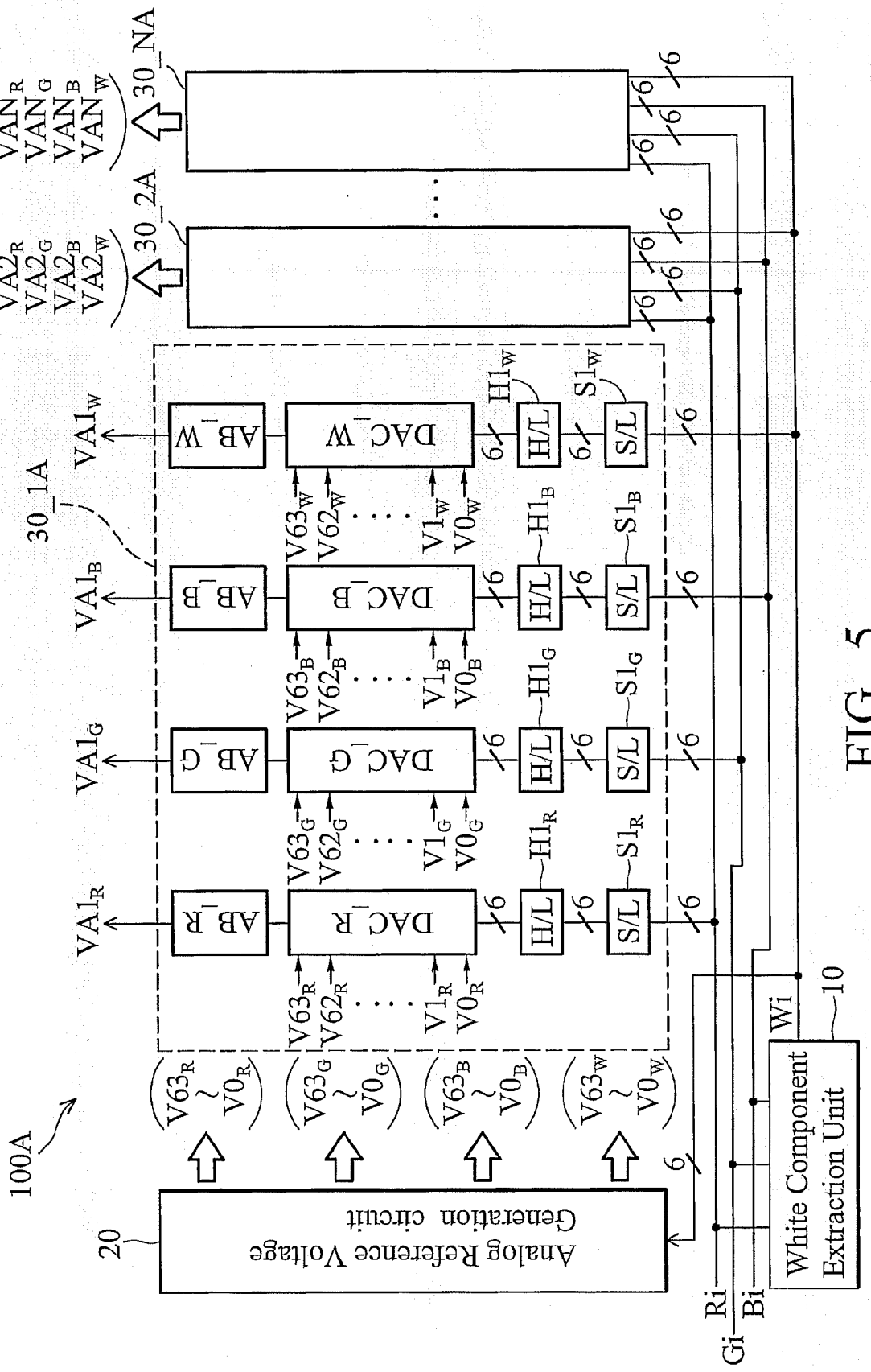
100A
20
Analog Reference Voltage Generation circuit
White Component Extraction Unit
10
Ri
Gi
Bi
Wi
30_1A
30_2A
30_NA
DAC_R
DAC_G
DAC_B
DAC_W
AB_R
AB_G
AB_B
AB_W
H/L
S/L
6

FIG. 5

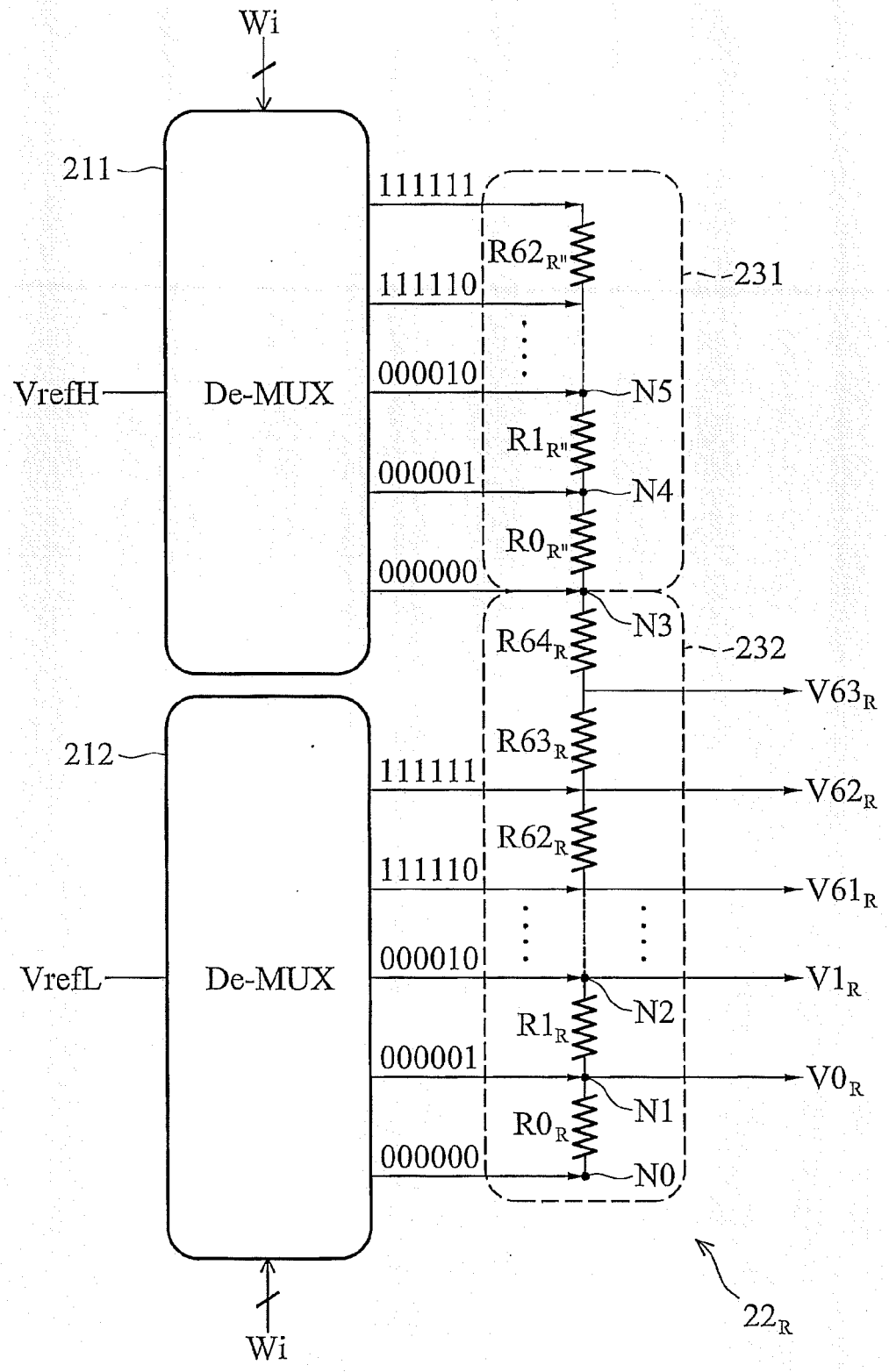
Wi
211
111111
R62R"
231
111110
VrefH
De-MUX
000010
N5
R1R"
000001
N4
R0R"
000000
N3
R64R
232
V63R
R63R
212
111111
V62R
R62R
111110
V61R
VrefL
De-MUX
000010
V1R
N2
R1R
000001
V0R
N1
R0R
000000
N0
22R
Wi

FIG. 6A

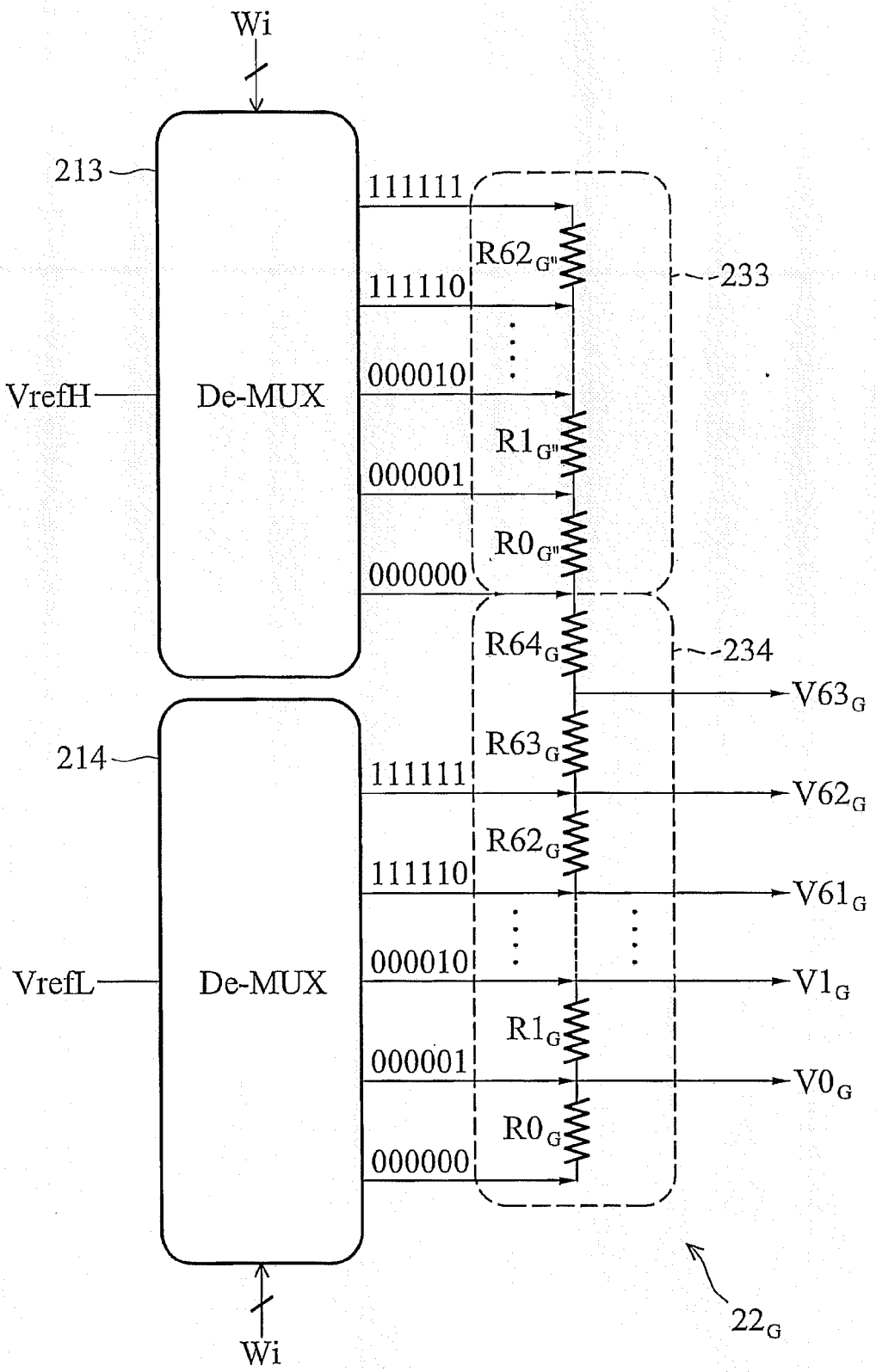
Wi
213
De-MUX
VrefH
214
De-MUX
VrefL
Wi
111111
111110
000010
000001
000000
R62G"
R1G"
R0G"
233
R64G
R63G
R62G
R1G
R0G
234
V63G
V62G
V61G
V1G
V0G
22G

FIG. 6B

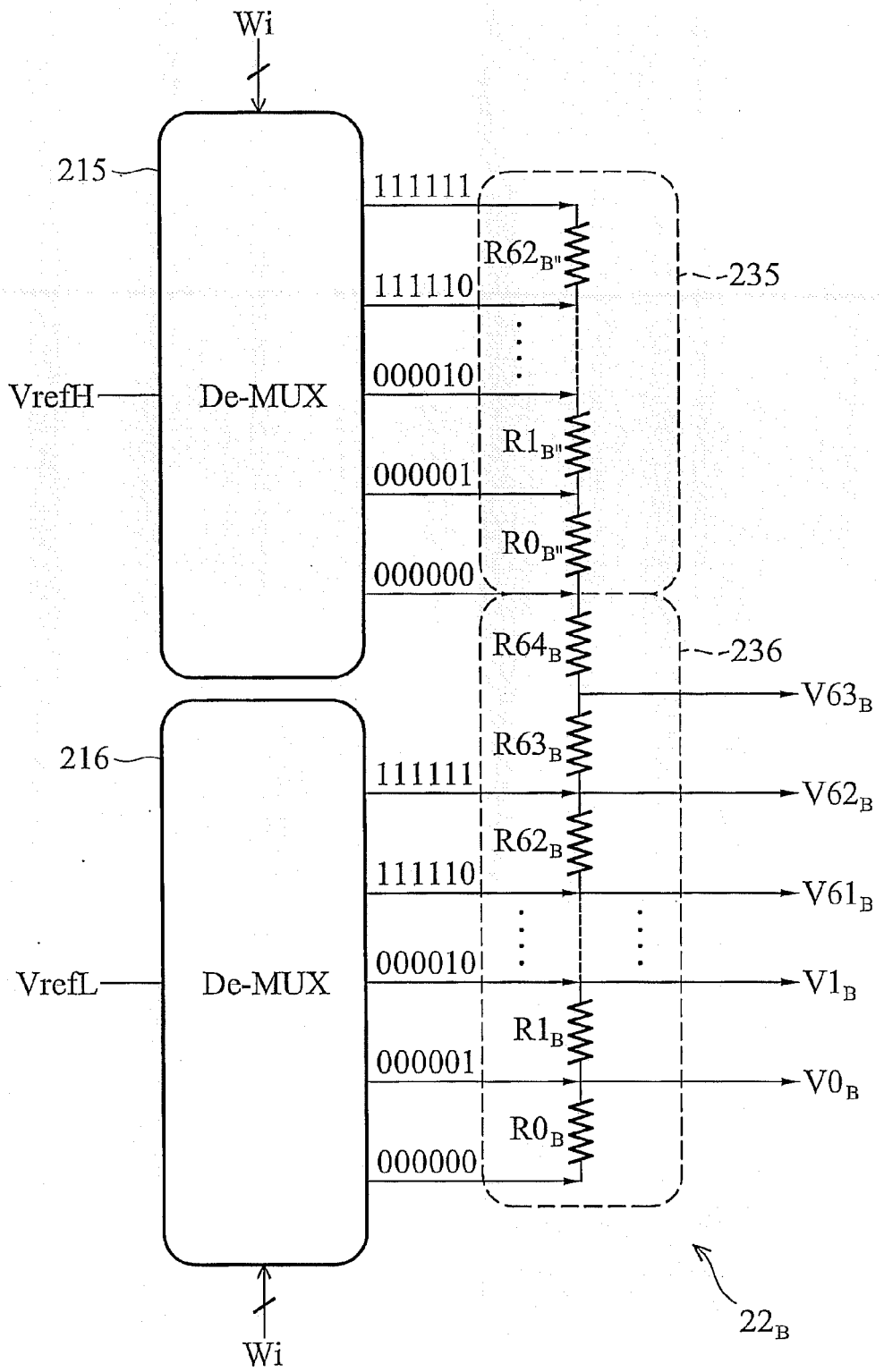
Wi
215
VrefH
De-MUX
111111
111110
000010
000001
000000
R62B"
R1B"
R0B"
235
R64B
R63B
R62B
R1B
R0B
236
V63B
V62B
V61B
V1B
V0B
216
VrefL
De-MUX
Wi
22B

FIG. 6C

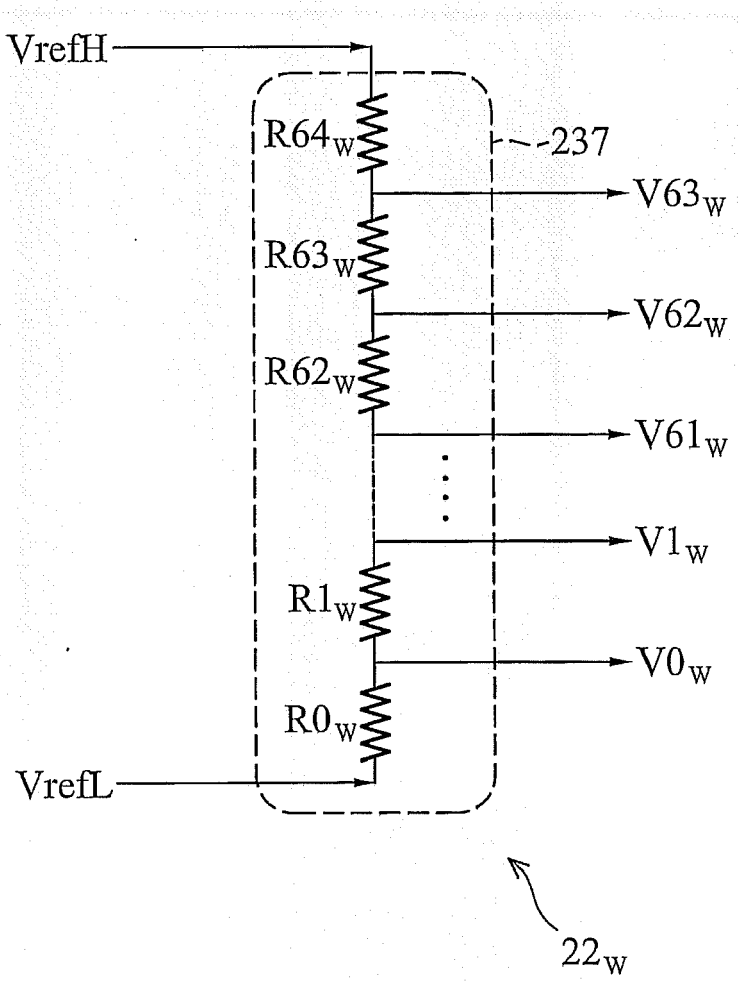
VrefH
R64W
237
V63W
R63W
V62W
R62W
V61W
V1W
R1W
V0W
R0W
VrefL
22W

FIG. 6D

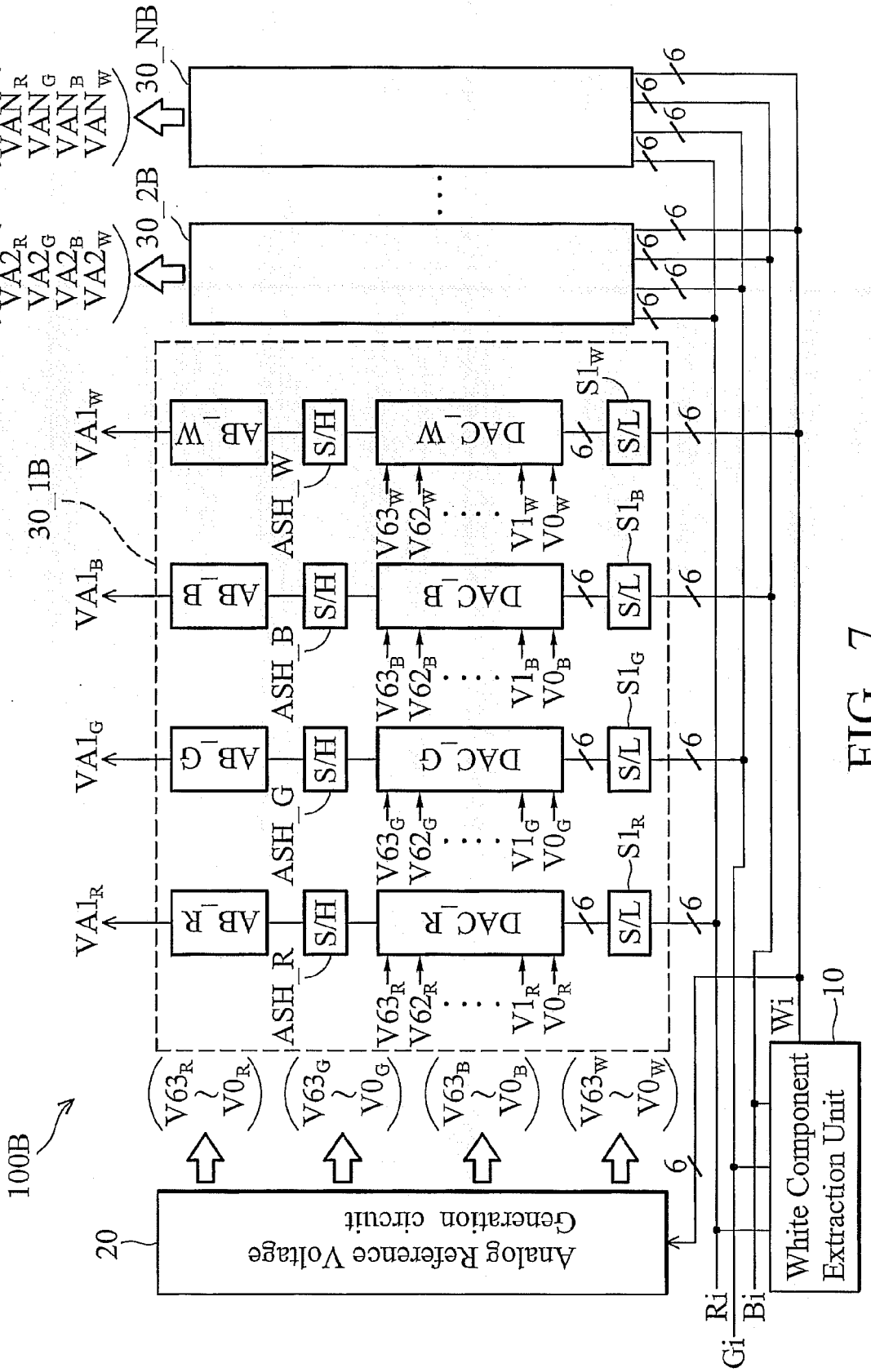
100B
20
Analog Reference Voltage Generation circuit
White Component Extraction Unit
10
Wi
Ri
Gi
Bi
30_1B
30_2B
30_NB
DAC_R
DAC_G
DAC_B
DAC_W
AB_R
AB_G
AB_B
AB_W
S/H
S/L
ASH_R
ASH_G
ASH_B
ASH_W
VA1R
VA1G
VA1B
VA1W
VA2R
VA2G
VA2B
VA2W
VANR
VANG
VANB
VANW
V63R
V62R
V1R
V0R
V63G
V62G
V1G
V0G
V63B
V62B
V1B
V0B
V63W
V62W
V1W
V0W
S1R
S1G
S1B
S1W
6

FIG. 7

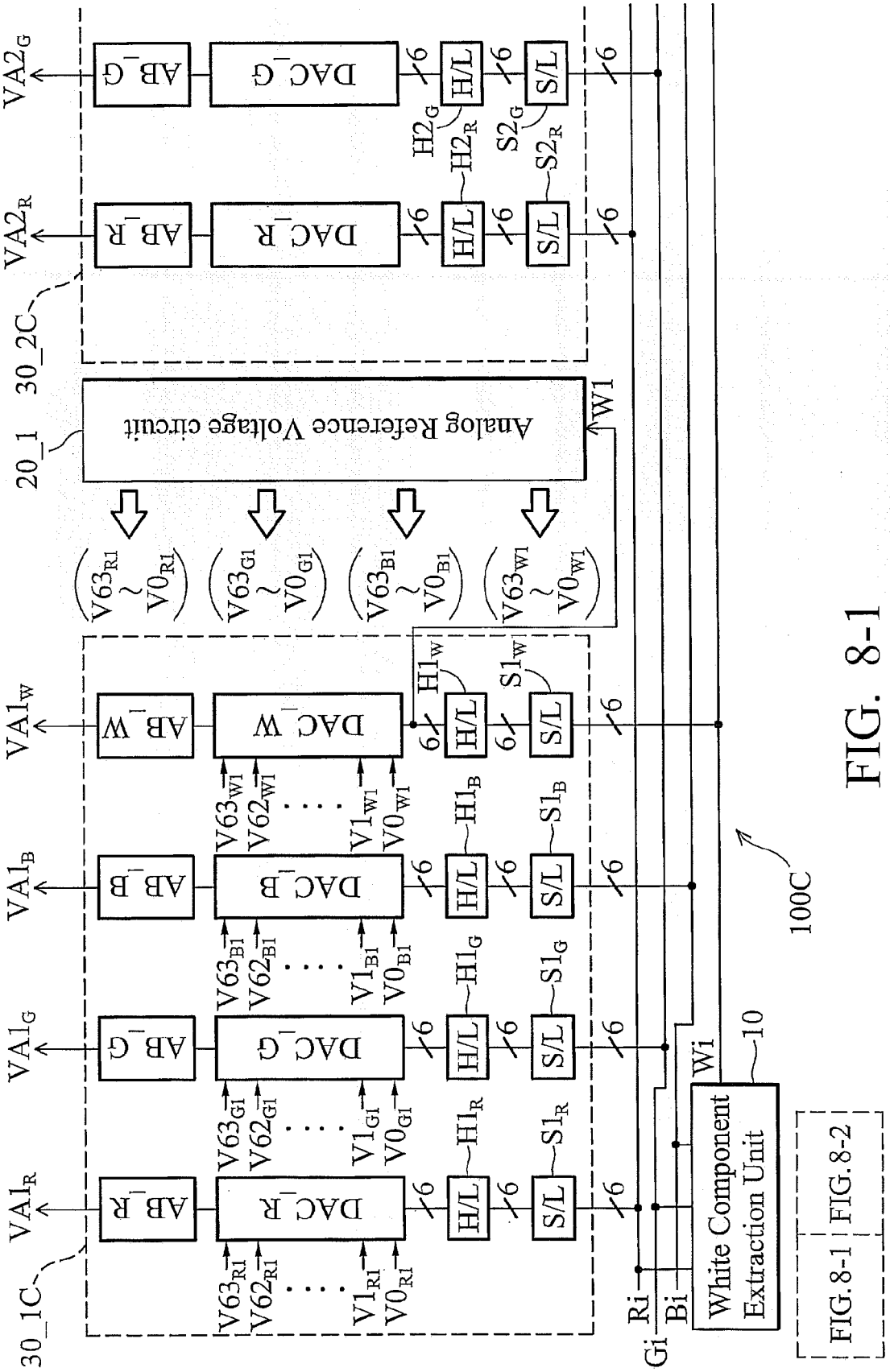
Analog Reference Voltage circuit
20_1
30_2C
30_1C
100C
W1
VA2G
VA2R
VA1W
VA1B
VA1G
VA1R
AB_G
AB_R
AB_W
AB_B
DAC_G
DAC_R
DAC_W
DAC_B
H/L
S/L
H2G
H2R
S2G
S2R
H1W
H1B
H1G
H1R
S1W
S1B
S1G
S1R
(V63R1 ~ V0R1)
(V63G1 ~ V0G1)
(V63B1 ~ V0B1)
(V63W1 ~ V0W1)
V63W1
V62W1
V1W1
V0W1
V63B1
V62B1
V1B1
V0B1
V63G1
V62G1
V1G1
V0G1
V63R1
V62R1
V1R1
V0R1
Ri
Gi
Bi
Wi
White Component Extraction Unit
10
FIG. 8-1 | FIG. 8-2

FIG. 8-1

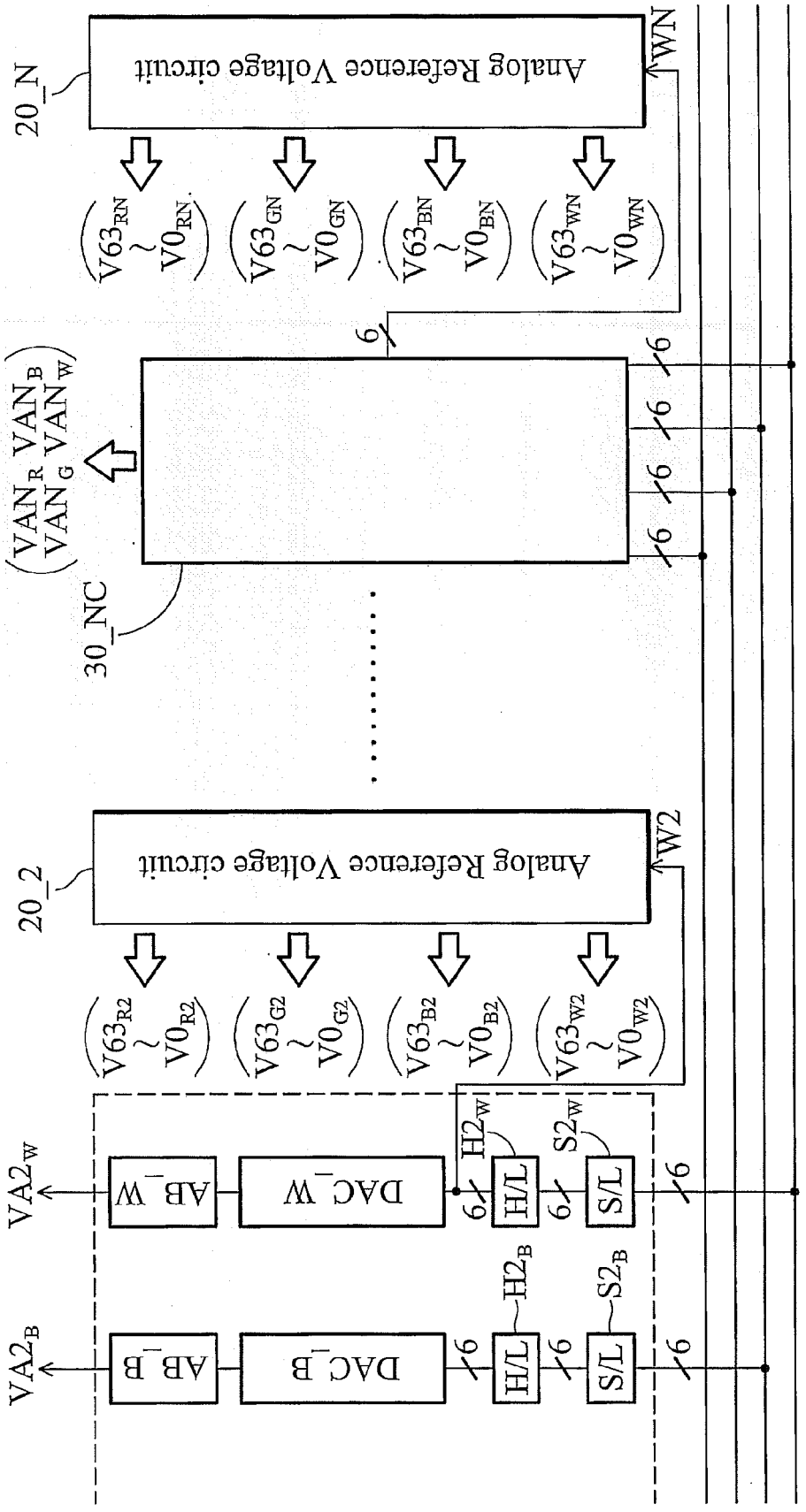
20_N
Analog Reference Voltage circuit
WN
$(V63_{RN} \sim V0_{RN})$
$(V63_{GN} \sim V0_{GN})$
$(V63_{BN} \sim V0_{BN})$
$(V63_{WN} \sim V0_{WN})$
6
$(VAN_R\ VAN_B\ VAN_G\ VAN_W)$
30_NC
20_2
Analog Reference Voltage circuit
W2
$(V63_{R2} \sim V0_{R2})$
$(V63_{G2} \sim V0_{G2})$
$(V63_{B2} \sim V0_{B2})$
$(V63_{W2} \sim V0_{W2})$
$VA2_W$
AB_W
DAC_W
$H2_W$
H/L
$S2_W$
S/L
$VA2_B$
AB_B
DAC_B
$H2_B$
H/L
$S2_B$
S/L
9
6

FIG. 8-2

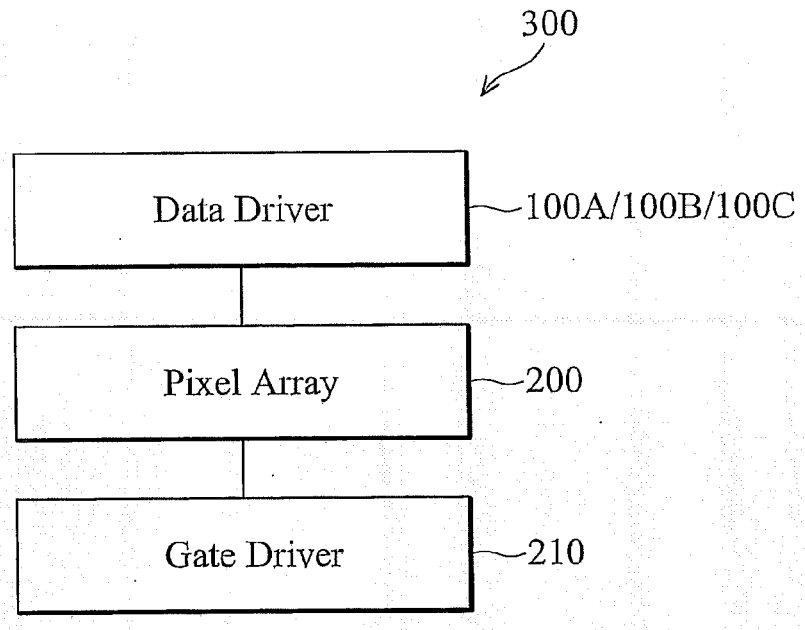
300
Data Driver
100A/100B/100C
Pixel Array
200
Gate Driver
210

FIG. 9

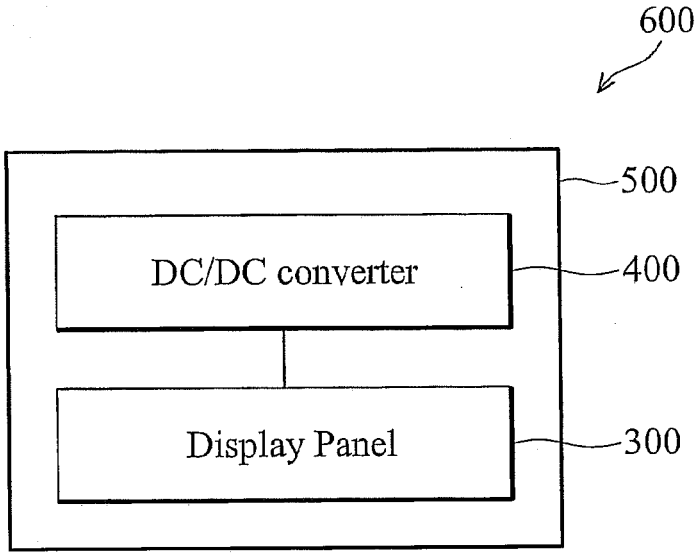
600
500
DC/DC converter
400
Display Panel
300

FIG. 10

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 06 11 2633

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (IPC)
X	YOJIRO MATSUEDA ET AL: "38.4: 6-bit AMOLED with RGB Adjustable Gamma Compensation LTPS TFT Circuit" 2005 SID INTERNATIONAL SYMPOSIUM. BOSTON, MA, MAY 24 - 27, 2005, SID INTERNATIONAL SYMPOSIUM, SAN JOSE, CA : SID, US, 24 May 2005 (2005-05-24), pages 1352-1355, XP007012301 * paragraphs 1., 2.1, 2.2 * * figures 2,3 *	1-19,22, 23	INV. G09G3/20 G09G3/32
X	EP 1 298 637 A (SAMSUNG ELECTRONICS CO., LTD) 2 April 2003 (2003-04-02) * paragraphs [0001], [0006], [0052], [0053], [0057] - [0062] *	1-19,22, 23	
A	EP 0 547 603 A (TEXAS INSTRUMENTS INCORPORATED) 23 June 1993 (1993-06-23) * page 2, line 42 - line 46 *	1,15	
A	US 2004/113875 A1 (MILLER MICHAEL E ET AL) 17 June 2004 (2004-06-17) * paragraphs [0026], [0027] *	1-23	TECHNICAL FIELDS SEARCHED (IPC) G09G
A	US 6 593 934 B1 (LIAW MING-JIUN ET AL) 15 July 2003 (2003-07-15) * figure 13 *	8-10	

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
Munich	4 August 2006	Auracher, S

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04-08-2006

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
EP 1298637 A	02-04-2003	CN 1414539 A	30-04-2003
		JP 2003186455 A	04-07-2003
		KR 2003027999 A	08-04-2003
		TW 533399 B	21-05-2003
		US 2003058235 A1	27-03-2003
EP 0547603 A	23-06-1993	CA 2084948 A1	19-06-1993
		DE 69232507 D1	25-04-2002
		DE 69232507 T2	02-10-2002
		JP 5273673 A	22-10-1993
		US 5233385 A	03-08-1993
US 2004113875 A1	17-06-2004	CN 1726593 A	25-01-2006
		EP 1573817 A1	14-09-2005
		JP 2006512732 T	13-04-2006
		WO 2004061963 A1	22-07-2004
US 6593934 B1	15-07-2003	NONE	

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