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(71) Applicant: **Shin-Etsu Handotai Co., Ltd**
Tokyo (JP)

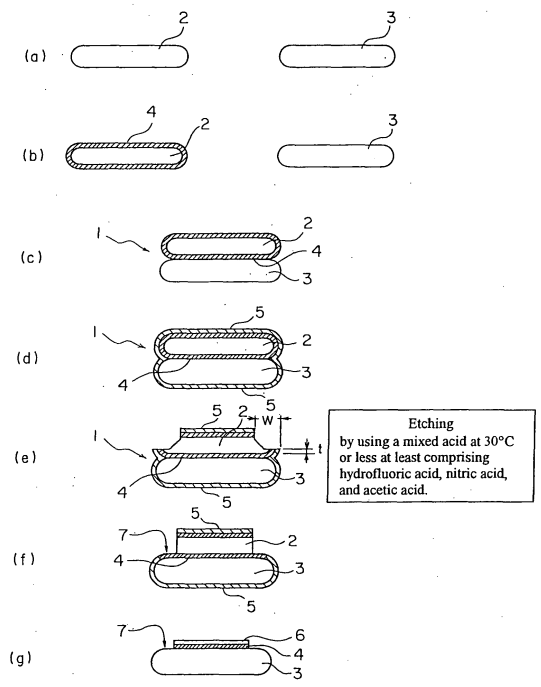
(72) Inventors:
- **OKABE, Keiichi**
  Chikuma-shi,
  Nagano 387-8555 (JP)
- **MIYAZAKI, Susumu**
  Chikuma-shi,
  Nagano 387-8555 (JP)

(74) Representative: **Wibbelmann, Jobst et al**
Wuesthoff & Wuesthoff
Patent- und Rechtsanwälte
Schweigerstrasse 2
81541 München (DE)

(54) PROCESS FOR MANUFACTURE OF BONDED WAFER

(57) The present invention provides a method for manufacturing a bonded wafer comprising steps of forming an oxide film on at least a surface of a base wafer or a surface of a bond wafer; bringing the base wafer and the bond wafer into close contact via the oxide film; subjecting these wafers to a heat treatment under an oxidizing atmosphere to bond the wafers together; grinding and removing the outer periphery of the bond wafer so that the outer periphery has a predetermined thickness; subsequently removing an unbonded portion of the outer periphery of the bond wafer by etching; and then thinning the bond wafer so that the bond wafer has a desired thickness, wherein the etching is conducted by using a mixed acid at 30°C or less at least comprising hydrofluoric acid, nitric acid, and acetic acid. Thus there is provided a method for manufacturing a bonded wafer by which unbonded portions of the outer periphery of the bond wafer are removed with a high selectivity ratio (R_{Si}/R_{SiO2}) without causing metallic contamination.

Fig.1



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Description

Technical Field

[0001] The present invention relates to a method for manufacturing a bonded wafer, in particular to a method of etching the unbonded portion of the outer periphery of the bond wafer.

Background Art

[0002] Bonded wafers are used as wafers for high performance devices. Each of the bonded wafers is manufactured by bonding a semiconductor wafer with another wafer or the like and then thinning the wafer on the side where devices are fabricated.

[0003] Specifically, for example, two mirror-polished silicon wafers are prepared, and an oxide film is formed at least on one of the wafers. Then these wafers are brought into close contact to each other and subjected to a heat treatment at a temperature of from 200 to 1200°C to increase bonding strength. After that, the wafer on the side where devices are fabricated (a bond wafer) is ground, polished and the like to thin the wafer so that the bond wafer has a desired thickness. As a result, a bonded SOI wafer comprising an SOI (Silicon On Insulator) layer can be manufactured.

[0004] It should be noted that the bonded wafer can be manufactured by directly bonding silicon wafers together without interposing an oxide film therebetween. Furthermore, as the base wafer, an insulator wafer made of quartz, silicon carbide, alumina, or the like can be used.

[0005] When the bonded wafer is manufactured as mentioned above, each of two mirror-surface wafers to be bonded has a portion referred to as a polishing sag, which has a slightly thinner thickness on the periphery, and a chamfered portion. Such portions are not bonded or left as unbonded portions having weak bonding strengths. When the bond wafer is thinned by grinding or the like in the presence of such unbonded portions, the unbonded portions delaminate in part in the thinning step. Therefore, the thinned bond wafer has a smaller diameter than the wafer to be a base (a base wafer). The bond wafer also has micro unevenness continuously formed in the periphery.

[0006] When such a bonded wafer is subjected to a device process, remained unbonded portions delaminate in the device process. This generates particles and deteriorate device yield.

[0007] In order to overcome the problems, there is proposed a method of removing the remained unbonded portions beforehand by alkaline etching using KOH, NaOH, or the like (see Japanese Patent Application Laid-open (kokai) No. 10-209093). In alkaline etching, the etching rate of an etchant against Si (R_{Si}) is fast, whereas the etching rate of the etchant against SiO_2 (R_{SiO2}) is slow. Therefore, the selectivity ratio (R_{Si}/R_{SiO2}) between the etching rates is large. In this case, on reaching a buried oxide film, etching from the bond wafer side automatically almost stops. In this way, use of alkaline etching is advantageous in that a buried oxide film is utilized as a protective film for protecting a base wafer from etching.

Disclosure of the Invention

[0008] It has turned out, however, that removing the unbonded portion by alkaline etching causes metallic contamination, and which can deteriorate electric characteristics of semiconductor devices.

[0009] The present invention has been accomplished in view of the aforementioned problems, and its object is to provide a method for manufacturing a bonded wafer wherein a selectivity ratio (R_{Si}/R_{SiO2}) between an etching rate against Si and an etching rate against SiO_2 is large, metallic contamination is not caused, and the unbonded portion of the outer periphery of a bond wafer is etched.

[0010] In order to achieve the aforementioned object, the present invention provides a method for manufacturing a bonded wafer comprising steps of forming an oxide film on at least a surface of a base wafer or a surface of a bond wafer; bringing the base wafer and the bond wafer into close contact via the oxide film; subjecting these wafers to a heat treatment under an oxidizing atmosphere to bond the wafers together; grinding and removing the outer periphery of the bond wafer so that the outer periphery has a predetermined thickness; subsequently removing an unbonded portion of the outer periphery of the bond wafer by etching; and then thinning the bond wafer so that the bond wafer has a desired thickness, wherein the etching is conducted by using a mixed acid at 30°C or less at least comprising hydrofluoric acid, nitric acid, and acetic acid.

[0011] In etching the unbonded portion of the outer periphery of the bond wafer by using the mixed acid at 30°C or less, the etching rate against Si (R_{Si}) is fast, whereas the etching rate against SiO_2 (R_{SiO2}) is slow. That is, the selectivity ratio (R_{Si}/R_{SiO2}) between the etching rate against Si and the etching rate against SiO_2 is large, and thus the etching rate decreases automatically on reaching a buried oxide film. In this way, the buried oxide film is utilized as a protective film for protecting the base wafer from etching, and the etching does not damage the base wafer. In addition, the etching by using the mixed acid does not cause metallic contamination.

[0012] In the above case, the etching is preferably conducted by spin etching.

[0013] Unlike the case of etching by dipping, when etching is conducted by spin etching, temperature increase of an etchant caused by the chemical reaction of the etching is small. Thus the etchant is easily controlled within temperatures equal to or less than 30°C, and which is sufficiently achieved by using a compact cooling means. Consequently, the etching can be conducted at a lower cost.

[0014] In summary, according to the present invention,

when the unbonded portion of the outer periphery of the bond wafer is etched by using a mixed acid at 30°C or less at least comprising hydrofluoric acid, nitric acid, and acetic acid, metallic contamination is not caused, and the selectivity ratio (R_{Si}/R_{SiO2}) between the etching rate against Si and the etching rate against SiO_2 becomes large. Thus a buried oxide film is utilized as a protective film for protecting the base wafer from etching, and the etching does not damage the base wafer.

Brief Explanation of the Drawings

[0015]

Fig. 1 is a flow chart showing an embodiment of the method for manufacturing a bonded wafer according to the present invention.
Fig. 2(a) is a graph showing the relationship between the liquid temperature of a mixed acid and its etching rate against Si (R_{Si}).
Fig. 2(b) is a graph showing the relationship between the liquid temperature of a mixed acid and its etching rate against SiO_2 (R_{SiO2}).
Fig. 3 is a graph showing the relationship between the liquid temperature of a mixed acid and the selectivity ratio (R_{Si}/R_{SiO2}) between the etching rates.
Fig. 4 is a graph showing evaluation results of metallic contamination in Example and Comparative Example.
Fig. 5 is a single-wafer-processing spin-etching apparatus that can be used in the method for manufacturing a bonded wafer according to the present invention.

Best Mode for Carrying out the Invention

[0016] Hereinafter, the present invention will be described further in detail. However, the present invention is not limited thereto.

[0017] Those skilled in the art conventionally recognize that etching using a mixed acid is not applicable to the case of etching and removing the unbonded portion of a bond wafer by etch stop method because the method requires sufficiently high selectivity ratio between etching rates. The present inventors, however, have experimentally studied and found that sufficiently usable selectivity ratio can be achieved by maintaining the temperature of a mixed acid in low temperatures, and also use of the mixed acid overcomes the problem of metallic contamination caused by alkaline etching. Thus the inventors have accomplished the present invention.

[0018] Fig. 1 is a schematic view showing an embodiment of the method for manufacturing a bonded wafer according to the present invention.

[0019] In Fig. 1, a bond wafer 2 and a base wafer 3 are prepared (Fig. 1(a)). The wafers are material wafers for fabricating an SOI wafer by bonding the wafers together. The bond wafer and the base wafer are not particularly restricted. For example, the wafers may be silicon single crystal wafers.

[0020] Next, among the prepared silicon single crystal wafers, the bond wafer 2 is subjected to a heat treatment to form an oxide film 4 on the surface of the bond wafer (Fig. 1(b)). The oxide film may be formed on the base wafer, or may be formed on both of the bond wafer and the base wafer.

[0021] Then the bond wafer 2 on which the oxide film is formed and the base wafer 3 are brought into close contact under a clean atmosphere (Fig. 1(c)). These wafers are subjected to a heat treatment under an oxidizing atmosphere to bond firmly the bond wafer 2 and the base wafer 3 together. Thus a bonded wafer 1 is obtained. The heat treatment may be conducted, for example, under conditions of an atmosphere containing oxygen or water vapor and at a temperature in the range of 200°C to 1200°C (Fig. 1(d)). As a result of the heat treatment, the bond wafer 2 and the base wafer 3 are bonded firmly together, and an oxide film (a bonding oxide film) 5 is formed on the whole outer surface of the bonded wafer 1.

[0022] The bonded wafer 1 thus bonded has portions where the bond wafer 2 and the base wafer 3 are not bonded in the region within 2 mm from the outer periphery. Such unbonded portions cannot be used as an SOI layer on which devices are fabricated. Furthermore, the unbonded portions delaminate in subsequent processes and which causes various problems. Therefore, the unbonded portions must be removed.

[0023] In order to remove the unbonded portions, as shown in Fig. 1(e), the outer periphery where the unbonded portions exist of the bond wafer 2 is firstly ground and removed so that the outer periphery has a predetermined width w and a predetermined thickness t. Grinding is used because rapid removing is possible and processing accuracy is good.
In the above case, the predetermined thickness t may be 20 to 150 μm.

[0024] Next, etching is conducted to provide a wafer shown in Fig. 1(f) in which the unbonded portions of the outer periphery of the bond wafer 2 are removed. The etchant used herein in the present invention is a mixed acid at 30°C or less at least comprising hydrofluoric acid, nitric acid, and acetic acid. For example, a mixed acid such as an aqueous solution comprising hydrofluoric acid: nitric acid: acetic acid = 15 wt%: 47 wt%: 5 wt% is preferably used. The mixed acid may further comprise phosphoric acid, sulfuric acid, or the like in addition to hydrofluoric acid, nitric acid, and acetic acid.

[0025] Bonded wafers were etched by using the mixed acid to investigate the relationship between the liquid temperature and the etching rate of the mixed acid. Fig. 2(a) shows measurement results of the relationship between the liquid temperature of the mixed acid and its etching rate against Si (R_{Si}). Fig. 2(b) shows measurement results of the relationship between the liquid temperature of the mixed acid and its etching rate against SiO_2 (R_{SiO2}). In addition, based on the data of Figs. 2,

the relationship between the liquid temperature of the mixed acid and the selectivity ratio (R_{Si}/R_{SiO2}) between the etching rates was obtained and the results are shown in Fig. 3.

[0026] In etching, the selectivity ratio between etching rates against silicon and oxide film is important. When the selectivity ratio is sufficiently large, for example, in Fig. 1(e), etching from the bond wafer 2 reaches the buried oxide film between the bond wafer 2 and the base wafer 3, the etching rate considerably decreases and the etching process substantially stops. That is, the oxide film functions as an etch stop layer and protects the base wafer from etching. Consequently, such problems do not occur in which etching proceeds in a short time and damages the base wafer.

[0027] As shown in Fig. 3, the selectivity ratio of the mixed acid sharply drops in temperatures greater than 30°C. When etching is conducted in temperatures greater than 30°C, the etching does not stop sharply on reaching the oxide film because the film does not function as an etch stop layer. As a result, problems occur such that etching proceeds in a short time and damages the base wafer, or dimples are generated in the terrace region of the base wafer.

[0028] In contrast, as shown in Fig. 3, the etchant having a liquid temperature of 30°C or less exhibits sufficiently large selectivity ratio, and the oxide film functions as an etch stop layer. Thus the etching stops sharply on reaching the oxide film, and the etching does not damage the base wafer protected by the oxide film, and dimples are not generated in the terrace region of the base wafer. The lower limit of the liquid temperature of the etchant is not particularly restricted, and any temperature is fine as long as etching can be conducted without any trouble.

[0029] Use of the mixed acid as an etchant according to the present invention does not cause metallic contamination. Conventional alkaline etching using NaOH, KOH, or the like as an etchant gives rise to a problem because such etching causes metallic contamination, and which leads to deterioration of the electric characteristics of semiconductor devices. In contrast, etching using the mixed acid according to the present invention does not cause metallic contamination, and yield can be increased.

[0030] The method of conducting etching by using the mixed acid according to the present invention is not particularly restricted, but spin etching is preferable. Unlike dipping, liquid temperature increase of an etchant caused by chemical reaction occurred in etching is small. In order to maintain the liquid temperature of an etchant equal to or less than 30°C, compact cooling equipment will suffice, and excessive operation cost for cooling equipment is not necessary. This enables reduction of equipment size and labor savings, thereby carrying out the present invention at low cost. Also, it is certainly possible to conduct the mixed acid etching by dipping.

[0031] Hereinafter, there is described an embodiment of the case of conducting the mixed acid etching by spin etching. An apparatus for conducting the spin-etching is not particularly restricted, and for example, an apparatus shown in Fig. 5 may be used. Etching is conducted as follows: the bonded wafer 1 is held by suction by using a wafer holding means 10; an etchant 9 is provided from a nozzle 8; and the bonded wafer 1 is spun at high rotational speed. In this way, the wafer is etched by rotating the wafer, whereby centrifugal force scatters the etchant 9 outward of the wafer. The scattered etchant 9 is recovered via a recovery cup 11.

[0032] Specifically, it is preferred to rotate a bonded wafer the base wafer side of which is held by suction by using a spin etching apparatus at 300 to 400 rpm while a mixed acid is fed to the upper surface of the bond wafer from a nozzle at a flow rate of 3 to 4 L/minute for 5 seconds or more depending on an intended etching removal.

[0033] Next, after the etching is conducted for a predetermined period to remove the unbonded portion, the wafer is rinsed to quench the mixed acid etching. For example, it is preferred to rotate the wafer subjected to the mixed acid etching at 500 to 700 rpm while pure water is fed to the upper surface of the bond wafer from a nozzle at a flow rate of 1 to 2 L/minute for 30 to 40 seconds.

[0034] Next, the wafer is dried. The rinsed wafer can be spin dried, for example, by rotating the wafer at 1400 to 1600 rpm for 30 to 50 seconds. After the wafer is spin dried, the wafer is removed from the spin etching apparatus. Thus the spin etching step is complete.

As a result of the etching, a terrace region 7 is formed (Fig. 1(f)).

[0035] Next, as shown in Fig. 1(g), the surface of the bond wafer 2 is thinned so that the bond wafer has a desired thickness to form an SOI layer 6. The way of thinning the bond wafer is not particularly restricted, and can be conducted by a standard manner such as grinding and polishing.

[0036] In this way, a bonded wafer according to the present invention can be manufactured.

[0037] The present invention is not restricted to the above mentioned method of conducting the mixed acid etching by spin etching. For example, the present invention can be conducted by dipping method of dipping a wafer into an etchant to etch the wafer, or by spraying a mixed acid.

[0038] In the method mentioned above, the oxide film 4 is formed on the bond wafer 2, and then the bond wafer 2 is brought into close contact with the base wafer 3. Alternatively, an oxide film is formed on the base wafer 3 and then the base wafer 3 is brought into close contact with the bond wafer 2; or oxide films are formed on both the bond wafer 2 and the base wafer 3 and then the wafers are brought into close contact with each other. The base wafer and the bond wafer that are used in the present invention are not restricted to silicon single crystal wafers.

EXAMPLES

[0039] Hereinafter, Examples of the present invention will be described. However, the present invention is not restricted thereto.

(Example, Comparative Example)

[0040] First, mirror-polished CZ wafers each having a diameter of 200 mm, conductivity type: p-type, and a resistivity of 4 to 6 Ω·cm were prepared. These wafers were used as a base wafer and a bond wafer.
These wafers were brought into close contact with each other according to the steps (a) to (c) in Fig. 1. Then the wafers were subjected to a bonding heat treatment at 1150°C under an oxygen atmosphere for 3 hours to prepare a bonded wafer 1 in Fig. 1(d).

[0041] Next, as shown in Fig. 1(e), the outer periphery of the bond wafer 2 was ground by using a grinding machine from the outer periphery toward the center of the wafer. The thickness t was 50 μm.

[0042] Then unbonded portions in the outer periphery of the bond wafer 2 were removed by etching.
In Example, etching was conducted by using a spin etching apparatus shown in Fig. 5 while a mixed acid (an aqueous solution of hydrofluoric acid: nitric acid: acetic acid = 15 wt%: 47 wt%: 5 wt%) was used as an etchant and the liquid temperature was maintained at 23°C (room temperature) by using a compact cooling apparatus. This mixed acid etching was conducted by rotating the bonded wafer at 350 rpm the base wafer side of which was held by suction, and feeding the mixed acid to the upper surface of the bond wafer at a flow rate of 3.5 L/ minute over 86 seconds. The etching removal was about 100 μm.
In Comparative Example, alkaline etching was conducted under the same conditions as those in Example except that NaOH was used as the etchant.

[0043] Then in order to quench the etching, the bonded wafer was rinsed by rotating the wafer at 600 rpm and feeding pure water to the upper surface of the bond wafer from a nozzle at a flow rate of 1 L/ minute over 35 seconds.

[0044] Then the rinsed bonded wafer was dried by rotating the wafer at 1500 rpm for 30 seconds. Thus the spin etching step was complete.

[0045] Next, the surface of the bond wafer 2 was thinned by grinding and polishing by using a surface grinding machine and a single-side polishing machine to form an SOI layer 6. Thus a wafer shown in Fig. 1(g) was obtained.

(Microscopic observation of terrace region)

[0046] The terrace regions of the SOI wafers obtained in Example and Comparative Example were inspected for the presence of dimples by using an optical microscope. As a result, dimples were hardly observed in both of the wafers. It has been established that use of the method according to the present invention enables etch stop as with the case of conducting alkaline etching and removal of unbonded portions by etching with sufficiently high selectivity ratio.

(Evaluation of metallic contamination)

[0047] The bonded wafers obtained in Example and Comparative Example were evaluated in terms of metallic contamination by atomic absorption method. The obtained results are shown in Fig. 4. As is evident from Fig. 4, metallic contamination occurred in Comparative Example where alkaline etching was conducted, whereas almost no or little metallic contamination occurred in Example where the mixed-acid etching according to the present invention was conducted.

[0048] It should be noted that the present invention is not limited to the embodiments described above. The above-described embodiments are mere examples, and those having substantially the same structure as technical ideas described in the appended claims and providing the similar functions and advantages are included in the scope of the present invention.

Claims

1. A method for manufacturing a bonded wafer comprising steps of forming an oxide film on at least a surface of a base wafer or a surface of a bond wafer; bringing the base wafer and the bond wafer into close contact via the oxide film; subjecting these wafers to a heat treatment under an oxidizing atmosphere to bond the wafers together; grinding and removing the outer periphery of the bond wafer so that the outer periphery has a predetermined thickness; subsequently removing an unbonded portion of the outer periphery of the bond wafer by etching; and then thinning the bond wafer so that the bond wafer has a desired thickness, wherein the etching is conducted by using a mixed acid at 30°C or less at least comprising hydrofluoric acid, nitric acid, and acetic acid.

2. The method for manufacturing a bonded wafer according to Claim 1, wherein the etching is conducted by spin etching.

Fig.1

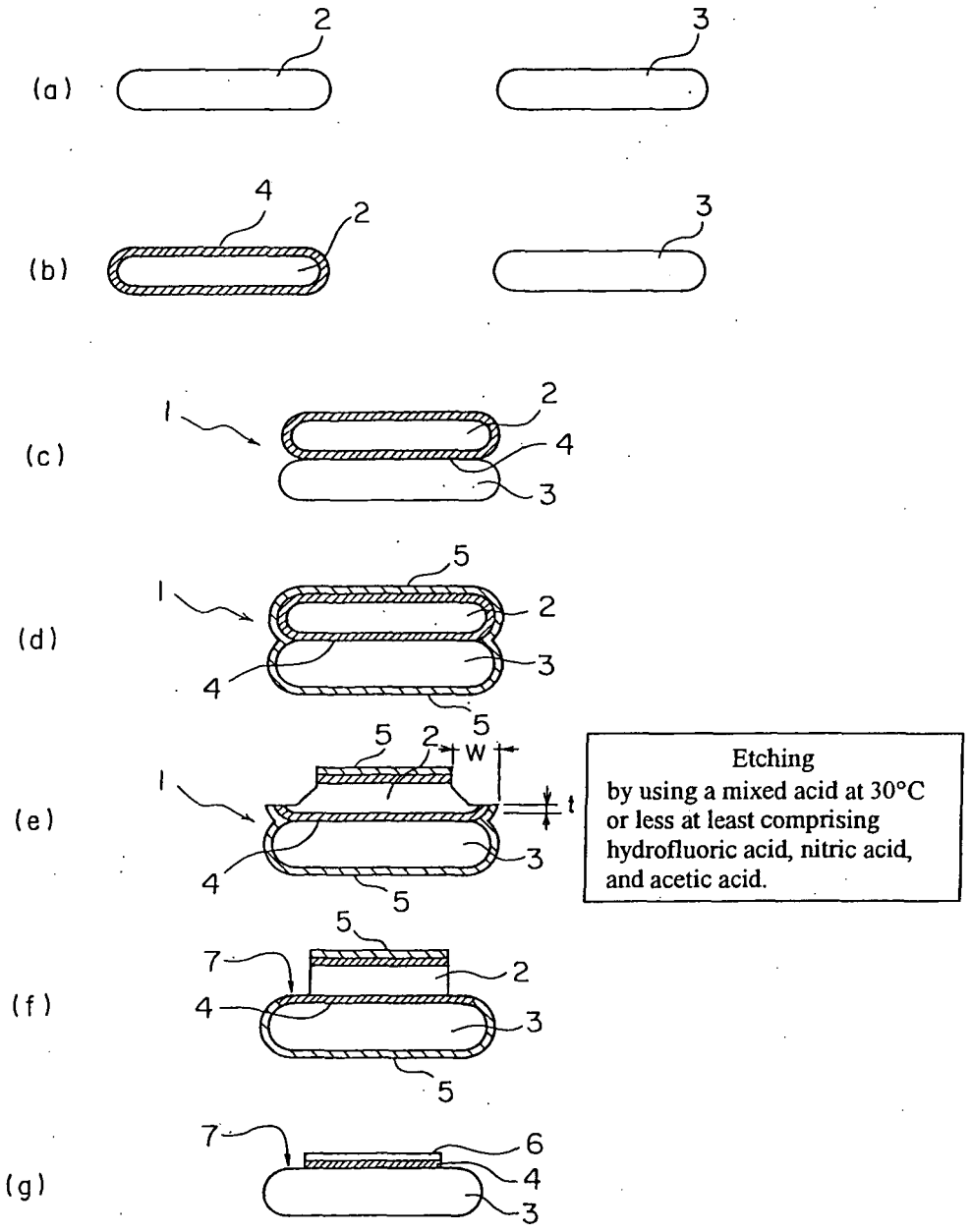
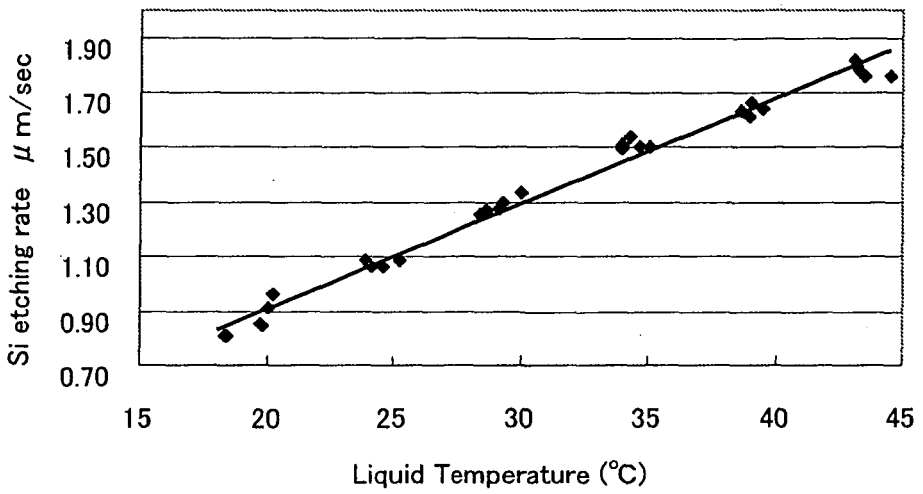

(a)
2
3
(b)
4
2
3
(c)
1
2
4
3
(d)
5
1
2
3
4
5
(e)
5
2
W
t
1
3
4
5
Etching
by using a mixed acid at 30°C
or less at least comprising
hydrofluoric acid, nitric acid,
and acetic acid.
(f)
5
7
2
4
3
5
(g)
7
6
4
3

Fig.2

(a)


Si etching rate μm/sec
1.90
1.70
1.50
1.30
1.10
0.90
0.70
15
20
25
30
35
40
45
Liquid Temperature (°C)

(b)

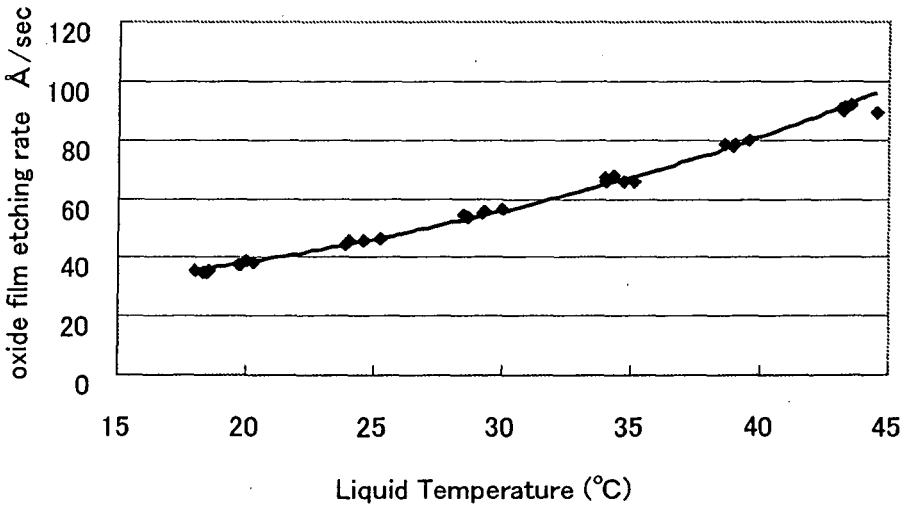

oxide film etching rate Å/sec
120
100
80
60
40
20
0
15
20
25
30
35
40
45
Liquid Temperature (°C)

Fig.3

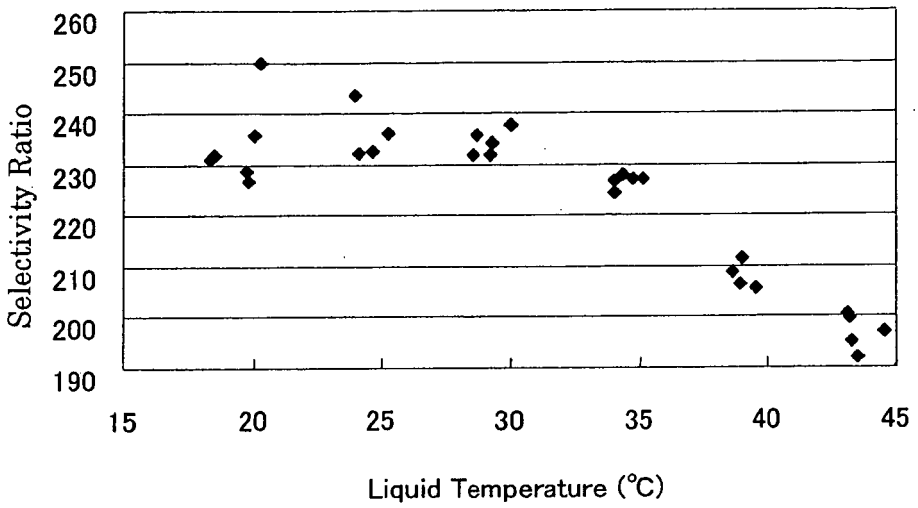

260
250
240
230
220
210
200
190
Selectivity Ratio
15
20
25
30
35
40
45
Liquid Temperature (°C)

Fig.4

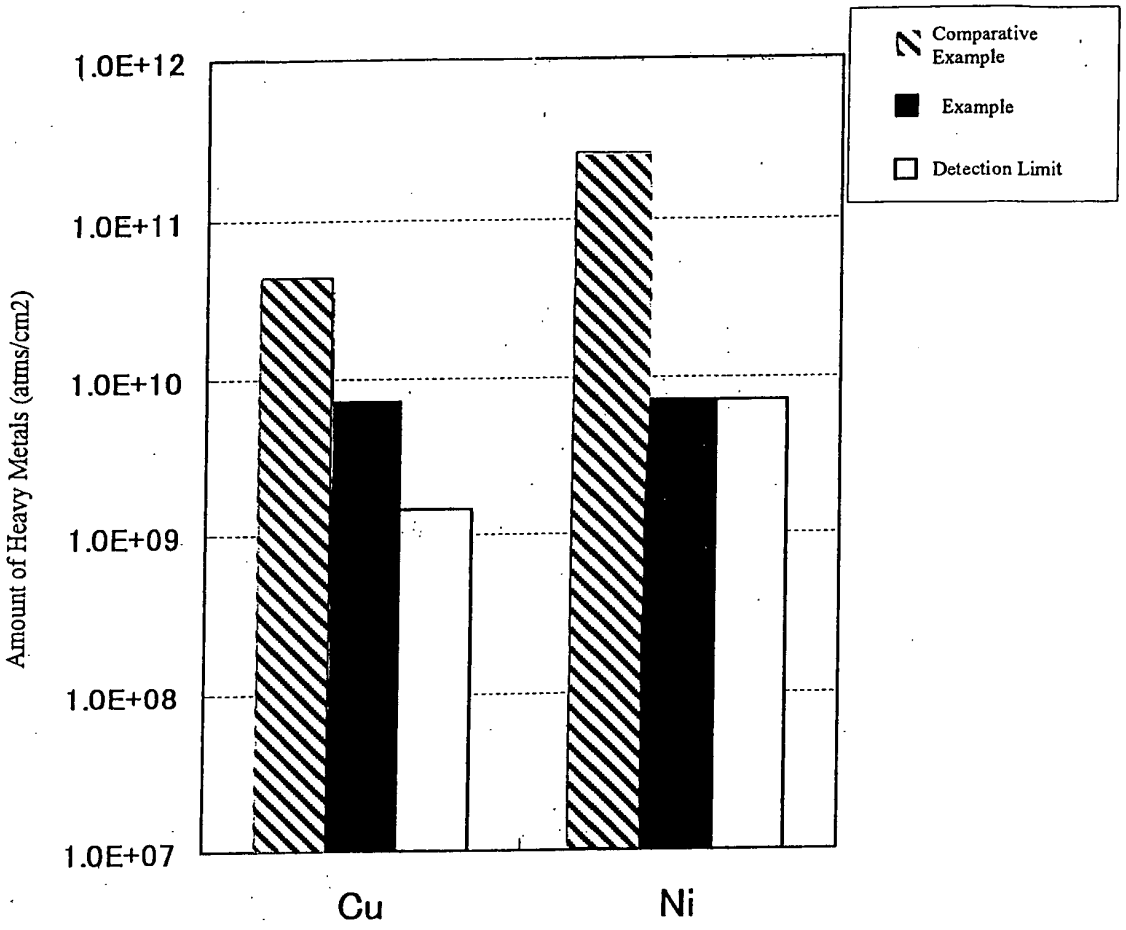
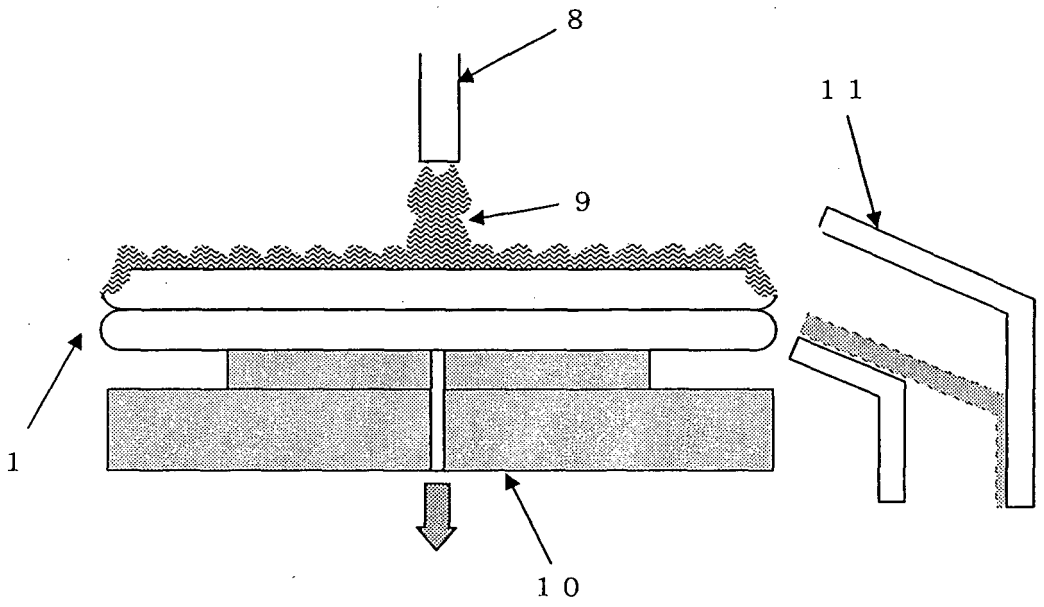

Comparative Example
Example
Detection Limit
1.0E+12
1.0E+11
1.0E+10
1.0E+09
1.0E+08
1.0E+07
Amount of Heavy Metals (atms/cm2)
Cu
Ni

Fig.5



INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP2006/309892

A. CLASSIFICATION OF SUBJECT MATTER
H01L21/02(2006.01)i, *H01L21/306*(2006.01)i, *H01L27/12*(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L21/02, H01L21/306, H01L27/12

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Jitsuyo Shinan Koho 1922-1996 Jitsuyo Shinan Toroku Koho 1996-2006
Kokai Jitsuyo Shinan Koho 1971-2006 Toroku Jitsuyo Shinan Koho 1994-2006

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	JP 06-061461 A (Mitsubishi Materials Corp.), 04 March, 1994 (04.03.94), Full text; Figs. 1 to 2 (Family: none)	1,2
Y	B. Schwartz et al., "Chemical Etching of Silicon", JOURNAL OF THE ELECTROCHEMICAL SOCIETY, Vol.108, No.4, 1961, pages 365 to 372	1,2
Y	JP 08-107091 A (Kyushu Komatsu Electronics Co., Ltd.), 23 April, 1996 (23.04.96), Full text; Figs. 1 to 2 & TW 303484 A	2

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

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"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
04 August, 2006 (04.08.06)	05 September, 2006 (05.09.06)
Name and mailing address of the ISA/ Japanese Patent Office Facsimile No.	Authorized officer Telephone No.

Form PCT/ISA/210 (second sheet) (April 2005)

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Patent documents cited in the description

- JP 10209093 A **[0007]**