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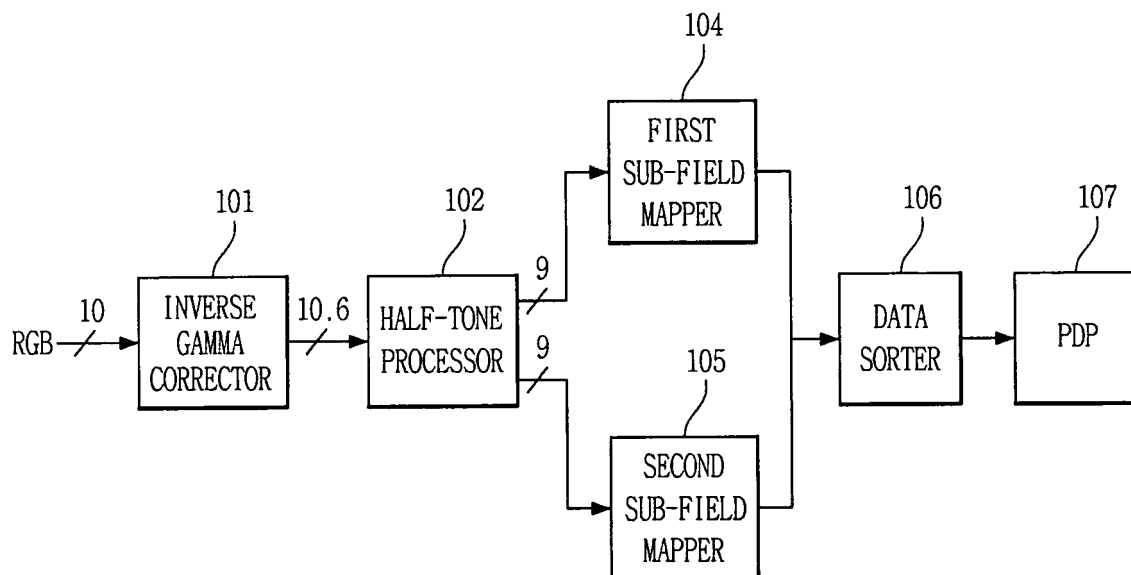
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(54) **Plasma display apparatus**

(57) A plasma display apparatus is disclosed which includes a first sub-field mapper for mapping inputted video data to a first sub-field group, a second sub-field mapper for mapping the same video data to a second

sub-field group, and a plasma display panel (PDP) for displaying an image formed by the data mapped to the first sub-field group and the data mapped to the second sub-field group consecutively within a frame.

Fig. 4



Description

Field of the Invention

[0001] The present invention relates to a display apparatus.

Description of the Background Art

[0002] In general, a plasma display apparatus is one of several contemporary display technologies, and includes a plasma display panel (hereinafter, PDP) where an image is shown, and a driver for driving the PDP. A PDP displays an image, when ultraviolet rays generated by electrical discharge in an inert gas mixture such as He+Xe, Ne+Xe, and He+Xe+Ne excites phosphors to emit visible light. The plasma display apparatus is thin and relatively easy to manufacture in large screen sizes. Recent technological developments have contributed to improve the image quality.

[0003] FIG. 1 is a perspective view showing a conventional 3-electrode alternating current (AC) surface discharge PDP.

[0004] As shown in the drawing, the conventional 3-electrode AC surface discharge PDP comprises a plurality of scan electrodes Y and a plurality of sustain electrodes Z which are formed on an upper substrate 10, and a plurality of address electrodes X formed on a lower substrate 18.

[0005] The discharge cells of a PDP are disposed at positions where the scan electrodes Y, the sustain electrodes Z and the address electrodes X are crossed with each other, and arranged in the form of a matrix.

[0006] Each of the scan electrodes Y and the sustain electrodes Z comprises a transparent electrode 12 and a metal bus electrode 11 which has a smaller linewidth than the transparent electrode 12 and formed at one edge of the transparent electrode 12. The transparent electrode 12 is generally formed of an indium tin oxide (ITO) on the upper substrate 10. The metal bus electrode 11 is generally formed of metal on the transparent electrode 12 to reduce voltage decrease caused by the highly resistant transparent electrode 12. An upper dielectric layer 13 and a protective layer 14 are stacked on the upper substrate 10 where the scan electrodes Y and the sustain electrodes Z are formed. In the upper dielectric layer 13, wall charges generated during plasma discharge are accumulated.

[0007] The protective layer 14 protects the address electrodes X, the scan electrodes Y, the sustain electrodes Z, and the upper dielectric layer 13 from sputtering during plasma discharge, and increases a secondary electron emission efficiency. The protective layer is generally formed of magnesium oxide (MgO).

[0008] The address electrodes X are formed in the lower substrate 18 in a direction crossing the scan electrodes Y1 to Yn and the sustain electrodes Z. In the lower substrate 18, a lower dielectric layer 17 and barrier ribs 15

are formed. A phosphor layer 16 is formed on the surface of the lower dielectric layer 17 and the barrier ribs 15. The barrier ribs 15 physically divide the discharge cells. The phosphor layer 16 is excited by ultraviolet ray generated during plasma discharge and generates visible light of any one among red, green and blue.

[0009] Inert gas mixture for discharge, such as He+Xe, Ne+Xe, and He+Xe+Ne, is injected into the discharge space of the discharge cells arranged between the upper and lower substrates 10 and 18 and the barrier ribs 15.

[0010] The 3-electrode AC surface discharge PDP is operated by dividing a frame into a plurality of sub-fields having a different light emission frequency to realize a gray level of image.

[0011] FIG. 2 describes an image representing method of a conventional plasma display apparatus. As shown in the drawing, when the plasma display apparatus represents image in 256 gray levels, a frame time (16.67ms) corresponding to a 1/60 second is divided into 8 sub-fields SF1 to SF8. Each of the sub-fields SF1 to SF8 is divided into a reset period for initializing the discharge cells, an address period for selecting a discharge cell, and a sustain period for realizing a gray level according to the discharge frequency number. The reset and address periods of each sub-field SF1 to SF8 are the same, whereas the sustain period and the discharge frequency number increase at a rate of 2^n ($n=0,1,2,3,4,5,6,7$) in each sub-field.

[0012] Meanwhile, when image is represented in the method of FIG. 2 in the plasma display apparatus, there is a problem that flickering occurs.

[0013] Generally, flickering occurs when the decay time of a phosphor is shorter than the frame frequency of video signals. For example, when the frame frequency is assumed to be 60Hz, video of one frame is displayed every 16.67 m/sec. Since the response time of the phosphor is faster than that, the screen flickers and image quality is deteriorated.

[0014] Particularly, the frame frequency is 50, which is relatively short, in a phase alternating line (PAL) method, and the flickering becomes more serious. In a system adopting the PAL method, the problem of flickering is reduced by arranging a plurality of groups of sub-fields in one frame.

[0015] FIG. 3 is a block view illustrating a structure of a conventional plasma display apparatus for processing video data.

[0016] Referring to FIG. 3, the conventional plasma display apparatus comprises an inverse gamma corrector 41, a half-tone processor 42, a sub-field mapper 43, and a plasma display panel (PDP) 44.

[0017] The inverse gamma corrector 41 performs inverse gamma correction onto digital video data, or read, green and blue (RGB) data, to linearize brightness change for the gray level value of a video signal.

[0018] The half-tone processor 42 diffuses the quantization error into adjacent cells to delicately control the brightness value. For this, the half-tone processor 42 di-

vides data into an integer part and a decimal part, and multiplies the decimal part by a predetermined error diffusion coefficient, for example, a Floyd-Steinberg coefficient.

[0019] The sub-field mapper 43 maps the digital video data inputted from the half-tone processor 42 to a sub-field pattern predetermined for each bit, and supplies the mapping data to the PDP through a data sorter (not shown).

[0020] However, when video data are processed as described above, a plasma display apparatus of the PAL method which divides one frame into a plurality of sub-field groups to suppress the flickering may have a contour step noise within a frame time when image is realized.

[0021] Also, there is a problem that the gray level representation ability is deteriorated unless the number of sub-fields is not increased.

SUMMARY OF THE INVENTION

[0022] Accordingly, an object of the present invention is to solve at least the problems and disadvantages of the background art.

[0023] It would be desirable to provide a plasma display apparatus that can minimize flickering and contour step noise which are generated when a plasma display panel (PDP) is driven.

[0024] A first embodiment of the present invention provides a plasma display apparatus which comprises a first sub-field mapper for mapping inputted video data to a first sub-field group, a second sub-field mapper for mapping the same video data to a second sub-field group, and a PDP for displaying an image formed by the data mapped to the first sub-field group and the data mapped to the second sub-field group consecutively within a frame.

[0025] A second embodiment of the present invention provides a plasma display apparatus which comprises a first gray level processor for modulating error-diffused data and processing a gray level of the data through dithering, a first sub-field mapper for mapping the gray level-processed data to a first sub-field group, a second gray level processor for modulating the error-diffused data and processing a gray level of the data through dithering, a second sub-field mapper for mapping the gray level-processed data to a second sub-field group, and a PDP for displaying an image formed by the data mapped to the first sub-field group and the data mapped to the second sub-field group consecutively within a frame.

[0026] The invention also provides corresponding methods.

[0027] The present invention improves gray level representation by minimizing flickering and contour step noise which are generated when a plasma display panel (PDP) is driven.

BRIEF DESCRIPTION OF THE DRAWINGS

[0028] The invention will be described in detail with reference to the following drawings in which like numerals refer to like elements.

FIG. 1 is a perspective view showing a conventional 3-electrode alternating current (AC) surface discharge plasma display panel (PDP);

FIG. 2 describes an image representation method of a conventional plasma display apparatus;

FIG. 3 is a block view illustrating a structure of a conventional plasma display apparatus for processing video data;

FIG. 4 is a block view describing a structure of a plasma display apparatus according to a first embodiment of the present invention;

FIGS. 5A to 5C show a weight arrangement of sub-fields included in a frame according to the first embodiment of the present invention; and

FIG. 6 is a block view describing a structure of a plasma display apparatus according to a second embodiment of the present invention.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

[0029] Preferred embodiments of the present invention will be described in a more detailed manner with reference to the drawings.

[0030] According to a first embodiment of the present invention, a plasma display apparatus comprises a first sub-field mapper for mapping inputted video data to a first sub-field group, a second sub-field mapper for mapping the same video data to a second sub-field group, and a PDP for displaying the data mapped to the first sub-field group and the data mapped to the second sub-field group consecutively within a frame time.

[0031] The sub-fields of each of the first sub-field group and the second sub-field group are arranged in a sequence that weights of the sub-fields are decreased.

[0032] The sub-fields of the first sub-field group are arranged in a sequence that weights of the sub-fields are increased, and the sub-fields of the second sub-field group are arranged in a sequence that weights of the sub-fields are decreased.

[0033] The sub-fields of the first sub-field group are arranged in a sequence that weights of the sub-fields are decreased, and the sub-fields of the second sub-field group are arranged in a sequence that weights of the sub-fields are increased.

[0034] One frame time approximately ranges from 16ms to 20ms.

[0035] According to a second embodiment of the present invention, a plasma display apparatus comprises a first gray level processor for modulating error-diffused data and processing a gray level of the data through dithering, a first sub-field mapper for mapping the gray level-

processed data to a first sub-field group, a second gray level processor for modulating the error-diffused data and processing a gray level of the data through dithering, a second sub-field mapper for mapping the gray level-processed data to a second sub-field group, and a PDP for displaying the data mapped to the first sub-field group and the data mapped to the second sub-field group consecutively within a frame time.

[0036] Each of the first gray level processor and the second gray level processor comprises a data modulating unit for correcting at least any one between brightness and color temperature of error-diffused data and a half-tone post-processing unit for dithering the modulated data.

[0037] Hereinafter, a plasma display apparatus of the present invention will be described in detail with reference to the accompanying drawings.

<1st Embodiment >

[0038] FIG. 4 is a block view describing a structure of a plasma display apparatus according to a first embodiment of the present invention.

[0039] The plasma display apparatus of the first embodiment comprises an inverse gamma corrector 101, a half-tone processor 102, a first sub-field mapper 104, a second sub-field mapper 105, a data sorter 106, and a PDP 107.

[0040] First, the inverse gamma corrector 101 performs 2.2 inverse gamma correction onto 10-bit digital video data, or RGB data, and supplies the inverse gamma-corrected digital video data in the form of 10-bit integer part and 6-bit decimal part to the half-tone processor 102.

[0041] The half-tone processor 102 delicately controls a brightness value by diffusing the quantization error of the decimal part of the inverse gamma-corrected digital video data, i.e., RGB data, into adjacent cells. For this, the half-tone processor 102 multiplies the decimal part by a predetermined error diffusion coefficient, for example, a Floyd-Steinberg coefficient. The digital video data error-diffused in the half-tone processor 102 are supplied to the first sub-field mapper 104 and the second sub-field mapper 105 in 9 bits.

[0042] The first sub-field mapper 104 maps the digital video data inputted from the half-tone processor 102 to sub-fields of a first sub-field group on a bit basis, and supplies the mapping data to the data sorter 106.

[0043] The second sub-field mapper 105 maps the digital video data inputted from the half-tone processor 102 to sub-fields of a second sub-field group on a bit basis, and supplies the mapping data to the data sorter 106.

[0044] The data sorter 106 combines the digital video data mapped to the first sub-field group and the digital video data mapped to the second sub-field group, and supplies the digital video data mapped to the first sub-field group to a data integrated circuit of the PDP, which is not illustrated in the drawing, and the digital video data

mapped to the second sub-field group to the data integrated circuit of the PDP consecutively within a frame time to thereby realize image on the PDP 107.

[0045] As described above, the plasma display apparatus of the first embodiment includes two sub-field mappers to map data to two sub-field groups included in one frame, and consecutively realizes the mapped data on the PDP to thereby prevent contour step noise.

[0046] The present embodiment presents two sub-field mappers but the number of sub-field mappers may be determined according to the number of sub-field groups included in one frame.

[0047] The plasma display apparatus according to the first embodiment of the present invention processes image by dividing one frame into a plurality of sub-field groups, e.g., a first sub-field group and a second sub-field group, supplying data mapped to each sub-field group to the PDP, and displaying image. Herein, one frame time (T) approximately ranges from 16ms to 20ms, and an arrangement sequence of the sub-fields by weight within one frame is as shown in FIG. 4.

[0048] FIGS. 5A to 5C show a weight arrangement of sub-fields included in a frame according to the first embodiment of the present invention.

[0049] As illustrated in the drawing, the weight of sub-fields included on one frame may be arranged in various forms in the first embodiment of the present invention.

[0050] Referring to FIG. 5A, one frame includes two or more (not shown) sub-field groups and each sub-field group SFG1 or SFG2 includes sub-fields arranged in a sequence that the weight of the sub-fields increases. In other words, the sub-fields of each sub-field group are arranged in a sequence that their gray levels increase. Referring to FIG. 5B, one frame includes two or more (not shown) sub-field groups and each sub-field group SFG1 or SFG2 includes the sub-fields arranged in a sequence that the weight of the sub-fields decreases.

[0051] Referring to FIG. 5C, one frame includes two or more (not shown) sub-field groups and each sub-field group SFG1 or SFG2 includes sub-fields arranged in a different sequence. In other words, the sub-fields of one sub-field group among the sub-field groups are arranged in a sequence that their weight expressed as gray levels increase or in a sequence that their weight expressed as gray levels decrease.

[0052] Meanwhile, although FIG. 5C shows sub-fields of one sub-field group arranged in a different sequence from a sequence that those of another sub-field group are arranged according to a predetermined rule, the sub-fields of each sub-field group may be randomly arranged without any rule on their weight.

[0053] In FIGS. 5A to 5C, 'Vsync' denotes a vertical sync signal for forming a frame, and 'SFP' denotes the size of weight according to a sub-field pattern.

[0054] When the weight arrangement sequence for the sub-fields of each sub-field group is various, it is possible to prevent contour noise phenomenon generated in still image, particularly, moving picture, and thus the image

quality can be improved.

<2nd Embodiment>

[0055] FIG. 6 is a block view describing a structure of a plasma display apparatus according to a second embodiment of the present invention.

[0056] Referring to FIG. 6, the plasma display apparatus suggested in the second embodiment of the present invention comprises an inverse gamma corrector 111, a half-tone pre-processor 112, a first gray level processor 113, a second gray level processor 114, a first sub-field mapper 115, a second sub-field mapper 116, a data sorter 17, and a PDP 118.

[0057] First, the inverse gamma corrector 111 performs 2.2 inverse gamma correction onto 10-bit digital video data, i.e., RGB data, and supplies the inverse gamma-corrected digital video data in the form of a 10-bit integer part and a 6-bit decimal part to the half-tone pre-processor 112.

[0058] The half-tone pre-processor 112 delicately controls a brightness value by diffusing a quantization error of the decimal part of the inverse gamma-corrected digital video data, i.e., RGB data, into adjacent cells. For this, the half-tone pre-processor 112 multiplies the decimal part by a predetermined error diffusion coefficient, for example, a Floyd-Steinberg coefficient. The digital video data error-diffused in the half-tone pre-processor 112 are supplied to the first and second gray level processors 113 and 114 in 9 bits.

[0059] The first and second gray level processors 113 and 114 modulate the error-diffused data and improve the gray level representation of the data through dithering. Particularly, each of the first and second gray level processors 113 and 114 comprises a data modulating unit 113a or 114a for correcting at least any one between the brightness and color temperature, and a half-tone post-processing unit 113b or 114b for dithering the modulated data.

[0060] The first data modulating unit 113a stores brightness correction data established based on the first sub-field group SFG1 to correct a brightness difference, when there is a difference in brightness between the first sub-field group SFG1 and the second sub-field group SFG2, or it stores color temperature correction data for correcting the color temperature of data mapped to the first sub-field group SFG1. The first data modulating unit 113a modulates the digital video data inputted from the half-tone pre-processor 112 in 1:1 based on the predetermined brightness correction data or color temperature correction data and supplies the modulated data to the first sub-field mapper 115.

[0061] The second data modulating unit 114a, too, stores brightness correction data established based on the second sub-field group SFG2 to correct a brightness difference, when there is a difference in brightness between the first sub-field group SFG1 and the second sub-field group SFG2, or it stores color temperature correc-

tion data for correcting the color temperature of data mapped to the second sub-field group SFG2. The second data modulating unit 114a modulates the digital video data inputted from the half-tone pre-processor 112 in 1:1 based on the predetermined brightness correction data or color temperature correction data and supplies the modulated data to the second sub-field mapper 116.

[0062] The first and second data modulating units 113a and 114a includes a Read Only Memory (ROM) for storing the brightness correction data or the color temperature correction data and a look-up table comprising a memory control circuit for designating the address of the ROM.

[0063] The first half-tone post-processing unit 113a dithers the data outputted from the first data modulating unit 113a with a dither mask which is optimally designed based on the first sub-field group (SFG1) to thereby make the quantization error of the decimal part a threshold value, and supplies 9-bit digital video data to the first sub-field mapper 115.

[0064] The second half-tone post-processing unit 114b dithers the data outputted from the second data modulating unit 114a with a dither mask which is optimally designed based on the second sub-field group (SFG2) to thereby make the quantization error of the decimal part a threshold value, and supplies 9-bit digital video data to the second sub-field mapper 116.

[0065] The first sub-field mapper 115 maps the digital video data inputted from the first half-tone post-processing unit 113b to a predetermined first sub-field group SFG1 on a bit basis and supplies the mapping data to the data sorter 117.

[0066] The second sub-field mapper 116 maps the digital video data inputted from the second half-tone post-processing unit 114b to a predetermined second sub-field group SFG2 on a bit basis and supplies the mapping data to the data sorter 117.

[0067] The data sorter 117 combines the digital video data mapped to the first sub-field group SFG1 and the digital video data mapped to the second sub-field group SFG2, supplies the digital video data mapped to the first sub-field group SFG1 to data integrated circuits of the PDP, which are not shown in the drawing, and then supplies the digital video data mapped to the second sub-field group SFG2 to data integrated circuits of the PDP consecutively within a frame time.

[0068] Meanwhile, the first data modulating unit 113a may perform inverse gamma correction onto the digital video data to be mapped to the first sub-field group SFG1, and the second data modulating unit 114a may perform inverse gamma correction onto the digital video data to be mapped to the second sub-field group SFG2. In this case, the inverse gamma corrector 111 is removed.

[0069] As described above, the plasma display apparatus of the second embodiment comprises two sub-field mappers to map data to two sub-field groups included in one frame. When it represents the mapped data on the PDP consecutively, it can prevent the contour step noise.

[0070] Also, the plasma display apparatus can improve gray level representation by correcting the brightness or color temperature of the data.

[0071] The plasma display apparatus of the second embodiment processes image by dividing one frame into a plurality of sub-field groups, e.g., a first sub-field group and a second sub-field group, which is the same as in the plasma display apparatus of the first embodiment, supplying data mapped to each sub-field group to the PDP, and displaying the image. Herein, one frame time (T) approximately ranges from 16ms to 20ms, and the sub-fields of one frame are arranged by weight in a sequence described in the plasma display apparatus of the first embodiment. Since the arrangement sequence is the same, further description on it will not be provided herein. The plasma display apparatus of the present invention is not limited to a case where the frequency of video signals is 50Hz but it can be applied to a case where the frequency of video signals is 60Hz, such as the National Television System Committee (NTSC) television.

[0072] The invention being thus described, it will be obvious that the same may be varied in many ways. Such variations are not to be regarded as a departure from the scope of the invention and all such modifications as would be obvious to one skilled in the art are intended to be included within the scope of the following claims.

Claims

1. A plasma display apparatus, comprising:

a first sub-field mapper for mapping inputted video data to a first sub-field group;
a second sub-field mapper for mapping the same video data to a second sub-field group;
and
a plasma display panel for displaying an image formed by the data mapped to the first sub-field group and the data mapped to the second sub-field group consecutively within a frame.

2. The plasma display apparatus as claimed in claim 1, wherein the sub-fields of each of the first sub-field group and the second sub-field group are arranged in a sequence that weights of the sub-fields are decreased.

3. The plasma display apparatus as claimed in claim 1, wherein the sub-fields of each of the first sub-field group and the second sub-field group are arranged in a sequence that weights of the sub-fields are increased.

4. The plasma display apparatus as claimed in claim 1, wherein the sub-fields of the first sub-field group are arranged in a sequence that weights of the sub-

fields are increased, and the sub-fields of the second sub-field group are arranged in a sequence that weights of the sub-fields are decreased.

5. The plasma display apparatus as claimed in claim 1, wherein the sub-fields of the first sub-field group are arranged in a sequence that weights of the sub-fields are decreased, and the sub-fields of the second sub-field group are arranged in a sequence that weights of the sub-fields are increased.

6. The plasma display apparatus as claimed in claim 1, wherein one frame time approximately ranges from 16ms to 20ms.

7. A method of operating a plasma display panel comprising:

mapping input video data to a first sub-field group;
mapping the same video data to a second sub-field group; and
displaying an image formed by the data mapped to the first sub-field group and the data mapped to the second sub-field group consecutively within a frame.

Fig. 1

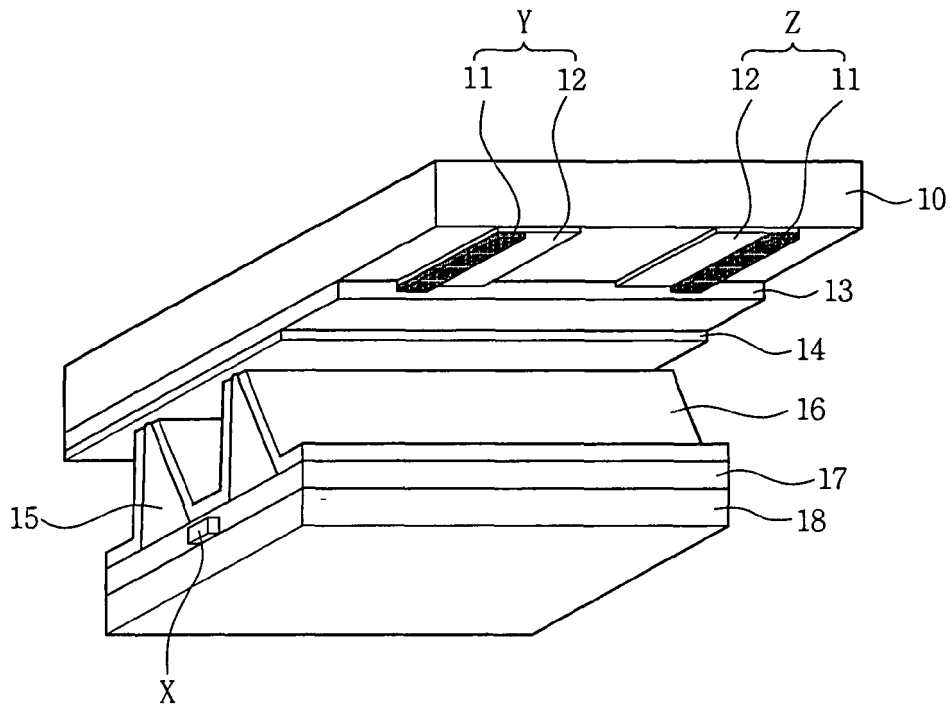


Fig. 2

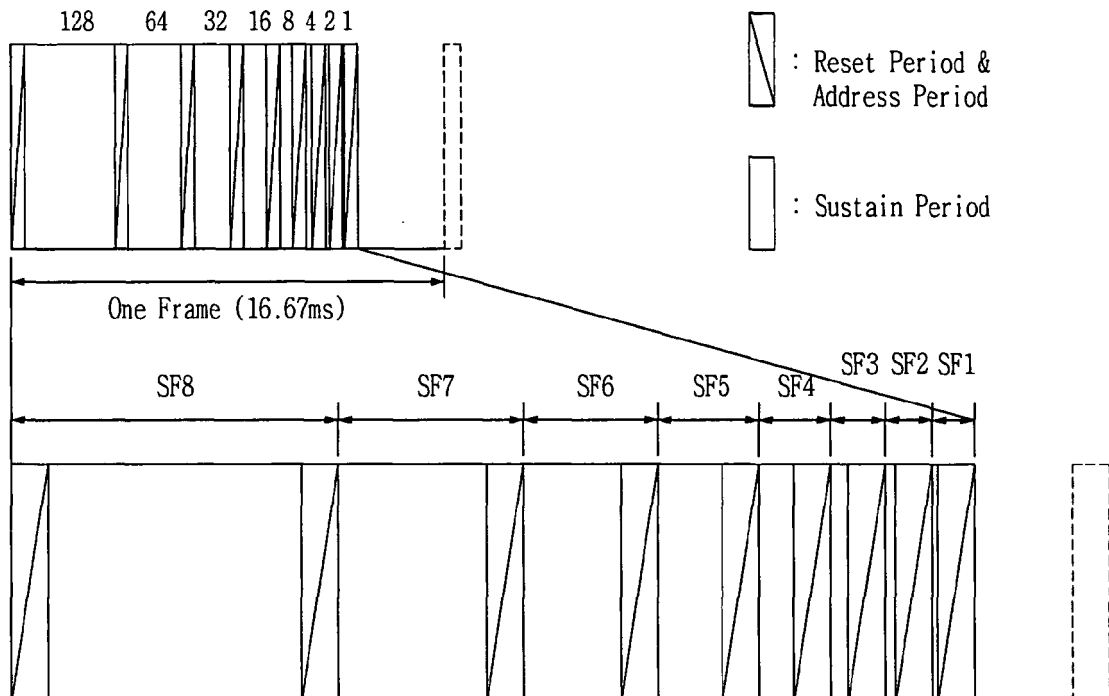


Fig. 3

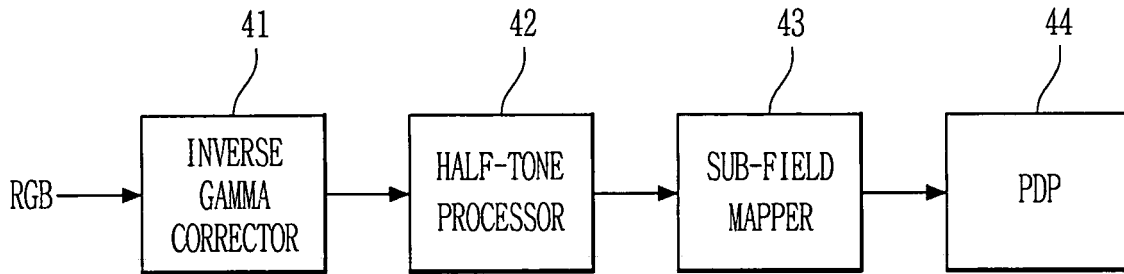


Fig. 4

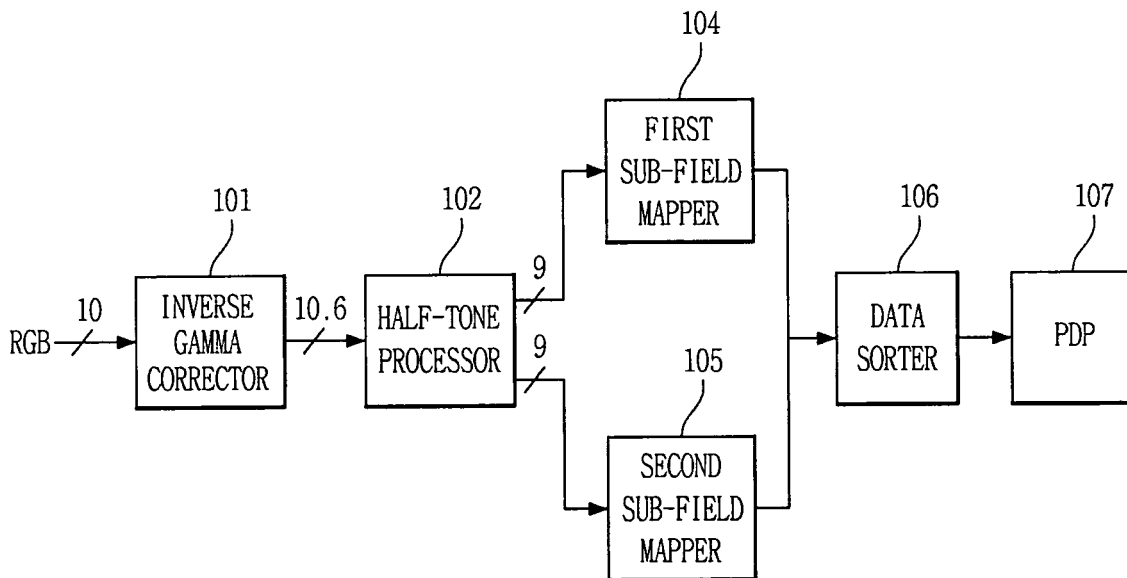


Fig. 5a

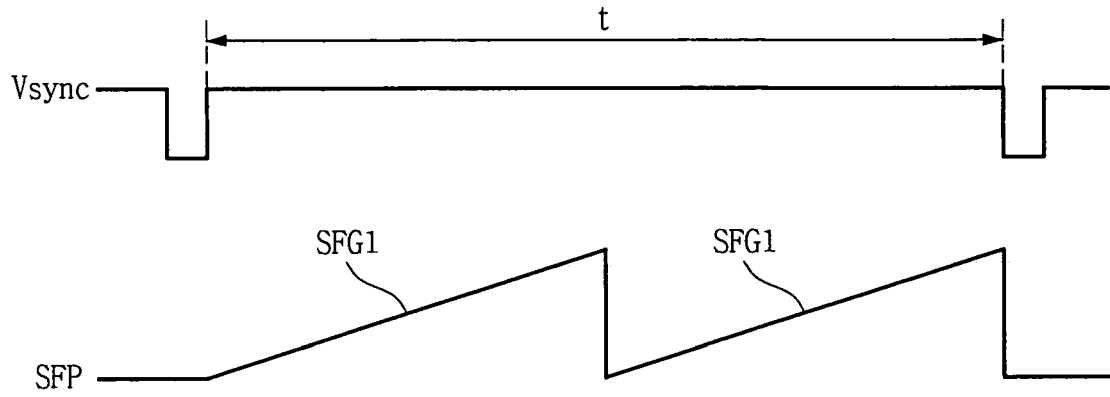


Fig. 5b

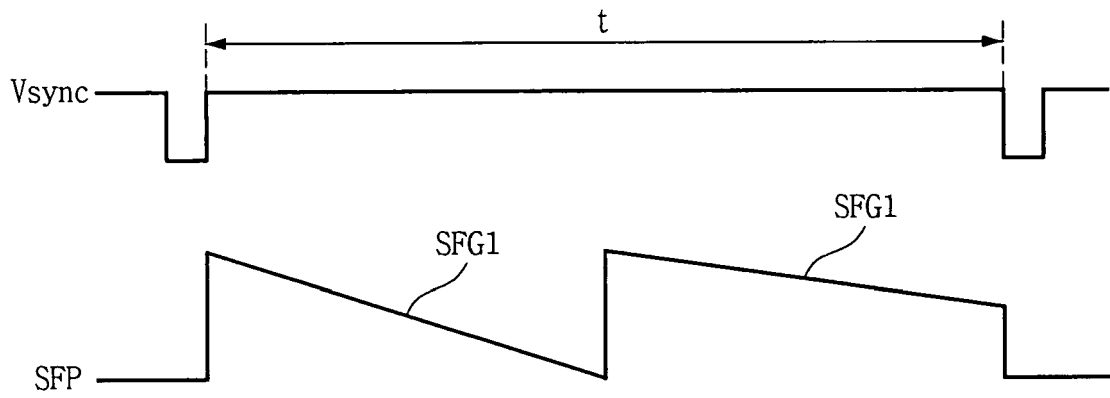


Fig. 5c

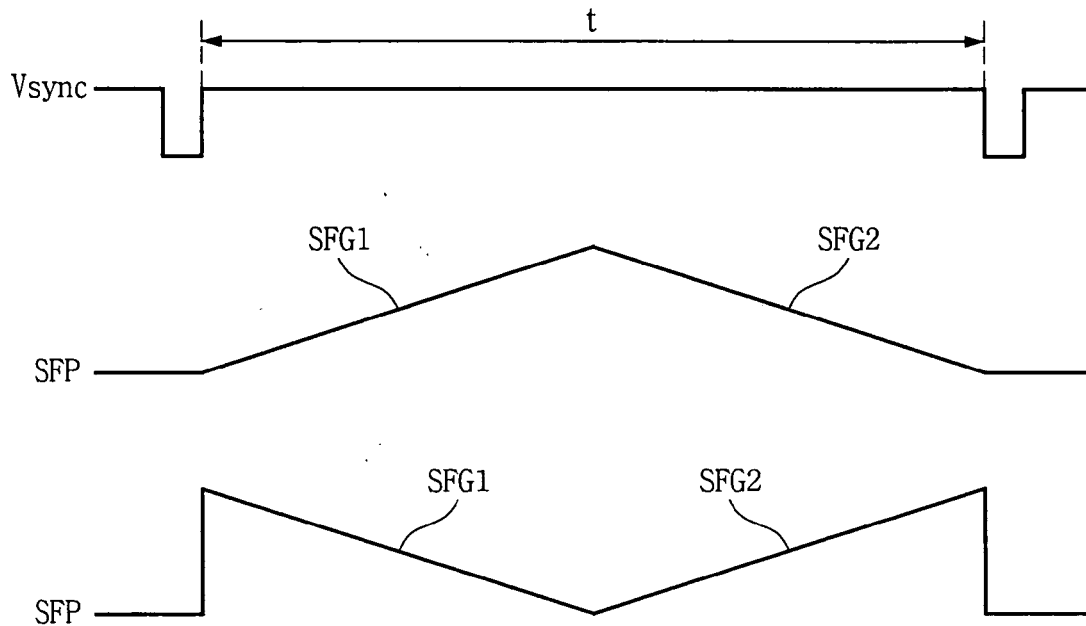
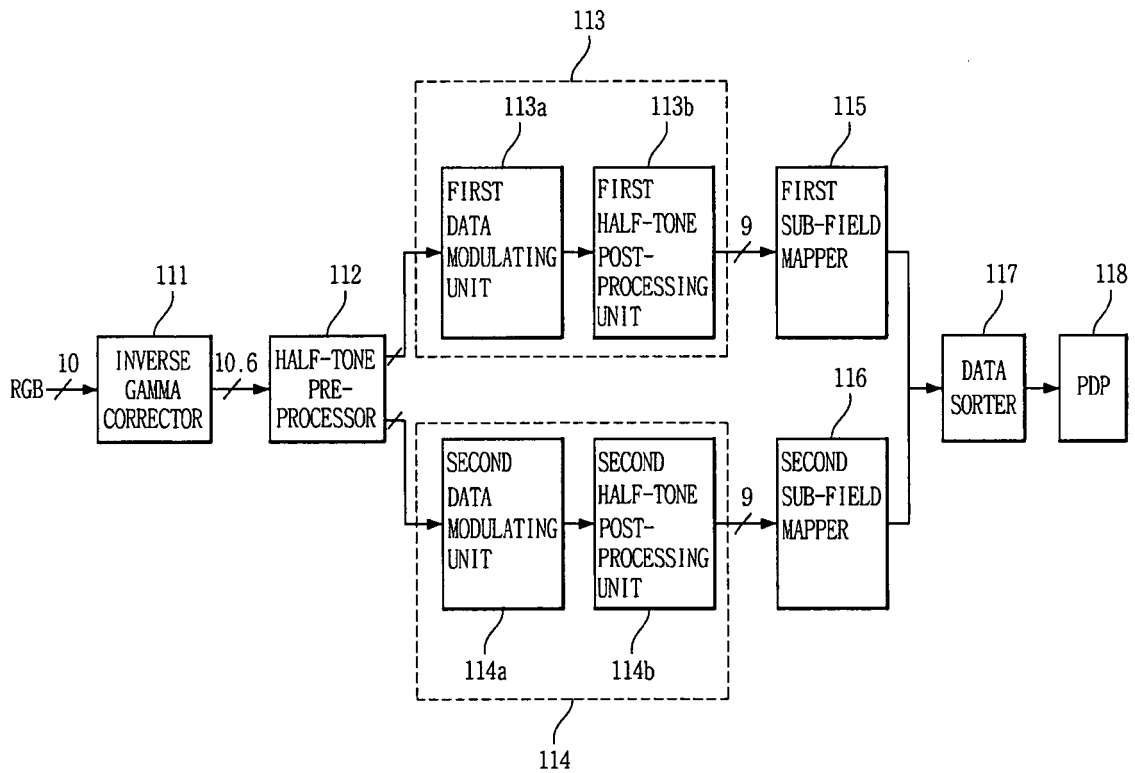


Fig. 6





European Patent
Office

EUROPEAN SEARCH REPORT

Application Number
EP 06 25 5670

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The present search report has been drawn up for all claims			
Place of search Munich		Date of completion of the search 30 January 2007	Examiner Giancane, Iacopo
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EPO FORM 1503 03.82 (P04C01)

**ANNEX TO THE EUROPEAN SEARCH REPORT
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EP 06 25 5670

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