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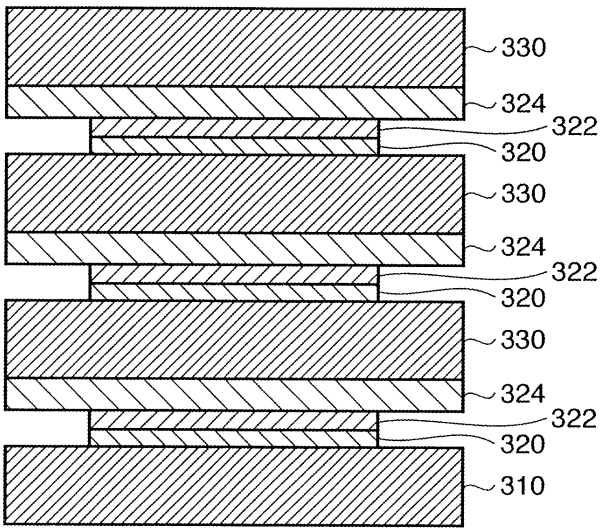
(54) **PROCESS FOR PRODUCING SEMICONDUCTOR SUBSTRATE**

(57) A semiconductor substrate fabrication method according to the first aspect of this invention is **characterized by** including a preparation step of preparing an underlying substrate, a stacking step of stacking, on the underlying substrate, at least two multilayered films each including a peeling layer and a semiconductor layer, and a separation step of separating the semiconductor layer.

FIG. 14



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Description

TECHNICAL FIELD

[0001] The present invention relates to a semiconductor substrate fabrication method.

BACKGROUND ART

[0002] A method of fabricating a GaN substrate using a sapphire underlying substrate has been conventionally proposed. The conventional GaN substrate fabrication method will be explained below with reference to Figs. 1 to 3. Figs. 1 to 3 are sectional views showing the steps in the GaN substrate fabrication method.

[0003] In a step shown in Fig. 1, a sapphire underlying substrate 110 is prepared as an underlying substrate. A peeling layer (low-temperature GaN buffer layer) 120 is grown on the sapphire underlying substrate 110 at a temperature (low temperature) lower than 1,000°C. The peeling layer 120 can be made of, e.g., a single-crystal material, polycrystalline material, or amorphous material of GaN. Then, a GaN layer 130 is grown at a temperature (high temperature) of about 1,000°C. The GaN layer 130 can be made of, e.g., a single-crystal material of GaN. In this manner, a structure 100 including the peeling layer 120 and GaN layer 130 is formed on the sapphire underlying substrate 110. Note that the peeling layer 120 also has a buffering function.

[0004] In a step shown in Fig. 2, the sapphire underlying substrate 110 and structure 100 (in a reaction chamber) are cooled from about 1,000°C to room temperature. The thermal expansion coefficient of the sapphire underlying substrate 110 is higher than that of the GaN layer 130. When the temperature is lowered from about 1,000°C to room temperature, therefore, a thermal stress resulting from the thermal expansion coefficient difference acts on the sapphire underlying substrate 110 and GaN layer 130, and warping occurs.

[0005] In a step shown in Fig. 3, the peeling layer 120 is melted by the laser lift-off method or the like. This separates the GaN layer 130 from the sapphire underlying substrate 110. That is, a GaN substrate is fabricated by separating the GaN layer 130 from the sapphire underlying substrate 110. In this state, the GaN layer 130 produces a portion in which the internal stress has reduced, and a portion in which the internal stress remains. This may crack the GaN layer 130.

[0006] The separated GaN layer 130 warps because the distribution of strain changes along the crystal growth direction. Accordingly, even when the GaN layer is planarized by a mechanical polishing step, the crystal orientation is distorted as shown in Fig. 3.

[0007] To reduce this warping, a method of forming a gap between the sapphire underlying substrate 110 and peeling layer 120 has been proposed (e.g., patent reference 1).

Patent Reference 1: Japanese Patent Laid-Open No. 2004-39810

DISCLOSURE OF INVENTION

[0008] In the technique disclosed in patent reference 1, only one semiconductor substrate can be fabricated from the underlying substrate. This decreases the throughput (productivity) in the fabrication of semiconductor substrates.

[0009] The present invention provides a semiconductor substrate fabrication method capable of increasing the throughput.

[0010] A semiconductor substrate fabrication method according to the first aspect of the present invention is characterized by comprising a preparation step of preparing an underlying substrate, a stacking step of stacking, on the underlying substrate, at least two multilayered films each including a peeling layer and a semiconductor layer, and a separation step of separating the semiconductor layer.

[0011] A semiconductor substrate fabrication method according to the second aspect of the present invention is characterized in that in the separation step, at least two semiconductor layers are separated by selectively etching the peeling layers by using a chemical solution, in addition to having the characteristic of the semiconductor substrate fabrication method according to the first aspect of the present invention.

[0012] A semiconductor substrate fabrication method according to the third aspect of the present invention is characterized in that in the stacking step, stacking is continuously performed without atmospheric exposure, in addition to having the characteristic of the semiconductor substrate fabrication method according to the first or second aspect of the present invention.

[0013] A semiconductor substrate fabrication method according to the fourth aspect of the present invention is characterized in that in the stacking step, stacking is performed in the same apparatus, in addition to having the characteristic of the semiconductor substrate fabrication method according to the first or second aspect of the present invention.

[0014] A semiconductor substrate fabrication method according to the fifth aspect of the present invention is characterized in that the underlying substrate and the semiconductor layer are made of a single crystal of a compound semiconductor, in addition to having the characteristic of the semiconductor substrate fabrication method according to any one of the first to fourth aspects of the present invention.

[0015] A semiconductor substrate fabrication method according to the sixth aspect of the present invention is characterized in that the underlying substrate and the semiconductor layer are made of a compound of a group-III element and nitrogen, in addition to having the characteristic of the semiconductor substrate fabrication method according to any one of the first to fifth aspects of the present invention.

[0016] A semiconductor substrate fabrication method according to the seventh aspect of the present invention is characterized in that the underlying substrate and the semiconductor layer are made of the same material, in addition to having the characteristic of the semiconductor substrate fabrication method according to any one of the first to sixth aspects of the present invention.

[0017] A semiconductor substrate fabrication method according to the eighth aspect of the present invention is characterized in that the peeling layer comprises at least one of a metal layer and a metal nitride layer, in addition to having the characteristic of the semiconductor substrate fabrication method according to any one of the first to seventh aspects of the present invention.

[0018] A semiconductor substrate fabrication method according to the ninth aspect of the present invention is characterized in that in the stacking step, the metal nitride layer is formed by nitriding the metal layer in a reaction furnace which grows the semiconductor layer, in addition to having the characteristic of the semiconductor substrate fabrication method according to the eighth aspect of the present invention.

[0019] A semiconductor substrate fabrication method according to the 10th aspect of the present invention is characterized in that the multilayered film includes a buffer layer between the peeling layer and the semiconductor layer, in addition to having the characteristic of the semiconductor substrate fabrication method according to any one of the first to ninth aspects of the present invention.

[0020] A semiconductor substrate fabrication method according to the 11th aspect of the present invention is characterized in that the buffer layer is made of a single crystal of a compound semiconductor, in addition to having the characteristic of the semiconductor substrate fabrication method according to the 10th aspect of the present invention.

[0021] A semiconductor substrate fabrication method according to the 12th aspect of the present invention is characterized in that the buffer layer is made of a compound of a group-III element and nitrogen, in addition to having the characteristic of the semiconductor substrate fabrication method according to the 10th or 11th aspect of the present invention.

[0022] A semiconductor substrate fabrication method according to the 13th aspect of the present invention is characterized in that the buffer layer and the semiconductor layer are made of the same material, in addition to having the characteristic of the semiconductor substrate fabrication method according to any one of the 10th to 12th aspects of the present invention.

[0023] The present invention can increase the throughput.

BRIEF DESCRIPTION OF DRAWINGS

[0024]

Fig. 1 is a sectional view showing a step in a conventional GaN substrate fabrication method;
Fig. 2 is a sectional view showing another step in the conventional GaN substrate fabrication method;
Fig. 3 is a sectional view showing still another step in the conventional GaN substrate fabrication method;
Fig. 4 is a sectional view of a step showing a problem to be solved by the present invention;
Fig. 5 is a sectional view of another step showing the problem to be solved by the present invention;
Fig. 6 is a sectional view of still another step showing the problem to be solved by the present invention;
Fig. 7 is a sectional view showing a step in a semiconductor substrate fabrication method according to an embodiment of the present invention;
Fig. 8 is a sectional view showing another step in the semiconductor substrate fabrication method according to the embodiment of the present invention;
Fig. 9 is a sectional view showing still another step in the semiconductor substrate fabrication method according to the embodiment of the present invention;
Fig. 10 is a sectional view showing still another step in the semiconductor substrate fabrication method according to the embodiment of the present invention;
Fig. 11 is a sectional view showing still another step in the semiconductor substrate fabrication method according to the embodiment of the present invention;
Fig. 12 is a sectional SEM photograph showing a sample obtained by the steps shown in Figs. 7 to 11;
Fig. 13 is a sectional view showing still another step in the semiconductor substrate fabrication method according to the embodiment of the present invention;
Fig. 14 is a sectional view showing still another step in the semiconductor substrate fabrication method according to the embodiment of the present invention; and
Fig. 15 is a sectional view showing still another step in the semiconductor substrate fabrication method according to the embodiment of the present invention.

BEST MODE FOR CARRYING OUT THE INVENTION

[0025] Problems to be solved by the present invention will be explained in detail below with reference to Figs. 4 to 6. Figs. 4 to 6 are sectional views of steps showing the problems to be solved by the present invention. Although the following explanation will be made by taking a method of fabricating a GaN substrate (semiconductor substrate) by using a GaN underlying substrate (underlying substrate) as an example, the present invention is also applicable to a method of fabricating another semiconductor substrate by using another underlying substrate. The other underlying substrate can be made of a

nitride such as InN, AlN, InGaN, AlGaN, InAlN, or AlInGaIV, a group-IV material such as SiC or Si, an oxide such as Al_2O_3, $MgAl_2O_4$, $LiGa_2O_4$, or ZnO, or a nitridable metal such as Fe, Cr, Mo, Ta, Nb, Ti, or Cu. The other semiconductor substrate can be made of a nitride such as AlN, InN, or AlGaInN, or an oxide such as ZnO, ZnMgO, ZnCdO, or ZnMgCdO.

[0026] In a step shown in Fig. 4, a GaN underlying substrate 210 is prepared as an underlying substrate. A peeling layer (metal buffer layer) 220 is formed on the GaN underlying substrate 210. The peeling layer 220 can be made of a nitridable metal such as Fe, Cr, Mo, Ta, Nb, Ti, or Cu.

[0027] A GaN layer (semiconductor layer) 230 is grown on the peeling layer 220 at about 1,000°C. The GaN layer 230 can be made of, e.g., a single-crystal material of GaN. In this manner, a structure 200 including the peeling layer 220 and GaN layer 230 is formed on the GaN underlying substrate 210. Note that the peeling layer 220 also has a buffering function.

[0028] In a step shown in Fig. 5, the GaN underlying substrate 210 and structure 200 (in a reaction chamber) are cooled from about 1,000°C to room temperature. The thermal expansion coefficient of the GaN underlying substrate 210 is almost equal to that of the GaN layer 230. When the temperature is lowered from about 1,000°C to room temperature, therefore, almost no thermal stress resulting from the thermal expansion coefficient difference acts on the GaN underlying substrate 210 and GaN layer 230, and almost no warping occurs.

[0029] In a step shown in Fig. 6, the peeling layer 220 is selectively etched by using a chemical solution. This separates the GaN layer 230 from the GaN underlying substrate 210. That is, a GaN substrate is fabricated by separating the GaN layer 230 from the GaN underlying substrate 210. In this state, the internal stress is almost uniform in the GaN layer 230. This reduces the possibility of cracking of the GaN layer 230.

[0030] As described above, the GaN substrate fabrication method shown in Figs. 4 to 6 generally fabricates only one GaN substrate from the GaN underlying substrate 210. Accordingly, the throughput of the fabrication of GaN substrates is often insufficient.

[0031] A semiconductor substrate fabrication method according to an embodiment of the present invention will be explained below with reference to Figs. 7 to 15. Figs. 7 to 11 and 13 to 15 are sectional views showing the steps in the semiconductor substrate fabrication method according to the embodiment of the present invention. Fig. 12 is a sectional SEM photograph of a sample obtained by the steps shown in Figs. 7 to 11. Although the following explanation will be made by taking a method of fabricating a GaN substrate (semiconductor substrate) by using a GaN underlying substrate (underlying substrate) as an example, the present invention is also applicable to a method of fabricating another semiconductor substrate by using another underlying substrate. The other underlying substrate can be made of a nitride such as InN, AlN, InGaN, AlGaN, InAlN, or AlInGaN, a group-IV material such as SiC or Si, an oxide such as Al_2O_3, $MgAl_2O_4$, $LiGa_2O_4$, or ZnO, or a nitridable metal such as Fe, Cr, Mo, Ta, Nb, Ti, or Cu. The other semiconductor substrate can be made of a nitride such as AlN, InN, or AlGaInN, or an oxide such as ZnO, ZnMgO, ZnCdO, or ZnMgCdO.

[0032] In addition, a method using HVPE (Hydride Vapor Phase Epitaxy) will be explained as an example, but the present invention can also be applied to a method using, e.g., MOCVD (Metal-Organic Chemical Vapor Deposition), MOVPE (Metal-Organic Vapor Phase Epitaxy), MBE (Molecular Beam Epitaxy), or the dissolution growth method.

[0033] In a step shown in Fig. 7, a GaN underlying substrate 310 is prepared as an underlying substrate. The thickness of the GaN underlying substrate 310 is preferably 100 to 500 μm.

[0034] Note that a term "multilayered film" means a film including two or more layers in this specification.

[0035] A peeling layer (metal buffer layer) 320a is deposited on the GaN underlying substrate 310 by sputtering. The peeling layer 320a is a nitridable metal layer. The peeling layer 320a can be made of a nitridable metal such as Fe, Cr, Mo, Ta, Nb, Ti, or Cu. The thickness of the peeling layer 320a is preferably 15 to 75 nm.

[0036] Note that the peeling layer 320a may also be formed by an e-beam evaporator, a thermal evaporator, or the crystal growth method such as CVD, MOCVD, or MBE.

[0037] In a step shown in Fig. 8, a portion (upper layer) of the peeling layer 320a is nitrided in an ambience of hydrogen gas containing ammonia at a substrate temperature of 500°C to 1,000°C. Even if a native oxide film exists on the surface of the peeling layer 320a, a strong reducing action of ammonia reduces and nitrides this native oxide film. As a consequence, the peeling layer 320a divides into a first peeling layer 320 and second peeling layer 322. The first peeling layer (metal buffer layer) 320 is an unnitrided layer of the peeling layer 320a, and can be made of a nitridable metal such as Fe, Cr, Mo, Ta, Nb, Ti, or Cu. The second peeling layer (metal nitride layer) 322 is a nitrided layer of the peeling layer 320a, and can be made of a metal nitride such as Fe_2N, CrN, MoN, TaN, NbN, TiN, or CuN. The first peeling layer 320 is favorably Cr. The second peeling layer 322 is favorably CrN.

[0038] Note that the first peeling layer 320 also has a buffering function. Similarly, the second peeling layer 322 also has a buffering function. Note also that in the step shown in Fig. 8, the second peeling layer 322 may also be formed by entirely nitriding the peeling layer 320a. When the second peeling layer 322 is formed by entirely nitriding the peeling layer 320a, the thickness of the second peeling layer 322 is preferably 15 to 75 nm. Depending on the nitrogen conditions, however, the thickness of the second peeling layer 322 is sometimes smaller than that of the peeling layer 320a.

[0039] The flow rate of ammonia, the nitriding temperature, and the nitriding time mainly determine the conditions of the process of forming the uniform second peeling layer 322 on the surface of the peeling layer 320a. The process conditions for the purpose are favorably an ammonia flow rate of 1 (1/min), a nitriding temperature of 1,000°C or more, and a nitriding time of 5 min or more.

[0040] The second peeling layer 322 functions as a nucleus for forming GaN layers (a buffer layer 332 and GaN layer 330) in a step shown in Fig. 9 to be described below. Accordingly, the steps shown in Figs. 8 and 9 are preferably successively performed without atmospheric exposure as will be described below.

[0041] In the step shown in Fig. 9, the buffer layer 332 is grown on the second peeling layer 322 at a temperature (low temperature) of about 600°C to 1,000°C. More specifically, HCl gas is supplied to a Ga metal material box formed upstream of a reaction chamber via a reaction tube. In the Ga metal material box, the HCl gas and Ga cause a chemical reaction to form GaCl gas. This GaCl gas is supplied from the Ga metal material box to the reaction chamber via the reaction tube. In the reaction chamber, the ammonia-containing hydrogen gas used in the step shown in Fig. 8 remains near the surface of the second peeling layer 322. In the reaction chamber, therefore, the GaCl gas and ammonia gas cause a chemical reaction to form the buffer layer 332 on the second peeling layer 322. The buffer layer (GaN buffer layer) 332 can be made of, e.g., a single-crystal material, polycrystalline material, or amorphous material of GaN. The thickness of the buffer layer 332 is preferably a few ten Å to a few ten μm. The growth temperature of the buffer layer 332 is favorably 800°C to 1,100°C, and more favorably, about 900°C.

[0042] Since the buffer layer 332 is made of the same material (GaN) as that of the GaN layer (semiconductor layer) 330 to be described later, the GaN layer (semiconductor layer) 330 can easily grow.

[0043] Note that the buffer layer 332 may also be made of a material different from that of the GaN layer (semiconductor layer) 330 to be described later. For example, the buffer layer 332 may also be made of a nitride such as AlN, Al_xGa_yN, In_xGa_yN, or $Al_xGa_yIn_zN$ (wherein $0 < x < 1$, $0 < y < 1$, and $0 < z < 1$), or an oxide such as ZnO.

[0044] In a step shown in Fig. 10, the GaN layer (semiconductor layer) 330 is grown on the buffer layer 332 at a temperature (high temperature) of 1,000°C or more. The GaN layer (thick GaN layer) 330 can be made of, e.g., a single-crystal material of GaN. Practical conditions are basically the same as those in the step shown in Fig. 9, except that the flow rate of the HCl gas supplied to the Ga metal material box is high, and the temperature in the reaction chamber is high. Accordingly, the GaN layer 330 grows at a rate (e.g., about 100 μm/h or more) higher than that in the step shown in Fig. 9. The thickness of the GaN layer 330 is preferably 100 to 500 μm. The growth temperature of the GaN layer 330 is preferably 1,000°C or more. As a consequence, a multilayered film ML1 including the first peeling layer 320, second peeling layer 322, buffer layer 332, and GaN layer 330 is formed on the GaN underlying substrate 310.

[0045] Note that the GaN layer 330 may also be controlled to have a conductivity type such as an n-type or p-type by doping a slight amount of an impurity such as Si or Mg during or after the growth.

[0046] In the step shown in Fig. 11, the GaN underlying substrate 310 and multilayered film ML1 (in the reaction chamber) are cooled from about 1,000°C to room temperature. The thermal expansion coefficient of the GaN underlying substrate 310 is almost equal to that of the GaN layer 330. When the temperature is lowered from about 1,000°C to room temperature, therefore, almost no thermal stress resulting from the thermal expansion coefficient difference acts on the GaN underlying substrate 310 and GaN layer 330, and almost no warping occurs.

[0047] For example, the multilayered film ML1 as shown in the sectional SEM photograph of Fig. 12 is obtained by steps similar to those shown in Figs. 7 to 11. As shown in Fig. 12, the GaN underlying substrate 310 and GaN layer 330 have a flat shape. This makes it possible to estimate that almost no warping has occurred in the GaN underlying substrate 310 and GaN layer 330.

[0048] As shown in Fig. 13, a plurality of multilayered films ML1 to ML3 are formed on the GaN underlying substrate 310 by successively repeating the steps shown in Figs. 7 to 11 without atmospheric exposure. In this way, a structure 300 including the multilayered films ML1 to ML3 is formed on the GaN underlying substrate 310.

[0049] The steps shown in Figs. 7 to 11 can be performed in the same apparatus or in different apparatuses. When these steps are performed in different apparatuses, the individual reaction chambers are connected by a mechanism capable of transferring the substrate without exposing it to the atmosphere.

[0050] In steps shown in Figs. 14 and 15, the first peeling layers 320 and second peeling layers 322 are simultaneously selectively etched by using a chemical solution. That is, as shown in Fig. 14, the first peeling layers 320 and second peeling layers 322 are etched sideways.

[0051] When the first peeling layers 320 are made of, e.g., Cr, the etchant (chemical solution) is preferably an aqueous solution mixture of perchloric acid ($HClO_4$) and ammonium cerium secondary nitrate. When the first peeling layers 320 are made of, e.g., Cu, the etchant (chemical solution) is preferably an aqueous nitric acid (HNO_3) solution. The etching rate of the etchant (chemical solution) can be controlled by the temperature and concentration.

[0052] When the first peeling layers 320 and second peeling layers 322 are etched, as shown in Fig. 15, a plurality of units of the GaN layers 330 and buffer layers 332 are separated from the GaN underlying substrate 310. That is, a plurality of GaN substrates SB1 to SB3 are simultaneously fabricated by separating the units of the GaN layers 330 and buffer layers 332 from the GaN

underlying substrate 310. In this state, the internal stress is almost uniform in each GaN layer 330. This reduces the possibility of cracking of each GaN layer 330.

[0053] The buffer layers 332 form portions of the GaN substrates SB1 to SB3 without being etched by the etchant (chemical solution).

[0054] Note that in the step shown in Fig. 13, a viscous material may also hold the multilayered films ML1 to ML3 and the GaN underlying substrate 310. In this case, the GaN substrates SB1 to SB3 may also be simultaneously fabricated by dissolving this viscous material after the first peeling layers 320 and second peeling layers 322 are etched. This makes it possible to stably fabricate the GaN substrates SB1 to SB3.

[0055] Since the GaN substrates SB1 to SB3 are simultaneously fabricated in the steps shown in Figs. 14 and 15 as described above, the throughput of the fabrication of the GaN substrates SB1 to SB3 can be increased. Also, since the steps shown in Figs. 7 to 11 are successively repeated without atmospheric exposure, it is possible to save the time of evacuation and the time of atmospheric exposure (purging), and further increase the throughput of the fabrication of the GaN substrates. Furthermore, since the GaN substrates SB1 to SB3 are simultaneously fabricated, the fabrication conditions of the GaN substrates SB1 to SB3 can be made uniform, so the variations in quality of the GaN substrates SB1 to SB3 can be reduced.

[0056] Note that the steps shown in Figs. 7 to 11 and the steps shown in Figs. 14 and 15 may also be successively performed without atmospheric exposure. In this case, it is possible to save the time of transfer of samples (lots), and further increase the throughput of the fabrication of GaN substrates.

[0057] Note also that the number of the multilayered films included in the structure (the structure 300 shown in Fig. 13) is not limited to three and may also be two or more except three. Increasing the number of the multilayered films included in the structure can further increase the throughput of the fabrication of GaN substrates.

(Experimental Example)

[0058] Three GaN substrates SB1 to SB3 were continuously formed by performing the steps shown in Figs. 7 to 15 (the semiconductor substrate fabrication method according to the embodiment of the present invention) described above. The time required from the supply of the samples to the carrying out of the GaN substrates SB1 to SB3 was 26 hrs.

[0059] On the other hand, after the steps shown in Figs. 7 to 11 were performed, a first peeling layer 320 and second peeling layer 322 as shown in Fig. 11 were etched, and a unit of a GaN layer 330 and buffer layer 332 was separated from a GaN underlying substrate 310 under the same conditions as shown in Fig. 13, thereby separately in turn fabricating GaN substrates SB1 to SB3. The time required from the supply of the samples to the carrying out of the GaN substrates SB1 to SB3 was 52 hrs.

[0060] As described above, the throughput when three semiconductor substrates are continuously formed is about twice that when three semiconductor substrates are separately formed.

Claims

1. A semiconductor substrate fabrication method **characterized by** comprising:

   a preparation step of preparing an underlying substrate;
   a stacking step of stacking, on the underlying substrate, at least two multilayered films each including a peeling layer and a semiconductor layer; and
   a separation step of separating the semiconductor layer.

2. A semiconductor substrate fabrication method according to claim 1, **characterized in that**,
   in the separation step, at least two semiconductor layers are separated by selectively etching the peeling layers by using a chemical solution.

3. A semiconductor substrate fabrication method according to claim 1 or 2, **characterized in that**,
   in the stacking step, stacking is continuously performed without atmospheric exposure.

4. A semiconductor substrate fabrication method according to claim 1 or 2, **characterized in that**,
   in the stacking step, stacking is performed in the same apparatus.

5. A semiconductor substrate fabrication method according to any one of claims 1 to 4, **characterized in that**
   the underlying substrate and the semiconductor layer are made of a single crystal of a compound semiconductor.

6. A semiconductor substrate fabrication method according to any one of claims 1 to 5, **characterized in that**
   the underlying substrate and the semiconductor layer are made of a compound of a group-III element and nitrogen.

7. A semiconductor substrate fabrication method according to any one of claims 1 to 6, **characterized in that**
   the underlying substrate and the semiconductor layer are made of the same material.

8. A semiconductor substrate fabrication method according to any one of claims 1 to 7, **characterized in that**
the peeling layer comprises at least one of a metal layer and a metal nitride layer.

9. A semiconductor substrate fabrication method according to claim 8, **characterized in that**,
in the stacking step, the metal nitride layer is formed by nitriding the metal layer in a reaction furnace which grows the semiconductor layer.

10. A semiconductor substrate fabrication method according to any one of claims 1 to 9, **characterized in that**
the multilayered film includes a buffer layer between the peeling layer and the semiconductor layer.

11. A semiconductor substrate fabrication method according to claim 10, **characterized in that**
the buffer layer is made of a single crystal of a compound semiconductor.

12. A semiconductor substrate fabrication method according to claim 10 or 11, **characterized in that**
the buffer layer is made of a compound of a group-III element and nitrogen.

13. A semiconductor substrate fabrication method according to any one of claims 10 to 12, **characterized in that**
the buffer layer and the semiconductor layer are made of the same material.

FIG. 1

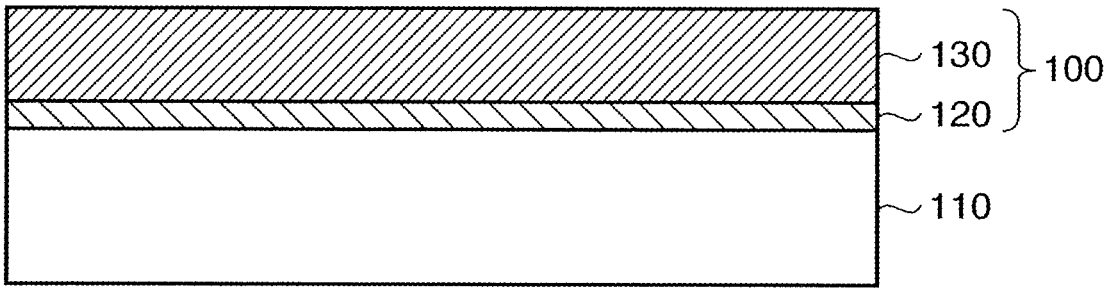

FIG. 2

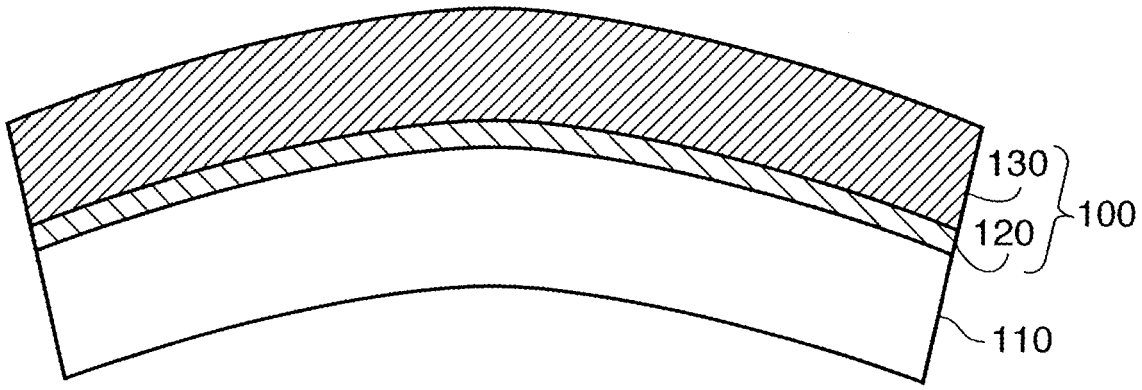

FIG. 3

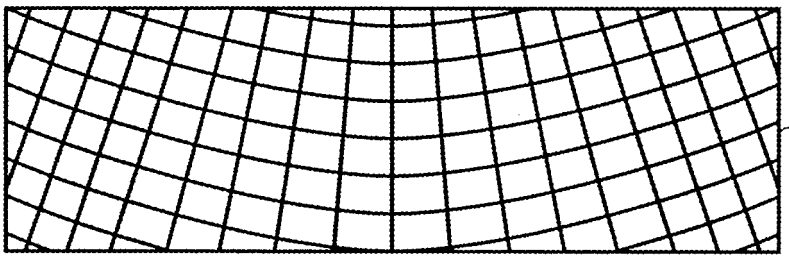

FIG. 4

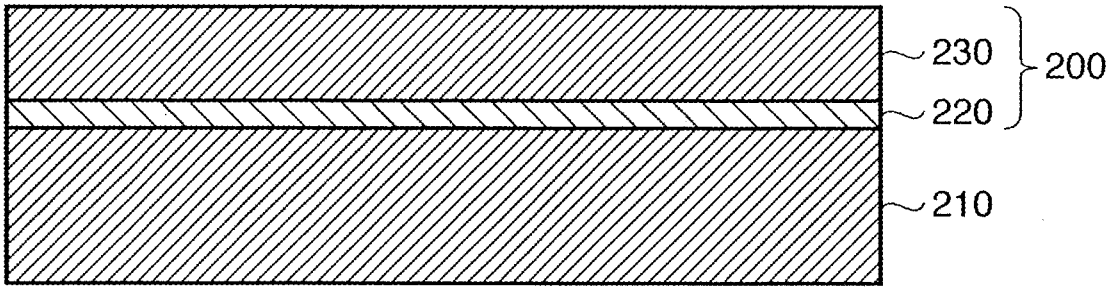

FIG. 5

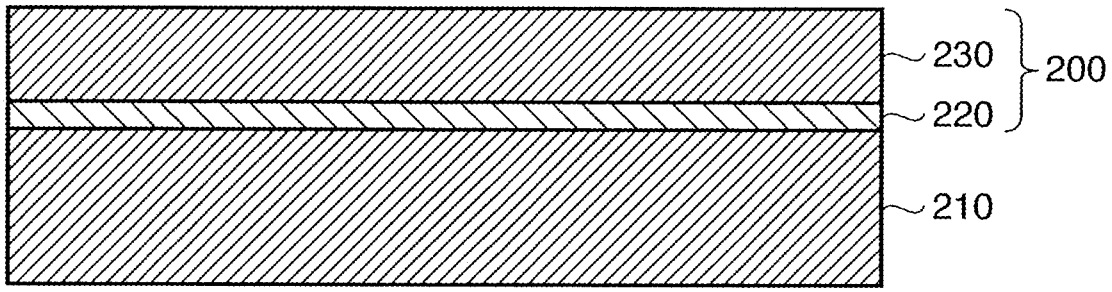

FIG. 6

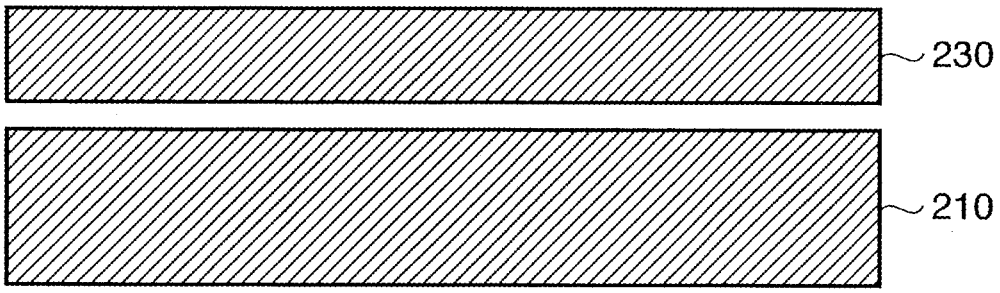

FIG. 7

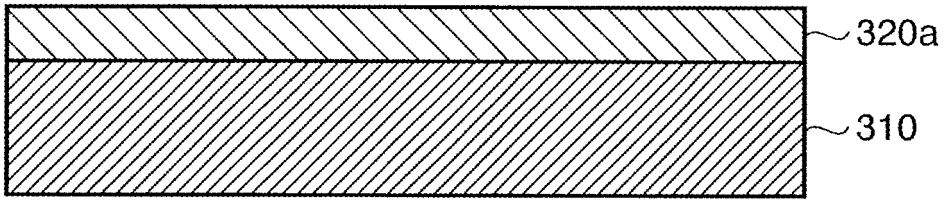

FIG. 8

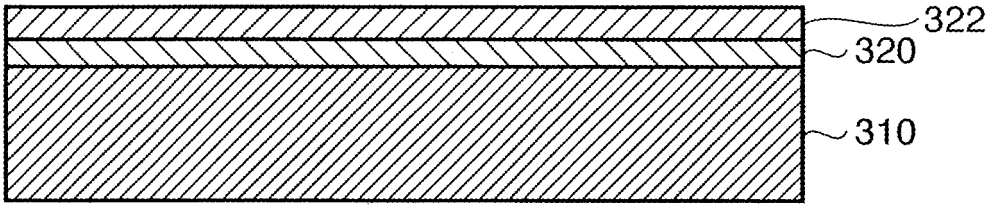

FIG. 9

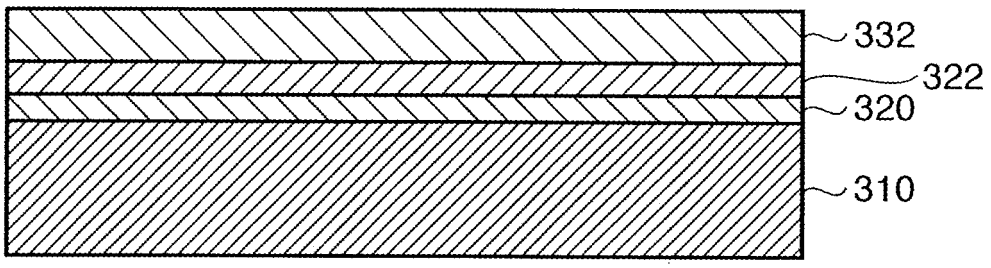

FIG. 10

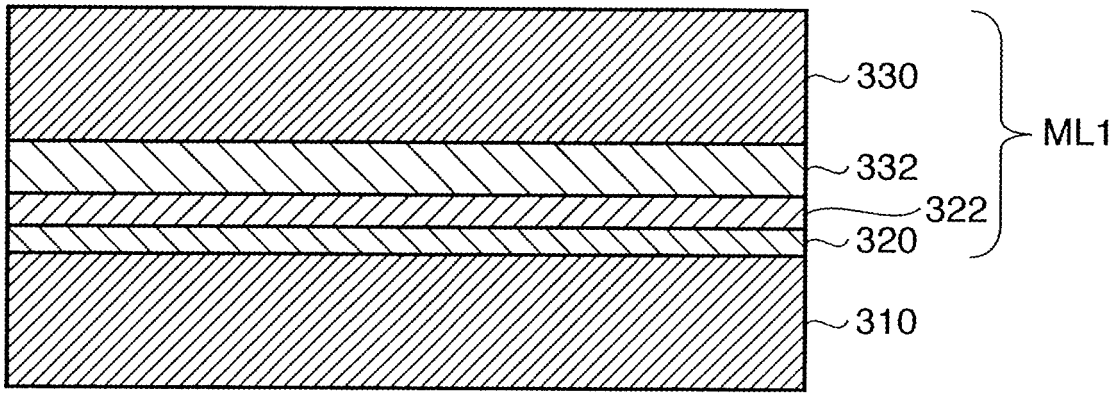

FIG. 11

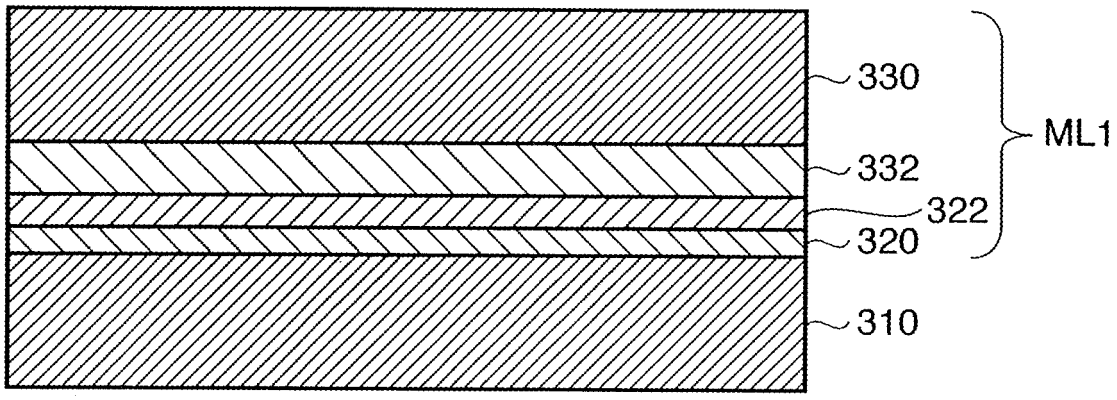

FIG. 12

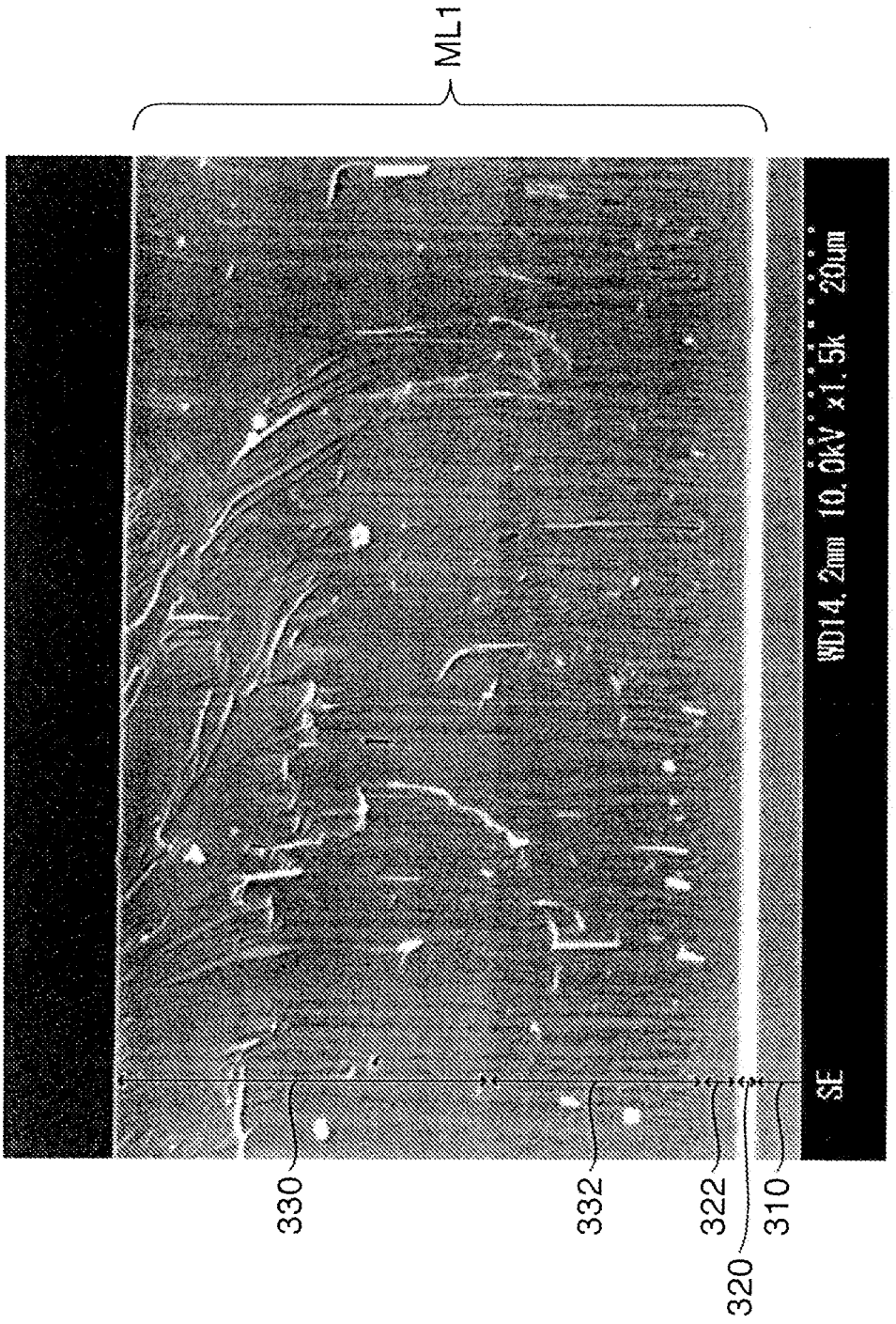

FIG. 13

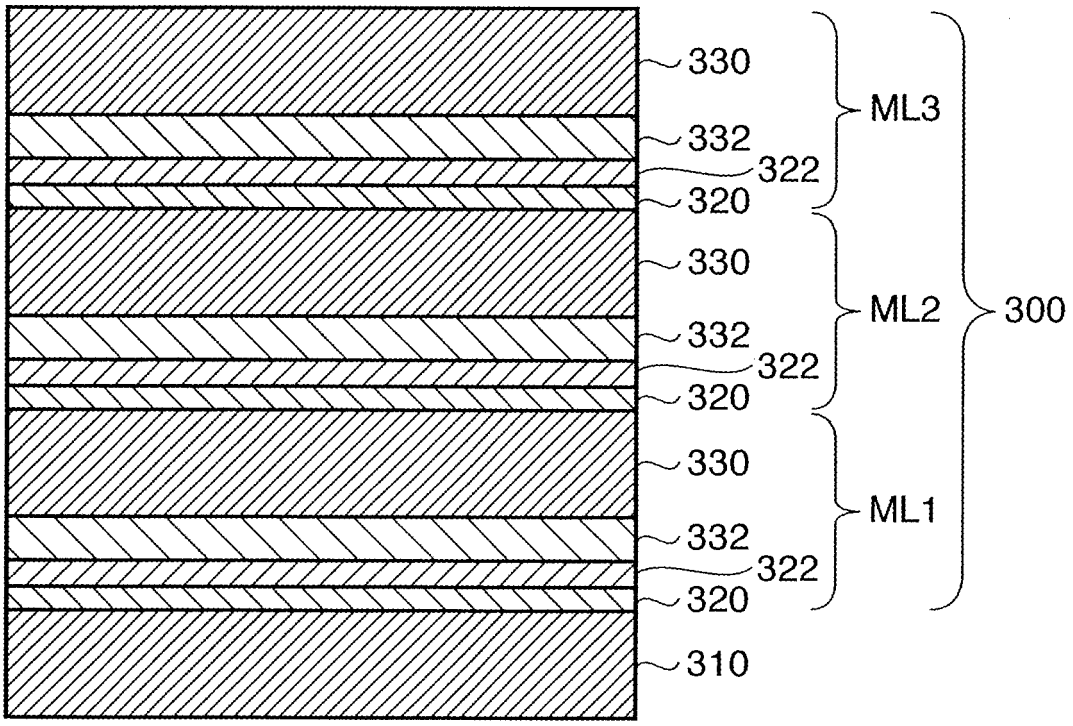
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FIG. 14

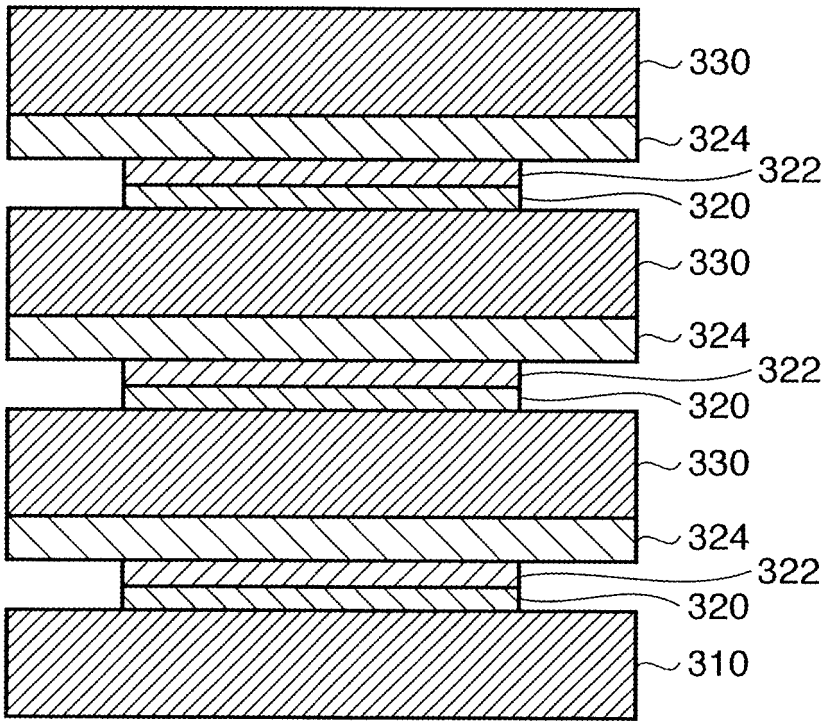
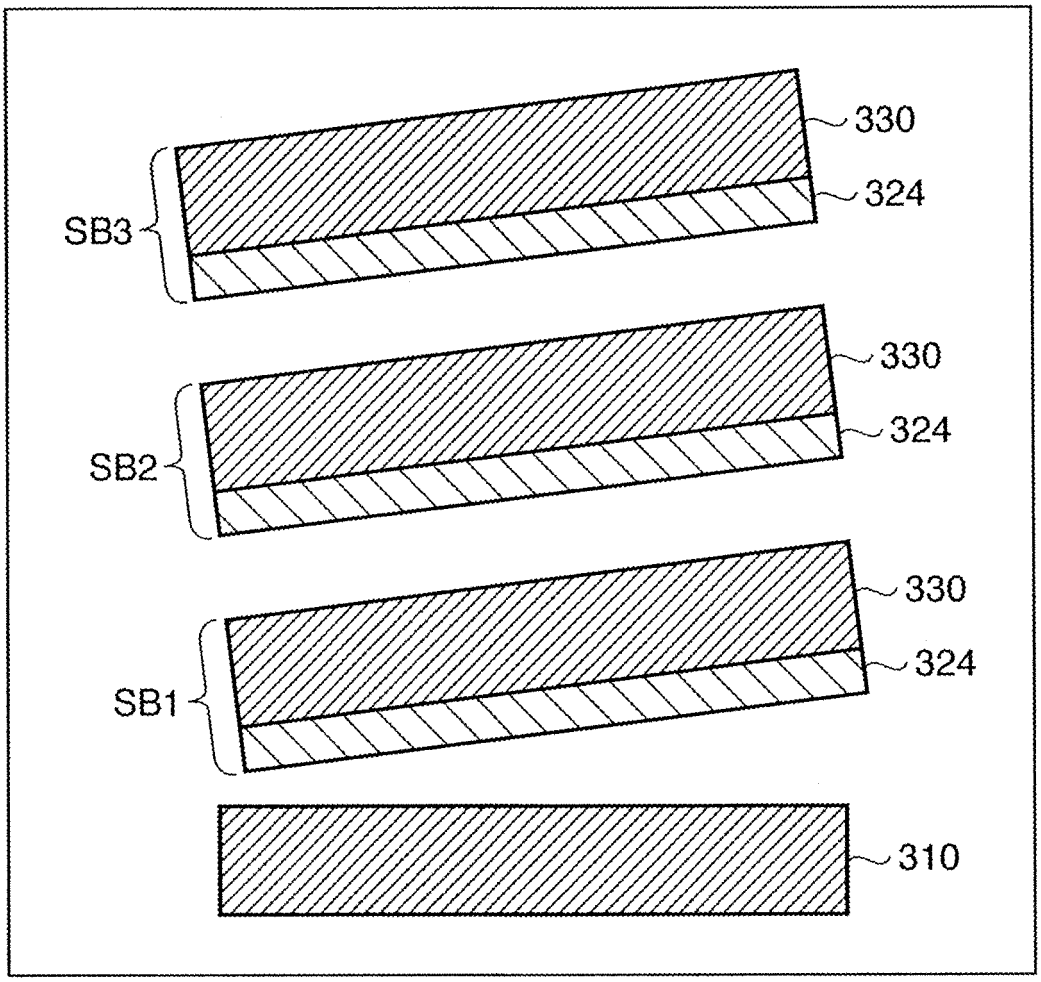


FIG. 15



INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP2006/316635

A. CLASSIFICATION OF SUBJECT MATTER
C30B29/38(2006.01)i, *C23C16/01*(2006.01)i, *C23C16/34*(2006.01)i, *H01L21/205*(2006.01)i, *H01L21/338*(2006.01)i, *H01L29/778*(2006.01)i, *H01L29/812*(2006.01)i, *H01L33/00*(2006.01)i, *H01S5/323*(2006.01)i
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
C30B29/38, C23C16/01, C23C16/34, H01L21/205, H01L21/338, H01L29/778, H01L29/812, H01L33/00, H01S5/323

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Jitsuyo Shinan Koho 1922-1996 Jitsuyo Shinan Toroku Koho 1996-2006
Kokai Jitsuyo Shinan Koho 1971-2006 Toroku Jitsuyo Shinan Koho 1994-2006

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
JST7580(JDream2), JSTPlus(JDream2), G-Search

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X Y	JP 2005-001928 A (Fujikura Ltd.), 06 January, 2005 (06.01.05), Full text; Fig. 3 (Family: none)	1-7 8-13
Y	NIKKAN KOGYO SHINBUN, 07 April, 2005 (07.04.05), page 24, 'Tohokudai Chikka Galium Template Kiban Kagaku Etching de Anka ni'	8
Y	Kyokugen Ri et al., "MBE-ho ni yoru Teion CrxN Buffer-so o Mochiita GaN no Seicho", Dai 51 Kai Oyo Butsurigaku Kankei Rengo Koenkai Koen Yokoshu, 28 March, 2004 (28.03.04), No.1, page 364, middle part, 28p-YK-5	8,9

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Date of the actual completion of the international search	Date of mailing of the international search report
20 September, 2006 (20.09.06)	03 October, 2006 (03.10.06)
Name and mailing address of the ISA/ Japanese Patent Office Facsimile No.	Authorized officer Telephone No.

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INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP2006/316635

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	JP 04-297023 A (Nichia Chemical Industries, Ltd.), 21 October, 1992 (21.10.92), Claims & EP 0497350 A1 & US 5290393 A	10-13
A	JP 2000-049092 A (Matsushita Electronics Corp.), 18 February, 2000 (18.02.00), Claims & US 6218207 B1	8,9
A	JP 2002-316898 A (Hitachi Cable, Ltd.), 31 October, 2002 (31.10.02), Claims (Family: none)	1-8

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REFERENCES CITED IN THE DESCRIPTION

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Patent documents cited in the description

- JP 2004039810 A **[0007]**