



(11) **EP 1 933 221 B1**

(12) **EUROPEAN PATENT SPECIFICATION**

(45) Date of publication and mention
of the grant of the patent:
21.03.2012 Bulletin 2012/12

(51) Int Cl.:
G05F 1/56 (2006.01)

(21) Application number: **06025990.0**

(22) Date of filing: **14.12.2006**

(54) **Voltage regulator with an improved transient response**

Spannungsregler mit verbessertem transientem Ansprechverhalten

Régulateur de tension avec réponse transitoire améliorée

(84) Designated Contracting States:
DE FR GB IT

(43) Date of publication of application:
18.06.2008 Bulletin 2008/25

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- **GABRIEL A RINCON-MORA ET AL: "A Low-Voltage, Low Quiescent Current, Low Drop-Out Regulator" IEEE JOURNAL OF SOLID-STATE CIRCUITS, IEEE SERVICE CENTER, PISCATAWAY, NJ, US, vol. 33, no. 1, January 1998 (1998-01), XP011060653 ISSN: 0018-9200**

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Description

[0001] The present invention relates to voltage regulators, especially to voltage regulators having a low voltage drop, a low current consumption and a fast transient response.

[0002] A low voltage drop over the voltage regulator is achieved by the use of a MOSFET as a voltage regulating element together with a charge pump providing a sufficiently high gate potential which has to be higher than the output voltage of the voltage regulator, in the case of a low drop regulator even higher than the input voltage of the voltage regulator.

[0003] In order to guarantee a substantially constant output voltage, the gate of the voltage regulating MOSFET (e.g. a power MOSFET) is supplied with a bias current provided by a charge pump and controlled by a closed loop control system. That is, the output voltage of the voltage regulator is received by a controller which controls the gate current (and therefore the gate voltage) of the voltage regulating MOSFET such, that the output voltage of the voltage regulator remains substantially constant.

[0004] In response to an upward step of the load current (i.e. the output current) the output voltage will slightly drop due to the higher voltage drop over the voltage regulating MOSFET. Triggered by this voltage drop the controller will increase the gate current for charging the gate-source-capacitance of the voltage regulating MOSFET in order to increase the conductivity of the voltage regulating MOSFET thus re-adjusting the output voltage to its desired value.

[0005] The time which is needed to compensate for the disturbance in the output voltage induced by the step in a load current is determined by the loop bandwidth of the closed loop control system and especially dependent on the value of the gate-source-capacitance of the voltage regulating MOSFET.

[0006] With a given value of the gate-source-capacitance of the voltage regulating MOSFET the speed of the closed loop control system can only be increased by increasing the gate current which charges the gate of the MOSFET. This gate current is supplied by a charge pump, as explained before, and, in order to minimize power consumption, an increase of the maximum gate current which would entail a more costly charge pump is not desirable.

[0007] The US patent application publication number US 2004/0239304 describes a low dropout voltage regulator having a pass transistor coupled between a power source and the load, the pass transistor having a gate, a drain, a source and a back-gate which is bias with respect to the source of the pass transistor. The bias-voltage for the back-gate is substantially a fractional part of the forward voltage of a diode.

[0008] It is an object of the current invention to provide an improved voltage regulator which is able to compensate for disturbances in its output voltage induced by

changes in the load current very quickly.

[0009] This object is achieved by the voltage regulator of claim 1 and by the method for controlling a field effect transistor of claim 8. Several embodiments and enhancements of the invention are covered by the dependent claims.

[0010] A voltage regulator comprises a power field effect transistor having a threshold voltage, a drain terminal receiving an input voltage, a source terminal providing an output voltage and a load current, a gate terminal responsive to a control signal, and a bulk terminal. The voltage regulator further comprises a control loop circuit responsive to the output voltage and providing the control signal. The control loop circuit is adapted for adjusting said control signal to such a value that the output voltage is regulated to a desired (constant) value. Additionally the threshold voltage of the power field effect transistor is modified dependent on the load current. Alternatively the threshold voltage can be modified dependent on the output voltage or on both, the output voltage and the load current.

[0011] In one embodiment of the invention the voltage regulator additionally comprises a switching circuit for modifying the threshold voltage. The switching circuit is responsive to the output voltage and/or to the load current and it is adapted for connecting the bulk terminal of the field effect transistor with either the source terminal or a constant potential dependent on the load currents and/or the output voltage.

[0012] The invention also comprises a method for controlling the power field effect transistor which was defined above. In one embodiment the method comprises the step of modifying the threshold voltage dependent on the load current and/or the output voltage. This can be done, for example, by a connecting the bulk terminal of the field effect transistor with either the source terminal or a constant potential dependent on the load current and/or the output voltage.

[0013] The following discussion explains the invention in more detail based on the figures.

Figure 1 shows a conventional voltage regulator with a power MOSFET as a regulating element and a feedback circuit for regulating the output voltage to a desired constant value.

Figure 2 shows one embodiment of the inventive voltage regulator comprising a switching circuit for modifying the threshold voltage of the voltage regulating power MOSFET.

Figure 3 shows the embodiment of figure 2 with the switching circuit being illustrated in more detail.

Figure 4 shows timing diagrams of the load current, the output voltage and the gate voltage illustrating the step response of a voltage reg-

ulator according to figure 1.

Figure 5 shows timing diagrams of the load current, the output voltage, the gate voltage and the bulk voltage illustrating the step response of an inventive voltage regulator according to figure 2 or 3.

[0014] In the figures, unless otherwise indicated, the same reference notations refer to the same components or the same signals with the same meaning.

[0015] Figure 1 shows a simple voltage regulator using a power MOSFET Mp as a voltage regulating element. In the embodiment shown in figure 1 a n-MOS transistor is used whose drain terminal D is connected to a first supply terminal receiving an input voltage Vin and whose source terminal S is connected to an output terminal providing an output voltage Vout and a load current Iload. For compensating for high frequency current spikes a capacitance Cout is connected between the source terminal S and a second supply terminal, e.g. a ground terminal GND. The voltage regulator further comprises a feedback circuit 10 for regulating the output voltage Vout, i.e. the source potential of the power MOSFET, to a desired (e.g. constant) value.

[0016] The feedback circuit 10 comprises a controller 13 whose input is connected to the source terminal S and responsive to the output voltage Vout. The output of the controller 13 provides a controller voltage Vc received by the gate of a controlling transistor 12 whose source terminal is connected to the ground terminal GND and whose drain terminal is connected to the gate G of the voltage regulating power MOSFET Mp and to a current source 11 providing a bias current Ibias to the gate G and to the controlling transistor 12. The current source 11 is connected to a third supply terminal receiving a supply voltage Vcp provided by a charge pump (not shown).

[0017] The function of the feedback circuit can be easily understood with the help of the timing diagrams shown in figure 4. Figure 4 illustrates the step response of the output voltage Vout, the controller voltage Vc, and the gate voltage Vg to an upward step of the load current Iload. In the circuit of figure 1 with a given output voltage Vout, a given load current Iload, and a given supply voltage Vin the drain-source voltage Vds of the power MOSFET Mp has been adjusted by the feedback circuit 10 such, that drain-source voltage Vds (i.e. the product $R_{DS} \times I_{load}$ of the drain-source resistance RDS and the load current Iload) is equal to the difference between the supply voltage Vin and the output voltage Vout. An upward step of the load current Iload firstly results in a drop of the output voltage Vout. Triggered by this voltage drop the controller 13 reduces the controller voltage Vc, i.e. the gate voltage of the controlling transistor 12, thus increasing the fractional part of the bias current Ibias used for charging the gate (i.e. the gate-source-capacitance) of the power MOSFET Mp. An increased gate charge

results in a higher gate voltage Vg of the power MOSFET and in a lower drain-source voltage Vds (i.e. in a lower drain-source resistance RDS) which compensates for the higher load current Iload, thus readjusting the output voltage to its desired (constant) value.

[0018] The time which is needed to readjust the drop in the output voltage Vout to its desired constant value depends on the time the feedback circuit 10 needs to react to a drop in the output voltage, i.e. the loop delay time tL, the time which is needed to charge the gate-source capacitance of the power MOSFET Mp, i.e. the charging time tC. The loop delay time tL depends on the bandwidth of the feedback circuit 10 and is usually much smaller than the charging time tC. To decrease the overall delay time tD ($tD = tL + tC$) it is necessary to reduce the charging time tC, which could be done by increasing the bias current Ibias which would entail higher costs for the current source 11 and the charge pump.

[0019] Another possibility to improve the overall delay tD time without the need for increasing the bias current Ibias is shown in figure 2. compared to the circuit of figure 1 a current measurement means 30 is connected in series to the drain-source path of the power MOSFET Mp. In the case of figure 2 the current measurement means is connected between the drain terminal D of the power MOSFET Mp and the supply terminal receiving Vin. The current measurement means 30 provides a measurement signal S30 which depends on the load current Iload. The voltage regulator further comprises a switching circuit 20 being responsive to the load current Iload (or, strictly speaking, to the measurement signal S30). The switching circuit 20 is connected to the output terminal providing the output voltage Vout (i.e. the source potential) and with the bulk terminal B of the power MOSFET Mp. The switching circuit comprises a switch SW responsive to the measurement signal S30. The switch SW is adapted for connecting the bulk terminal B of the power MOSFET Mp with either the source terminal S or a constant potential V2 dependent on the value of the load current Iload or the measurement signal S30 respectively.

[0020] The constant potential V2 is preferably lower than the output voltage Vout and can also be equal to ground potential GND. An "ordinary" MOSFET would have its bulk terminal B connected to its source terminal S. Compared to this switching state (a first switching state) the threshold voltage of the power MOSFET Mp increases, if the switch SW connects the bulk terminal B of the power MOSFET Mp with the constant potential V2 being lower than the source potential (Vout) of the power MOSFET Mp. This state of the switch SW is further referred to as the second switching state. The function of the circuit is explained in more detail by reference to figures 3 and 5.

[0021] Figure 3 shows the embodiment of figure 2 wherein the measurement means 13 and the switching circuit 20 are illustrated in more detail. The measurement circuit 13 comprises a shunt resistor R, a voltage source

providing the offset voltage V_{os} and a comparator 31. The shunt resistor is connected to the drain terminal D of the power MOSFET Mp with its first terminal in series to the drain-source path of the power MOSFET. A second terminal of the shunt resistor R is connected to a non-inverting input of the comparator 31 and the first terminal of the shunt resistor R is also connected to the inverting input of the comparator 31 via the voltage source providing the offset voltage V_{os} . The output signal of the comparator assumes a first logic level, e.g. a high level, if the load current I_{load} is higher than a reference current defined by the quotient $I_{ref} = V_{os}/R$ of the shunt resistor R and the offset voltage V_{os} . Of course any other method for measuring the load current I_{load} and comparing it with a reference current is applicable (e.g. a sense-FET).

[0022] Additionally to the embodiment shown in figure 2 the switching 20 circuit comprises a comparator 23, an AND-gate 22 with an inverting and a non-inverting input, and transistors M1, M2 provide the functionality of the switch SW. The comparator 23 is adapted for comparing the output voltage V_{out} with a reference voltage V_{ref} and for providing an output signal which assumes a first logic level, e.g. a high level, if the output voltage is higher than the reference voltage. The output of the comparator 23 is connected with the non-inverting input of the AND-gate 22. The inverting input of the AND-gate 22 is connected with the output of the comparator 31 which has been described above. The AND-gate 22 provides a switching signal S22 controlling the switching states of the transistors M1, M2.

[0023] In the current embodiment the switching signal S22 assumes a first logic level, e.g. a high level, if the load current I_{load} is lower than a reference current defined by the quotient V_{os}/R and the output voltage is higher than the reference voltage V_{ref} . Then the first p-MOS transistor M1 is switched to an off-state and the n-MOS transistor M2 is switched to an on-state, thus isolating the bulk terminal B of the power MOSFET Mp from the output terminal providing the output voltage V_{out} (and also from its source terminal S) and connecting the bulk terminal B of the power MOSFET Mp with the constant potential V2 which is - in the current case - equal to the ground potential.

[0024] If either the output voltage drops below the reference voltage V_{ref} or the load current rises above the reference current defined by the quotient V_{os}/R the output logic level of one of the comparators 23, 31 will change and the output signal S22 of the AND-gate 22 will switch to a second logic level, e.g. a low level, thus switching on the p-MOS transistor M1 and switching off the n-MOS transistor M2 and the p-MOS transistor M3. The bulk terminal B of the power MOSFET Mp is then connected to the source terminal S of the power MOSFET Mp and isolated from the constant potential V2.

[0025] Connecting the bulk terminal either with a constant potential V2 or with the source terminal S will change the threshold voltage of the voltage regulating power MOSFET Mp. The effect of this change of the

threshold voltage on the speed of the feedback circuit can easily be explained by the help of figure 5. Figure 5 shows, like figure 4, timing diagrams of the load current I_{load} , the output voltage V_{out} , the control voltage V_c , the gate voltage V_g , and the bulk voltage V_b . The left hand side of the timing diagram of I_{load} shows the load current I_{load} dropping below the reference current $I_{ref} = V_{out}/R$. As a consequence the bulk terminal B is isolated from the source terminal S and connected with a constant potential V2. This results in an increase of the threshold voltage of the power MOSFET Mp and the controller 13 (via the controlling transistor 12) has to adjust the gate voltage V_g to a higher value, i.e. the gate G of the power MOSFET Mp is precharged during the second switching state when the load current I_{load} is below the reference current and the output voltage V_{out} is above the reference voltage V_{ref} . In response to an upward step in the load current I_{ref} a drop in the output voltage V_{out} will be observed. Due to the rise of the load current I_{load} the bulk terminal B of the power MOSFET Mp will again be connected with the source terminal S and therefore the threshold voltage of the power MOSFET Mp is decreased again. Due to the fact, that the gate G of the power MOSFET Mp was precharged before, less charge is necessary to increase the gate voltage to a value necessary for compensating for the increase load current. As a consequence the feedback circuit 10 can react much faster for regulating the output voltage V_{out} to its desired constant value and the charging time t_C is greatly reduced, thus improving the overall performance of the voltage regulator.

Claims

1. A voltage regulator comprising

- a power field effect transistor (Mp) having a threshold voltage (V_{th}), a drain terminal receiving an input voltage (V_{in}), a source terminal providing an output voltage (V_{out}) and a load current (I_{load}), a gate terminal responsive to a control signal (V_g), and a bulk terminal,
- a control-loop circuit (10) responsive to said output voltage (V_{out}) and providing said control signal (V_g), said control circuit being adapted for adjusting said control (V_g) signal to such a value that said output voltage (V_{out}) is regulated to a constant value, and
- a switching circuit (20) responsive to said output voltage (V_{out}) and/or to said load current (I_{load}), said switching circuit being adapted for connecting said bulk terminal (B) either with said source terminal (S) or with a constant potential (V2) lower than a source potential (V_{out}) of the transistor dependent on said load current and/or said output voltage (V_{out}), such that said threshold voltage (V_{th}) of said power field effect tran-

sistor (Mp) is modified dependent on said load current (Iload) and/or said output voltage (Vout).

2. The voltage regulator of claim 1, wherein said switching circuit (20) is adapted for

- connecting said bulk terminal (B) with said source terminal (S), if said load current (Iload) is higher than a reference current, and for
- connecting said bulk terminal (B) with said constant potential (V2), if said load current (Iload) is lower than said reference current.

3. The voltage regulator of claim 1, wherein said switching circuit (20) is adapted for

- connecting said bulk terminal (B) with said source terminal (S), if said output voltage is lower than a reference voltage, and for
- connecting said bulk terminal (B) with said constant potential (V2), if said output voltage is higher than said reference voltage.

4. The voltage regulator of claim 1, wherein said switching circuit (20) is adapted for

- connecting said bulk terminal (B) with said source terminal (S), if said load current (Iload) is higher than a reference current and said output voltage is lower than a reference voltage, and for
- connecting said bulk terminal (B) with said constant potential (V2), if said load current (Iload) is lower than said reference current and said output voltage is higher than said reference voltage.

5. The voltage regulator of claim 1, 2, 3, or 4, wherein said constant potential (V2) is equal to a ground potential (GND).

6. A method for controlling a power field effect transistor (Mp) having a threshold voltage (Vth), a drain terminal receiving an input voltage (Vin), a source terminal providing an output voltage (Vout) and a load current (Iload), a gate terminal responsive to a control signal (Vg), and a bulk terminal; said method for regulating the output voltage to a desired constant value comprising:

- modifying said threshold voltage dependent on said load current (Iload) and/or said output voltage (Vout), by connecting said bulk terminal either with said source terminal or with a constant potential (V2) lower than a source potential (Vout) of the transistor (Mp) dependent on said load current (Iload) and/or said output voltage (Vout).

7. The method of claim 6 further comprising:

- comparing said load current (Iload) with a reference current,
- connecting said bulk terminal with said source terminal, if said load current (Iload) is higher than said reference current, or connecting said bulk terminal with a constant potential (V2), if said load current (Iload) is lower than said reference current.

8. The method of claim 6 further comprising:

- comparing said output voltage (Vout) with a reference voltage,
- connecting said bulk terminal with said source terminal, if said output voltage (Vout) is lower than said reference voltage, or connecting said bulk terminal with a constant potential (V2), if said output voltage (Vout) is higher than said reference voltage.

9. The method of claim 6 further comprising:

- comparing said load current (Iload) with a reference current,
- comparing said output voltage (Vout) with a reference voltage,
- connecting said bulk terminal with said source terminal, if said load current (Iload) is higher than said reference current and said output voltage (Vout) is lower than said reference voltage, or connecting said bulk terminal with a constant potential (V2), if said load current (Iload) is lower than said reference current and if said output voltage (Vout) is higher than said reference voltage.

40 Patentansprüche

1. Spannungsregler, der Folgendes umfasst:

- einen Leistungsfeldeffekttransistor (Mp) mit einer Schwellwertspannung (Vth), einen Drainanschluss, der eine Eingangsspannung (Vin) erhält, einen Sourceanschluss, der eine Ausgangsspannung (Vout) und einen Laststrom (Iload) liefert, einen Gateanschluss, der auf ein Steuersignal (Vg) reagiert, und einen Bulk-Anschluss,
- eine Steuerschleifenschaltung (10), die auf die Ausgangsspannung (Vout) reagiert und das Steuersignal (Vg) liefert, wobei die Steuerschaltung ausgelegt ist zum Einstellen des Steuersignals (Vg) auf einen derartigen Wert, dass die Ausgangsspannung (Vout) auf einen konstanten Wert geregelt wird, und

- einen Schaltkreis (20), der auf die Ausgangsspannung (Vout) und/oder auf den Laststrom (Iload) reagiert, wobei der Schaltkreis ausgelegt ist zum Verbinden des Bulk-Anschlusses (B) entweder mit dem Sourceanschluss (S) oder mit einem konstanten Potential (V2) unter einem Sourcepotential (Vout) des Transistors abhängig von dem Laststrom und/oder der Ausgangsspannung (Vout), so dass die Schwellwertspannung (Vth) des Leistungsfeldeffekttransistors (Mp) in Abhängigkeit von dem Laststrom (Iload) und/oder der Ausgangsspannung (Vout) modifiziert wird. 5 10
2. Spannungsregler nach Anspruch 1, wobei der Schaltkreis (20) ausgelegt ist zum 15
- Verbinden des Bulk-Anschlusses (B) mit dem Sourceanschluss (S), falls der Laststrom (Iload) höher ist als ein Referenzstrom, und zum 20
- Verbinden des Bulk-Anschlusses (B) mit dem konstanten Potential (V2), falls der Laststrom (Iload) niedriger ist als der Referenzstrom.
3. Spannungsregler nach Anspruch 1, wobei der Schaltkreis (20) ausgelegt ist zum 25
- Verbinden des Bulk-Anschlusses (B) mit dem Sourceanschluss (S), falls die Ausgangsspannung niedriger ist als ein Referenzstrom, und zum 30
- Verbinden des Bulk-Anschlusses (B) mit dem konstanten Potential (V2), falls die Ausgangsspannung (Iload) höher ist als der Referenzstrom. 35
4. Spannungsregler nach Anspruch 1, wobei der Schaltkreis (20) ausgelegt ist zum
- Verbinden des Bulk-Anschlusses (B) mit dem Sourceanschluss (S), falls der Laststrom (Iload) höher ist als ein Referenzstrom und die Ausgangsspannung niedriger ist als eine Referenzspannung, und zum 40
- Verbinden des Bulk-Anschlusses (B) mit dem konstanten Potential (V2), falls der Laststrom (Iload) niedriger ist als der Referenzstrom und die Ausgangsspannung höher ist als die Referenzspannung. 45 50
5. Spannungsregler nach Anspruch 1, 2, 3 oder 4, wobei das konstante Potential (V2) gleich einem Massepotential (GND) ist.
6. Verfahren zum Steuern eines Leistungsfeldeffekttransistors (Mp) mit einer Schwellwertspannung (Vth), einem Drainanschluss, der eine Eingangsspannung (Vin) erhält, einem Sourceanschluss, der eine Ausgangsspannung (Vout) und einen Laststrom (Iload) liefert, einem Gateanschluss, der auf ein Steuersignal (Vg) reagiert, und einem Bulk-Anschluss; wobei das Verfahren zum Regeln der Ausgangsspannung auf einen gewünschten Konstantwert Folgendes umfasst:
- Modifizieren der Schwellwertspannung in Abhängigkeit von dem Laststrom (Iload) und/oder der Ausgangsspannung (Vout) durch Verbinden des Bulk-Anschlusses entweder mit dem Sourceanschluss oder mit einem konstanten Potential (V2) unter einem Sourcepotential (Vout) des Transistors (Mp) in Abhängigkeit von dem Laststrom (Iload) und/oder der Ausgangsspannung (Vout).
7. Verfahren nach Anspruch 6, das weiterhin Folgendes umfasst:
- Vergleichen des Laststroms (Iload) mit einem Referenzstrom;
- Verbinden des Bulk-Anschlusses mit dem Sourceanschluss, falls der Laststrom (Iload) höher ist als der Referenzstrom, oder Verbinden des Bulk-Anschlusses mit einem konstanten Potential (V2), falls der Laststrom (Iload) niedriger ist als der Referenzstrom.
8. Verfahren nach Anspruch 6, das weiterhin Folgendes umfasst:
- Vergleichen der Ausgangsspannung (Vout) mit einer Referenzspannung,
- Verbinden des Bulk-Anschlusses mit dem Sourceanschluss, falls die Ausgangsspannung (Vout) niedriger ist als die Referenzspannung, oder Verbinden des Bulk-Anschlusses mit einem konstanten Potential (V2), falls die Ausgangsspannung (Vout) höher ist als die Referenzspannung.
9. Verfahren nach Anspruch 6, das weiterhin Folgendes umfasst:
- Vergleichen des Laststroms (Iload) mit einem Referenzstrom,
- Vergleichen der Ausgangsspannung (Vout) mit einer Referenzspannung,
- Verbinden des Bulk-Anschlusses mit dem Sourceanschluss, falls der Laststrom (Iload) höher ist als der Referenzstrom und die Ausgangsspannung (Vout) niedriger ist als die Referenzspannung, oder Verbinden des Bulk-Anschlusses mit einem konstanten Potential (V2), falls der Laststrom (Iload) niedriger ist als der Referenzstrom und falls die Ausgangsspannung (Vout) höher ist als die Referenzspannung.

Revendications

1. Régulateur de tension comprenant

- un transistor (Mp) de puissance à effet de champ ayant une tension (V_{th}) de seuil, une borne de drain recevant une tension (V_{in}) d'entrée, une borne de source procurant une tension (V_{out}) de sortie et un courant (I_{load}) de charge, une borne de grille sensible à un signal (V_g) de commande et une borne de gâchette en bloc, 5
- un circuit (10) de boucle de commande sensible à la tension (V_{out}) de sortie et procurant le signal (V_g) de commande, le circuit de commande étant conçu pour ajuster le signal de commande (V_g) à une valeur telle que la tension (V_{out}) de sortie soit régulée à une valeur constante, et 10
- un circuit (20) de commutation sensible à la tension (V_{out}) de sortie et/ou au courant (I_{load}) de charge, le circuit de commutation étant conçu pour relier la borne (B) de gâchette en bloc soit à la borne (S) de source, soit à un potentiel (V_2) constant inférieur à un potentiel (V_{out}) de source du transistor, en fonction du courant de charge et/ou de la tension (V_{out}) de sortie de manière à ce que la tension (V_{th}) de seuil du transistor (Mp) de puissance à effet de champ soit modifié en fonction du courant (I_{load}) de charge et/ou de la tension (V_{out}) de sortie. 20 25 30

2. Régulateur de tension suivant la revendication 1, dans lequel le circuit (20) de commutation est conçu pour 35

- relier la borne (B) de gâchette en bloc à la borne (S) de source si le courant (I_{load}) de charge est plus grand qu'un courant de référence, et pour
- relier la borne (B) de gâchette en bloc au potentiel (V_2) constant si le courant (I_{load}) de charge est plus petit que le courant de référence. 40

3. Régulateur de tension suivant la revendication 1, dans lequel le circuit (20) de commutation étant conçu pour 45

- relier la borne (B) de gâchette en bloc à la borne (S) de source si la tension de source est plus basse qu'une tension de référence, et pour
- relier la borne (B) de gâchette en bloc au potentiel (V_2) constant si la tension de sortie est plus haute que la tension de référence. 50

4. Régulateur de tension suivant la revendication 1, dans lequel le circuit (20) de commutation est conçu pour 55

- relier la borne (B) de gâchette en bloc à la borne

(S) de source si le courant (I_{load}) de charge est plus grand qu'un courant de référence et si la tension de sortie est plus basse qu'une tension de référence, et pour

- relier la borne (B) de gâchette en bloc au potentiel (V_2) constant si le courant (I_{load}) de charge est plus petit que le courant de référence et si la tension de sortie est plus haute que la tension de référence.

5. Régulateur de tension suivant la revendication 1, 2, 3 ou 4 dans lequel le potentiel (V_2) constant est égal à un potentiel (GND) de terre.

6. Procédé de commande d'un transistor (Mp) de puissance à effet de champ ayant une tension (V_{th}) de seuil, un transistor (Mp) de puissance à effet de champ ayant une tension (V_{th}) de seuil, une borne de drain recevant une tension (V_{in}) d'entrée, une borne de source procurant une tension (V_{out}) de sortie et un courant (I_{load}) de charge, une borne de grille sensible à un signal (V_g) de commande et une borne de gâchette en bloc ; le procédé de régulation de la tension de sortie à une valeur constante souhaitée comprenant : 25

- on modifie la tension de seuil en fonction du courant (I_{load}) de charge et/ou de la tension (V_{out}) de sortie en reliant la borne de gâchette en bloc soit à la borne de source soit à un potentiel (V_2) constant plus bas qu'un potentiel (V_{out}) de source du transistor (Mp) en fonction du courant (I_{load}) de charge et/ou de la tension (V_{out}) de sortie. 30

7. Procédé suivant la revendication 6, dans lequel en outre :

- on compare le courant (I_{load}) de charge à un courant de référence,
- on relie la borne de gâchette en bloc à la borne de source si le courant (I_{load}) de charge est plus grand que le courant de référence ou on relie la borne de gâchette en bloc à un potentiel (V_2) constant si le courant (I_{load}) de charge est plus petit que le courant de référence.

8. Procédé suivant la revendication 6, dans lequel en outre :

- on compare la tension (V_{out}) de sortie à une tension de référence,
- on relie la borne de gâchette en bloc à la borne de source si la tension (V_{out}) de sortie est plus basse que la tension de référence ou on relie la borne de gâchette en bloc à un potentiel (V_2) constant si la tension (V_{out}) de sortie est plus haute que la tension de référence.

9. Procédé suivant la revendication 6, dans lequel en outre :

- on compare le courant (I_{load}) de charge à un courant de référence, 5
- on compare la tension (V_{out}) de sortie à une tension de référence,
- on relie la borne de gâchette en bloc à la borne de source si le courant (I_{load}) de charge est plus grand que le courant de référence et si la tension (V_{out}) de sortie est plus basse que la tension de référence ou on relie la borne de gâchette en bloc à un potentiel (V_2) constant, si le courant (I_{load}) de charge est plus petit que le courant de référence et si la tension (V_{out}) de sortie est plus haute que la tension de référence. 10 15

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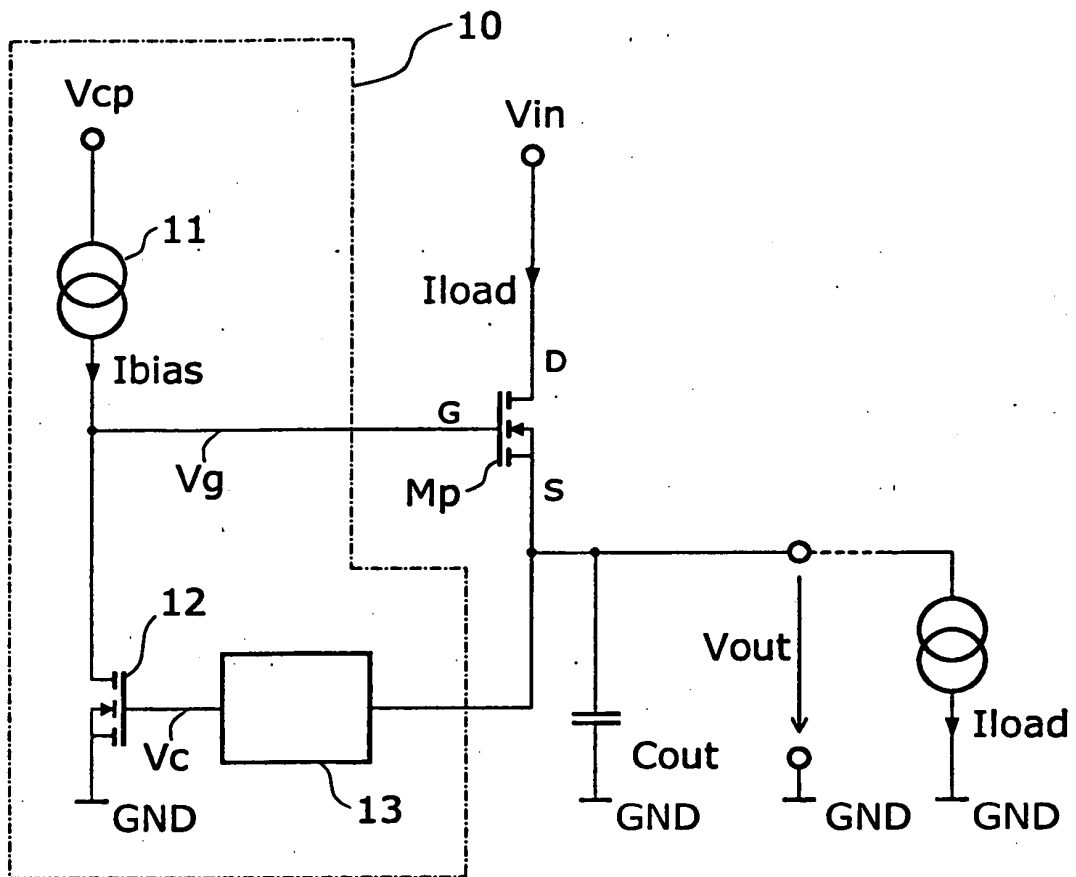


Fig. 1

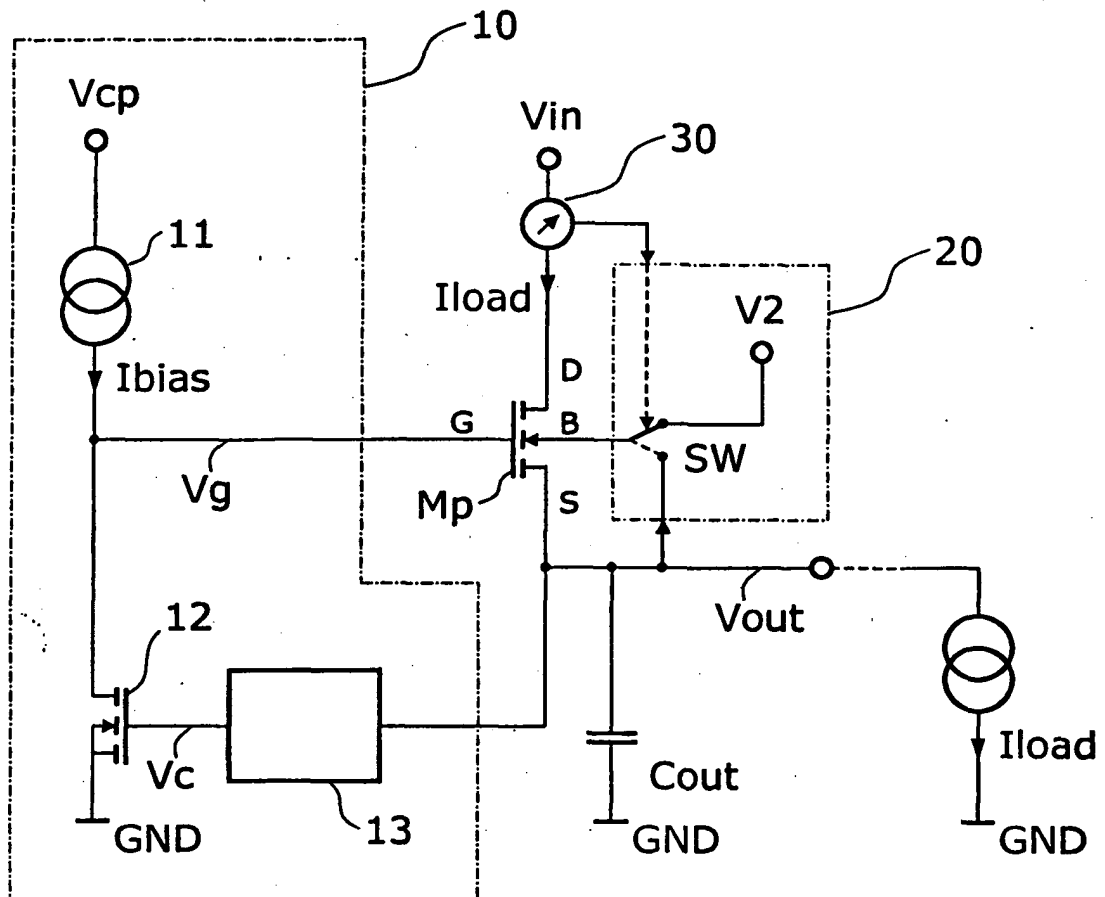


Fig. 2

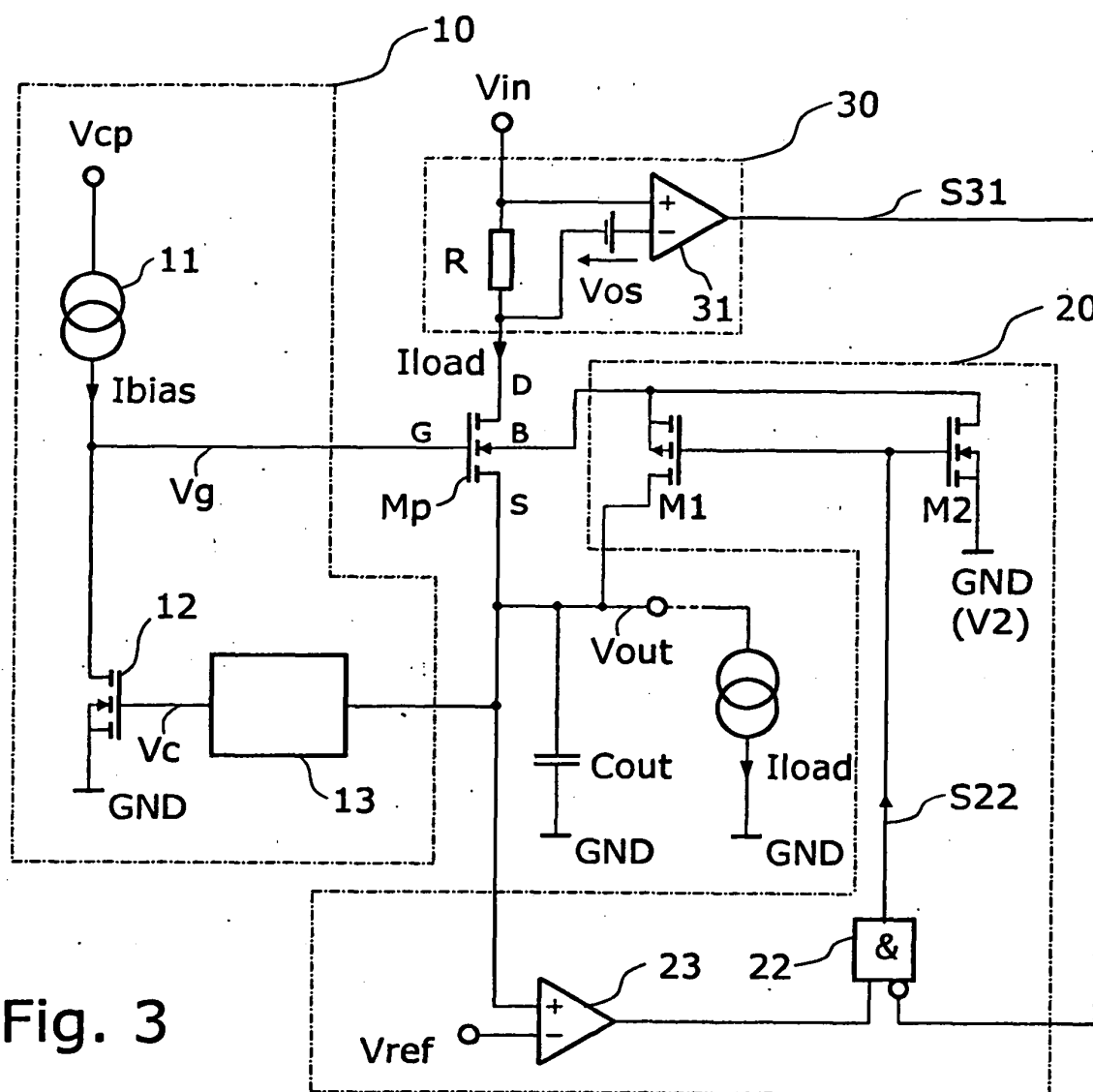


Fig. 3

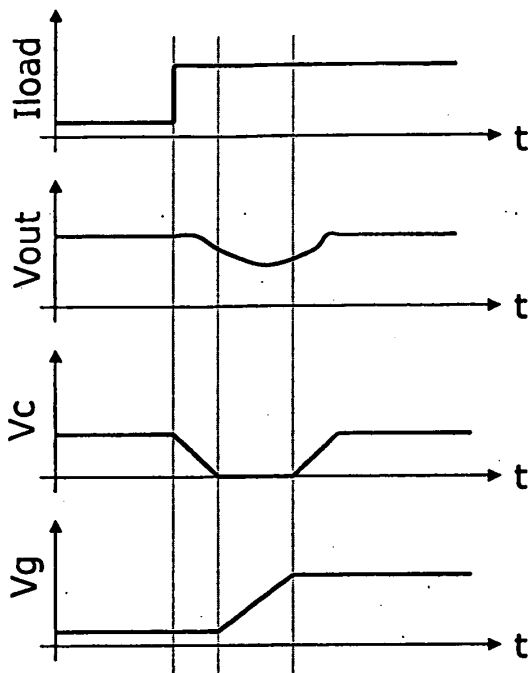


Fig. 4

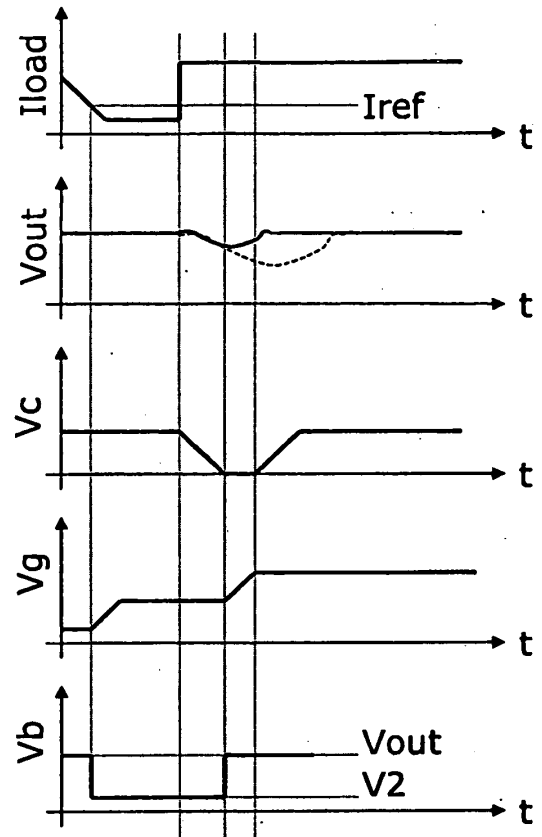


Fig. 5

REFERENCES CITED IN THE DESCRIPTION

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Patent documents cited in the description

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