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(54) Circuit structure of high performance time-to-digital converter

(57) The invention discloses a circuit structure of a high performance time-to-digital converter including a delay link loop generating low bit data, a counter generating high bit data and a compensated control source The delay link loop counts low bits and sends a thus-generated signal in a specific cycle to the counter. The counter accumulates a period of the signal in the specific cycle as high bits of the time-to-digital converter. The compensated control source compensates and controls a voltage signal of the delay link loop. The invention has the following advantages: a high measurement precision; a fast processing speed; the connection of the outputs of the latches with the high bit counter can ensure correctness of cycle and carry; the introduction of the compensated control source can ensure consistency of the system; and no high requirement is exerted on the components, and hence the circuit structure is easy to implement.

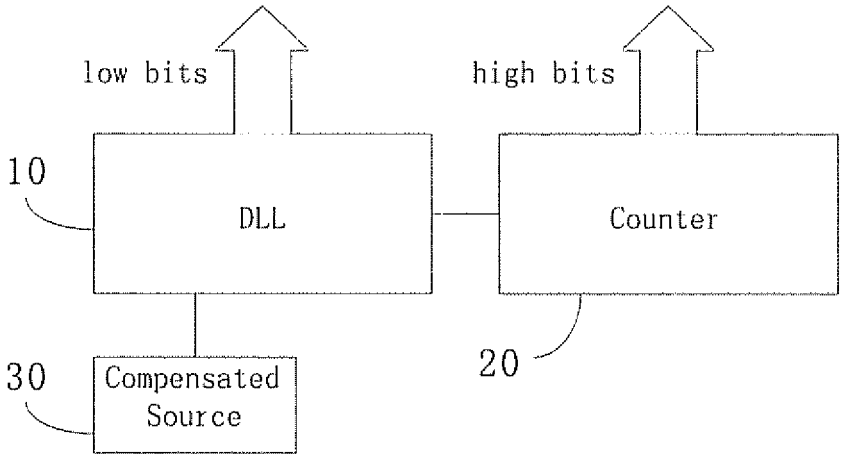

Fig. 1

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Description

Field of the Invention

[0001] The present invention relates to a circuit structure and in particular to a circuit structure of a high performance time-to-digital converter for converting a time interval into a digital signal.

Background of the Invention

[0002] A Time-to-Digital converter (TDC) refers to a timer for converting a time interval into a digital signal.

[0003] A basic time-to-digital converter uses a counter to count a series of digital pulses within a time range to be tested. Although stable high speed pulses can be realized by an existing oscillator counting method, the resultant power consumption and noise may be unacceptable. An actually effective method is to measure a large time at a relatively low measuring frequency and to perform a special process on the time remainder shorter than one cycle of the measured period for the purpose of precise measurement.

[0004] For this precise measurement in need of the special process, several commonly used measuring methods are as follows.

[0005] A capacitor voltage method: within the range of a part to be tested, a capacitor is charged with a current and then is discharged after it becomes fully charged. The time user for one charge and discharge is referred to as one cycle. During a period shorter than one cycle, the voltage of the capacitor varies with the charging time, and the magnitude of the voltage is converted into a digital magnitude using an Analog-to-Digital converter (ADC), thereby realizing precise measurement for the period shorter than one cycle. This method may be disadvantageous in that a high precision Analog-to-Digital ADC converter is required and a design thereof has to take a series of complex factors into account; it is difficult to guarantee linearity of the capacitor voltage; and the charging current is liable to interference from external conditions.

[0006] A time extension method: it is analogous to the above method except that at the end of the period to be tested, the capacitor is discharged with a rated current far smaller than the charging current until the voltage of the capacitor drops to a voltage at initial charging; and during discharging, this much multiplied period is measured using a timer. Although this method is superior greatly to the previous one, the charging current has to be larger than the discharging current by a plurality of times for the purpose of a high precision, and thus the discharging current have to be very small and the charging current has to be large in order to attain a sufficiently large ratio of charging current to discharging current An excessively small discharging current is liable to interference and it is infeasible to realize an excessively large charging current. Further, an additional period dedicated for processing is required for discharging the capacitor slowly at the end of the measured period, thus failing to implement continuous time-to-digital conversion.

[0007] A vernier caliper method: the basic principle is that three sets of pulse waveforms, i.e. a set of reference pulses and two sets of trigger pulses, are generated, where the two sets of trigger pulses each have a cycle identical to that of the other but slightly different from that of the set of reference pulses, and the three sets of pulses are counted respectively by three counters; at the start of start pulses, the start counter counts the start pulses and stops counting when the start pulses overlap with the reference pulses; likewise, the end counter counts end pulses until they overlap with the reference pulses; and the reference counter counts the reference pulses between the start pulses and the start of the end pulses. This method has a resolution determined by the difference between the cycles of the two kinds of pulses. It is disadvantageous in that a phase discriminator with a high discrimination of phase difference is required; and an additional period is required for awaiting the overlap of the terminal pulses with the reference pulses at the end of the measured period, thus failing to implement continuous time-to-digital conversion.

Summary of the Invention

[0008] Embodiments of the invention provide a circuit structure of a high performance time-to-digital converter which employs a fully digital method, uses a CMOS gate level delay as a minimum measurement unit, and can achieve a high measurement precision.

[0009] The embodiments of the invention provide the following technical solutions.

[0010] A circuit structure of a high performance time-to-digital converter includes a delay link loop configured to generate low bit data, a counter configured to generate high bit data and a compensated control source. The delay link loop counts low bits and sends a thus-generated signal in a specific cycle to the counter. The counter accumulates a period of the signal in the specific cycle as high bits of the time-to-digital converter. The compensated control source compensates and controls a voltage signal of the delay link loop.

[0011] The delay link loop includes a delay unit loop, comparators, latches, a coder and an initialization unit. A start signal STA turns on the delay unit loop via the initialization unit. A signal output from the delay unit loop is converted into a digital signal via the comparators. The digital signal is output via the latches and is particularly output via the last

latch as a carry signal. An end signal END enables the latches to latch data at this time and to send the latched data to the coder The coder converts and outputs the data as low bits of the time-to-digital converter.

[0012] The delay unit loop includes a plurality of connected full differential buffers The last buffer is connected with the first buffer in antiphase, and each of the remaining buffers is connected with the next buffer in phase.

[0013] Each of the buffers includes a P channel field effect transistor, a signal switch EN and MOS transistors MP1, MP2, MN1, MN2, MN3 and MN4. Sources of the MOS transistors MN1, MN2, MN3 and MN4 are connected with each other and then are grounded. Gates of the MOS transistors MN and MN3 are connected with each other and then are connected sequentially with drains of the MOS transistors MN2 and MN3 and an output terminal OUT-. Gates of the MOS transistors MN2 and MN4 are connected with each other and then are connected sequentially with drains of the MOS transistors MN4 and MN1 and an output terminal OUT+. The P channel field effect transistor has a source connected with a supply voltage VDD, a gate connected with a voltage signal V_{BP} of the compensated control source and a drain connected via the signal switch EN with sources of the MOS transistors MP1 and MP2 respectively. Drains of the MOS transistors MP1 and MP2 are connected respectively with the output terminals OUT- and OUT+. Gates of the MOS transistors MP1 and MP2 are connected respectively with input terminals IN+ and IN-, A full differential structure with a dual-terminal input and a dual-terminal output is thus formed, which controls a transmission delay through a voltage controlled current sour-ce.

[0014] The counter is a traveling wave counter including a plurality of D flip-flops and counts the carry signal from the delay link loop as a high bit output of the time-to-digital converter.

[0015] The compensated control source includes a low drop out regulator LDO, a current source buffer, a PMOS current mirror, an NMOS current mirror, a bias voltage output transistor and a current setting resistor. The low drop out regulator LDO is connected sequentially with the PMOS current mirror, the current source buffer, the NMOS current mirror and the current setting resistor and provides an internal operation voltage AVDD and a series of reference voltages. The current source buffer and the current setting resistor are connected and cooperate with each other to generate an original reference current which is mirrored by the PMOS current mirror and the NMOS current mirror and is output through the bias voltage output transistor as a voltage signal V_{BP}.

[0016] Provided between the PMOS current mirror and the low drop out regulator LDO is a current division PMOS compensated transistor with a gate connected with the low drop out regulator LDO and a drain connected with the PMOS current mirror.

[0017] Provided between the NMOS current mirror and the low drop out regulator LDO is a current division NMOS compensated transistor with a gate connected with the low drop out regulator LDO and a drain connected with the NMOS current mirror.

[0018] A supply voltage of the bias voltage output transistor is connected with a supply voltage VDD.

[0019] The low drop out regulator LDO includes a reference source BANDGAP, an error amplifier, an output transistor and voltage division resistors. The reference source BANDGAP has one terminal connected with a negative input terminal of the error amplifier and the other terminal connected with the current source buffer. A positive input terminal of the error amplifier is connected between the voltage division resistors. An output terminal of the error amplifier is connected with a gate of the output transistor. A drain of the output transistor is connected sequentially with the voltage division resistors for voltage division and output.

[0020] The principle of the embodiments of the invention is as follows.

[0021] The delay link loop counts low bits, and the core part thereof includes n (a positive integer) buffers each with a transmission delay of time Δt. After $2n\Delta t$, the buffers have experienced a status reciprocation within a cycle and resume the status prior to the $2n\Delta t$ where the cycle is $T=2n\Delta t$. The output data of the buffers is latched in the latches. The carry of the low bit counter is output via the data latch of the last buffer to the high bit counter. The high bit counter is incremented by one upon each cycle of operation of the low bit counter, and the latched data of the last buffer is carried. Therefore, it can be ensured that the cycle of the low bit data matches the carry at the moment of stopping measurement

[0022] The counter counts the signals in the cycle of T delivered from the delay link loop in a way that the counter is incremented by one upon each period of T as a high bit of the Time-to-Digital Converter. The period of T is 2n (n is the number of stages in the delay link loop) times the minimum measurement precision Δt. n is chosen appropriately to ensure that the counter can count properly the signals in the cycle of T. The last bit of the high bit counter is an overflow bit. When the counter counts to the last bit and is inversed, it indicates that the counter overflows.

[0023] For the delay link loop implemented with a CMOS circuit, the transmission delay Δt of each buffer varies with a change of external conditions, including a change of temperature change, a change of supply voltage, a process variation during fabrication, etc. Due to the compensated control source, the fluctuation range of Δt can be shortened significantly so that readings of the Time-to-Digital Converter are highly consistent under various conditions.

[0024] The circuit structure of the high performance time-to-digital converter has the following advantages.

[0025] 1. A high measurement precision: the minimum time resolution is one buffer transmission delay.

[0026] 2. A fast processing speed: data is generated in real time at the end of measurement without any additional processing time.

[0027] 3. The connection of the outputs of the latches with the high bit counter can ensure correctness of both cycle and carry.

[0028] 4. The introduction of the compensated control source can ensure consistency of the system despite various variations in temperature, voltage, process, etc.

[0029] 5. No high requirement is exerted on the components of the circuit structure, and therefore the circuit structure is easy to implement.

Brief Description of the Drawings

[0030] The embodiments of the invention will be further described hereinafter with reference to the embodiments thereof and the accompanying drawings in which:

[0031] Fig.1 is a block diagram illustrating the principle of an embodiment of the invention;

[0032] Fig.2 is a circuit principle diagram of a delay link loop according to an embodiment of the invention;

[0033] Fig.3 is a timing waveform diagram of a delay link loop according to an embodiment of the invention;

[0034] Fig.4 is a circuit principle diagram of a buffer according to an embodiment of the invention;

[0035] Fig.5 is a circuit principle diagram of a counter according to an embodiment of the invention;

[0036] Fig.6 is a timing waveform diagram of a counter according to an embodiment of the invention; and

[0037] Fig.7 is a circuit principle diagram of a compensated source circuit according to an embodiment of the invention.

Detailed Description of the Invention

[0038] Referring to Fig,1, the circuit structure of a high performance time-to-digital converter includes a delay link loop 10 configured to generate low bit data, a counter 20 configured to generate high bit data, and a compensated control source 30.

[0039] Referring to Fig.2, the delay link loop 10 includes a delay unit loop 101, a set of comparators 102, a set of latches 10.3, a coder 104 and an initialization unit 105.

[0040] The delay unit loop 101 includes n (a positive integer) buffers each with two positive and negative differential input terminals and two positive and negative differential output terminals. Each buffer is connected with the next buffer via their in-phase terminals, and the last buffer has a positive output terminal connected with the negative input terminal of the first buffer and a negative output terminal connected with the positive input terminal of the first buffer to thereby realize inversion. A dual-terminal signal output from each buffer is converted by one of the comparators COMP into a uni-terminal signal which is in turn output via one of the latches. The last latch outputs a carry signal entering the high bit counter 20 via a carry terminal. The outputs of the latches are coded by the coder 104 as low bits of the Time-to-Digital Converter.

[0041] Initially the Time-to-Digital Converter is enabled and the first buffer is in a non-conducting status, that is, no input can be passed to the output. The initialization unit 105 structured simply with a pull-up P transistor and a pull-down N transistor sets the signals output from the first buffer in a way that the positive terminal is set at a low level and the negative terminal is set at a high level. Since the remaining buffers are conducting, the differential signals are passed down. At this time the outputs of all the comparators COMP are low bits (denoted with 0).

[0042] When a start signal STA is provided, the initialization unit 105 is disabled and the first buffer conducts. Since the signal output of the last buffer is connected with the input of the first buffer in antiphase, the output of the first stage is inverted after a transmission delay of time Δt, and the output of the first comparator COMP is at a high level (denoted with 1); the output of the second stage is inverted after another transmission delay of time Δt; and so on. A transmission delay timing diagram is illustrated in Fig.3. The outputs of the comparators COMP are passed to the latches, and the outputs of the latches vary with time as depicted in the table below.

Time	b1b2b3b4··· ··· b(n-1)bn
0	0000··· ··· 00
Δt	1000··· ··· 00
$2\Delta t$	1100··· ··· 00
... ...	... ...
$n\Delta t$	1111··· ··· 11
$(n+1)\Delta t$	0111··· ··· 11
... ...	... ...

(continued)

Time	b1b2b3b4··· ··· b(n-1)bn
(2n-1) Δ t	0000··· ···01
2n Δ t	0000··· ···00

[0043] When an end signal END is provided, the data at this time is latched in the latches, and the end signal END is output to the latches in a clock tree form to ensure that all the latches latch the data at the same time

[0044] Referring to Fig .4, the buffer includes a P channel field effect transistor, a signal switch EN and MOS transistors MP1, MP2, MN1, MN2, MN3 and MN4. The P channel field effect transistor has a source connected with a supply voltage VDD, a gate connected with a voltage signal V_{BP} of the compensated control source and a drain connected via the signal switch EN with sources of the MOS transistors MP1 and MP2, respectively. Drains of the MOS transistors MP1 and MP2 are connected respectively with output terminals OUT- and OUT+, and gates of the MOS transistors MP1 and MP2 are connected respectively with input terminals IN+ and IN-. The P channel field effect transistor is used for an input due to the possibility of fabricating it into a separate well to reduce interference from external. Since a small transmission delay is necessary for a high precision, the MOS transistors shall be made in as a small size as possible to reduce power consumption and the transmission delay. In this high speed circuit, the time for inversion of an MOS transistor is determined primarily by the time it takes for a gate capacitor to be charged and discharged to a threshold voltage and by an equivalent RC delay over a metal line in a pattern. A smaller MOS transistor results in a small gate capacitor, and a shorter and thinner wire results in a small RC delay, thereby resulting in a small transmission delay. Sources of the MOS transistors MN1, MN2, MN3 and MN4 are connected with each other and then are grounded. Gates of the MOS transistors MN1 and MN3 are connected with each other and then are connected sequentially with drains of the MOS transistors MN2 and MN3 and the output terminal OUT-. Gates of the MOS transistors MN2 and MN4 are connected with each other and then are connected sequentially with drains of the MOS transistors MN4 and MN1 and the output terminal OUT+. Thus a full differential structure with a dual-terminal input and a dual-terminal output is formed. A voltage controlled current source converts a bias voltage into a current to control the transmission delay. The differential structure can, on one hand, reduce common mode interference, and on the other hand, select in-phase transmission or in-antiphase transmission. The MOS switch is controlled by a signal switch EN, and before STA is enabled, the switch of the first stage is opened and the switches of the remaining stages are closed.

[0045] The comparator COMP is a conventional fast hysteresis comparator, and a design thereof shall take a small size and a large current into account.

[0046] The latch is a part of a master-slave D flip-flop which is in a conducting status during normal operation where its output is equal to its input. Upon arrival of a latch signal (here the END signal), the input signal at this time is latched in an inverter loop, and the output is kept unchanged despite the jumping input.

[0047] The coder functions to convert the latched data into binary codes. It is recommended that the number of the stages takes a power of 2^k, so that the code output is of (k+1) bits. Taking k=3 as an example, n=8, and at this time there are 8 delay units. The codes are as depicted in the following table.

Time	b1b2b3b4 b5b6b7b8	Code output
0	00000000	0000
Δ t	10000000	0001
2 Δ t	11000000	0010
3 Δ t	11100000	0011
4 Δ t	11110000	0100
5 Δ t	11111000	0101
6 Δ t	11111100	0110
7 Δ t	11111110	0111
8 Δ t	11111111	1000
9 Δ t	01111111	1001
10 Δ t	00111111	1010
11 Δ t	00011111	1011

(continued)

Time	b1b2b3b4 b5b6b7b8	Code output
12 Δ t	00001111	1100
13 Δ t	00000111	1101
14 Δ t	00000011	1110
15 Δ t	00000001	1111
16 Δ t	00000000	0000 carry

[0048] Referring to Fig.5, the counter 20 is a traveling wave counter including m (a positive integer) D flip-flops triggered with a falling edge. When the output bn of the last buffer in Fig.2 jumps from 1 to 0 after a cycle, the carry signal gives a falling edge, and the first stage Qk+1 of the traveling wave counter jumps; when Qk+1 jumps from 1 to 0 after a cycle, the second stage Qk+2 jumps; and so on The cycles of the carry signals are counted, the timing of which is as illustrated in Fig.6.

[0049] When the highest bit Qk+m of the traveling wave counter jumps from 1 to 0, the $(m+1)^{th}$ D flip-flop acts in a way that the OF output is 1, indicating that the counter overflows.

[0050] The D flip-flop Dff is a conventional master-slave D flip-flop triggered with a falling edge. In such a way of connection, a current stage jumps by a cycle and the next stage jumps by half a cycle, thus implementing binary counting Description of its structure is omitted here.

[0051] The low bit timer including the delay unit loop 10 and the high bit timer including the counter 20 may simply function well as a time-to-digital converter, but readings of the Time-to-Digital Converter for a fixed period of time fluctuate in a relatively large range along with an external supply voltage fluctuation, a change of temperature and a process variation.

[0052] The reading fluctuation is largely due to a delay fluctuation of the delay unit loops 101. Since the voltage controlled current source control is adopted for the delay unit loops 101, we can know from a simulation under the condition of a constant current (the current does not fluctuate along with the temperature, voltage and process fluctuations) that the delay link loop 10 fluctuates mainly along with a MOS transistor model but rarely along with the temperature and supply voltage fluctuations. In a simulation of readings of the Time-to-Digital Converter for a fixed period of time, the readings of the Time-to-Digital Converter obtained in FF (a fast N transistor and a fast P transistor, i.e., an extreme process angle) and SS (a slow N transistor and a slow P transistor, i.e., another extreme process angle) have a deviation of approximately 20% relative to TT (a typical case). The FF readings are 20% more than the TT readings, and the SS readings are 20% less than the TT readings. Therefore such a compensated control source is required that firstly it shall be a constant current source and secondly it can decrease the current in the case of FF and increase the current in the case of SS.

[0053] Referring to Fig.7, the compensated control source 30 includes a low drop out regulator LDO 301, a current source buffer 302, a PMOS compensated transistor 303, an NMOS compensated transistor 304, a PMOS current mirror 305, an NMOS current mirror 306, a bias voltage output transistor 307 and a current setting resistor 308. The low drop out regulator LDO 301 is connected sequentially with the PMOS compensated transistor 303, the PMOS current mirror 305, the current source buffer 302, the NMOS compensated transistor 304, the NMOS current mirror 306 and the current setting resistor 308.

[0054] The low drop out regulator LDO 301 includes a reference source BANDGAP configured to generate a voltage V_{BG} with a temperature coefficient of zero, an error amplifier, an output transistor and a voltage division resistor- The low drop out regulator LDO 301 generates an internal operation voltage AVDD and a series of reference voltages, and all the voltages are of a temperature coefficient of zero.

[0055] The current source buffer 302 and the current setting resistor 308 function to generate an original reference current If there is a high requirement on a value of the current, an external resistor is used as the current setting resistor 308, and at this time the reference voltage V_{REF} is a voltage with a temperature coefficient of zero. If the current with a deviation is allowable, an internal resistor is used as the current setting resistor 308, and at this time the reference voltage V_{REF} is a reference voltage with the same temperature coefficient as that of the internal resistor, and a voltage with a specific temperature coefficient can be introduced from inside the reference source BANDGAP. Thus the temperature coefficient of the current can be counteracted, and the inherent deviation of the current will only be a resistor process deviation.

[0056] After the original reference current is mirrored twice by the current mirror 305 and the current mirror 306, the bias voltage transistor 307 converts the current signal into a voltage signal V_{BP} to be connected with the bias voltage V_{BP} of the buffer in Fig.2. The supply voltage of the bias voltage transistor 307 and the supply voltage of the buffers in

the delay link loop are connected to the same potential VDD. There is provided at the PMOS current mirror 305 a current division PMOS compensated transistor 303 with a source connected with a reference voltage V_1 generated by the voltage division resistor of the low drop out regulator LDO 301. The V_1 is set appropriately so that the PMOS compensated transistor 303 is provided with a constant gate supply voltage V_1-V_{AVDD}. If the PMOS transistor operates at a fast process angle, a larger current is drawn therefrom (relative to a typical case), so that the current eventually flowing to the buffer illustrated in Fig.4 becomes smaller, thereby increasing the delay to counteract the immoderately small delay due to the fast PMOS transistor in the buffer. If the PMOS transistor operates at a slow process angle, a smaller current is drawn therefrom (relative to a typical case), so that the current eventually flowing to the buffer illustrated in Fig.4 becomes larger, thereby decreasing the delay to counteract the immoderately large delay due to the slow PMOS transistor in the buffer. There is provided at the NMOS current mirror 306 a current division NMOS compensated transistor 304 with a source connected with a reference voltage V_2 generated by the voltage division resistor of the low drop out regulator LDO 301, so that the NMOS compensated transistor 304 is provided with a constant gate supply voltage V_2. If the NMOS transistor operates at a fast process angle, a larger current is drawn therefrom (relative to a typical case), so that the current eventually flowing to the buffer illustrated in Fig.4 becomes smaller, thereby increasing the delay to counteract the immoderately small delay due to the fast NMOS transistor in the buffer. If the NMOS transistor operates at a slow process angle, a smaller current is drawn therefrom (relative to a typical case), so that the current eventually flowing to the buffer illustrated in Fig.4 becomes larger, thereby decreasing the delay to counteract the immoderately large delay due to the slow NMOS transistor in the buffer.

[0057] The following table depicts simulated readings at different process angles during a process through driving the inventive TDC by different current sources for measurement within a fixed period of time.

Process angle	FF	TT	SS
Conventional constant current source	648	523	437
Compensated current source	511	523	501

[0058] As can be seen from the above table, the readings of the Time-to-Digital Converter are highly consistent during different processes with the process compensated scheme for the delay unit loop 101.

[0059] The basic principle and main features of the invention and the advantages thereof have been illustrated and described above. Those skilled in the art shall appreciate that the invention should not be limited to the above embodiments and the descriptions of the embodiments are provided merely to illustrate the principle of the invention Various variations and improvements are possible to the invention without departing from the spirit and scope of the invention, and such variations and improvements fall within the scope of the invention as defined in the following claims and equivalents thereof.

Claims

1. A circuit structure of a high performance time-to-digital converter, **characterized by** comprising a delay link loop configured to generate low bit data, a counter configured to generate high bit data and a compensated control source; wherein the delay link loop is further configured to count low bits and send a thus-generated signal in a specific cycle to the counter, the counter is further configured to accumulate a period of the signal in the specific cycle as high bits of the time-to-digital converter, and the compensated control source is configured to compensate and control a voltage signal of the delay link loop.

2. The circuit structure according to claim 1, **characterized in that** the delay link loop comprises a delay unit loop, comparators, latches, a coder and an initialization unit; wherein a start signal (STA) turns on the delay unit loop via the initialization unit; a signal output from the delay unit loop is converted into a digital signal via the comparators; the digital signal is output via the latches and is particularly output via the last latch as a carry signal; an end signal (END) enables the latches to latch data at this time and to send the latched data to the coder; and the coder is configured to convert and output the data as low bits of the time-to-digital converter.

3. The circuit structure according to claim 2, **characterized in that** the delay unit loop comprises a plurality of connected full differential buffers, wherein the last buffer is connected with the first buffer in antiphase, and each of the remaining buffers is connected with the next buffer in phase.

4. The circuit structure according to claim 3, **characterized in that** each of the buffers comprises a **P** channel field

effect transistor, a signal switch (EN) and a first and second PMOS transistors (MP1, MP2), and a first to fourth NMOS transistors (MN1, MN2, MN3 and MN4); wherein sources of the first to fourth NMOS transistors (MN1, MN2, MN3 and MN4) are connected with each other and then are grounded; gates of the first and third NMOS transistors (MN1 and MN3) are connected with each other and then are connected sequentially with drains of the second and third NMOS transistors (MN2 and MN3) and a negative output terminal (OUT-); gates of the second and fourth NMOS transistors (MN2 and MN4) are connected with each other and then are connected sequentially with drains of the fourth and first NMOS transistors (MN4 and MN1) and a positive output terminal (OUT+); the P channel field effect transistor has a source connected with a supply voltage (VDD), a gate connected with a voltage signal (V_{BP}) of the compensated control source and a drain connected via the signal switch (EN) with sources of the first and second PMOS transistors (MP1 and MP2), respectively; drains of the first and second PMOS transistors (MP1 and MP2) are connected respectively with the negative and positive output terminals (OUT- and OUT+); and gates of the first and second PMOS transistors (MP1 and MP2) are connected respectively with a positive and negative input terminals (IN+ and IN-), thereby forming a full differential structure with a dual-terminal input and a dual-terminal output, which controls a transmission delay through a voltage controlled current source.

5. The circuit structure according to any one of claims 1 to 4, **characterized in that** the counter is a traveling wave counter comprising a plurality of D flip-flops and is further configured to count the carry signal from the delay link loop as a high bit output of the time-to-digital converter.

6. The circuit structure according to any one of claims 1 to 5, **characterized in that** the compensated control source comprises a low drop out regulator (LDO), a current source buffer, a PMOS current mirror, an NMOS current mirror, a bias voltage output transistor and a current setting resistor; wherein the low drop out regulator (LDO) is connected sequentially with the PMOS current mirror, the current source buffer, the NMOS current mirror and the current setting resistor and is configured to provide an internal operation voltage (AVDD) and a series of reference voltages; and the current source buffer and the current setting resistor are connected and cooperate with each other to generate an original reference current which is mirrored by the PMOS current mirror and the NMOS current mirror and is output through the bias voltage output transistor as a voltage signal (V_{BP}).

7. The circuit structure according to claim 6, **characterized in that** provided between the PMOS current mirror and the low drop out regulator (LDO) is a current division PMOS compensated transistor with a gate connected with the low drop out regulator (LDO) and a drain connected with the PMOS current minor.

8. The circuit structure according to claim 6, **characterized in that** provided between the NMOS current mirror and the low drop out regulator (LDO) is a current division NMOS compensated transistor with a gate connected with the low drop out regulator (LDO) and a drain connected with the NMOS current mirror.

9. The circuit structure according to claim 6, **characterized in that** a supply voltage of the bias voltage output transistor is connected with a supply voltage (VDD).

10. The circuit structure according to claim 6, **characterized in that** the low drop out regulator (LDO) comprises a reference source (BANDGAP), an error amplifier, an output transistor and voltage division resistors; wherein the reference source (BANDGAP) has one terminal connected with a negative input terminal of the error amplifier and the other terminal connected with the current source buffer; a positive input terminal of the error amplifier is connected between the voltage division resistors; an output terminal of the error amplifier is connected with a gate of the output transistor; and a drain of the output transistor is connected sequentially with the voltage division resistors for voltage division and output.

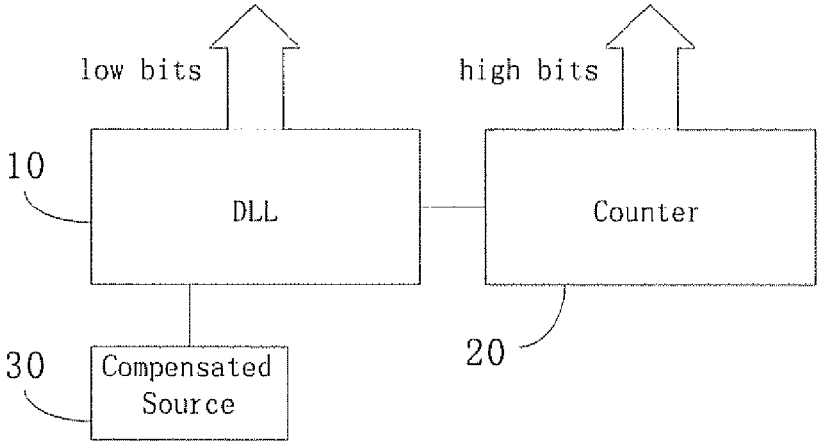
low bits
high bits
10
DLL
Counter
20
30
Compensated Source

Fig. 1

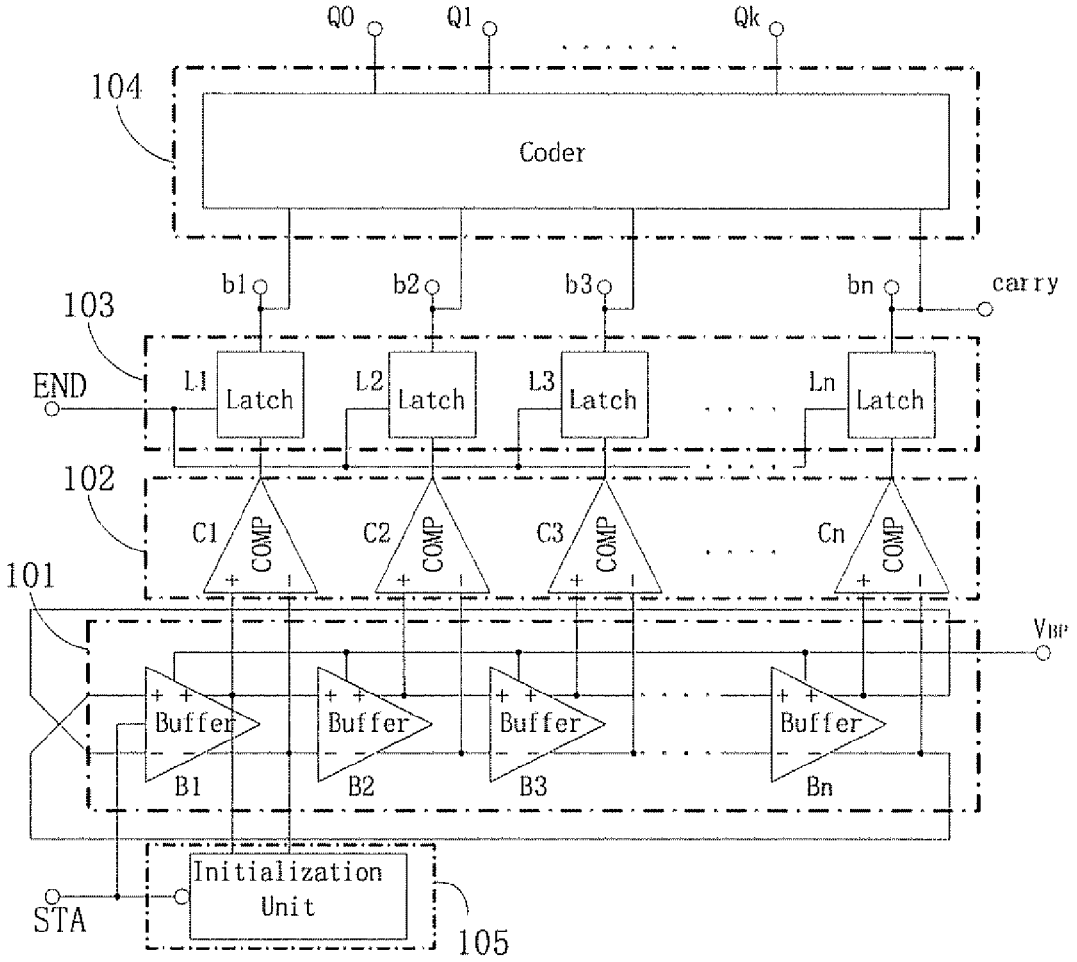
Q0
Q1
Qk
104
Coder
b1
b2
b3
bn
carry
103
END
L1
Latch
L2
Latch
L3
Latch
Ln
Latch
102
C1
COMP
C2
COMP
C3
COMP
Cn
COMP
101
VBP
Buffer
B1
Buffer
B2
Buffer
B3
Buffer
Bn
Initialization Unit
STA
105

Fig. 2

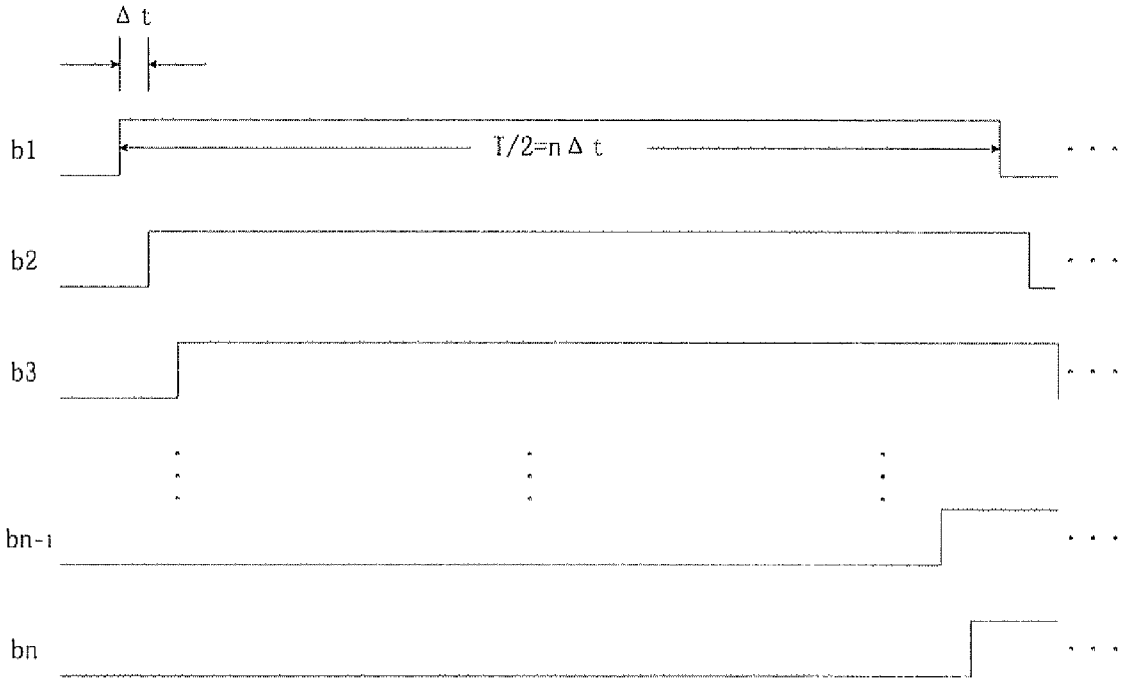
Δ t
b1
T/2=n Δ t
b2
b3
bn-1
bn

Fig. 3

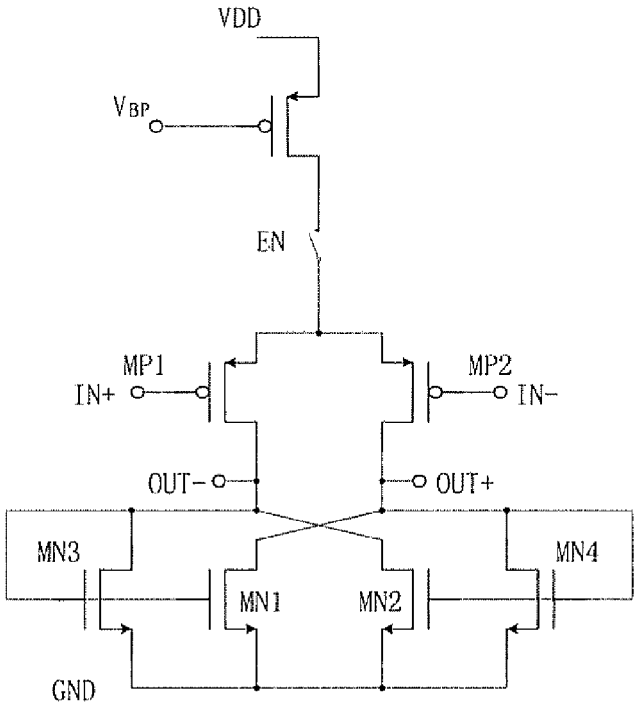
VDD
VBP
EN
MP1
IN+
MP2
IN-
OUT-
OUT+
MN3
MN4
MN1
MN2
GND

Fig. 4

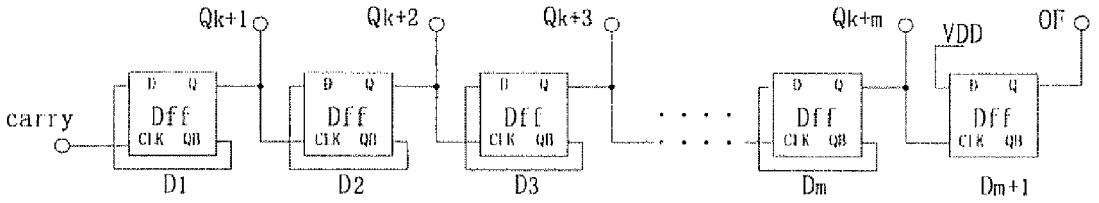
Qk+1
Qk+2
Qk+3
Qk+m
VDD
OT
carry
D Q
Dff
CLK QB
D1
D2
D3
Dm
Dm+1

Fig. 5

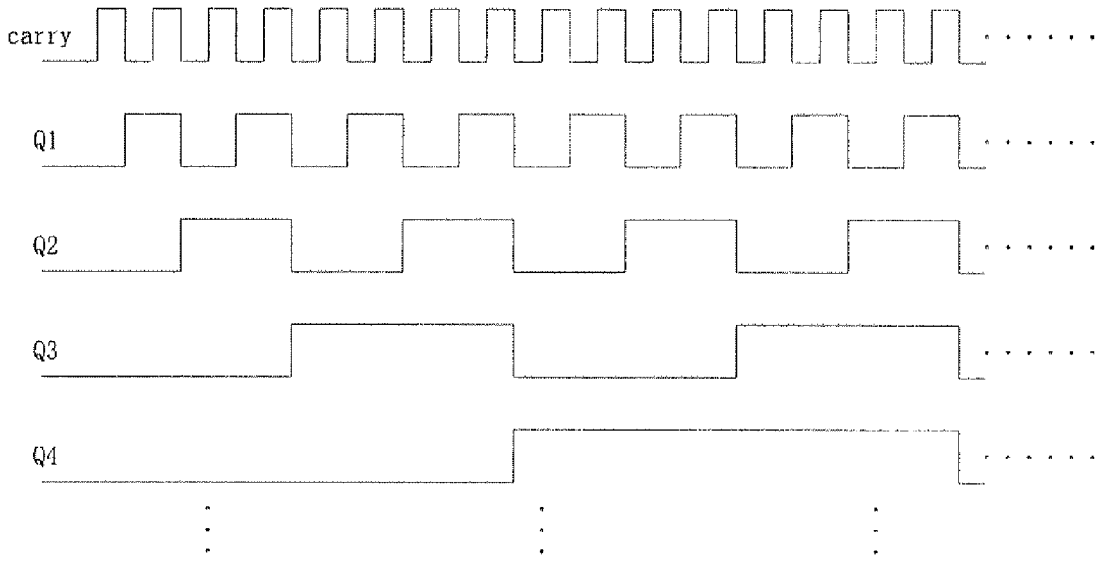
carry
Q1
Q2
Q3
Q4

Fig. 6

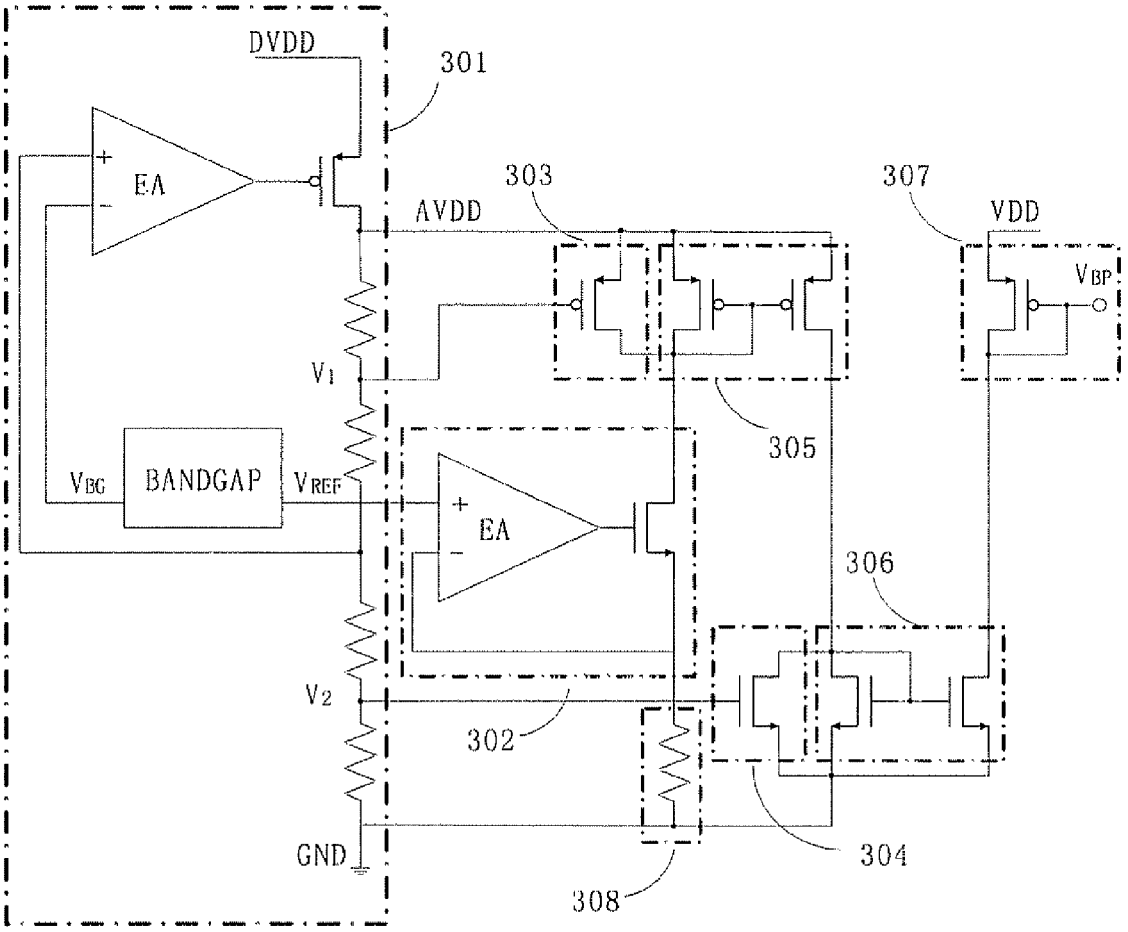
DVDD
301
EA
303
307
AVDD
VDD
VBP
V1
305
VBG
BANDGAP
VREF
EA
306
V2
302
GND
304
308

Fig. 7