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(54) PROCESS FOR PRODUCING SOI WAFER AND SOI WAFER

(57) Ion injection is performed to a single crystal silicon wafer to form an ion injection layer, the ion injection surface of the single crystal silicon wafer and/or the surface of the transparent insulation substrate are/is processed using plasma and/or ozone, the ion injection surface of the single crystal silicon wafer and the surface of the transparent insulation substrate are bonded to each other, by bringing them into close contact with each other at room temperature, with the ion injection surface and the surface as bonding surfaces, an SOI wafer is obtained by mechanically peeling the single crystal silicon wafer by giving an impact to the ion injection layer, to form an SOI layer on the transparent insulation substrate, and thermal processing for flattening the SOI layer surface is performed to the SOI wafer, under an atmosphere of an inert gas, a hydrogen gas, and a mixture gas of them.

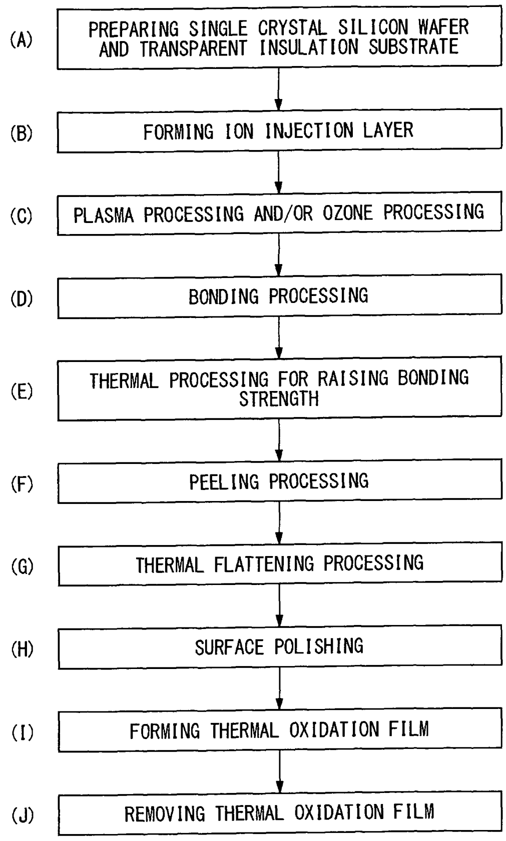

FIG. 1

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Description

TECHNICAL FIELD

[0001] The present invention relates to a manufacturing method of an SOI wafer and to an SOI wafer. Particularly, the present invention relates to a manufacturing method of an SOI wafer in which an SOI layer is formed on a transparent insulation substrate, and to the SOI wafer. The present application relates to Japanese Patent Applications No. 2004-380591 filed on December 28, 2004 and No. 2005-374889 filed on December 27, 2005, the contents of which are incorporated herein by reference, if applicable.

BACKGROUND ART

[0002] An SOI wafer including an SOI (silicon on insulator) structure in which a silicon single crystal layer is formed on an insulator is suited for fabricating a semiconductor integrated circuit of a high density, and is expected to be applied to optical devices such as "TFT-LCD" (thin film transistor - liquid crystal display).

[0003] An SOI wafer in which an SOI layer is formed on a transparent silica substrate is used as such an optical device, for example. In this case, the substrate is a complete insulator, and so does not affect the mobility of the carrier within the SOI layer. Consequently, the mobility of the carrier in the SOI layer will be extremely high, thereby yielding a noticeable effect particularly when driven in high frequency. In addition, in such an SOI wafer, a driving circuit can be formed in an integral manner in the periphery of the TFT region, which enables high density mounting.

[0004] In such an SOI wafer for use as an optical device, the thickness of the SOI layer should be as thin as about 0.5μm, for example. Accordingly, the bonding strength between the silica substrate and the SOI layer should be sufficiently strong and firm to endure grinding, polishing for making the SOI layer to be as thin as the level of the stated thickness, and to withstand the thermal and mechanical stresses exercised onto the SOI layer in manufacturing the device. To enhance the bonding strength, it has been required to perform thermal processing under a high temperature.

[0005] However, the thermal expansion coefficient differs between a silica substrate and an SOI layer. This occasionally causes stress due to thermal deformation during the thermal processing for bonding, during the cooling processing after the bonding, or during the grinding or polishing processing, thereby causing the silica substrate or the SOI layer to crack, or to break due to flaking. Such a problem is not confined to a case where the insulation transparent substrate is made of silica, and may equally happen when bonding a single crystal silicon wafer to a substrate having a different thermal expansion coefficient.

[0006] So as to solve the mentioned problem, a technology has been disclosed for alleviating the effect of thermal stress incident to thermal processing, by performing a thermal bonding processing process and a thin film process alternately and step by step, in an SOI wafer manufacturing method adopting a hydrogen ion injection peeling method (e.g. Patent Document No. 1).
Patent Document No. 1: Japanese Patent Application Publication No. 11-145438

DISCLOSURE OF THE INVENTION

PROBLEMS TO BE SOLVED BY THE INVENTION

[0007] Regarding a manufacturing method of an SOI wafer in which an SOI layer is formed on a transparent insulation substrate, the present invention aims to provide a manufacturing method of an SOI wafer and to provide an SOI wafer, by which thermal deformation, flaking, cracking, or the like attributable to the difference in thermal expansion coefficient between a transparent insulation substrate and an SOI layer is prevented with a simple process, and the resulting SOI layer has a highly even film thickness.

MEANS FOR SOLVING THE PROBLEMS

[0008] So as to achieve the above objectives, as a first embodiment of the present invention, provided is a manufacturing method for manufacturing an SOI wafer by bonding a single crystal silicon wafer to a transparent insulation substrate, and thereafter making the single crystal silicon wafer to be thinned to form an SOI layer on the transparent insulation substrate, the manufacturing method at least including: a step of forming an ion injection layer within the single crystal silicon wafer, by injecting at least one of a hydrogen ion and a rare gas ion from a surface of the single crystal silicon wafer; a step of processing the ion injection surface of the single crystal silicon wafer and/or a surface of the transparent insulation substrate using plasma and/or ozone; a step of bonding the ion injection surface of the single crystal silicon wafer to a surface of the transparent insulation substrate, by bringing them into close contact with each other in a room temperature, with the processed surface(s) as bonding surface(s); a step of obtaining an SOI wafer, by mechanically peeling the single crystal silicon wafer by giving an impact to the ion injection layer, to form an SOI layer on the transparent insulation substrate; and a step of performing thermal processing for flattening a surface of the SOI layer, to the resulting SOI wafer, under an atmosphere of an inert gas, a hydrogen gas, or a mixture gas of the inert gas and the hydrogen gas.

[0009] By processing the ion injection surface of the single crystal silicon wafer and/or the surface of the transparent insulation substrate using plasma and/or ozone, an OH group will be increased and activated on the injection surface of the wafer and/or a surface of the substrate. If the single crystal silicon wafer and the transparent insulation substrate, under such a state, are brought into close contact with each other at room temperature to be bonded, with the processed surface(s) as the bonding surface(s), the surfaces brought into close contact will be firmly bonded by means of hydrogen bonding, to obtain sufficiently firm bonding even without providing high temperature thermal processing for raising the bonding strength in later stages. In addition, since the bonding surfaces are firmly bonded to each other in the above way, thereafter a thin SOI layer can be formed on the transparent insulation substrate by mechanically peeling the single crystal silicon wafer by giving an impact to the ion injection layer. This means that a thin film can be obtained even without performing thermal processing for peeling. This further indicates that an SOI wafer can be manufactured without causing thermal deformation, flaking, cracking, or the like attributable to the difference in thermal expansion coefficient between the transparent insulation substrate and the single crystal silicon wafer. In addition, since the hydrogen ion injection peeling method is used, it is possible to manufacture an SOI wafer whose SOI layer has a thin film thickness, a favorable film thickness evenness, and excellent crystallization. Furthermore, the thermal processing for flattening the surface of the SOI layer under an atmosphere of an inert gas, a hydrogen gas, or a mixture gas of them is performed after the formation of the SOI layer. Therefore, it is possible to remove the surface roughness caused in the peeling step, and to remove the crystal defect or damages caused in the vicinity of the SOI layer surface due to ion injection.

[0010] In this case, after the step of performing thermal processing for flattening a surface of the SOI layer, it is preferable to include: a step of forming a thermal oxide layer on the surface of the SOI layer by performing thermal oxidation to the SOI wafer to which the thermal processing has been performed; and a step of reducing a thickness of the SOI layer by removing the thermal oxide layer.

In this way, by forming the thermal oxide layer on the surface of the SOI layer by performing thermal oxidation to the SOI wafer provided with thermal processing for flattening the SOI layer surface, and by reducing the same to reduce the thickness of the SOI layer, it is possible to manufacture an SOI wafer in which an SOI layer has a thinner film thickness, a more favorable film thickness evenness, and from which the surface roughness, the crystal defect, or the damages are more sufficiently removed.

[0011] Between the step of bonding and the step of obtaining an SOI wafer, it is preferable to include a step of raising a bonding strength by performing thermal processing to the bonded wafer under a temperature of 100-300 degrees centigrade.

As in the above way, if the single crystal silicon wafer and the transparent insulation substrate bonded to each other are subjected to the mechanical peeling step for giving an impact to the ion injection layer, after raising the bonding strength by performing thermal processing of a low temperature of 100-300 degrees centigrade which does not cause thermal deformation, it is possible to manufacture an SOI wafer by more assuredly preventing the generation of flaking, cracking, or the like of the bonding surfaces attributable to the mechanical stress.

[0012] It is preferable that a temperature used in the step of performing thermal processing for flattening a surface of the SOI layer is 1100-1350 degrees centigrade

As in the above way, by setting the temperature used in the thermal processing for flattening the SOI layer surface to be equal to or greater than 1100 degrees centigrade, it is possible to alleviate the surface roughness in a relatively short time. In addition, if the temperature is equal to or smaller than 1350 degrees centigrade, an SOI can be manufactured without causing a problem such as heavy metal impurity contamination or unfavorable endurance of the thermal processing furnace.

[0013] It is preferable that the transparent insulation substrate is one of a silica substrate and a sapphire (alumina) substrate.

As in the above way, if the transparent insulation substrate is one of a silica substrate and a sapphire (alumina) substrate, it is possible to manufacture an SOI wafer suitable for fabricating an optical device, since these substrates have a favorable optical characteristic.

[0014] Further, it is preferable that an ion injection dose used in the step of forming an ion injection layer is greater than $8\times10^{16}/\text{cm}^2$.

As in the above way, by setting the ion injection dose to be greater than $8\times10^{16}/\text{cm}^2$ in forming the ion injection layer, the mechanical peeling becomes easy.

[0015] In addition, the present invention provides an SOI wafer manufactured according to any of the manufacturing methods recited above.

As in the above way, an SOI wafer manufactured according to any of the above-described manufacturing methods has not caused any thermal deformation, flaking, cracking, or the like during manufacturing, as well as having a thinner film thickness and a more favorable film thickness evenness, having excellent crystallization, and having an SOI layer on a transparent insulation substrate having high carrier mobility, useful for manufacturing various devices.

EFFECT OF THE INVENTION

[0016] By adopting the manufacturing method of an SOI wafer according to the present invention, the surfaces to be bonded are processed with plasma and/or ozone prior to bonding of the single crystal silicon wafer and the transparent insulation substrate, which increase and activates the OH group on the surfaces. If the single crystal silicon wafer and the transparent insulation substrate, under such a state, are brought into close contact with each other at room temperature to be bonded, the surfaces brought into close contact will be sufficiently firm bonding even without providing high temperature thermal processing for raising the bonding strength in later stages. In addition, since the bonding surfaces are firmly bonded to each other in the above way, thereafter a thin SOI layer can be formed on the transparent insulation substrate by mechanically peeling the single crystal silicon wafer by giving an impact to the ion injection layer. This means that a thin film can be obtained even without performing thermal processing for peeling. This further indicates that an SOI wafer can be manufactured without causing thermal deformation, flaking, cracking, or the like attributable to the difference in thermal expansion coefficient between the transparent insulation substrate and the single crystal silicon. Furthermore, the thermal processing for flattening the surface of the SOI layer under an atmosphere of an inert gas, a hydrogen gas, or a mixture gas of them is performed after the formation of the SOI layer. Therefore, it is possible to remove the surface roughness caused in the peeling step. Upon necessity, by thereafter forming the thermal oxide layer on the surface of the SOI layer and by reducing the same to reduce the thickness of the SOI layer, the SOI layer will have a thinner film thickness, a more favorable film thickness evenness, and from which the surface roughness, the crystal defect, or the damages are more sufficiently removed.

[0017] In addition, the SOI wafer according to the present invention is an SOI wafer that does not cause thermal deformation, flaking, cracking, or the like during manufacturing, has a thinner film thickness, a more favorable evenness in film thickness, excellent crystallization, and an SOI layer on a transparent insulation substrate having high carrier mobility, useful for manufacturing various devices.

BRIEF DESCRIPTION OF THE DRAWINGS

[0018] Fig. 1 is a process diagram showing one example of a manufacturing method of an SOI wafer, according to the present invention.

BEST MODE FOR CARRYING OUT THE INVENTION

[0019] As mentioned above, regarding a manufacturing method of an SOI wafer in which an SOI layer is formed on a transparent insulation substrate, so as to prevent thermal deformation, flaking, cracking, or the like attributable to the difference in thermal expansion coefficient between a transparent insulation substrate and an SOI layer, a technology has been already disclosed by which the effect of the thermal stress incident to thermal processing is alleviated by performing a thermal bonding processing process and a thin film process alternately and step by step, in an SOI wafer manufacturing method adopting a hydrogen ion injection peeling method. However for the purpose of improving the productivity of the SOI wafer, a new technology has been nevertheless desired for solving the stated problem by a smaller number of processes and in a short time.

[0020] In view of this, the inventors of the present invention have conceived to enhance the bonding strength without performing the thermal processing by preprocessing the surfaces to be bonded using plasma and/or ozone processing, and to perform peeling mechanically instead of thermal processing.

[0021] In addition, in the conventional ion injection peeling method, mirror polishing has been conducted by using polishing (e.g. so-called "touch polish") that removes an extremely small thickness of 5-400nm, for removing surface roughness called "haze" caused in the peeling process, and for removing crystal defects or damages caused in the vicinity of the SOI layer surface in the ion injection. However, there is a possibility of reducing the film thickness evenness of the SOI layer by the mentioned polishing that includes a mechanical processing aspect.

In view of the above, so as to prevent such reduction in film thickness evenness of the SOI layer, the inventors of the present invention have completed the present invention, by conceiving of an idea to obtain an SOI layer having a thinner film thickness and a more favorable film thickness evenness and from which surface roughness, crystal defects, or damages are sufficiently removed, by performing thermal processing to flatten the surface of the SOI layer in an atmosphere of an inert gas, a hydrogen gas, or a mixture of these gases after the formation of the SOI layer to remove the surface roughness or the like caused in the peeling process, and by thereafter forming thermal oxidation on the SOI layer surface as necessary and removing it to reduce the thickness of the SOI layer.

As follows, some aspects of the present invention are described by way of embodiments. The present invention will not be limited to the following embodiments.

[0022] Fig. 1 is a process diagram showing one example of a manufacturing method of an SOI wafer, according to the present invention.

[0023] First, a single crystal silicon wafer and a transparent insulation substrate are prepared (process A).

The single crystal silicon wafer is not particularly limited as long as it is obtained by slicing a single crystal grown by the Czochralski method for example, which for example has a diameter of 100-300mm, a conductivity type of P-type or N-type, and a resistivity of about 10Ω•cm.

The transparent insulation substrate is not also particularly limited. However if either a silica substrate or a sapphire (alumina) substrate, both having a favorable optical characteristic, is used as a transparent insulation substrate, it is possible to manufacture an SOI wafer suitable for fabricating an optical device.

[0024] Next, at least one of a hydrogen ion and a rare gas ion is injected from the surface of the single crystal silicon wafer, to form an ion injection layer in the wafer (process B).

For example, at least one of a hydrogen ion and a rare gas ion in a predetermined dose is injected from the surface of the single crystal silicon wafer, with an injection energy capable of forming an ion injection layer at the depth corresponding to a predetermined SOI layer thickness (e.g. the depth of smaller than or equal to 0.5μm), while keeping the temperature of the single crystal silicon wafer to 250-450 degrees centigrade. An exemplary condition may be the injection energy of 20-100keV and the injection dose of 1×10^{16} - 1×10^{17}/cm^2 . Here, so as to facilitate the peeling at the ion injection layer, the ion injection dose should preferably be equal to or greater than 8×10^{16}/cm^2. In addition, if the ion injection is performed through an insulation film such as a thin silicon oxide layer formed in advance on a surface of the single crystal silicon wafer, an advantage of restraining channeling of the injected ion will be obtained.

[0025] Next, the ion injection surface of this single crystal silicon wafer and/or the surface of the transparent insulation substrate are/is processed with plasma and/or ozone (process C).

In adopting plasma processing, a single crystal silicon wafer and/or a transparent insulation substrate, to which cleansing such as RCA cleansing has been performed, are/is placed in a vacuum chamber, and a gas for plasma processing (hereinafter simply "plasma gas") is introduced. Then the single crystal silicon wafer and/or the transparent insulation substrate are/is subjected to high frequency plasma of about 100W for about 5-10 seconds, to perform plasma processing to the surface thereof. In processing a single crystal silicon wafer, for oxidizing the surface thereof, the plasma gas may be plasma of an oxygen gas. For not oxidizing the surface of a single crystal silicon wafer, the plasma gas may be a hydrogen gas, an argon gas, a mixture gas of them, or a mixture gas of a hydrogen gas and a helium gas. Any gas is usable for processing of a transparent insulation substrate.

[0026] In adopting ozone processing, a single crystal silicon wafer and/or a transparent insulation substrate, to which cleansing such as RCA cleansing has been performed, are/is placed in a chamber to which atmospheric air is introduced, and a plasma gas such as a nitrogen gas, an argon gas, or the like is introduced. Then the surfaces are treated with ozone processing by generating high frequency plasma to convert the oxygen in the atmospheric air into ozone. Here, it is possible to perform any one of plasma processing and ozone processing, or it is also possible to perform both of plasma processing and ozone processing.

[0027] By processing with plasma and/or ozone, the organic substances on the surface of the single crystal silicon wafer and/or the transparent insulation substrate are oxidized to be removed, and instead the OH group on the surface is increased and activated. The surface to be processed may be a bonding surface. For a single crystal silicon wafer, the surface to be processed is an ion injection surface. The processing is desirably performed to both of a single crystal silicon wafer and a transparent insulation substrate. However the processing may be performed to only one of the single crystal silicon wafer and the transparent insulation substrate.

[0028] Then, the ion injection surface of the single crystal silicon wafer and the surface of the transparent insulation substrate, to which plasma processing and/or ozone processing are/is provided, are brought into close contact with each other at room temperature to be bonded, with the ion injection surface and the surface as the bonding surfaces (process D).

In the process C, at least one of the ion injection surface of the single crystal silicon wafer and the surface of the transparent insulation substrate is processed by plasma processing and/or ozone processing. Consequently, the respective surfaces of the single crystal silicon wafer and of the transparent insulation substrate are able to be bonded to each other firmly, with a strength that can endure the mechanical peeling in the later processes, by simply bringing them into close contact to each other, under a reduced pressure or a normal pressure, and in a temperature of about a general room temperature, for example. This means that thermal bonding processing of equal to or more than 1200 degrees centigrade is not necessary, and so it is preferable since there is no possibility of causing thermal deformation, flaking, cracking, or the like attributable to the difference in thermal expansion coefficient, which is a problem inherent in heating processes.

[0029] After this, the bonded wafer may be subjected to thermal processing of a low temperature of 100-300 degrees centigrade, for enhancing the bonding strength (process E).

For example, when the transparent insulation substrate is made of silica, the thermal expansion coefficient is smaller than that of silicon (i.e. Si: 2.33×10^{-6}, and silica: 0.6×10^{-6}). Therefore if the silica transparent insulation substrate is heated after being bonded to the silicon wafer having about the same thickness, the silicon wafer will break when exceeding 300 degrees centigrade. Thermal processing of a relatively low temperature as in this process E is desirable since it does not have a possibility of causing thermal deformation, flaking, cracking, or the like attributable to the difference in thermal expansion coefficient. Note that in adopting a thermal processing furnace (i.e. a batch processing type), a sufficient advantage is obtained if the thermal processing time is about 0.5-24 hours.

[0030] Next, a single crystal silicon wafer is mechanically peeled by giving an impact to the ion injection layer, to form an SOI layer on the transparent insulation substrate (process F).

In the hydrogen ion injection peeling method, thermal processing is performed to the bonded wafer in an inert gas atmosphere of about 500 degrees centigrade, to perform thermal peeling by means of a rearrangement effect of crystal and an aggregating effect of air bubbles of injected hydrogen. In contrast, the present invention performs mechanical peeling by giving an impact to an ion injection layer, and so there is no possibility of causing thermal deformation, flaking, cracking, or the like that would happen incident to heating.

For giving an impact to the ion injection layer, a jet of fluid such as gas, liquid, or the like is blown continuously or discontinuously from the side surface of the bonded wafer, for example. However, another method may be adopted as long as the method causes mechanical peeling by impact.

[0031] Next, thermal processing for flattening the surface (i.e. the peeling surface) of the SOI layer is performed to the SOI wafer obtained in the above manner, under an atmosphere of an inert gas, a hydrogen gas, or a mixture gas of them (process G).

Accordingly, it is possible to remove the surface roughness caused by the peeling process, or the crystal defect or the damages caused by the ion injection in the vicinity of the SOI layer surface.

Note that it is preferable to perform the thermal processing for flattening the surface of the SOI layer under the temperature of 1100-1350 degrees centigrade. By performing the thermal processing under the temperature of equal to or above 1100 degrees centigrade, the surface roughness can be alleviated in a relatively short time. If the temperature is equal to or smaller than 1350 degrees centigrade, a problem such as heavy metal impurity contamination or unfavorable endurance of the thermal processing furnace will not be caused in the thermal processing. Note that the film thickness of the SOI layer is already sufficiently thin, there is no fear of causing thermal deformation, flaking, cracking, or the like, even if the thermal processing of such a high temperature is performed.

[0032] In performing thermal processing using a thermal processing furnace of a normal heater type (i.e. a batch type), an adequate thermal processing time may be in the range of 10 minutes to 8 hours, so as to achieve a sufficient thermal processing effect while not reducing the productivity, although it may be true that the thermal processing time may depend on the temperature under which the thermal processing is performed. In contrast, when performing the thermal processing using an RTA (rapid thermal annealing) apparatus, it is preferable that the thermal processing temperature is greater than or equal to 1200 degrees centigrade and the thermal processing time is 1-120 second(s). It is also possible to perform both of the thermal processing of a batch furnace type and the thermal processing using an RTA apparatus.

[0033] The thermal processing atmosphere may be an atmosphere of an inert gas, a hydrogen gas, or a mixture gas of them. However it is preferable that the hydrogen gas content is smaller than or equal to 25%, since the possibility of causing erosion to the bonding interface becomes greater and the possibility of generating the slip dislocation due to thermal processing becomes greater, if the ratio of the hydrogen gas is great. Furthermore from the viewpoint of security, the hydrogen gas content should preferably be smaller than or equal to the explosive limit (i.e. 4%). As the inert gas, an argon gas that is most advantageous in terms of cost and versatility may be desirable, however helium or the like may also be used.

[0034] As necessary, the surface may be slightly polished using touch polish or the like, after the thermal processing (process G) for flattening the SOI layer surface, to the extent that "removed thickness" (i.e. the thickness removed from the surface by the polishing) is equal to or smaller than 70nm, in particular equal to or smaller than 50nm (process H).

According to the process, the long period component of the surface roughness (e.g. the period of about 1-10μm) can be alleviated. The short period component (e.g. the period of equal to or smaller than 1μm) of the surface roughness is sufficiently removed by the thermal processing of the process G. However, so as to more assuredly remove the long period component, it is preferable to perform slight polishing. Once the thermal processing is performed, the surface roughness and the damages to the surface have already been removed by a large degree. Therefore, the thickness to be further removed can be largely reduced compared to conventional cases. In particular, the removed thickness can be reduced down to half or smaller. This enables to alleviate the long period component of the surface roughness, while restraining the adverse effect to the film thickness evenness of the thin film.

[0035] Next, as necessary, the thermal oxidation is performed to the SOI wafer already provided with thermal processing, thereby forming a thermal oxide layer (so-called "sacrifice oxide layer") on the surface of the SOI layer (process I).

The thermal oxide layer formed on the surface of the SOI layer in this way is able to take in the crystal defect or the damages left unremoved even after the process G, and it becomes possible to to cause the SOI layer to have a thin film having a predetermined thickness without hardly reducing the film thickness evenness. For example, the thermal oxide layer may be formed by performing pyrogenic oxidation under a temperature of 950 degrees centigrade. However, the forming method of the oxide layer is not particularly limited.

[0036] Lastly, by removing the formed thermal oxide layer, the thickness of the SOI layer is reduced (process J). The removal of the thermal oxide layer may be performed by impregnating the wafer with an aqueous solution that contains HF, for example.

As a result, the SOI wafer in which an SOI layer is formed on a transparent insulation substrate is obtained.

[0037] The SOI wafer produced by the processes of A-J has not caused any thermal deformation, flaking, cracking, or the like, during manufacturing, as well as having a thin film thickness, a favorable film thickness evenness, excellent crystallization, and an SOI layer on a transparent insulation substrate having high carrier mobility, useful for manufacturing various devices.

In particular, the touch polish can be either omitted, or can be restrained to a very small removed thickness. Therefore, it is possible to obtain an SOI wafer that assuredly prevents impairment in film thickness evenness that would happen attributable to polishing that includes a mechanical processing aspect.

Moreover, such an SOI wafer is particularly suited for fabrication of an optical device such as a TFT-LCD, because of having an SOI layer on the transparent insulation substrate.

Embodiment Example

(Embodiment Example)

[0038] A single crystal silicon wafer having a diameter of 200mm and one surface thereof being subjected to mirror polishing is prepared, as a wafer for forming an SOI layer. A silicon oxide layer of 100nm is formed on the surface of the single crystal silicon wafer by thermal oxidization. The surface roughness (Ra) of the oxidization layer at the surface subjected to mirror polishing (i.e. a surface to be bonded) was 0.2nm. The measurement was performed to the measurement region of $10\mu m \times 10\mu m$ using an atom force microscope.

[0039] As a transparent insulation substrate, a synthetic silica wafer having a diameter of 200mm and one surface thereof being subjected to mirror polishing is prepared. The surface roughness (Ra) of the transparent insulation substrate at the surface subjected to mirror polishing (i.e. a surface to be bonded) was 0.19nm. The apparatus and the method of measuring have the same condition as the oxide layer of the single crystal silicon wafer.

[0040] A hydrogen ion is selected as the ion to be injected to a single crystal silicon wafer through the silicon oxide layer of 100nm, and the ion is injected under a condition of an injection energy of 35keV and an injection dose of $9 \times 10^{16}/cm^2$. The injection depth of the single crystal silicon layer was 0.3nm.

[0041] Next, the single crystal silicon wafer to which ion has been injected is placed in a plasma processing apparatus, and an air is introduced as a plasma gas. Then the high frequency plasma processing is performed for 5-10 seconds by applying a high frequency of 13.56MHz under a reduced pressure condition of 2Torr between parallel plate electrodes having a diameter of 300mm under a high frequency power of 50W.

[0042] As for a synthetic silica wafer, the wafer is placed in a chamber to which an atmospheric air is introduced, and an argon gas is introduced as a plasma gas in narrow space between electrodes. Then by applying a high frequency between the electrodes to generate plasma, the oxygen in the atmospheric air becomes ozonized by the existence of the atmospheric air between the plasma and the substrate. The surface to be bonded is processed by means of the ozone. The processing time was set to 5-10 seconds.

[0043] The wafers to which surface processing was performed in the above manner were brought into close contact at room temperature, to start bonding by strongly pressing one end of the both wafers in the thickness direction. Then after 48 hours in the room temperature, the bonding surface was observed by human eyes. As a result, the bonding was confirmed to extend throughout the substrate.

So as to confirm the bonding strength, one of the wafers is fixed, and the wafer surface of the other wafer is provided with a stress in the parallel direction, in an attempt to perform displacement in the lateral direction, however the displacement did not occur.

[0044] Next, so as to peel the ion injection layer by giving an impact thereto, blades of paper cutting scissors were placed at the side surface of the bonded wafers in a diagonal position, thereby knocking in wedges several times. Accordingly, the peeling was caused at the ion injection layer, thereby obtaining an SOI wafer and a remaining single crystal silicon wafer.

[0045] This SOI wafer was subjected to thermal processing of 1200 degrees centigrade under the atmosphere of 100% argon for 60 minutes. Furthermore, polishing is performed to remove the thickness of 50nm, to remove the long period component as well as the short period component of the SOI layer surface roughness. As a result, surface roughness at the same level as a wafer provided with normal mirror polishing has been obtained.

[0046] The inside-surface film thickness evenness of this SOI layer was also measured. As a result, the film thickness variation is restrained to equal to or smaller than ±10nm within the wafer surface, which has confirmed favorable film thickness evenness. Furthermore, the crystallization of the SOI layer was evaluated by a SECCO defect evaluation using a liquid resulting from diluting the SECCO etching liquid according to a predetermined method. The confirmed defect density was 2×10^3 - $6 \times 10^3/cm^2$ which is a favorable value.

[0047] The above-described embodiments do not limit the invention. The above-described embodiments are only illustrative, and includes a configuration substantially the same as the technical concept recited in the claims of the invention. Any configuration that has the same effects or advantages is intended to be included in the technical concept of the present invention.

Claims

1. A manufacturing method for manufacturing an SOI wafer by bonding a single crystal silicon wafer to a transparent insulation substrate, and thereafter making the single crystal silicon wafer to be thinned to form an SOI layer on the transparent insulation substrate, the manufacturing method **characterized in** performing at least:

    a step of forming an ion injection layer within the single crystal silicon wafer, by injecting at least one of a hydrogen ion and a rare gas ion from

a surface of the single crystal silicon wafer;
a step of processing the ion injection surface of the single crystal silicon wafer and/or a surface of the transparent insulation substrate using plasma and/or ozone;
a step of bonding the ion injection surface of the single crystal silicon wafer to a surface of the transparent insulation substrate, by bringing them to close contact with each other in a room temperature, with the processed surface(s) as bonding surface(s);
a step of obtaining an SOI wafer, by mechanically peeling the single crystal silicon wafer by giving an impact to the ion injection layer, to form an SOI layer on the transparent insulation substrate; and
a step of performing thermal processing for flattening a surface of the SOI layer, to the resulting SOI wafer, under an atmosphere of an inert gas, a hydrogen gas, or a mixture gas of the inert gas and the hydrogen gas.

2. The manufacturing method as set forth in Claim 1, **characterized in** performing, after the step of performing thermal processing for flattening a surface of the SOI layer:

a step of forming a thermal oxide layer on the surface of the SOI layer by performing thermal oxidation to the SOI wafer to which the thermal processing has been performed; and
a step of reducing a thickness of the SOI layer by removing the thermal oxide layer.

3. The manufacturing method as set forth in any one of Claim 1 and Claim 2, **characterized in** performing, after the step of bonding and before the step of obtaining an SOI wafer:

a step of raising a bonding strength by performing thermal processing to the bonded wafer under a temperature of 100-300 degrees centigrade.

4. The manufacturing method as set forth in any one of Claims 1-3, **characterized in that**:

a temperature used in the step of performing thermal processing for flattening a surface of the SOI layer is 1100-1350 degrees centigrade.

5. The manufacturing method as set forth in any one of Claims 1-4, **characterized in that**:

the transparent insulation substrate is one of a silica substrate and a sapphire (alumina) substrate.

6. The manufacturing method as set forth in any one of Claims 1-5, **characterized in that**:

an ion injection dose used in the step of forming an ion injection layer is greater than $8\times10^{16}/\mathrm{cm}^2$.

7. An SOI wafer manufactured according to the manufacturing method as recited in any one of Claims 1-6.

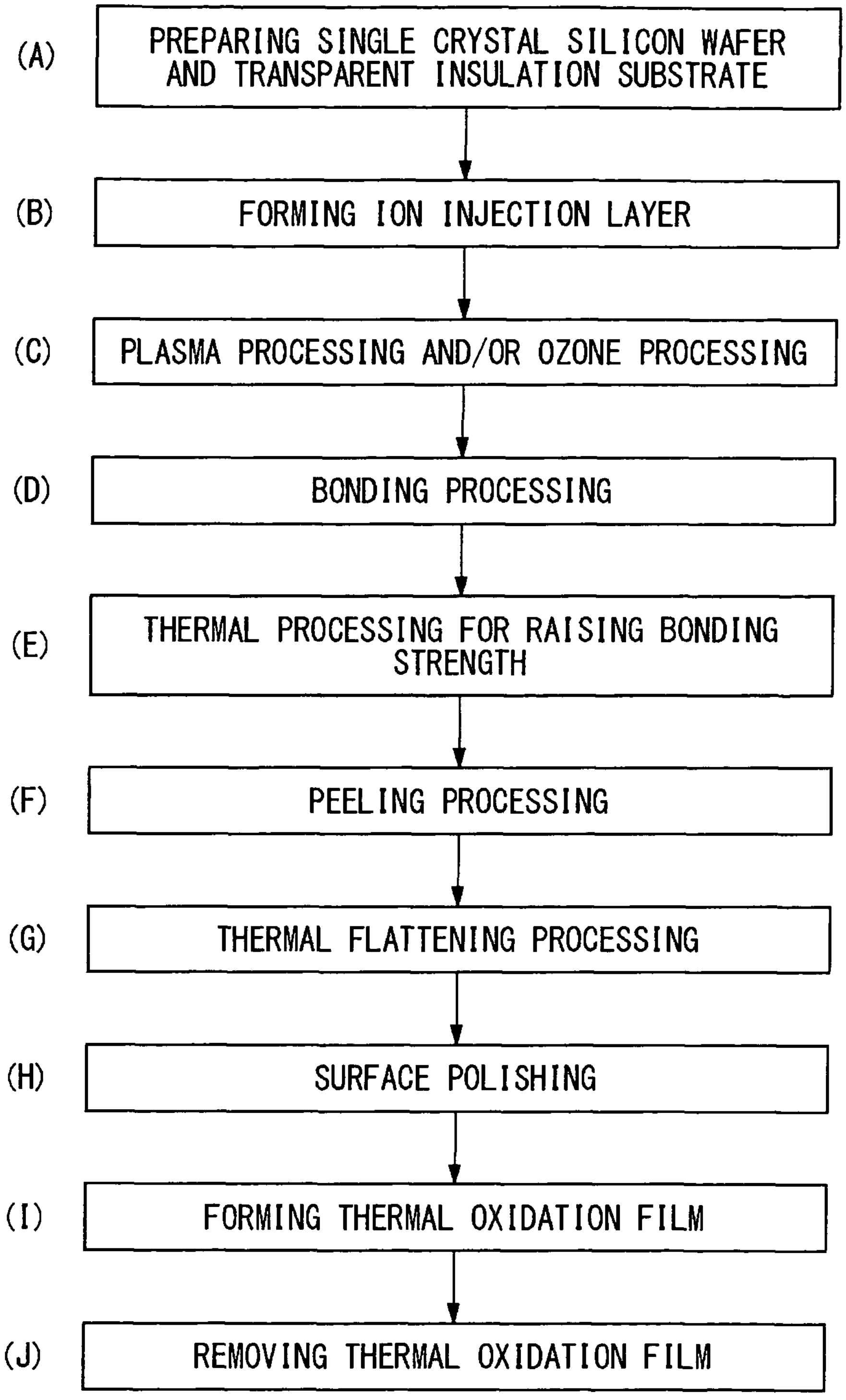
(A)
PREPARING SINGLE CRYSTAL SILICON WAFER AND TRANSPARENT INSULATION SUBSTRATE
(B)
FORMING ION INJECTION LAYER
(C)
PLASMA PROCESSING AND/OR OZONE PROCESSING
(D)
BONDING PROCESSING
(E)
THERMAL PROCESSING FOR RAISING BONDING STRENGTH
(F)
PEELING PROCESSING
(G)
THERMAL FLATTENING PROCESSING
(H)
SURFACE POLISHING
(I)
FORMING THERMAL OXIDATION FILM
(J)
REMOVING THERMAL OXIDATION FILM

FIG. 1

INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP2006/313909

A. CLASSIFICATION OF SUBJECT MATTER
H01L21/02(2006.01)i, *H01L21/762*(2006.01)i, *H01L27/12*(2006.01)i

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
H01L21/02, H01L21/762, H01L27/12

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Jitsuyo Shinan Koho	1922-1996	Jitsuyo Shinan Toroku Koho	1996-2006
Kokai Jitsuyo Shinan Koho	1971-2006	Toroku Jitsuyo Shinan Koho	1994-2006

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	JP 2001-511608 A (Silicon Genesis Corp.), 14 August, 2001 (14.08.01), Full text; Figs. 1 to 21 & WO 99/06110 A1 & US 6153524 A & US 2002/0098713 A1 & GB 2343550 A & AU 9886757 A	1-7
Y	JP 07-249749 A (Canon Inc.), 26 September, 1995 (26.09.95), Full text; Figs. 1 to 6 (Family: none)	1-7

☒ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:

"A"	document defining the general state of the art which is not considered to be of particular relevance
"E"	earlier application or patent but published on or after the international filing date
"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O"	document referring to an oral disclosure, use, exhibition or other means
"P"	document published prior to the international filing date but later than the priority date claimed
"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&"	document member of the same patent family

Date of the actual completion of the international search 05 October, 2006 (05.10.06)	Date of mailing of the international search report 17 October, 2006 (17.10.06)
Name and mailing address of the ISA/ Japanese Patent Office Facsimile No.	Authorized officer Telephone No.

Form PCT/ISA/210 (second sheet) (April 2005)

INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP2006/313909

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	JP 2000-036583 A (Canon Inc.), 02 February, 2000 (02.02.00), Full text; Figs. 1 to 31 & EP 961312 A2 & US 2003/0170990 A1 & KR 99088324 A & CN 1241803 A & TW 454346 A	1-7
Y	WO 2003/009386 A1 (Shin-Etsu Handotai Co., Ltd.), 30 January, 2003 (30.01.03), Full text; Fig. 1 & EP 1408551 A1 & US 2003/0181001 A1 & CN 1465104 A & KR 2004029292 A	2
A	Takao ABE et al., "Hariawase SOI Wafer no Kongo no Tenkai", Oyo Butsuri, Vol.66, No.11, 1997, pages 1220 to 1224	1-7
A	JP 03-091227 A (Nippon Soken, Inc.), 16 April, 1991 (16.04.91), Full text; Figs. 1 to 7 & US 5383993 A	1-7
A	JP 05-029183 A (Fuji Electric Co., Ltd.), 05 February, 1993 (05.02.93), Full text; Figs. 1 to 5 (Family: none)	1-7
A	JP 2001-244444 A (Tien-Hsi Lee), 07 September, 2001 (07.09.01), Full text; Figs. 1 to 10 & US 6486008 B1 & TW 452866 A	1-7

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- JP 2005374889 A **[0001]**
- JP 11145438 A **[0006]**