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(54) **Corrected DE translation: Differenzzeit-Digital-Wandler Corrected FR translation: Convertisseur temps différentiel-numérique**

(57) The invention relates to a time-to-digital converter comprising: a first input (300) for receiving a first digital signal (A) having a first pulse duration; a second input (310) for receiving a second digital signal (B) having a second pulse duration, said first digital signal (A) and said second digital signal (B) having an overlapping pulse duration and non-overlapping pulse durations; a delay chain comprising several pulse delaying components (330.1-330.n) for time measuring, and an output (351) for outputting a time signal representing the difference between the first pulse duration (TA) and the second pulse duration (TB). Further, the inventive time-to-digital converter is characterized in that said delay chain (330.1-330.n) measures both non-overlapping pulse durations, so that no duplication of the delay chain is necessary.

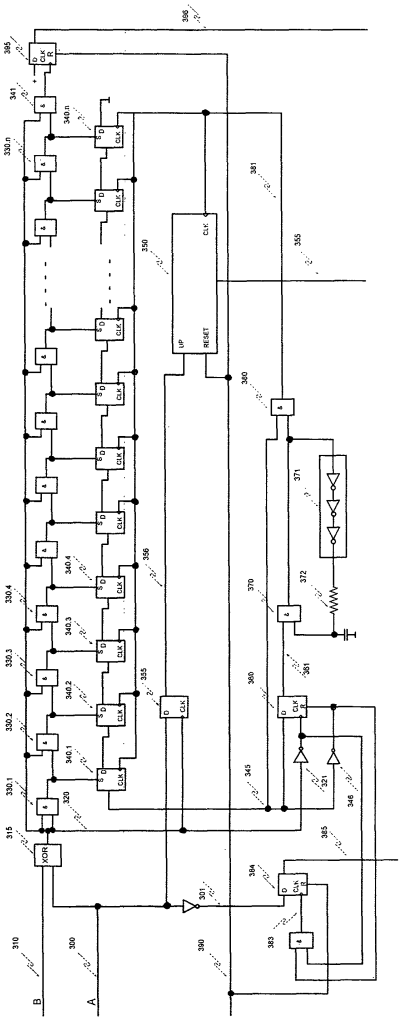

Fig 3

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Description

Field of the invention

[0001] The invention pertains to the field of electronic systems and circuits used for obtaining a digital representation of the duration of time intervals (time-to-digital converters) and to the field of frequency measurements and frequency generation.

Background of the invention

[0002] Citations:

1. J. Kalisz, Metrologica 41, 18 (2004).
2. R. Nutt, "Digital Time Intervalometer" Rev. Sci. Instrum. 39, 1342 (1968).
3. A.E. Stevens et al., "A Fast Low-Power Time-to-Voltage Converter for High Luminosity Collider Detectors", IEEE Trans. Nuclear Science 36, 517 (1989).
4. R. Szymanovsky and J. Kalisz, "Field Progammable Gate Array Time Counter with Two-stage Interpolation", Rev. Sci. Instr. 76, 045104 (2005).

[0003] Time-to-digital converters are used to measure the duration of short single electrical pulses or of short time intervals between consecutive events (1). The range of time durations to be measured is usually of the order of a few hundred nanoseconds or less. Time resolutions of tens of picoseconds can be obtained.

[0004] In experimental nuclear physics time-to-digital converters measure the time between the instant of creation of highly energetic elementary particles by an interaction in a particle accelerator and the instant of detection of secondary particles by ionization events at a particular position in a suitable detector. In time of flight mass spectrometric applications they measure the time taken by particles of different velocities to traverse a given distance. In short distance radar ranging applications they measure the time interval between emission of a signal and reception of the first reflected echo.

[0005] Longer time intervals are measured by counting clock periods. The beginning of the time interval and the beginning of the first counted clock period are in general not synchronous. The same is true for the end of the time interval and the end of the last counted period. Counting methods give only a truncated value for the duration of a time interval which is not equal to an exact integral number of periods of the clock. Their time resolution is limited by the duration of the clock period. Time-to-digital converters are therefore used to measure the short dead times between the beginning resp. the end of a long time interval and the beginning of the first resp. the end of the last clock period. The resolution of a time duration measurement can thereby be improved and will be limited only by the duration of the time element represented by the least significant bit of the time-to-digital conversion result. Frequency measuring apparatus based on counting clock periods combined with time-to-digital converters for improving the resolution are known as interpolating counters.

[0006] An early known technique for measuring the described dead times with high resolution consists in producing a stretched replica of the short interval to be measured and measuring the duration of the stretched version by counting periods of a reference frequency (2). Different methods for stretching a time interval to another interval of longer duration are known. In (2) a stretching factor of 256 was obtained by charging a capacitor via a small resistor during the short interval and discharging it via a much larger resistor for generating the longer interval. The charging and discharging times are in inverse proportion to the resistor values.

[0007] Charging a capacitor by a constant current during the interval to be measured and then measuring the voltage change on the capacitor by a analog to digital converter is a common time-to-digital converter technique also known as time to amplitude conversion (3). It is not limited to short time intervals.

[0008] A different approach uses a chain of delay elements and determines the number of delay elements traversed by a signal between the beginning of the time interval and the end of the interval. A common implementation of this approach is indicated in Fig. 1. It includes a number of bistable D-flipflops 120 which are initially in their reset states. The edge of a logic signal on an input line 100 marking the start of the interval traverses a series of gates 110, generating delayed replicas of the signal which are presented to the D-inputs of the D-flipflops 120. The logic values at these inputs are stored in the D-flipflops 120 by a common clock signal on a clock input 130 representing the end of the interval. Only the flipflops whose D-input has been reached by a delayed replica of the start signal will change their states. The number of flipflops that have changed their state is determined by a readout circuit 140, producing a digital representation 150 of the time elapsed between the start and the end of the interval. Several more elaborate examples of this approach have been described.

[0009] Delay chain based time-to-digital converters commonly use field programmable gate arrays (FPGA) or custom designed application specific integrated circuits (ASIC) for their hardware implementation (4). This allows for very short delay times (of the order of nanoseconds or below) of the individual delay elements and for good uniformity of their delays. The temperature dependence of the delay times can be compensated simultaneously for all delay elements on the common silicon chip by diverse techniques.

[0010] In known implementations of interpolating counters the dead times at the beginning and at the end of the counting interval are measured with separate time-to-digital converters although only the time difference between the two dead times is needed to correct the truncated frequency measurement. The accumulated delay

time deviations of the individual delay elements can be corrected from separate calibration tables before the final difference of their digital time representations is formed.

[0011] The present invention of a delay chain based differential time-to-digital converter avoids a duplication of delay chains for measuring the time difference between two consecutive non-overlappping time intervals. It uses a single delay chain and a single set of flipflops for recording the duration of the intervals. It allows for the correction of delay time deviations of the individual delay elements using a single calibration table.

[0012] Besides the application in interpolating counters there are other applications in which only the time duration difference of two consecutive non-overlapping time intervals are needed. As an example in the field of moving vehicle safety guarding one may consider the measurement of the velocity of a moving target relative to the ranging source by measuring the difference in duration of two consecutive radar ranging intervals.

[0013] In the field of radio communications it is often required to generate control signals for stabilizing the frequency of an high frequency oscillator relative to a fixed lower frequency reference oscillator. When the oscillation periods of the oscillators are not in an integral number relation rather complex solutions are required to solve this problem since it is not possible to simply phase-lock a unique integer submultiple of the higher frequency to the lower reference frequency. Current solutions for this problem use controlled switching between two or more different submultiples of the higher frequency and/or dithered phase comparisons. The present invention provides a more direct solution by measuring the difference between the duration of the period of the reference oscillator and a nearly equal duration of an appropriate constant multiple of periods of the oscillator to be stabilized, and using the deviation of the measured time difference from the desired time difference as the control signal for the controlled oscillator in a negative feedback loop.

Summary of the invention

[0014] Therefore, it is an object of the invention to provide a time-to-digital converter for the measurement of the time duration difference of two nearly equal time intervals without the need of duplicated delay chains.

[0015] The invention provides a solution to the problem of measuring the time duration difference between two overlapping time intervals with short time differences between their beginnings and endings, as well as to the problem of measuring the difference in duration of two non-coincident non-overlapping time intervals of short duration, separated by a time interval of much longer duration.

[0016] The measurement situations for which the present invention provides an innovative solution are depicted in figure 2. In this figure the two time intervals T_A and T_B, whose duration difference must be determined, are represented by two binary signals A and B whose beginnings and ends are not exactly coincident. The non-overlapping parts of A and B have short time durations t1 and t2. Four possible cases can be distinguished, in which (T_A - T_B) is given by (t1 + t2) resp. (t1 - t2), (-t1 - t2) or (-t1 + t2). Independent measurements of the short time intervals t1 and t2 must be made and combined in the appropriate manner to determine (T_A - T_B). The proposed invention uses a single delay-chain for measuring t1 as well as t2 and combines the outcomes of these measurements in an automatic manner to produce directly the desired result (T_A - T_B).

[0017] Time-to-digital converters deliver a digital representation of the time duration of a time interval between a start and a stop signal, usually in the submicrosecond range. In many applications, however, such as in frequency measurements by interpolating counters, the time quantity needed is the time difference between two such intervals. Known solutions to obtain this quantity use duplicate time-to-digital converters measuring separately the durations of the two intervals and obtain the required result by subtracting the outcome of the two measurements.

[0018] It is the object of the current invention to avoid this duplication and to generate the required quantity by reusing the same elements for generating a result which is a direct digital representation of the time duration difference of the measured intervals.

[0019] The invention avoids the afore-mentioned duplication of the delay chain by using the same delay chain for measuring both non-overlapping pulse durations. Therefore, the invention provides a time-to-digital converter comprising a first input for receiving a first digital signal having a first pulse duration and a second input for receiving a second digital signal having a second pulse duration, wherein the first digital signal and the second digital signal have an overlapping pulse duration and non-overlapping pulse durations as mentioned above. Further, the time-to-digital converter according to the invention comprises a delay chain having several pulse delaying components (e.g. AND-gates) for time measuring. Finally, the time-to-digital converter comprises an output for outputting a time signal representing the difference between the first pulse duration and the second pulse duration. The inventive time-to-digital converter is characterized in that the afore-mentioned delay chain measures both non-overlapping pulse durations, so that no duplication of the delay chain is necessary thereby avoiding the afore-mentioned disadvantages of the conventional time-to-digital converters.

[0020] In a preferred embodiment of the time-to-digital converter, an XOR-gate is provided connecting the first input and the second input of the time-to-digital converter to the input of the delay chain, so that the delay chain is exclusively measuring the non-overlapping pulse durations of the first digital signal and the second digital signal. The XOR-gate triggers the delay chain during the non-overlapping pulse durations only. However, the XOR-gate does not trigger the delay chain, when both digital

signals are inactive, i.e. low. Further, the XOR-gate does not trigger the delay chain during the overlapping pulse durations of both digital signals. Therefore, the delay chain does not measure the first pulse duration of the first digital signal and the second pulse duration of the second digital signal, but the non-overlapping pulse durations, so that no duplication of the delay chain is necessary.

[0021] It has already been mentioned above that the pulse delaying components of the delay chain are preferably AND-gates. However, the invention is not restricted to embodiments in which the pulse delaying components of the delay chain are AND-gates. For example, other types of logical gates can be used as pulse delaying components of the delay chain.

[0022] Further, the time-to-digital converter according to the invention preferably comprises a single shift register for buffering the time measured by the delay chain, wherein the shift register is being set by the delay chain in parallel. Therefore, the shift register is preferably a so-called parallel-in, serial-out (PISO) type shift register. In a preferred embodiment of the invention, the individual pulse delaying components (e.g. AND-gates) of the delay chain are connected to the individual cells (e.g. flip-flops) of the shift register, so that the shift register is parallely loaded by the delay chain.

[0023] It has already been mentioned above that the shift register preferably comprises several flip-flops, which are connected in series. However, the invention is not restricted to shift registers comprising several flip-flops. Instead, other conventional types of shift registers can be used in the framework of the invention.

[0024] Further, the time-to-digital converter of the invention preferably comprised a counter, which is fed by the shift register and which counts the output of the shift register. The counter is preferably an up/down counter, which counts either upwards or downwards depending on the output of the shift register.

[0025] Further, the time-to-digital converter of the invention preferably comprises a control circuit controlling the counting direction of the afore-mentioned counter depending on the first digital signal or the second digital signal, so that the counter calculates either

a) the sum of the non-overlapping time durations or
b) the difference of the non-overlapping time durations or
c) the inverted sum of the non-overlapping time durations or
d) the inverted difference of the non-overlapping time durations.

[0026] It has already been mentioned above that the time-to-digital converter preferably comprises a shift register, which is being loaded parallely by the delay chain. In an embodiment of the invention, the time-to-digital converter comprises several shift registers arranged in parallel, each being loaded by a corresponding section of the delay chain. For example, a first shift register is loaded by a first section of the delay chain, whereas a second shift register is loaded by a second section of the delay chain. In this embodiment, the time-to-digital converter preferably comprises a decoder, which is fed by the parallel shift registers. This embodiment comprising several parallel shift registers allows a faster readout.

[0027] Further, the afore-mentioned decoder is preferably implemented in hardware as a memory lookup table. Moreover, an adder/subtractor is preferably connected to the decoder, wherein the adder/subtractor either adds or subtracts the measured non-overlapping time durations.

[0028] In this embodiment, the time-to-digital converter preferably comprises an accumulator register being connected to the output of the adder/subtractor, wherein the accumulator register calculates a digital representation of the number of pulse delaying components of the delay chain being set during a measured time interval.

[0029] Further, the time-to-digital converter preferably comprises a correction circuit correcting deviations of the individual delay times of the components of the delay chain. The correction circuit preferably comprises a lookup table in which the delay deviations of the individual components of the delay chain are stored. Further, an adder/subtractor is preferably provided for adding or subtracting the stored deviations from the measured values.

[0030] In an embodiment of the invention, the time-to-digital converter comprises a lookup table in which the accumulated delay time of the components of the delay chain is stored and which is addressed by the decoder. In this embodiment, the time-to-digital converter preferably comprises a first output register storing the first non-overlapping pulse duration and a second output register storing the second non-overlapping pulse duration. Further, an adder/subtractor is preferably provided for either adding or subtracting the first non-overlapping pulse duration and the second non-overlapping pulse duration.

[0031] In the afore-mentioned embodiments of the invention, the time-to-digital converter preferably comprises an overflow detection circuit detecting an overflow of the delay chain. Therefore, the overflow detection circuit preferably comprises a flip-flop connected to the end of the delay chain, so that the flip-flop of the overflow detection circuit is set, when a pulse has travelled through the entire delay chain.

[0032] Finally, it has to be mentioned that the time-to-digital converter can be implemented in hardware as a field programmable gate array (FPGA) or as an application specific integrated circuit (ASIC). However, the invention is not restricted to the afore-mentioned hardware implementations of the time-to-digital converter.

Short description of drawings

[0033]

Figure 1 shows the measuring principle of a time-to-

digital converter based on a chain of delay elements.

Figure 2 shows the measurement situations for which the present invention provides an efficient new solution.

Figure 3 shows the schematic diagram of the preferred embodiment of the delay chain and of the delay chain readout mechanism for obtaining the outcome of interval comparisons as exemplified in figure 2 by a differential time-to-digital converter according to the current invention.

Figure 4 shows the schematic diagram of an alternate embodiment with reduced readout time.

Figure 5 shows the mapping table between the input lines and the output lines of the decoder used in figure 4.

Figure 6 shows the schematic diagram for obtaining the accumulated delay time deviations by the traversed delay elements in the delay chain from a single correction table, or for obtaining the desired differential time difference directly as the output of the preferred embodiment with the use of a single table of individual delay values.

Figure 7 shows how to obtain the accumulated delay deviations or the direct differential time representation of the compared time intervals with embodiments that achieve short readout times.

Figure 8 shows an application of the present invention using an interpolating counter with a differential-timeto-digital converter according to the one of the described embodiments.

Detailed description of the drawings

[0034] The signal flow in a preferred embodiment of the current invention is presented by the schematic diagram in figure 3. Two input signal A and B, corresponding to the signals A and B of figure 2, are presented on input lines 300 resp. 310. It is assumed for this embodiment that the total duration of the input signals A and B is much longer that the short durations of their non-overlapping parts.

[0035] An EXCLUSIVE-OR gate 315, fed by the input lines 300 and 310, generates a signal on a line 320 which is active during a first time interval of duration t1, started by the rising edge of the earliest of one of the input signals A or B and ended by the rising edge of the later of the input signals A or B.

[0036] The signal generated by the EXCLUSIVE-OR gate 315 on the line 320 is again active for a second time interval t2 which begins at the falling edge of the earliest ending of one of the input signals A or B and ends with the falling edge of the remaining input signal A or B. There will thus be two active periods of the output of the EXCLUSIVE-OR gate 315, which will be distinguished in the following description as the first measured time interval or the interval t1, and the second measured time interval or the interval t2.

[0037] The line 320 is used to simultaneously enable all of two-input AND-gates 330.1, 330.2, 330.2,...,330.n of a delay chain via one of the AND-inputs. The outputs of the AND-gates 330.1,...,330.n are connected to the direct SET-inputs of a corresponding chain of D-flipflops 340.1,...,340.n. Initially all flipflops all in the inactive state. The line 320 is connected also to the other input of the first AND-gate 330.1, which thereby generates at its output a first delayed replica of the signal on the line 320. The output of the AND-gate 330.1 feeds the remaining AND-input of the second AND-gate 330.2, which, if still enabled by the signal on the line 320, produces an additionally delayed second replica. The generation of delayed replicas will continue along the daisy-chained AND-gates as long as the enabling signal on the line 320 remains active. It will stop when the signal on the line 320 becomes inactive. This blocks the propagation of the last produced replica at one of the AND-gates in the chain and also inactivates the outputs of the previous AND-gates. The number of AND-gates that had activated their outputs up to this time is given by the duration of the signal on the line 320 divided by the propagation delay of a single AND-gate. The activated signals at the outputs of these AND-gates have directly set a corresponding flip-flop in the chain of the D-flipflops 340.1, 340.2,..., 340.n via their direct set input. The number of consecutive flipflops that have switched to their set states is a measure of the time duration of the signal on the line 320, which is active only during the time intervals t1 and t2.

[0038] Since for the embodiment of the invention shown in figure 3 it has been assumed that a sufficiently long time period elapses between the end of t1 and the beginning of t2, a simple readout mechanism for determining the number of activated flipflops during t1 and for resetting them to the inactive state before the beginning of t2 is implemented. The D-flipflops 340.1, 340.2,..., 340.n are connected as a shift register. The shift register input begins at the D-input of the D-flipflop 340.n, which is clocked into the inactive state by the common clock input for all flipflops of the chain. A shift output 345 is taken from the first D-flipflop 340.1. The number of clock transitions needed to empty the shift register is counted by an up-down counter 350. The counting direction is determined by the signal on a line 356, which is connected to the up/down selector input of the up/down counter 350. The generation of this signal will be described below.

[0039] The embodiment shown in figure 3 creates an internal clock signal to drive the shift register and the

counter. The clock signal shall only be active after the measuring cycle of each measured time interval and it shall only be active as long as there are activated flipflops in the shift register. This is achieved by the configuration of circuit elements comprising a D-flipflop 360, an AND-gate 370, inverting gates 371, an RC-delay 372 and an AND-gate 380. The D-flipflop 360 is driven to the reset state by an inverting gate 346 whenever the shift output 345 of the last shift register D-flipflop 340.1 is not set. The clock input of the D-flipflop 360 is connected via an inverter 321 to the line 320. The D-flipflop 360 will be set at the end of a measured time interval by the falling edge of the signal on the line 320 only if the signal on its D-input, connected to the shift output 345, is active. This is the case if one or more consecutive flipflops (starting with the D-flipflop 340.1) have been set by delayed replicas of the rising edge on the line 320. If the D-flipflop 360 is activated in this way at the end of a measuring interval, its output on a line 361 enables a free running oscillator formed by the AND-gate 370, the RC-delay 372 and an odd number of the inverting gates 371. The AND-gate 380 passes the clock output as long as the output of the shift register D-flipflop 340.1 remains set. The passed clock signal 381 shifts the content of the shift register to its output at the D-flipflop 340.1 and simultaneously increments or decrements the content of the up-down counter 350. The running oscillator is stopped when the signal on the shift output 345 of the D-flipflop 340.1 is or becomes inactive. The number of clock pulses on the output of the AND-gate 380 will be equal to the number of activated flipflops in the shift register. At the end of two consecutive measuring intervals and the corresponding readouts of the shift register the counter presents at its outputs the measured positive or negative difference or sum of the number of delay elements traversed during the measured intervals, depending on the value of the up/down signal on the line 356.

[0040] The signal on the input line 300, which is either active or inactive during the active state of the EXLUSIVE OR output on the line 320, selects the counting direction. The state of the signal on the input line 300 is sampled by a D-flipflop 355, which is clocked at the beginning of the first as well as of the second measured time interval by the rising edge of the signal on the line 320. If the signal on the input line 300 is active at the sampling instant, the active output of the D-flipflop 355 indicates that the input signal A on the input line 300 is active earlier than the input signal B on the input line 310 at the beginning of said intervals, or that the input signal A is still active after the input signal B became inactive at the end of said intervals. In this case the number of traversed delay elements must be counted positive. When the inactive state of the input line 300 is sampled, the number of traversed delay elements must be counted negative. The counting direction is indicated by the output state of the sampling D-flipflop 355 on the line 356, which is connected to the up/down selector or the up/down counter 350.

[0041] The content of the up-down counter 350 with at least (m+2)-bit counting range is the desired digital representation of the time duration difference of the two consecutive non-overlapping time intervals, separated by a time period sufficiently long to empty the shift register. $M=\log_2 n$ is the number of bits required for the binary representation of the number n of delay elements in the chain. One additional bit is required because the counter must be able to represent the sum as well as the difference of the durations of t1 and t2. One additional bit is required for the sign of the result.

[0042] A rising signal on line 385 indicates that the measured result is available at the output lines. At this time all other circuits elements have been returned to their original state. The line 385 is the output of a D-flipflop 384 which is clocked to by the rising edge of the signal on a line 383.

[0043] This occurs after the second measured time interval when the first inactive bit of the content of the shift register has been shifted out, or, if none of the flipflops of the shift register were set during that interval, it occurs at the end of the second time interval. The D-flipflop 384 samples the inverted state of the input signal A on the input line 300 via an inverter 301, therefore it will not be clocked to its active state between interval t1 and interval t2 because the input signal A is then active.

[0044] The delay chain of the AND-gates 330.1 to 330.n is extended by one more AND-gate 341. If the AND-gate 341 is still enabled via its connection to the line 320 when its other input is reached by a last delayed replica of the rising edge on the line 320, an overflow of the delay chain has occurred. The output of the AND-gate 341 then sets a flipflop 395, which is not part of the shift register chain but serves as an overflow error indicator by presenting an active error flag signal on a line 396, which can be tested when the result of a measurement is read by readout circuitry not shown in the diagram of figure 3.

[0045] After reading the content of the result counter by other circuitry not shown in figure 3, the up/down counter 350, the error indicator flipflop 395 and the ned of measurement indicator 384 can be reset by a RESET input line 390. The differential time duration of the two consecutive intervals is obtained by multiplying the measured count number by the average delay time of a delaying AND-gate.

[0046] The embodiment of the invention presented in figure 3 is very efficient in its number of hardware components. It can easily be realized by discrete circuit elements as well as by implementations in a FPGA or ASIC.

[0047] There may be applications in which the assumption of a silent period between the compared intervals, of sufficiently long duration for reading out an n-element shift register, is not fulfilled. Figure 4 shows an example of alternate embodiments that shortens the time required for reading out the number of flipflops set by the delay chain. In this example the readout time is reduced by a factor four as compared to the preferred embodiment

shown in figure 3.

[0048] Instead of connecting the flipflops to form a single long shift register as in the previous embodiment they are connected to form four parallel shift registers. This is done by feeding the D-input of flipflop 440.1 from the output of flipflop 440.5, the D-input of flipflop 440.2 from the output of flipflop 440.6 and so on: the input of flipflop 440.x is connected to the output of 440.x+4. There are now four parallel shift registers whose outputs are the outputs of the flipflops 440.1 resp. 440.2, 440.3 and 440.4. Circuit element 450 is a 4-to-3 decoder, producing at its three output lines the digital representation of the number of input lines that are set.

[0049] Since only consecutively numbered flipflops may be set by the delay chain, the number of possible combinations of active inputs to the decoder is limited. The mapping of input lines to output lines for the decoder 450 is shown in figure 5. Such a mapping is easily obtained by known circuit combinations (priority encoders) or it can be implemented as a fixed 3-bit memory lookup table addressed by the 4 input lines. Instead of an up-down counter the embodiment in figure 4 uses an adder/subtractor 460 and a clocked accumulator register 470 for obtaining the required digital representation of the number of flipflops set during a measured interval.

[0050] The outputs of the decoder 450 for the first measured interval are added or subtracted into the accumulator register 470 under control of the signal on line 456, which corresponds to the line 356 in figure 3. With a larger number of parallel shift registers and a wider decoder the readout times can be further reduced. It is even possible to read the entire set of flipflops by a single clock pulse by using an n-bit wide lookup table.

[0051] Figure 6 shows how the preferred embodiment of figure 3 can be enhanced by a mechanism that accounts for the deviations of the delay times of the individual delay elements from the average value. This mechanism generates a digital representation of the correction value that must be added to the differential time calculated from the differential number of flipflops activated in the compared intervals.

[0052] The signed individual deviations from the average value of the time delay of the AND-gates 630.1, 630.2,...,630.n of the delay chain from figure 3 are stored in lookup table 600 in figure 6. Said delay deviations are stored at consecutive binary addresses beginning at address 0 of lookup table 600. The signals on the m address lines of lookup table 600 are the output signals of an m-bit binary counter 650, which counts the number of clock pulses produced by a clock signal generator 660 to 680 after each single measured interval. Contrary to the up-down counter 350 in figure 3, the counter 650 counts only upwards, and it is reset to zero after the last counted clock signal transition by the signal on line 646. The configuration of the clock signal generator 660 to 680 is the same as the circuit elements 360 to 380 in figure 3.

[0053] The values of delay deviations appearing at the output lines of lookup table 600 appear at the A input lines of the adder/subtractor 610. The B input lines of the adder/subtractor 610 are supplied by the outputs of a clocked accumulator register 620. During the readout of the number of traversed delay elements by counting the number of clock pulses from the clock circuit, the counter 650 supplies the address of the deviation value for the next delay element in the chain that may have been traversed. The adder/subtractor adds resp. subtracts this value to resp. from the already accumulated sum of deviations. Only if said delay element was traversed will there be a clock pulse that saves the result of the addition resp. subtraction in the accumulator register. The Add/Subtract mode of the adder/subtractor 610 is controlled by the signal on a line 656, which is identical to the line 356 in figure 3. This signal is set active when the beginning of signal A on line 600 precedes the beginning of signal B on line 610, or if the end of signal A follows the end of signal B. It is inactive in the opposite cases. When he shift register readout of the two measured consecutive short time intervals is complete, accumulator register output lines 625 carry the digital representation of the total accumulated value of delay time corrections.

[0054] The configuration shown in figure 6 also applies to an embodiment in which the lookup table 600 contains the values of the individual time delays of the consecutive AND-gates in the delaying chain instead of their deviations from their common average value. At the expense of a wider bit-width for the lookup table 600, the adder/subtractor 610 and the accumulator register 620 of such an embodiment produces at the output lines 625 of the accumulator directly the digital representation of the differential time duration of the compared time intervals. The up/down counter 350 of figure 3 is superfluous in the case.

[0055] The embodiment using several parallel shift register for faster readout shown in figure 6 can also be enhanced to allow the correction for the deviations of the delay elements from their common average values or for giving directly the correct total differential delay time. An appropriate combination of circuit elements to achieve this is shown in figure 7.

[0056] With parallel shift registers a lookup table 700 in figure 7 does not store the individual delay time deviations or individual total delay times of individual delay elements. Instead, it stores, beginning at address 0, the total accumulated delay after traversion of 1, 2, 3,..., n consecutive delay elements. The address into the lookup table is supplied on output lines 775 of an accumulator register 770 whose content, initially zero, is incremented by an adder 760 at each clock pulse by the number represented by the signals on the output lines of an encoder 750, which is identical with the decoder 450 of figure 4. The addressed value in the lookup table is saved in a register 751 by a clock pulse on a line 752 when the readout content of the parallel shift registers refers to delay elements traversed during the first measured time interval. It is saved in a register 753 by a clock pulse on a line 754 when the content of the parallel shift registers

refers to delay elements traversed during the second time interval. The clock signals for the registers 751 resp. 753 are selected by a multiplexer 757, controlled by the signal on line 700. Since the content of the registers 751 resp. 753 is replaced by every clock signal, they contain, after the last clock pulse, the accumulated delay deviation of the traversed delay elements during the first resp. the second measured time interval. The contents of the register 753 is added to or subtracted from the content of the register 751 by the adder 760 under control of the signal on a line 756, equivalent to the line 356 in figure 3. The output lines of the adder 760 represent the accumulated corrections for delay elements that were traversed during the first time interval minus the corrections for the delay elements traversed during the second time interval. If the lookup table 700 contains the value of total delay accumulated after traversing the first, second, third,...,n-th delay element, the output lines of the adder 760 directly show the digital time representation of the time duration difference of the two measured consecutive time intervals. Before the beginning of a new differential measurement the content of the registers 770, 751 and 753 must be set to zero by an external reset signal on a line 790.

[0057] As an example of an application of the present inventio figure 8 shows how the enhanced time resolution of the differential-time-to-digital converter can be used in an instrument for measuring the frequency of a parameter-controlled oscillator with high accuracy in a short time. The block diagram of the instrument shown in figure 8 includes a stable crystal reference clock oscillator 800 that continuously generates f_{ref} clock pulses per second (called timing-clock pulses in the following) on a line 802. The frequency f_{par} of a parameter controlled oscillator 840 may be controlled by an internal parameter, e.g. by the mass dependent resonance frequency of a quartz crystal in a feedback-driven microbalance, or by a external parameter, e.g. the voltage applied to the voltage controlled oscillator of a voltage to frequency converter. The parameter-controlled oscillator 840 continuously generates clock pulses per second (called counting-clock pulses in the following) on a line 842. In this example it is assumed that the duration of one period of the frequency f_{par} of the parameter-controlled oscillator 840 is shorter than the total delay length of the n delay elements of a differential-time-to-digital converter 870.

[0058] Figure 8 also shows a set of synchronizing flipflops 805, 810, 815 for starting and ending a timing-interval signal A on a line 830 synchronously with a first resp. a last rising timing clock transition on the line 802, and a timing counter 820 for counting a predefined number of said timing clock transitions. The timing counter 820 has an input CT/LD connected to the line 830. As long as the timing-interval signal on this line is inactive, the timing counter 820 is preloaded from a register 822 with the predefined number m_A of required counts. When the timing-interval signal is active it enables down-counting this number on consecutive rising transitions of timing clock pulses on the line 802. The timing counter 820 has an output STOP connected to line 824 which becomes active when the content of the counter becomes the number one. When the stop signal on line 824 and the timing-interval signal on the line 830 are both active, AND-gate 826 activates the signal on a line 828, thereby resetting the flip-flops 805 and 810. The next timing-clock pulse on the line 802 will count the predefined number m_A down to zero and simultaneously end the timing-interval signal because the D input of the flipflop 815 has become inactive. This synchronizer and counter arrangement garantees that the duration of the timing-interval signal is exactly equal to m_A clock periods of the reference clock oscillator 800. A pre-selected number m_A can be set in the register 822 by external control signals not shown in figure 8.

[0059] Figure 8 shows an inverter 850 and a flipflop 855 for synchronizing the beginning and the end of a counting-interval signal B on a line 835, synchronously with falling transitions of the counting-clock pulses generated on the line 842 by the parameter-controlled oscillator 840.

[0060] The timing-interval signal on the line 830 starts with the second rising transition of the timing-clock signal following an externally applied active transition of the signal on line 801. The timing-interval signal is fed to the differential-time-to-digital converter 870 where it is identical to the input signal A of figure 3. This signal starts the measuring cycle.

[0061] The counting-interval B generated by the flipflop 855 starts with the first falling transition of a counting-clock pulse on the line 842 following the beginning of the timing-interval signal A and it ends with the first falling transition on the line 842 following the end of the timing-interval A. The rising transitions of counting-clock pulses on the line 842 that fall within the counting-interval are enabled by an AND-gate 858 and counted by a binary counter represented by the counter 860. Using alternate transitions of the counting-clock pulses for synchronization and counting prevents loss of counting pulses in case of metastability of the flipflop 855 when the starting the timing-interval on the line 830, sensed at the D-input, coincides with the rising clock transition on a line 852 at the clock input of the flipflop 855. After the end of the counting-interval B the number m_B of counting-clock pulses counted within the interval is available at output lines 865 of the counter 860.

[0062] The timing-interval A represents a predefined number m_A of timing-clock periods of known period duration $t_A = 1/f_{ref}$. The counting-interval B represents a counted number m_B of counting-clock periods with period duration $t_B = 1/f_{par}$. Interval B starts after the start of interval A and ends after the end of interval A. The difference in time duration of these intervals is at most one period of the frequency of the parameter-controlled oscillator 840. The time duration of this difference is measured by the differential-time-to-digital converter 870, whose inputs are the timing-interval signal A on the line

830 and counting-interval signal B on the line 835. The digital representation of the duration of the fractional part of the number of counting-clock periods that fits in the predefined number of timing-clock periods, measured in units of the time delay of the delay elements, is available at output lines 875 (corresponding to lines 355 of figure 3) of the differential-time-to-digital converter 870. The end of the measuring cycle is indicated when an output 885 of the differential-time-to-digital converter 870 becomes activated. The signal on the output 885 is identical with the signal on line 385 of figure 3. The signals on lines 890 and 869 correspond to the external reset signal on the reset input line 390 resp. the overflow signal on the line 396 of figure 3.

[0063] The frequency f_B of the parameter-dependent oscillator is the obtained using the equation

$$f_B = f_A \ (m_B/(m_A + N_{TDC} f_A t_d)$$

where f_A is the frequency of the reference oscillator, m_B the number of parameter-dependent oscillator clock pulses counted by a counter 860, m_A the number of reference oscillator clock pulses defining the timing-interval duration, N_{TDC} the (signed) output number of the differential-time-to-digital converter 870 and t_d the duration of a single delay element in the in the delay chain of the differential-time-to-digital converter.

[0064] The advantage of using an interpolating counter for the frequency measurement of a parameter-controlled oscillator is the enhanced accuracy of the measurement result, which is available in a shorter time than with a straight counter. This is an important advantage when the frequency of the parameter-dependent oscillator must be monitored continuously and when the frequency-controlling parameter is time dependent. The relative error of a measurement of an unknown frequency using a simple counter (in which the duration of the counting interval T_B is not measured with a differential-time-to-digital converter, but assumed to be equal to that of the timing-interval T_A), is of the order of $\pm\tau_B/T_A$, where τ_B is the duration of one period of the unknown frequency. In contrast, the relative error of the measurement with an interpolating counter using a differential-time-to-digital converter, is of the order of $\pm t_d/T_A$, where t_d is the time delay of a single delay element of the delay chain of the differential-time-to-digital converter. For frequency measurements in the range of several MHz more than hunderdfold improvement in measurement accuracy using the same measurement time can be achieved.

[0065] The foregoing detailed description of the preferred and other embodiments of the present invention has been presented for the purpose of illustration. It is not intended to be exhaustive or to limit the invention to the precise form of this preferred embodiment or to other exemplary embodiments disclosed. Obviously, replacement of the assumed active logic levels of the described signals by alternate logic levels and corresponding replacements of described functional elements, e.g. replacement of AND-gates by OR gates, or other modifications and variations such as the replacement of a lookup table by combinatorial logic circuitry etc. will be apparent to practitioners skilled in this art. The embodiments have been chosen to best explain the invention and some of its practical applications.

List of reference numerals

[0066]

100	Input line
110	Gates
120	D-flipflops
130	Clock input
140	Readout circuit
150	Digital representation of the time
300	Input line
301	Inverter
310	Input line
315	EXCLUSIVE-OR-gate
320	Line
321	Inverter
330.1,...,330.n	AND-gates
340.1,...,340.n	D-flipflops
341	AND-gate
345	Shift output
346	Inverting gate
350	Up/down counter
355	D-flipflop
356	Line
360	D-flipflop
361	Line
370	AND-gate
371	Inverting gates
372	RC-delay
380	AND-gate
381	Clock signal
383	Line
384	D-flipflop
385	Line
390	Reset input line
395	Flipflop
396	Line
400	Input line
410	Input line
415	EXCLUSIVE-OR-gate
420	Line
421	Inverter
440.1,...,440.n	D-flipflops
441	AND-gate
446	Inverting gate
450	Decoder
455	D-flipflop

456	Line
460	Adder/subtracter
470	Accumulator register
471	Inverting gates
472	RC-delay
484	D-flipflop
495	Flipflop
496	Line
600	Lookup table
610	Adder/subtracter
615	EXCLUSIVE-OR-gate
620	Accumulator register
621	Inverter
625	Output lines
630.1,...,-630.n	AND-gates
640.1,...,640.n	D-flipflops
641	AND-gate
646	Line
650	Counter
655	D-flipflop
656	Line
670	Accumulator register
684	D-flipflop
695	Flipflop
700	Input line
702	Adder/subtractor
703	Register
715	EXCLUSIVE-OR-gate
721	Inverter
730.1,...,730.n	AND-gates
740.1,...,740.n	D-flipflops
741	AND-gate
746	Inverting gate
750	Encoder
751	Register
753	Register
754	Line
755	D-flipflop
756	Line
757	Multiplexer
760	Adder
770	Accumulator register
771	Inverting gates
772	RC-delay
775	Output lines
780	AND-gate
790	Line
795	D-flipflop
800	Clock oscillator
801	Line
802	Line
805	Flipflop
810	Flipflop
815	Flipflop
820	Timing counter
822	Register
824	Line
826	AND-gate
828	Line
830	Line
835	Line
840	Parameter controlled oscillator
842	Line
850	Flipflop
852	Line
855	Flipflop
858	AND-gate
860	Counter
865	Output lines
869	Line
870	Differential time-to-digital converter
875	Output lines
885	Output of the differential time-to-digital converter
890	Line
A	input signal
B	input signal
TA	Pulse duration of the input signal A
TB	Pulse duration of the input signal B

Claims

1. Time-to-digital converter comprising:

a) a first input (300) for receiving a first digital signal (A) having a first pulse duration (TA),

b) a second input (310) for receiving a second digital signal (B) having a second pulse duration (TB), said first digital signal (A) and said second digital signal (B) having an overlapping pulse duration ($t_{OVERLAP}$) and non-overlapping pulse durations (t1, t2),

c) a delay chain comprising several pulse delaying components (330.1-330.n) for time measuring, and

d) an output (351) for outputting a time signal representing the difference between the first pulse duration (TA) and the second pulse duration (TB)

characterized in that

e) said delay chain (330.1-330.n) measures both non-overlapping pulse durations (t1, t2).

2. Time-to-digital converter according to claim 1, **characterized by** an XOR-gate (315) connecting said first input (300) and said second input (310) to said delay chain, so that the delay chain is exclusively measuring the non-overlapping pulse durations (t1, t2) of the first digital signal (A) and the second digital signal (B).

3. Time-to-digital converter according to one of the preceding claims, **characterized in that** said pulse delaying components (330.1-330.n) of said delay chain are logical gates.

4. Time-to-digital converter according to claim 3, **characterized in that** said logical gates of said delay chain are AND-gates.

5. Time-to-digital converter according to one of the preceding claims, **characterized by** a single shift register (340.1-340.n) for buffering the time measured by said delay chain (330.1-330.n), said shift register (340.1-340.n) being set by said delay chain (330.1-330.n) in parallel.

6. Time-to-digital converter according to claim 5, **characterized by** a counter (350) being fed by said shift register (340.1-340.n) and counting the output of the shift register (340.1-340.n).

7. Time-to-digital converter according to claim 6, **characterized in that** said counter (350) is an up/down counter counting either upwards or downwards.

8. Time-to-digital converter according to claim 7, **characterized by** a control circuit (355) controlling the counting direction of the counter (350) depending on the first digital signal (A) or the second digital signal (B), so that the counter (350) calculates either

   a) the sum (t1+t2) of the non-overlapping time durations (t1, t2) or
   b) the difference (t1-t2) of the non-overlapping time durations (t1, t2) or
   c) the inverted sum (-t1-t2) of the non-overlapping time durations (t1, t2).
   d) the inverted difference (-t1+t2) of the non-overlapping time durations (t1, t2) or

9. Time-to-digital converter according to any of claims 1 to 4, **characterized by**

   a) several shift registers (440.1-440.n) arranged in parallel each being set by a corresponding section of the delay chain; and
   b) a decoder (450) being fed by said parallel shift registers (440.1-440.n).

10. Time-to-digital converter according to claim 9, **characterized in that** the decoder (450) is implemented in hardware as a memory lookup table.

11. Time-to-digital converter according to any of claims 9 to 10, **characterized by** an adder/subtractor (460) connected to said decoder (450) and either adding or subtracting the measured non-overlapping time durations (t1, t2).

12. Time-to-digital converter according to claim 11, **characterized by** a control circuit controlling the calculation type of said adder/subtractor depending on the first digital signal (A) or the second digital signal (B), so that the adder/subtractor calculates either

   a) the sum (t1+t2) of the non-overlapping time durations (t1, t2) or
   b) the difference (t1-t2) of the non-overlapping time durations (t1, t2) or
   c) the inverted sum (-t1-t2) of the non-overlapping time durations (t1, t2).
   d) the inverted difference (-t1+t2) of the non-overlapping durations (t1, t2) or

13. Time-to-digital converter according to claim 11 or 12, **characterized by** an accumulator register (470) being connected to the output of the adder/subtractor (460) and calculating a digital representation of the number of pulse delaying components of the delay chain set during a measured time interval.

14. Time-to-digital converter according to any of the preceding claims, **characterized by** a correction circuit correcting deviations of the individual delay times of the components of the delay chain.

15. Time-to-digital converter according to claim 14, **characterized in that** said correction circuit comprises a lookup table (600) in which the delay deviations of the individual components of the delay chain are stored.

16. Time-to-digital converter according to claim 15, **characterized by** an adder/subtractor (610) adding or subtracting the stored deviations from the measured values.

17. Time-to-digital converter according to any of claims 9 to 16, **characterized by** a lookup table (700) in which the accumulated delay time of the components of the delay chain is stored and which is addressed by the decoder.

18. Time-to-digital converter according to claim 17, **characterized by**

   a) a first output register (751) storing the first non-overlapping pulse duration (t1);
   b) a second output register (753) storing the second non-overlapping pulse duration (t2);
   c) an adder/subtractor (760) for either adding or subtracting the first non-overlapping pulse duration (t1) and the second non-overlapping pulse duration (t2).

19. Time-to-digital converter according to any of claims 5 to 18, **characterized in that** said shift register comprises several flip-flops being connected in series.

20. Time-to-digital converter according to one of the preceding claims, **characterized by** an overflow detec-

tion circuit (341, 395) detecting an overflow of the delay chain (330.1-330.n).

21. Time-to-digital converter according to claim 20, **characterized in that** said overflow detection circuit (341, 395) comprises a flip-flop (395) connected to the end of the delay chain (330.1-330.n).

22. Time-to-digital converter according to one of the preceding claims, **characterized by** a hardware implementation in

a) a field programmable gate array or
b) an application specific integrated circuit.

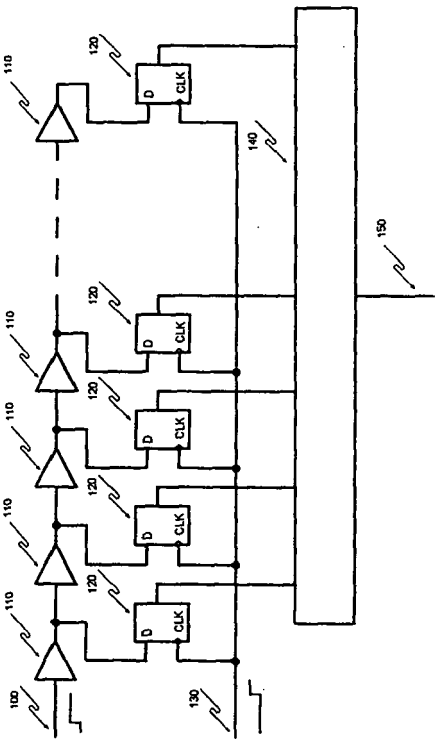


Fig. 1

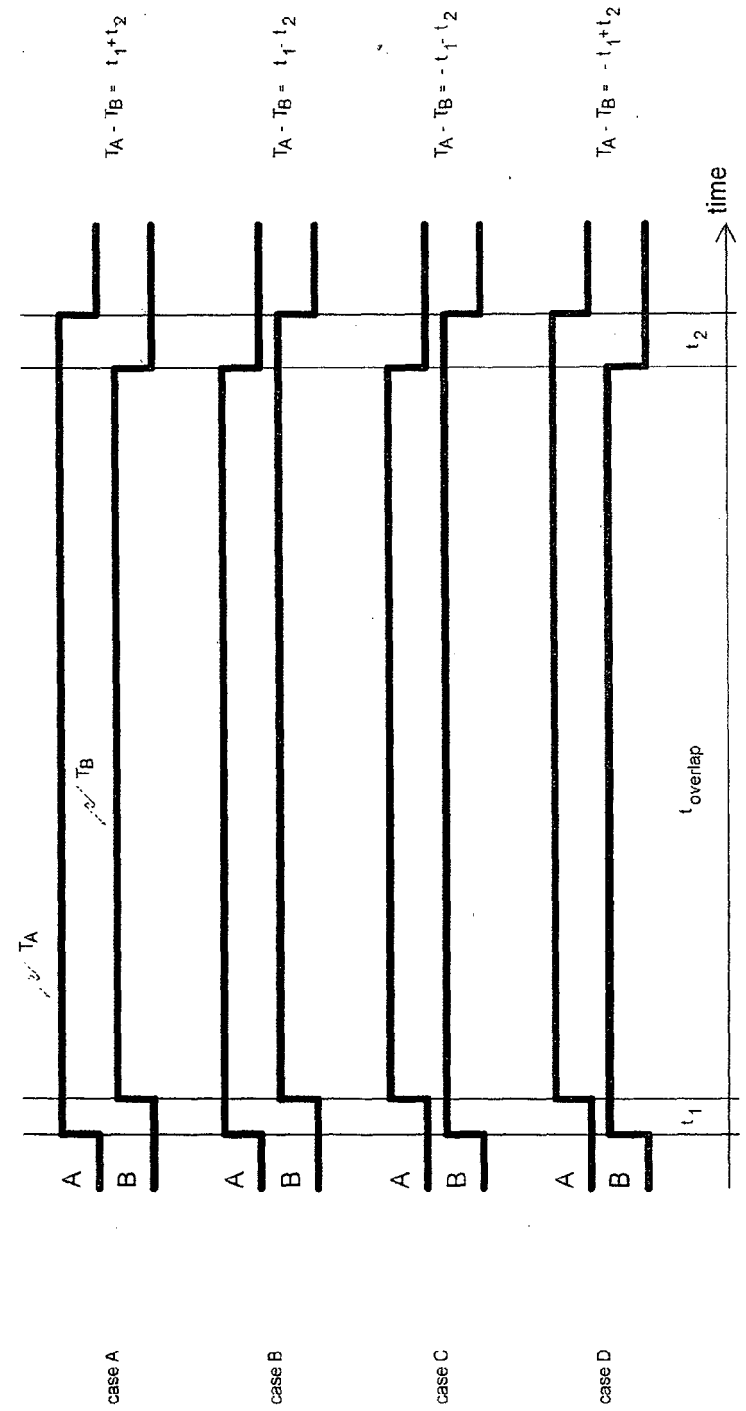

$T_A - T_B = t_1 + t_2$
$T_A - T_B = t_1 - t_2$
$T_A - T_B = -t_1 - t_2$
$T_A - T_B = -t_1 + t_2$
time
t_2
$t_{overlap}$
t_1
T_A
T_B
A
B
case A
case B
case C
case D

Fig. 2

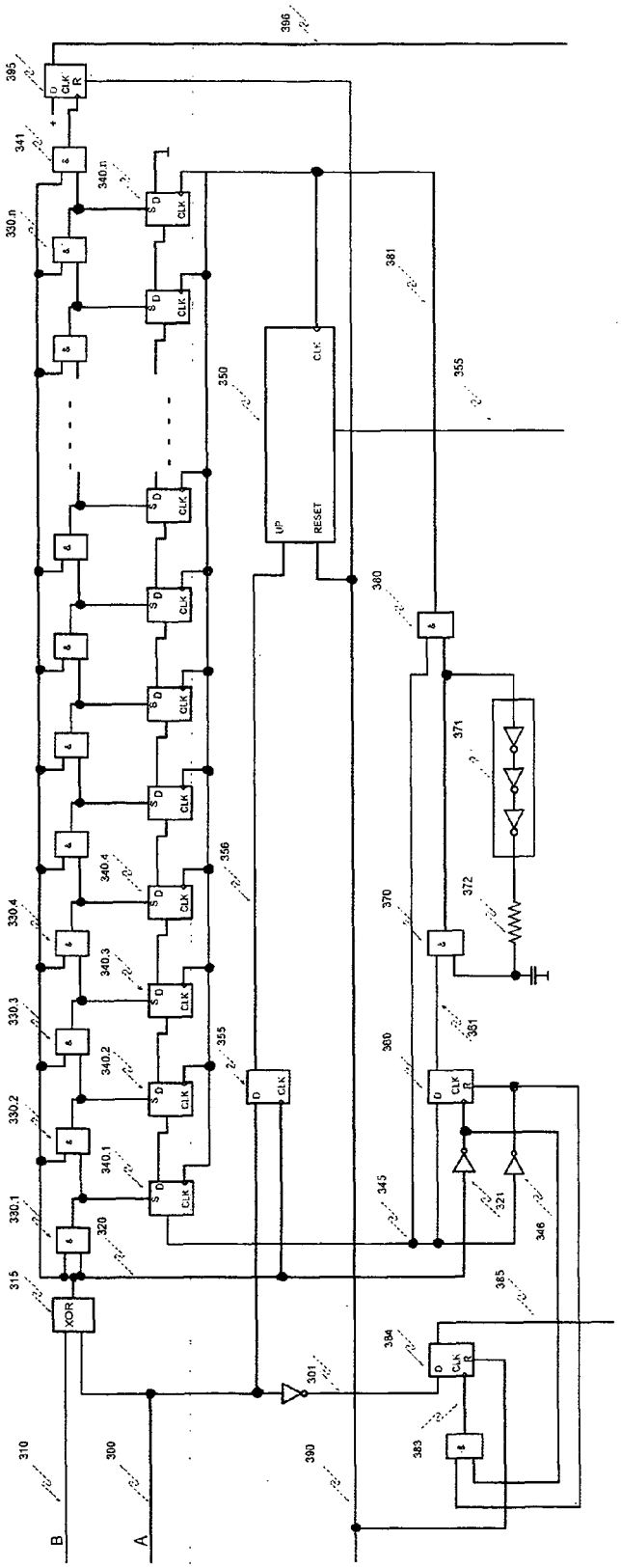
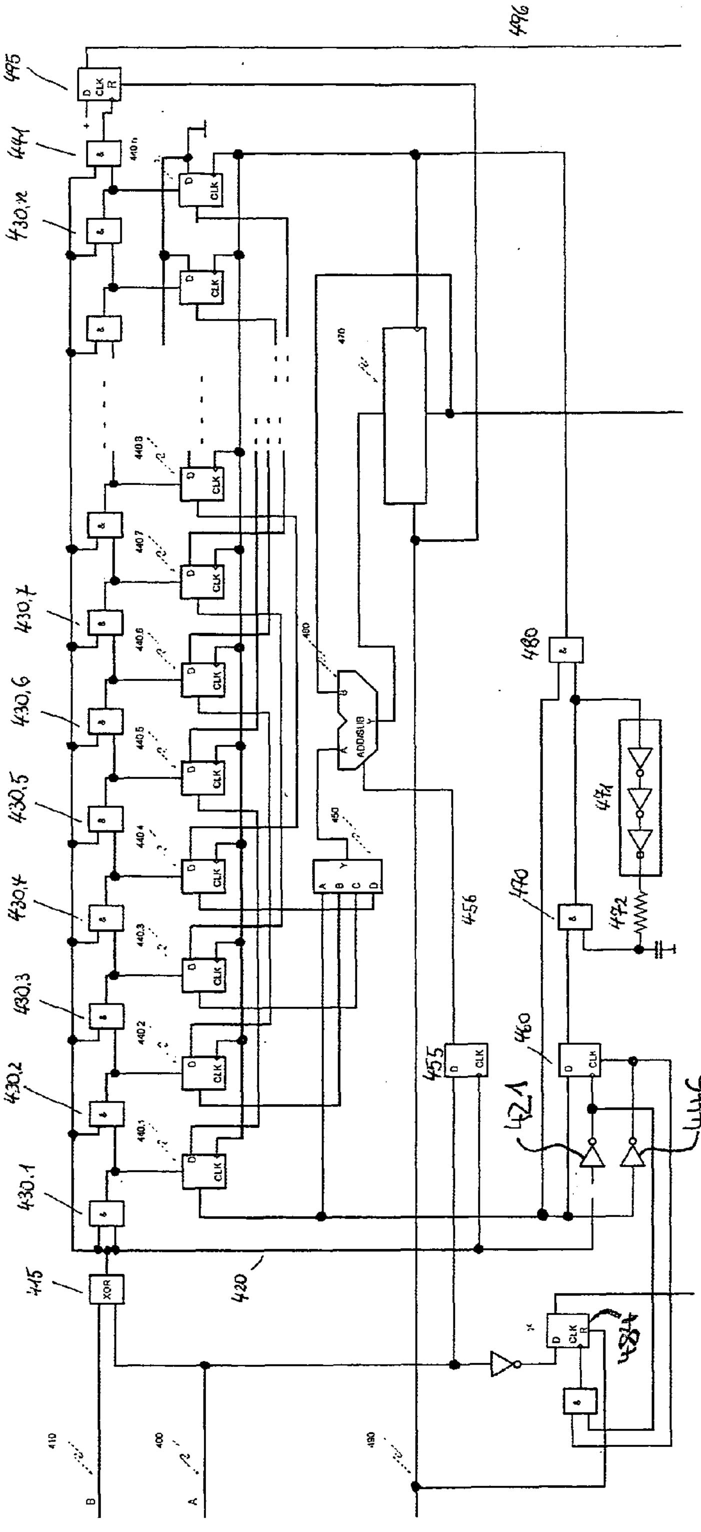

396
395
341
340.n
330.n
381
350
355
UP
RESET
CLK
360
371
372
370
356
340.4
330.4
340.3
330.3
340.2
330.2
340.1
330.1
320
345
321
346
315
XOR
385
384
301
383
310
300
390
B
A

Fig 3



496
495
441
430,n
430,7
430,6
430,5
430,4
430,3
430,2
430.1
415
XOR
420
ADD/SUB
455
456
460
470
480
471
472
421
446
B
A

Fig. 4

A	B	C	D	Y
0	0	0	0	000
1	0	0	0	001
1	1	0	0	010
1	1	1	0	011
1	1	1	1	100

Fig. 5

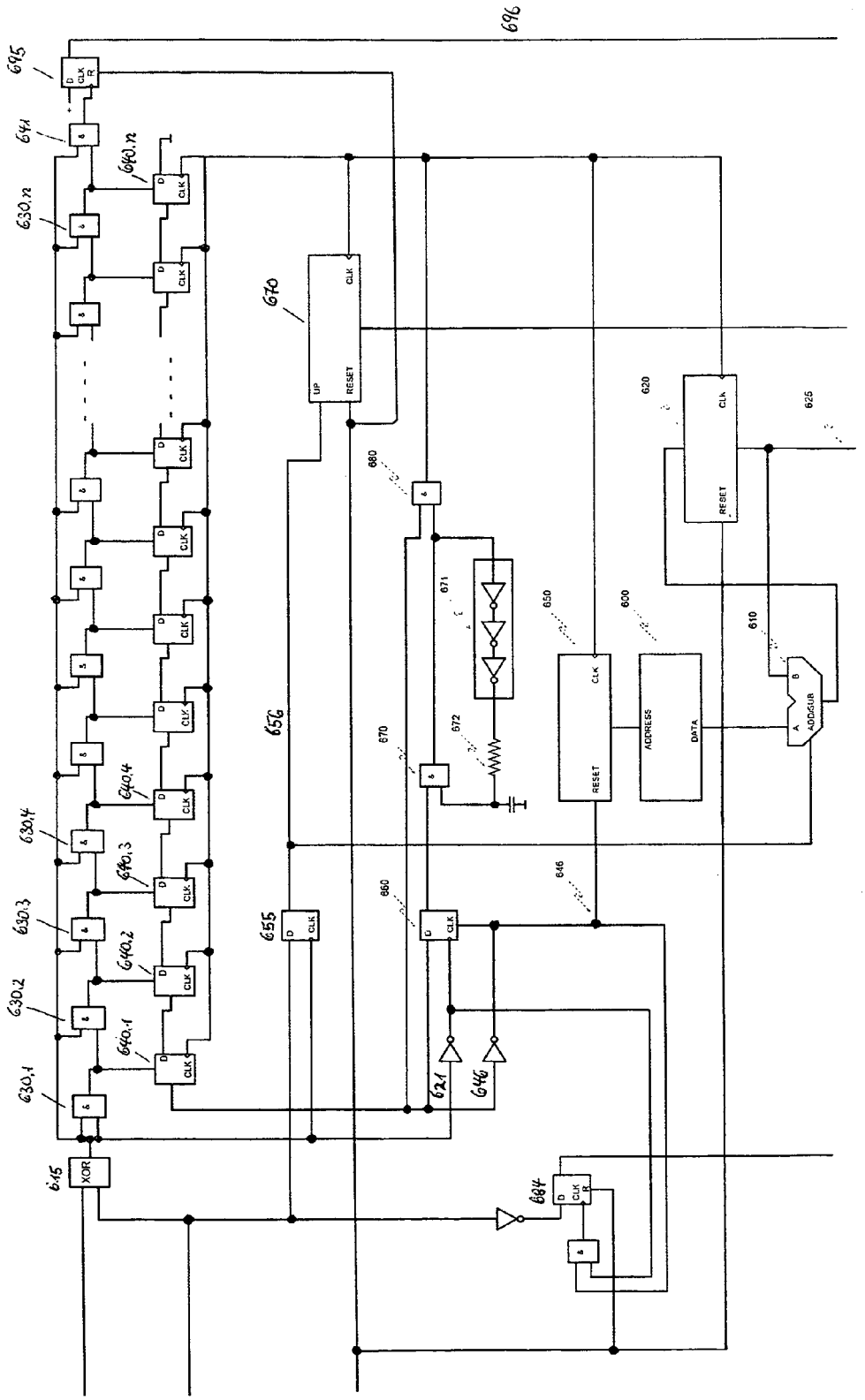

696
695
641
640.n
630.n
670
UP
RESET
CLK
620
625
680
671
650
600
610
672
670
656
ADDRESS
DATA
A
B
ADDSUB
640.4
630.4
640.3
630.3
640.2
630.2
640.1
630.1
655
660
646
621
646
615
XOR
684

Fig. 6

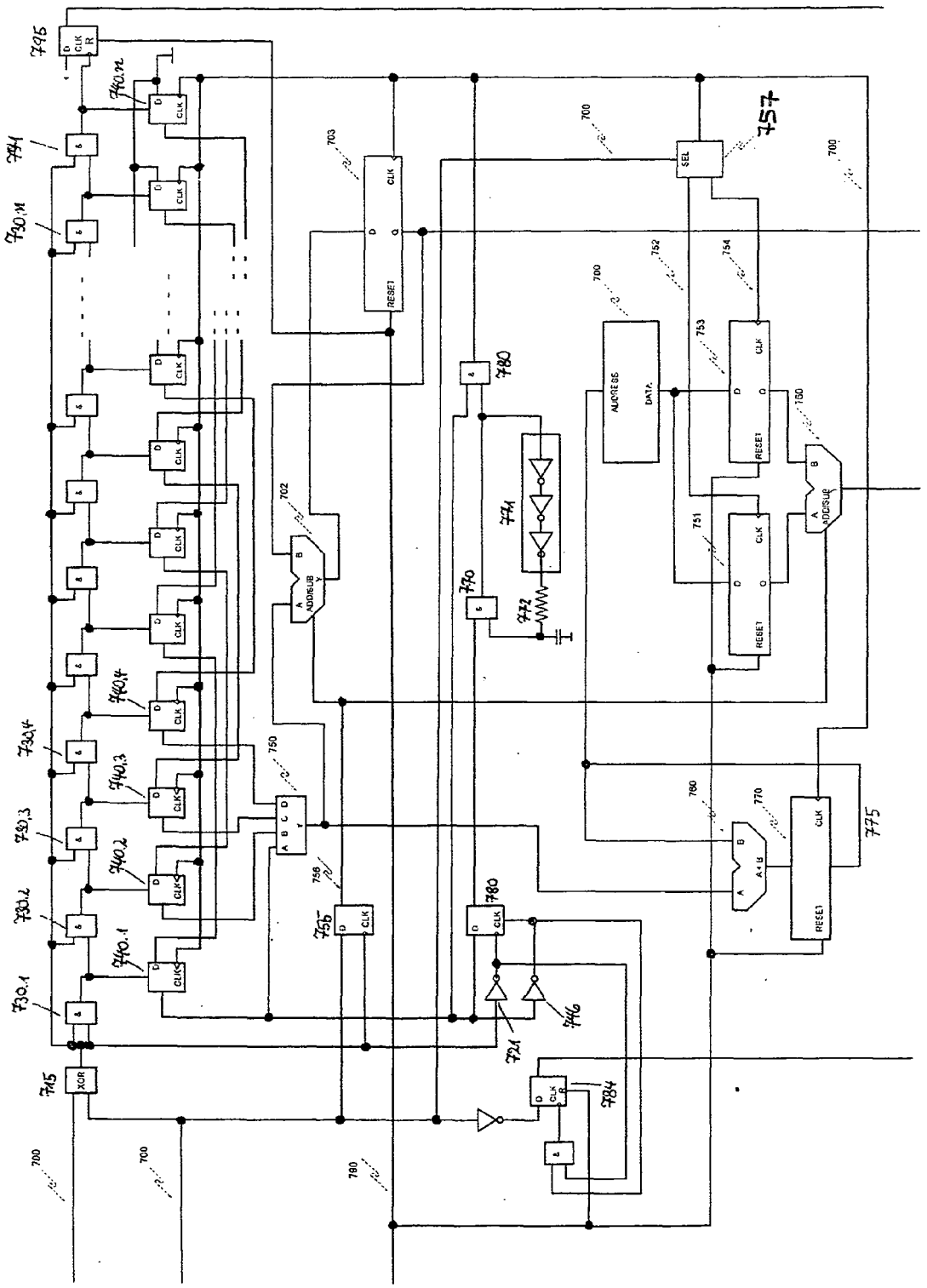


Fig. 7

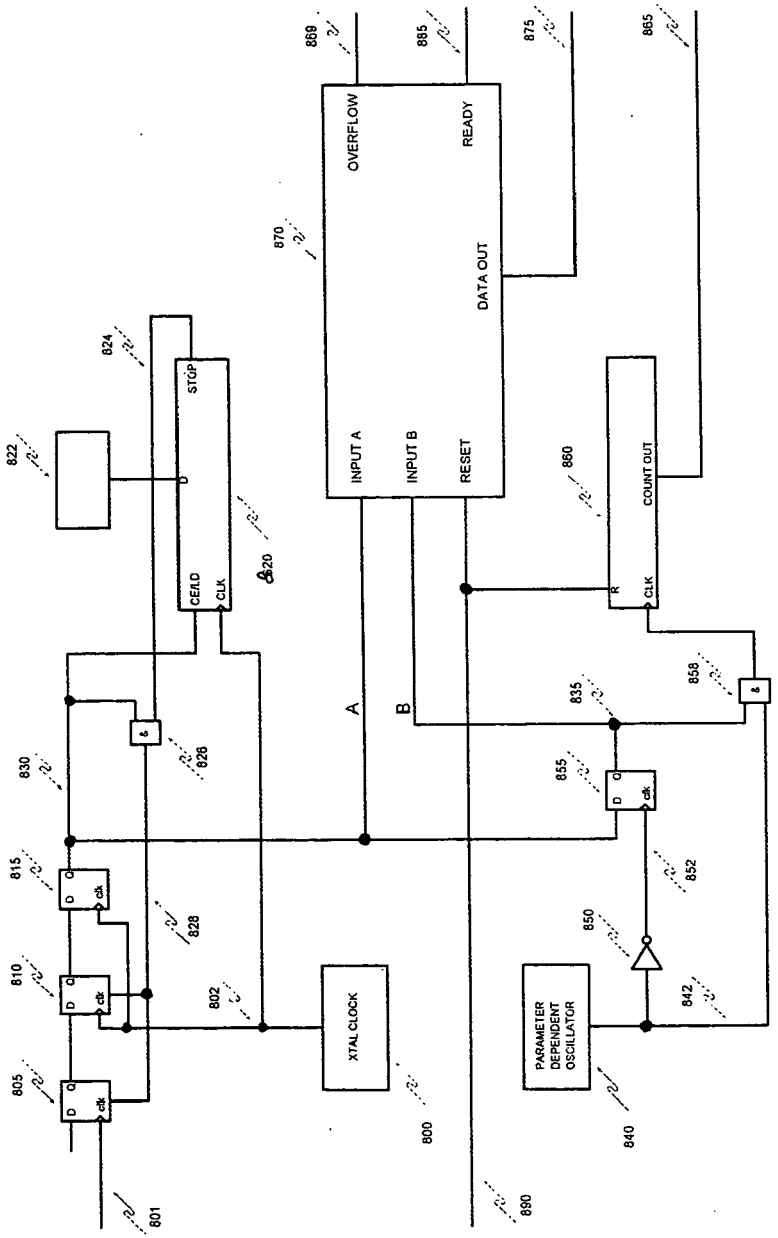

OVERFLOW
READY
DATA OUT
INPUT A
INPUT B
RESET
STOP
CE/LD
CLK
COUNT OUT
R
CLK
A
B
&
D Q
clk
XTAL CLOCK
PARAMETER DEPENDENT OSCILLATOR
869
885
875
865
870
824
822
820
860
858
835
855
852
850
842
840
830
826
815
828
810
802
805
800
801
890

Fig. 8

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 07 00 8128

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (IPC)
D,A	SZYMANOWSKI RAFAL ET AL: "Field programmable gate array time counter with two-stage interpolation" REVIEW OF SCIENTIFIC INSTRUMENTS, AMERICAN INSTITUTE OF PHYSICS, US, vol. 76, no. 4, 16 March 2005 (2005-03-16), pages 45104-45104, XP012079330 ISSN: 0034-6748 * figures 1,2 * -----	1	INV. H03M1/50 H03L7/08

TECHNICAL FIELDS SEARCHED (IPC)

H03M

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
The Hague	21 September 2007	Beindorff, Henk

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