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## (54) Method for applying dithering to video data and display device implementing said method

(57) The invention related to a method for processing video data of an input picture comprising the step of applying (30) a dithering function to the video data of at least a part of the input picture. According to the invention, it further comprises the steps of detecting (10) the presence or absence of a checker pattern in said part of the input picture, and selecting (20), among a plurality of dither functions, a dither function to be applied to said part of the input picture depending on the presence or absence of a checker pattern in said part of the input picture.

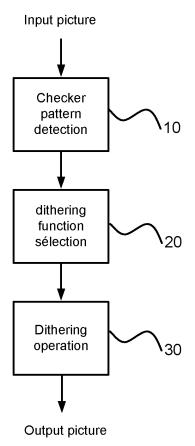


FIG.1

#### Description

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#### Field of the invention

<sup>5</sup> **[0001]** The invention relates to a method for processing video data of an input picture comprising a dithering step to refine the grayscale portrayal of the video data of the input picture and a device implementing said method.

#### Background of the invention

[0002] The invention will be described in the field of plasma display panels but is applicable to other types of display panels, for example LCD (Liquid Crystal Displays) or DLP (Digital Light Processing) projectors, wherein a dithering operation is required to improve the grayscale portrayal of the displayed pictures.

[0003] A PDP (Plasma Display Panel) utilizes a matrix array of discharge cells, which can only be "ON", or "OFF". Unlike a CRT in which grey levels are expressed by analogue control of the light emission, a PDP controls the grey level by modulating the number of light pulses per frame (sustain pulses). This time-modulation will be integrated by the eye over a period corresponding to the eye time response. Since the video amplitude is portrayed by the number of light pulses, occurring at a given frequency, more amplitude means more light pulses and thus more "ON" time. For this reason, this kind of modulation is also known as PWM, pulse width modulation.

**[0004]** This PWM is responsible for one of the PDP image quality problems: the poor grey scale portrayal quality, especially in the darker regions of the picture. This is due to the fact, that displayed luminance is linear to the number of pulses, but the eye response and sensitivity to noise is not linear. In darker areas the eye is more sensitive than in brighter areas. This means that even though modern PDPs can display ca. 255 discrete video levels, quantization error will be quite noticeable in the darker areas.

**[0005]** As mentioned before, a PDP uses PWM (pulse width modulation) to generate the different shades of grey. Contrarily to CRTs where luminance is approximately quadratic to applied cathode voltage, luminance is linear to the number of discharge impulses. Therefore an approximately digital quadratic gamma function has to be applied to video before the PWM.

**[0006]** Due to this gamma function, for smaller video levels, many input levels are mapped to the same output level. In other words, for darker areas, the output number of quantization bits is smaller than the input number, in particular for values smaller than 16 (when working with 8 bit for video input) that are all mapped to 0. This also counts for four bit resolution which is actually unacceptable for video.

**[0007]** One known solution to improve the quality of the displayed pictures is to artificially increase the number of displayed video levels by using dithering. Dithering is a known technique for avoiding losing amplitude resolution bits due to truncation. However, this technique only works if the required resolution is available before the truncation step. Usually this is the case in most applications, since the video data after a gamma operation used for pre-correction of the video signal has 16-bit resolution. Dithering can bring back as many bits as those lost by truncation in principle. However, the dithering noise frequency decreases, and therefore becomes more noticeable, with the number of dithered bits.

[0008] The concept of dithering shall be explained by the following example. A quantization step of 1 shall be reduced by dithering. The dithering technique uses the temporal integration property of the human eye. The quantization step may be reduced to 0, 5 by using 1-bit dithering. Accordingly, half of the time within the time response of the human eye there is displayed the value 1 and half of the time there is displayed the value 0. As a result the eye sees the value 0.5. Optionally, the quantization steps may be reduced to 0.25. Such dithering requires two bits. For obtaining the value 0.25 a quarter of the time the value 1 is shown and three quarters of the time the value 0. For obtaining the value 0.5 two quarters of the time the value 1 and two quarters of the time the value 0 is shown. Similarly, the value 0.75 may be generated. In the same manner quantization steps of 0.125 may be obtained by using 3-bit dithering. This means that 1 bit of dithering corresponds to multiply the number of available output levels by 2, 2 bits of dithering multiply by 4, and 3 bits of dithering multiply by 8 the number of output levels. A minimum of 3 bits of dithering may be required to give to the grey scale portrayal a 'CRT' look.

[0009] Dithering is still a major topic for today's display devices since it is difficult to find a good trade-off between pattern visibility and dithering noise produced by error diffusion for example. To this end a checker pattern is often used as first dithering bit since this is the less visible deterministic dithering pattern. A checker pattern applied to an input picture consists generally in rounding up the value of a first pixel of a first line, then rounding down the value of the next pixel of the first line, then rounding down the value of the next pixel of the first line ... and doing the opposite for the next line.... For clarification, rounding up means rounding up to the closest higher video level that can be displayed and rounding down means rounding down to the closest lower value that can be displayed. A checker pattern is illustrated by the following chart wherein a bit 0 or 1 is associated to each pixel of a block of 6x14 pixels, 0 meaning that the value of the pixel is rounding down and 1 meaning that the value

is rounding up.

| 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 |
| 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 |
| 1 | Λ | 1 | Ο | 1 | Ω | 1 | Ω | 1 | Λ | 1 | Λ | 1 | Ω |

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**[0010]** One way of implementing a checker pattern is to round up if the number (pixel\_counter+line\_counter) is equal to 1 modulo 2, and to round down if the number (pixel\_counter+line\_counter) is equal to 0 modulo 2. In a variant, the number (pixel\_counter+line\_counter) can be replaced by the number (pixel\_counter+line\_counter+frame\_counter) or other formulas.

**[0011]** It can be noted that the checker pattern added to the picture is not always noticeable in the final picture. This is the case for pictures with high contrast and lots of details in which every pixel has a video information quite different from its neighbor pixels. For such pictures or parts of pictures, the used dithering is not really visible, and so not so important.

**[0012]** Since checker pattern dithering is easy to implement and quite efficient, some rendering systems like some computers graphic cards use such a pattern to reduce the number of video bits or to perform some special effects. Unfortunately if a display device using this checker dithering pattern is connected to such a rendering system, some interferences can appear which generate clearly visible low frequency flicker, typically at half display refresh rate.

### Invention

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[0013] It is an object of the present invention to propose a solution for remedying to this problem.

**[0014]** The present invention concerns a method for processing video data of an input picture comprising applying a dithering function to the video data of at least a part of the input picture. According to the invention, it further comprises the steps of:

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- detecting the presence or absence of a checker pattern in the part of the input picture, and
- selecting, among a plurality of dithering functions, a dithering function to be applied to the part of the input picture depending on the presence or absence of a checker pattern in this part of the input picture.

[0015] In a specific embodiment, a checker pattern is detected in a block of pxq neighbor pixels if, in each row and column of pixels of said block, every pixel or the big majority of them is surrounded by pixels having higher video data or by pixels having lower video data.

**[0016]** In a specific embodiment, if no checker pattern is detected, the selected dithering function is a dithering pattern for at least the most significant dithering bit. This dithering pattern can be a checker pattern.

[0017] The invention concerns also a display device for displaying an input picture comprising dithering means for applying a dithering function to the video data of at least a part of the input picture. According to the invention, it further comprises:

- detection means for detecting the presence or absence of a checker pattern in the part of the input picture, and
- selection means for selecting, among a plurality of dithering functions, a dithering function to be applied to the part of the input picture depending on the presence or absence of a checker pattern in said part of the input picture.

#### Brief description of the drawings

[0018] Exemplary embodiments of the invention are illustrated in the drawings and are explained in more detail in the following description. In the drawings:

- Fig.1 shows the steps of the inventive method;
- Fig.2 represents a possible implementation of a display device according to the invention, and
- 55 Fig.3 shows a possible implementation of dithering means of the display device of figure 1.

#### **DESCRIPTION OF PREFERRED EMBODIMENTS**

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**[0019]** In the following detailed description, only certain exemplary embodiments of the present invention are shown and described, by way of illustration. As those skilled in the art would recognize, the described exemplary embodiments may be modified in various ways, all without departing from the spirit or scope of the present invention. Accordingly, the drawings and description are to be regarded as illustrative in nature, rather than restrictive.

**[0020]** According to the invention and as illustrated by figure 1, the presence of a checker pattern is detected (step 10) in at least a part of the input picture provided to the display device and a dithering function (among a plurality of dithering functions) to be used by the dithering means of the display device is selected (step 20) in accordance with the presence or absence of a checker pattern in this part of picture. The dithering step (step 30) is then applied to the part of input picture with the selected dithering function.

**[0021]** To detect the presence of a checker pattern in a part of picture, it is possible to detect if p consecutive pixels are in "saw teeth" formation (M or W), n being greater than 2. For p=5, this means a saw teeth formation is detected

if 
$$X_n < X_{n+1}$$
 AND  $X_{n+1} > X_{n+2}$  AND  $X_{n+2} < X_{n+3}$  AND  $X_{n+3} > X_{n+4}$ 

or if 
$$X_n > X_{n+1}$$
 AND  $X_{n+1} < X_{n+2}$  AND  $X_{n+2} > X_{n+3}$  AND  $X_{n+3} < X_{n+4}$ 

wherein  $X_n$  designates the video information of a pixel n.

If one of the two conditions is right, a checker pattern is detected.

**[0022]** It is possible to use other detection schemes, like detecting the presence of a checker pattern in a square form (same scheme but in 2 dimensions) using a similar method, and preferably allowing some exceptions. For such a small form like the one proposed previously with 5 pixels, it is not necessary to allow exceptions, but this could be required for bigger forms. What is meant by exceptions is explained hereinafter. If a checker pattern is present in a block of 5x9 pixels, we have:

wherein 1 represents a higher video information than 0.

**[0023]** Instead of expecting exactly this pattern, it could be allowed to have at a random place of the block a 0 instead of a 1 or the opposite. For example, at the **0 1 0** position (position where bold characters are used), the central pixel (represented by 1) is expected to have a higher value than its two neighbor pixels (represented by 0). An exception could be to allow this pixel to have a smaller value than these two pixels. This means that the following pattern would be accepted:

| 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 |

**[0024]** So when a checker pattern has been or not detected in a block of p consecutive pixels or a block of pxq neighbor pixels, a dithering function is to be selected and to be applied to said block of pixels by the dithering means.

**[0025]** If no checker pattern is detected in the block of pixels, a dithering function called default dithering function is selected and applied to said block of pixels. This default dithering function uses for example a checker pattern for the most significant dithering bit which is, as mentioned before, the less visible deterministic dithering pattern.

**[0026]** If a checker pattern is detected in the block of pixels, another predetermined dithering function is selected and applied to the block of pixels. This dithering function is defined to not generate interferences with a checker pattern. Such dithering function is for example a dither pattern like

#### EP 1 995 712 A1

| 1 | 1 | 0 | 0 |
|---|---|---|---|
| 1 | 1 | 0 | 0 |
| 0 | 0 | 1 | 1 |
| 0 | 0 | 1 | 1 |

**[0027]** If a checker pattern is detected in the block of pixels, another possibility is to decide randomly for each pixel of the block to round up or to round down, or to decide randomly for two neighbor pixels to round up the first pixel and to round down the second one or to do the opposite.

**[0028]** The dithering functions are for example dithering patterns stored in the form of Look-Up Tables (LUTs) in a memory of the display device or are mathematical functions.

**[0029]** Figure 2 illustrates a possible implementation for the algorithm in the case of a PDP. RGB input pictures indicated by the signals  $R_0$ ,  $G_0$  and  $B_0$  are forwarded to a gamma function block 100. It can consist of a look up table (LUT) or it can be formed by a mathematical function. The outputs  $R_1$ ,  $G_1$  and  $B_1$  of the gamma function block 10 are forwarded to a dithering block 120 which can take into account the pixel position and eventually the frame parity as temporal component for the computation of the dithering value. The dithering block 120 is controlled by a control signal C delivered by a control unit 180.

[0030] The video signals  $R_1$ ,  $G_1$ ,  $B_1$  subjected to the dithering in the dithering block 120 are output as signals  $R_2$ ,  $G_2$ ,  $B_2$  and are forwarded to a sub-field coding unit 14 which performs sub-field coding under the control of the control unit 180. [0031] The sub-field signals for each colour output from the sub-field coding unit 140 are indicated by reference signs  $SF_R$ ,  $SF_G$ ,  $SF_B$ . For plasma display panel addressing, these sub-field code words for one line are all collected in order to create a single very long code word which can be used for the linewise PDP addressing. This is carried out in a serial to parallel conversion unit 160 which is itself controlled by the plasma control unit 180. Furthermore, the control unit 180 generates all scan and sustain pulses for PDP control. It receives horizontal and vertical synchronizing signals for reference timing.

[0032] Figure 3 illustrates a possible implementation of the dithering block 120. It comprises a detection circuit 121 to detect the presence of a checker pattern in the video information delivered by the gamma function block 100, a selection circuit 122 for selecting a default dithering function or another predetermined function depending on the results delivered by the detection circuit 121 and a dithering block 123 to apply the selected dithering function to the video information coming from the gamma function block 100. The dithering functions are for example patterns stored in a memory 124.

[0033] The invention is not restricted to the disclosed embodiments and particularly to Plasma Display Panels. It can be applied to other types of display panels like LCDs or DLP projectors.

#### **Claims**

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- 1. Method for processing video data of an input picture comprising
  - applying (30) a dithering function to the video data of at least a part of the input picture,

#### characterized in that it further comprises the steps of:

- detecting (10) the presence or absence of a checker pattern in said part of the input picture, and
- selecting (20), among a plurality of dithering functions, a dithering function to be applied to said part of the input picture depending on the presence or absence of a checker pattern in said part of the input picture.
- 2. Method according to claim 1, wherein a checker pattern is detected in a block of pxq neighbor pixels if, in each row and column of pixels of said block, every pixel is surrounded by pixels having higher video data or by pixels having lower video data.
- 3. Method according to claim 1 or 2, wherein, if no checker pattern is detected, the selected dithering function is a dithering pattern for at least the most significant dithering bit.
- **4.** Method according to claim 3, wherein the dithering pattern is a checker pattern.
  - 5. Method according to claim 1 or 2, wherein at least one of the dithering functions is a look-up table.

## EP 1 995 712 A1

- **6.** Method according to claim 1 or 2, wherein at least one of the dithering functions is a mathematical function.
- 7. Display device for displaying an input picture comprising
  - dithering means (123) for applying a dithering pattern to the video data of at least a part of the input picture,

## characterized in that it further comprises:

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- detection means (121) for detecting the presence or absence of a checker pattern in said part of the input picture, and
- selection means (122) for selecting, among a plurality of dither patterns, a dither pattern to be applied to said part of the input picture depending on the presence or absence of a checker pattern in said part of the input picture.
- **8.** Display device according to claim 7, wherein it comprises memory means for storing at least one dither pattern as dithering functions.

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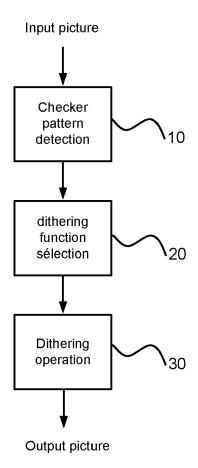
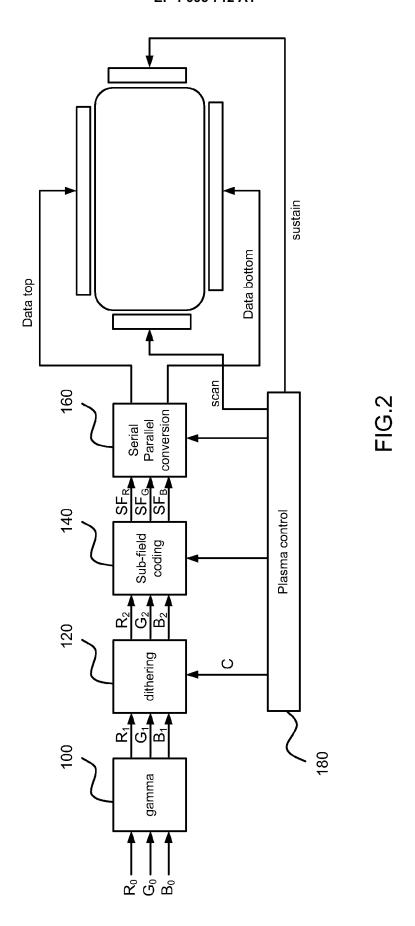


FIG.1



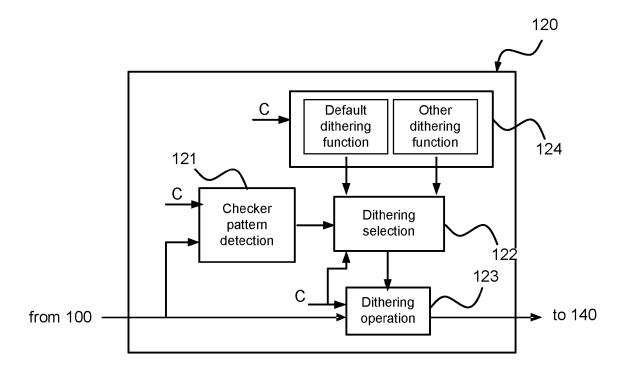


FIG.3



## **EUROPEAN SEARCH REPORT**

Application Number EP 07 30 1059

|   | DOCUMENTS CONSID  | ERED TO BE RELEVANT  |  |  |
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|   |   |  |  | TECHNICAL FIELDS<br>SEARCHED (IPC)<br>G09G<br>H04N |
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|   | The present search report has   | been drawn up for all claims   |  |  |
|   | Place of search   | Date of completion of the search                                     |  | Examiner   |
|   | The Hague   | 9 October 2007   | Far  | nning, Neil  |
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EPO FORM 1503 03.82 (P04C01) **G1** 

## ANNEX TO THE EUROPEAN SEARCH REPORT ON EUROPEAN PATENT APPLICATION NO.

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