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(54) **Digital phase-locked loop**

(57) Described herein is a digital phase-locked loop (10) designed to receive an input signal ($s_i(t)$), having an oscillator (40) and a phase detector (20). The oscillator (40) generates a first harmonic signal and a second harmonic signal having the same reference phase ($\phi_{VCO}(t)$), but for a phase offset of 90 degrees. The phase detector (20) calculates a quantity linearly proportional to the difference between the phase ($\phi_i(t)$) of the input signal ($s_i(t)$) and the reference phase ($\phi_{VCO}(t)$ by means of extraction of an in-phase component ($s_{ii}(t)$) and a quadrature component ($s_{iq}(t)$) of the input signal ($s_i(t)$) with respect to the reference phase ($\phi_{VCO}(t)$).

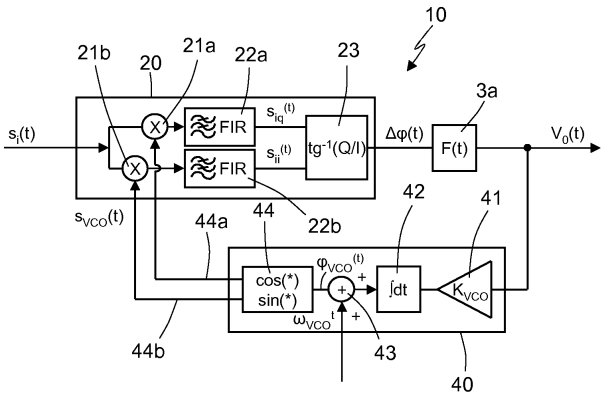

Fig.4

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