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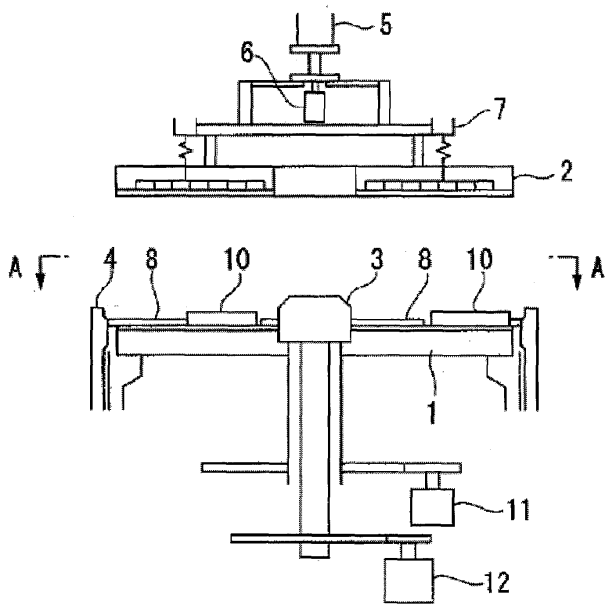
(54) Method and device for grinding both surfaces of semiconductor wafers

(57) A method of grinding semiconductor wafers including simultaneously grinding both surfaces of multiple semiconductor wafers being ground by rotating the multiple semiconductor wafers between a pair of upper and lower rotating surface plates in a state where the multiple wafers are held on a carrier so that centers of the multiple wafers are positioned on a circumference of a single circle, wherein a ratio of an area of a circle passing through the centers of the multiple wafers to an area of one of the multiple wafers is greater than or equal to 1.33 but less than 2.0; a rotational speed of the multiple wafers falls within a range of 5 to 80 rpm; and the grinding of the multiple wafers with the rotating surface plates are conducted with fixed abrasive grains in the presence of an alkali solution.

Fig. 1



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Description

BACKGROUND OF THE INVENTION

FIELD OF THE INVENTION

[0001] The present invention relates to a grinding method and a grinding device for semiconductor wafers. More particularly, it relates to a wafer grinding method and a wafer grinding device suited to large silicon wafers having a diameter of about 450 mm that employ a carrier to simultaneously grind both sides of a wafer between upper and lower surface plates.

DISCUSSION OF THE BACKGROUND OF THE INVENTION

[0002] In the simultaneous grinding of both surfaces of a wafer during the manufacturing of a semiconductor wafer from silicon or the like, anywhere from 1 to as many as about 10 workpieces (semiconductor wafers) are generally inserted into the carrier holding the work for grinding. The number of workpieces varies based on factors such as increasing productivity relating to device size, work diameter and the like; specifications that take into account the work track and permeation of abrasive solution; and the like.

[0003] Planetary gear-type devices can be employed in such grinding of both surfaces of semiconductor wafers. However, when a planetary gear-type grinding device is employed, outer circumference sagging (peripheral sagging) occurs, resulting in precluding the obtaining of wafers with a high degree of flatness. As a countermeasure to outer circumference sagging, a method seeking to improve flatness through carrier design is proposed in Japanese Unexamined Patent Publication (KOKAI) No. 2002-254299. This method is a technique (fixed dimension polishing) in which the thickness of a carrier is controlled with a high degree of precision so as to approach the final thickness of the work, to disperse stress acting on the outer circumference portion of the work into the carrier to obtain a flat work.

[0004] However, the method described in Japanese Unexamined Patent Publication (KOKAI) No. 2002-254299 does not prevent peripheral sagging of wafers.

[0005] Accordingly, the present inventors conducted extensive research into the relation between semiconductor wafers as works and the stress that acts on the carrier holding the semiconductor wafers. As a result, they discovered that by conducting polishing with a carrier in which the circle radius (PCD), which specifies the spacing of the holes as the radius of a circle passing through the center of the holes in the carrier, and/or in which the spacing between works, was set to within a prescribed range, it was possible to evenly disperse the pressure from the surface plates in the surface of the wafers to prevent peripheral sagging of wafers without diminishing productivity and without shortening the service life of the carrier.

[0006] The solution that was discovered was in the form of a device for polishing both surfaces of semiconductor wafers including a pair of upper and lower rotating surface plates; a sun gear provided in a rotating center portion between the upper and lower rotating surface plates; a ring-shaped inner-toothed gear positioned on an outer circumference portion between the upper and lower rotating surface plates; and a carrier composed of a planetary gear, the planetary gear meshing with the inner-toothed gear and sun gear and being positioned between the upper and lower rotating surface plates, wherein the carrier has multiple holes serving as holes receiving wafers being polished, and centers of the multiple holes are positioned on a circumference of a single circle, with a ratio of an area of a circle passing through the centers of the multiple holes to an area of one of the wafers being polished greater than or equal to 1.33 but less than 2.0, and the above device is described in Japanese Unexamined Patent Publication (KOKAI) No. 2009-4616, published on January 8, 2009.

[0007] A method of grinding semiconductor wafers including simultaneously polishing both surfaces of multiple semiconductor wafers being polished by rotating the multiple semiconductor wafers between a pair of upper and lower rotating surface plates in a state where the multiple semiconductor wafers are held on a carrier so that centers of the multiple semiconductor wafers are positioned on a circumference of a single circle, wherein a ratio of an area of a circle passing through the centers of the multiple semiconductor wafers to an area of one of the multiple semiconductor wafers is greater than or equal to 1.33 but less than 2.0, was also invented and a patent application relating to the above method was filed (identical to the above).

[0008] The size of the silicon wafers cut from single crystals of silicon is increasing in an about 10-year cycle. Device manufacturers hope to increase device manufacturing efficiency by increasing the size of the silicon wafers. In light of these circumstances, the manufacturing of silicon wafers with diameters of about 450 mm, about 1.5 times the current diameter of 300 mm, is planned for the near future.

[0009] Polishing of silicon wafers 450 mm in diameter will involve polishing of an area that is double or more that of conventional silicon wafers equal to or less than 300 mm in diameter. Thus, difficulty is anticipated in obtaining silicon wafers with the same flatness as in the past while maintaining production efficiency by the same method as before.

[0010] In particular, for silicon wafers 450 mm in diameter, it is difficult to obtain silicon wafers of the same flatness as in the past while maintaining production efficiency by the conventionally employed combination of lapping with free abrasive grains and grinding with fixed abrasive grains.

SUMMARY OF THE INVENTION

[0011] Thus, a non limiting aspect of the present invention provides for a method and device permitting the obtaining with good production efficiency of silicon wafers having the same degree of flatness as in the past despite an increased diameter.

[0012] The present inventors conducted extensive research into grinding large-diameter 450 mm silicon wafers -- the next generation of silicon wafersby adapting the semiconductor wafer polishing device of the above-cited patent application for use in grinding with fixed abrasive grains. As a result, it was discovered that conventional conditions for employing fixed abrasive grains caused clogging, precluding continuous grinding for extended periods. The present inventors conducted an extensive investigation into solving such clogging, and discovered a solution. The present invention was devised on that basis.

[0013] A first aspect of the present invention relates to a method of grinding semiconductor wafers including:

simultaneously grinding both surfaces of multiple semiconductor wafers being ground by rotating the multiple semiconductor wafers between a pair of upper and lower rotating surface plates in a state where the multiple semiconductor wafers are held on a carrier so that centers of the multiple semiconductor wafers are positioned on a circumference of a single circle, wherein
a ratio of an area of a circle passing through the centers of the multiple semiconductor wafers to an area of one of the multiple semiconductor wafers is greater than or equal to 1.33 but less than 2.0;
a rotational speed of the multiple semiconductor wafers falls within a range of 5 to 80 rpm; and
the grinding of the multiple semiconductor wafers with the rotating surface plates are conducted with fixed abrasive grains in the presence of an alkali solution.

[0014] The alkali solution may have a pH ranging from 12 to 15.

[0015] The semiconductor wafers may have a diameter ranging from 400 to 500 mm.

[0016] The ratio of an area of a circle passing through the centers of the multiple semiconductor wafers to an area of one of the multiple semiconductor wafers may be greater than or equal to 1.33 but less than or equal to 1.5.

[0017] A second aspect of the present invention relates to a device for grinding both surfaces of semiconductor wafers including:

a pair of upper and lower rotating surface plates including fixed abrasive grains;
a sun gear provided in a rotating center portion between the upper and lower rotating surface plates;
a ring-shaped inner-toothed gear positioned on an outer circumference portion between the upper and lower rotating surface plates;
a carrier composed of a planetary gear, the planetary gear meshing with the inner-toothed gear and sun gear and being positioned between the upper and lower rotating surface plates; and
an alkali solution feeding part, wherein
the carrier has multiple holes serving as holes receiving wafers being ground, and
centers of the multiple holes are positioned on a circumference of a single circle, with a ratio of an area of a circle passing through the centers of the multiple holes to an area of one of the wafers being ground greater than or equal to 1.33 but less than 2.0.

[0018] The ratio of an area of a circle passing through the centers of the multiple holes to an area of one of the wafers being ground may be greater than or equal to 1.33 but less than or equal to 1.5.

[0019] The present invention can provide a method and device permitting the obtaining with high production efficiency of silicon wafers having the same flatness as in the past despite an increased diameter.

[0020] Other exemplary embodiments and advantages of the present invention may be ascertained by reviewing the present disclosure and the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

[0021] The present invention will be described in the following text by the exemplary, non-limiting embodiments shown in the figures, wherein:

Fig. 1 is a front view descriptive of an implementation embodiment of the semiconductor wafer grinding device according to the present invention;

Fig. 2 is a plan view along section line A-A in Fig. 1; and

Fig. 3 is a plan view descriptive of an implementation embodiment of the semiconductor wafer grinding method according to the present invention and of the disposition of holes in a carrier.

DETAILED DESCRIPTION OF THE EMBODIMENTS

[0022] Unless otherwise stated, a reference to a compound or component includes the compound or component by itself, as well as in combination with other compounds or components, such as mixtures of compounds.

[0023] As used herein, the singular forms "a," "an," and "the" include the plural reference unless the context clearly dictates otherwise.

[0024] Except where otherwise indicated, all numbers expressing quantities of ingredients, reaction conditions, and so forth used in the specification and claims are to be understood as being modified in all instances by the term "about." Accordingly, unless indicated to the contrary, the numerical parameters set forth in the following specification and attached claims are approximations that may vary depending upon the desired properties sought to be obtained by the present invention. At the very least, and not to be considered as an attempt to limit the application of the doctrine of equivalents to the scope of the claims, each numerical parameter should be construed in light of the number of significant digits and ordinary rounding conventions.

[0025] Additionally, the recitation of numerical ranges within this specification is considered to be a disclosure of all numerical values and ranges within that range. For example, if a range is from about 1 to about 50, it is deemed to include, for example, 1, 7, 34, 46.1, 23.7, or any other value or range within the range.

[0026] The following preferred specific embodiments are, therefore, to be construed as merely illustrative, and non-limiting to the remainder of the disclosure in any way whatsoever. In this regard, no attempt is made to show structural details of the present invention in more detail than is necessary for fundamental understanding of the present invention; the description taken with the drawings making apparent to those skilled in the art how several forms of the present invention may be embodied in practice.

[0027] The first aspect of the present invention relates to a method of grinding semiconductor wafers including simultaneously grinding both surfaces of multiple semiconductor wafers being ground by rotating the multiple semiconductor wafers between a pair of upper and lower rotating surface plates in a state where the multiple semiconductor wafers are held on a carrier so that centers of the multiple semiconductor wafers are positioned on a circumference of a single circle, wherein a ratio of an area of a circle passing through the centers of the multiple semiconductor wafers to an area of one of the multiple semiconductor wafers is greater than or equal to 1.33 but less than 2.0; a rotational speed of the multiple semiconductor wafers falls within a range of 5 to 80 rpm; and the grinding of the multiple semiconductor wafers with the rotating surface plates are conducted with fixed abrasive grains in the presence of an alkali solution.

[0028] The method of grinding semiconductor wafers according to the present invention can be carried out, for example, with the devise for grinding both surfaces of semiconductor wafers according to the second aspect of the present invention. The device includes a pair of upper and lower rotating surface plates including fixed abrasive grains; a sun gear provided in a rotating center portion between the upper and lower rotating surface plates; a ring-shaped inner-toothed gear positioned on an outer circumference portion between the upper and lower rotating surface plates; a carrier composed of a planetary gear, the planetary gear meshing with the inner-toothed gear and sun gear and being positioned between the upper and lower rotating surface plates; and an alkali solution feeding part, wherein the carrier has multiple holes serving as holes receiving wafers being ground, and centers of the multiple holes are positioned on a circumference of a single circle, with a ratio of an area of a circle passing through the centers of the multiple holes to an area of one of the wafers being ground greater than or equal to 1.33 but less than 2.0.

[0029] As for the semiconductor wafer grinding method according to the present invention, details regarding the fact that the positions at which the wafers are held within the carrier are disposed so that the centers of the multiple wafers are positioned on a circumference of a single circle and the fact that the ratio of an area of a circle passing through the centers of the multiple wafers to an area of one of the multiple wafers is greater than or equal to 1.33 but less than 2.0 will be described, with the details of the above grinding device further below.

[0030] In the semiconductor wafer grinding method according to the present invention, wafers are ground by rotating surface plates using fixed abrasive grains. In this process, the rotational speed of the wafers being ground falls within a range of 5 to 80 rpm. The above range of the rotational speed of the wafers being ground is specified for the following reasons. When the rotational speed of the wafers being ground is less than 5 rpm, grinding rate becomes low. When 80 rpm is exceeded, the wafer may jump. Within the range of 5 to 80 rpm, wafers can be ground with fixed abrasive grains without lowering of the grinding rate and jumping of the wafer.

[0031] However, when conducting grinding by rotating the wafer being ground at a speed falling within a range of 5 to 80 rpm with fixed abrasive grains, grinding debris is generated by the fixed abrasive grains. When the fixed abrasive

grains are not regularly dressed, grinding efficiency decreases. Accordingly, in the present invention, to remove grinding debris, grinding by rotating surface plates is conducted in the presence of an alkali solution. Conducting grinding by rotating surface plates in the presence of an alkali solution can prevent clogging of the fixed abrasive grains. The alkali solution employed in this process desirably has a pH of 12 to 15, which is more strongly alkaline than the alkali solution conventionally employed in lapping with free abrasive grains. The reason for using a strongly alkaline solution is to facilitate dissolution of Si (silicon) during processing.

[0032] The alkali solution is continuously or intermittently fed onto the surfaces ground by the rotating surface plates. The quantity of alkali solution that is fed can be suitably determined by taking into account the rotational speed of the wafers being ground, the coarseness of the fixed abrasive grains, and the like; for example, 1 to 3 L/minute can be employed. Examples of the alkali solution are hydroxides of alkali metals (Li, Na, K).

[0033] The surface plates employed to grind the semiconductor wafers may include grid-like pellets on surfaces of fixed abrasive grains facing the wafer surfaces. Examples of such grinding-use surface plates are metal bonded grindstones and resin bonded grindstones containing diamond as the abrasive grain.

[0034] An embodiment of implementing the grinding method and semiconductor wafer grinding device employed in the present invention will be described based on the drawings. Fig. 1 is a front view describing the semiconductor wafer grinding device, and Fig. 2 is a plan view along section line A-A in Fig. 1.

[0035] As indicated in Figs. 1 and 2, the semiconductor wafer grinding device can be equipped with a horizontally supported ring-shaped lower surface plate (rotating surface plate) 1, a ring-shaped upper surface plate (rotating surface plate) 2 opposing lower surface plate 1 from above, a sun gear 3 positioned to the inside of ring-shaped lower surface plate 1, and a ring-shaped inner-toothed gear 4 positioned outside lower surface plate 1.

[0036] A motor 11 drives rotation of lower surface plate 1. Upper surface plate 2 is suspended via a joint 6 from a cylinder 5, and is driven to rotate in the opposite direction by a separate motor from the motor 11 driving lower surface plate 1. An alkali solution feeding part (also referred to as a feeder), including a tank 7 for feeding alkali solution between upper surface plate 2 and lower surface plate 1, is also provided. Both sun gear 3 and inner-toothed gear 4 are independently driven to rotate by a motor 12 separate from the motors driving the surface plates.

[0037] Fixed abrasive grains are provided on the opposing surfaces of lower surface plate 1 and upper surface plate 2.

[0038] Multiple carriers 8 are set on lower surface plate 1 so as to surround sun gear 3. The various carriers 8 that are set in place mesh to the inside with sun gear 3 and to the outside with inner-toothed gear 4. Holes 9 receiving semiconductor wafers (works or workpieces) 10 are provided eccentrically in each of the carriers 8. The thickness of each of carriers 8 is set to be either identical to the target value for the final finished thickness of wafers 10, or to be slightly smaller.

[0039] To grind wafers 10, multiple carriers 8 are set onto lower surface plate 1 with upper surface plate 2 in a raised state, and wafers 10 are set in holes 9 in each of the carriers 8. Upper surface plate 2 is lowered, and a prescribed pressure is applied to each of wafers 10. In this state, while feeding grinding solution between lower surface plate 1 and upper surface plate 2, each of lower surface plate 1, upper surface plate 2, sun gear 3, and inner-toothed gear 4 is rotated at a prescribed speed in a prescribed direction.

[0040] Thus, multiple carriers 8 between upper surface plate 1 and lower surface plate 2 undergo planetary motion, in which they revolve around sun gear 3, while rotating. The wafers 10 held on each of carriers 8 contact the fixed abrasive grains above and below in the presence of the alkali solution, simultaneously grinding both the upper and lower surfaces thereof. The grinding conditions can be set so that both surfaces of wafers 10 are uniformly ground and all of multiple wafers 10 are uniformly ground.

[0041] During grinding, the torque of motor 11 driving lower surface plate 1, or the torque of the motor driving upper surface plate 2, can be monitored. When this torque drops by a preset ratio -- 10 percent, for example -- after having assumed a stable level, upper surface plate 2 can be raised to finish grinding. Thus, the final finished thickness of wafers 10 can be stably managed with high precision to be slightly thinner than or identical to the thickness of the carrier before grinding.

[0042] Since the carriers 8 may deteriorate due to friction with the surface plates, the material of the carriers 8 desirably has high resistance to abrasion and a low coefficient of friction with the fixed abrasive grains, and is desirably highly chemically resistant, for example, in pH 12 to 15 alkali solutions. Examples of carrier materials satisfying such conditions are stainless steel, epoxy resin, phenol resin, and polyimide resin. Further examples include but are not limited to FRPs (fiber-reinforced plastics) including such resins reinforced with a fiber such as glass fiber, carbon fiber, or aramid fiber. Since carriers 8 are employed to hold wafers 10, they cannot decrease much in strength.

[0043] Fig. 3 is a plan view descriptive of the semiconductor wafer grinding method and disposition of holes in the carrier in the present implementation embodiment.

Multiple holes 9 are provided as shown in Fig. 3 in a carrier 8; there are three such spots in the present implementation embodiment.

[0044] In carrier 8 of the present implementation embodiment, the centers C9 of each of the three holes 9 are positioned on the circumference of a circle P that is concentric with carrier 8 and disposed at equal intervals on circle P so as to

be rotationally symmetric about a point relative to center CP (the center of carrier 8) of circle P. The size of holes 9 is such that the ratio of the area of circle P passing through centers C9 of holes 9 to the area of one of holes 9, each of which is nearly equal in area to wafers 10, is greater than or equal to 1.33 but less than 2.0, preferably greater than or equal to 1.33 but less than or equal to 1.5.

[0045] That is, the radius R of circle P and the radius r of hole 9 are set so that:

$$1.33 \ldots < (R/r)^2 \leq 1.5$$

[0046] The lower limit of the range specified by this area ratio (radius ratio squared) need only be greater than or equal to 1.3333..., and may be greater than or equal to 1.334.

[0047] A ratio of the area of circle P passing through the centers C9 of holes 9 in carrier 8 to the area of one of holes 9 that falls below the above range is undesirable in that only two holes 9 can be provided within a carrier 8, the wafers processed in a single carrier 8 cannot be uniformly processed, and no effect is realized in preventing sagging of wafers 10. An upper limit of the above ratio of areas of greater than or equal to 2 is undesirable in that when holes 9 are provided in three spots in carrier 8, the distance between wafers 10 becomes excessive and no effect is realized in preventing sagging of wafers 10. An upper limit of the above ratio of areas of greater than or equal to 2 is undesirable in that when four or more holes 9 are provided in carrier 8, the pressure that concentrates is not adequately dispersed, precluding a preventive effect on sagging of wafers 10. Although sagging can be prevented when the upper limit of the above ratio of areas is set to greater than 1.5 but less than 2, less than or equal to 1.5 is desirable for obtaining finished product wafers of adequate flatness.

[0048] The size of wafer 10 and hole 9 can be roughly identical. When wafer 10 is 200 mm in diameter, hole 9 can be 201 mm in diameter, and when wafer 10 is 300 mm in diameter, hole 9 can be 302 mm in diameter.

[0049] In the present implementation embodiment, as set forth above, the use of carriers 8, in which holes 9 are formed, to grind both surfaces of wafers 10 makes it possible to prevent peripheral sagging in wafers 10 and to manufacture polished wafers of a high degree of flatness.

[0050] According to the present implementation embodiment, reducing the distance between semiconductor wafers 10 that are being ground on both surfaces to bring wafers 10 close together makes it possible to grind each of the wafers 10 positioned in holes 9 in three spots on a single carrier 8 in a manner approaching that achieved when grinding a single wafer 10. Thus, according to the present implementation embodiment, it is possible to keep the length over which pressure concentrates to just part of the total length of the perimeter of a single wafer 10, that is, to reduce the concentration of pressure in the perimeter portion of wafer 10 from flexible pads on the surfaces of surface plates 1 and 2 due to the difference in thickness of wafer 10 and carrier 8, resulting in reduction of portions significantly ground in the perimeter portion of wafer 10. Thus, it is possible to alleviate the concentration of grinding pressure over the entire circumference of the perimeter portion in a single wafer 10 when grinding is completed, which is thought to permit a reduction in the sagging produced in the perimeter portion in individual wafers 10.

[0051] In the present implementation embodiment, three carriers 8 are configured. However, greater or fewer suitable numbers of carriers 8 are possible. Additionally, so long as the disposition of holes 9 or wafers 10 in each carrier 8 is configured as set forth above, various configurations of the grinding device are possible.

[0052] Wafer 10 can be a silicon wafer or a wafer of some other semiconducting material. The present invention can be applied to wafers with diameters of 200 mm, 300 mm, as well as 450 mm or the like. The method and device according to the present invention are particularly suited to the grinding of large silicon wafers 400 to 500 mm in diameter.

EXAMPLES

[0053] The present invention will be described in detail below based on examples. However, the present invention is not limited to the examples.

[0054] Grinding devices configured as in the above implementation embodiment and carriers of different ratios of areas of circle P and holes 9 were prepared. These carriers were used to grind semiconductor wafers (silicon wafers) 10 and the flatness thereof was measured after grinding.

[0055] Details of grinding conditions and the like are indicated below.

Wafer subjected to grinding:	450 mm silicon wafer
Grinding device:	20B dual-surface grinder made by Speed Fam
Fixed abrasive grains:	Diamond
Alkali solution:	pH 14

(continued)

Grinding pressure:	200 g/cm^2
Carrier:	Made of stainless steel
Number of wafers ground:	5 carriers respectively having 3 holes (total 15 wafer batch)
Area ratios of circle P to hole 9:	138%, 144%, 150%, 163%

[0056] Following grinding, flatness (TTV: total thickness variation (micrometers)) was measured with an ADE (electrostatic capacitance surface flatness measuring device). The results indicated that wafers having flatness identical to conventionally ground wafers had been obtained.

[0057] The present invention is useful in the field of semiconductor wafer manufacturing.

[0058] Although the present invention has been described in considerable detail with regard to certain versions thereof, other versions are possible, and alterations, permutations and equivalents of the version shown will become apparent to those skilled in the art upon a reading of the specification and study of the drawings. Also, the various features of the versions herein can be combined in various ways to provide additional versions of the present invention. Furthermore, certain terminology has been used for the purposes of descriptive clarity, and not to limit the present invention. Therefore, any appended claims should not be limited to the description of the preferred versions contained herein and should include all such alterations, permutations, and equivalents as fall within the true spirit and scope of the present invention.

[0059] Having now fully described this invention, it will be understood to those of ordinary skill in the art that the methods of the present invention can be carried out with a wide and equivalent range of conditions, formulations, and other parameters without departing from the scope of the invention or any embodiments thereof.

[0060] The citation of any publication is for its disclosure prior to the filing date and should not be construed as an admission that such publication is prior art or that the present invention is not entitled to antedate such publication by virtue of prior invention.

Claims

1. A method of grinding semiconductor wafers comprising:

simultaneously grinding both surfaces of multiple semiconductor wafers being ground by rotating the multiple semiconductor wafers between a pair of upper and lower rotating surface plates in a state where the multiple semiconductor wafers are held on a carrier so that centers of the multiple semiconductor wafers are positioned on a circumference of a single circle, wherein
a ratio of an area of a circle passing through the centers of the multiple semiconductor wafers to an area of one of the multiple semiconductor wafers is greater than or equal to 1.33 but less than 2.0;
a rotational speed of the multiple semiconductor wafers falls within a range of 5 to 80 rpm; and
the grinding of the multiple semiconductor wafers with the rotating surface plates are conducted with fixed abrasive grains in the presence of an alkali solution.

2. The method of grinding according to claim 1, wherein the alkali solution has a pH ranging from 12 to 15.

3. The method of grinding according to claim 1 or 2, wherein the semiconductor wafers have a diameter ranging from 400 to 500 mm.

4. The method of grinding according to any of claims 1 to 3, wherein the ratio of an area of a circle passing through the centers of the multiple semiconductor wafers to an area of one of the multiple semiconductor wafers is greater than or equal to 1.33 but less than or equal to 1.5.

5. A device for grinding both surfaces of semiconductor wafers comprising:

a pair of upper and lower rotating surface plates comprising fixed abrasive grains;
a sun gear provided in a rotating center portion between the upper and lower rotating surface plates;
a ring-shaped inner-toothed gear positioned on an outer circumference portion between the upper and lower rotating surface plates;
a carrier comprised of a planetary gear, the planetary gear meshing with the inner-toothed gear and sun gear and being positioned between the upper and lower rotating surface plates; and

an alkali solution feeder, wherein
the carrier has multiple holes configured to receive respective wafers being ground, and
centers of the multiple holes are positioned on a circumference of a single circle, with a ratio of an area of a circle passing through the centers of the multiple holes to an area of one of the wafers being ground greater than or equal to 1.33 but less than 2.0.

6. The device for grinding according to claim 5, wherein the ratio of an area of a circle passing through the centers of the multiple holes to an area of one of the wafers being ground is greater than or equal to 1.33 but less than or equal to 1.5.

Fig. 1

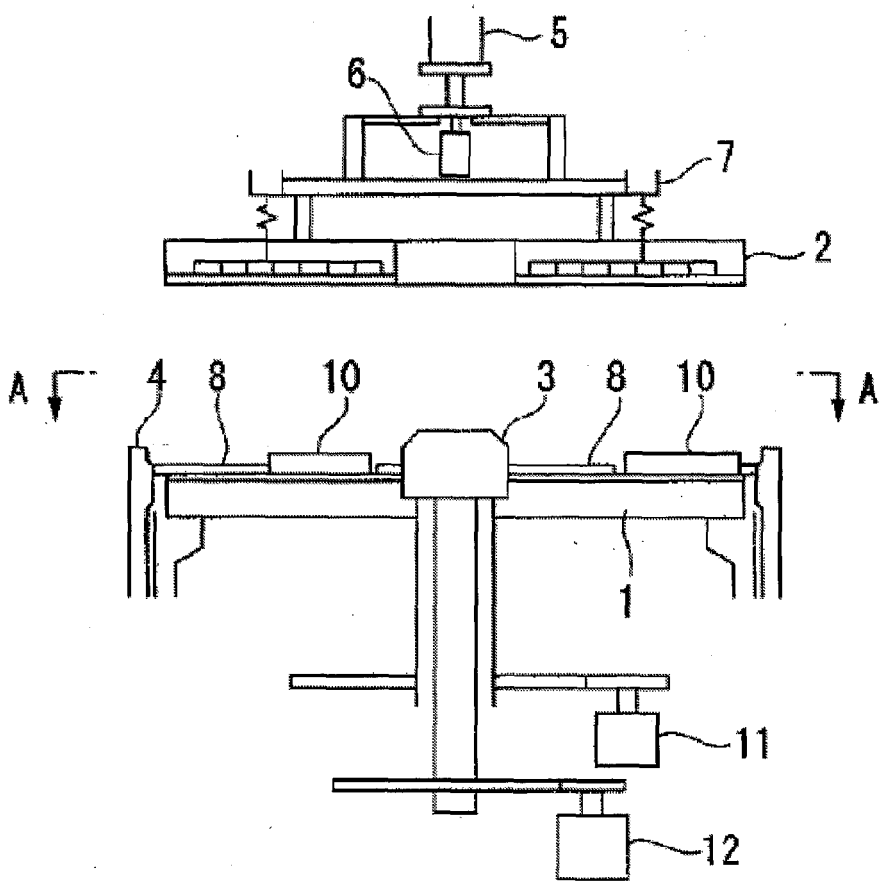


Fig. 2

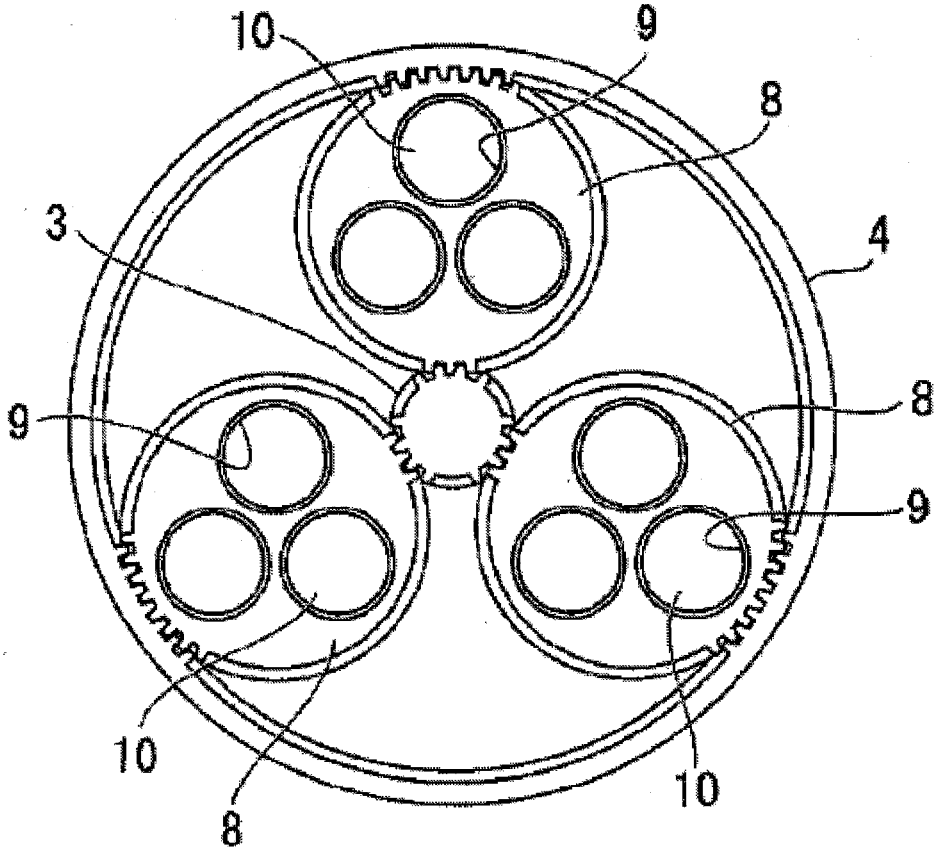
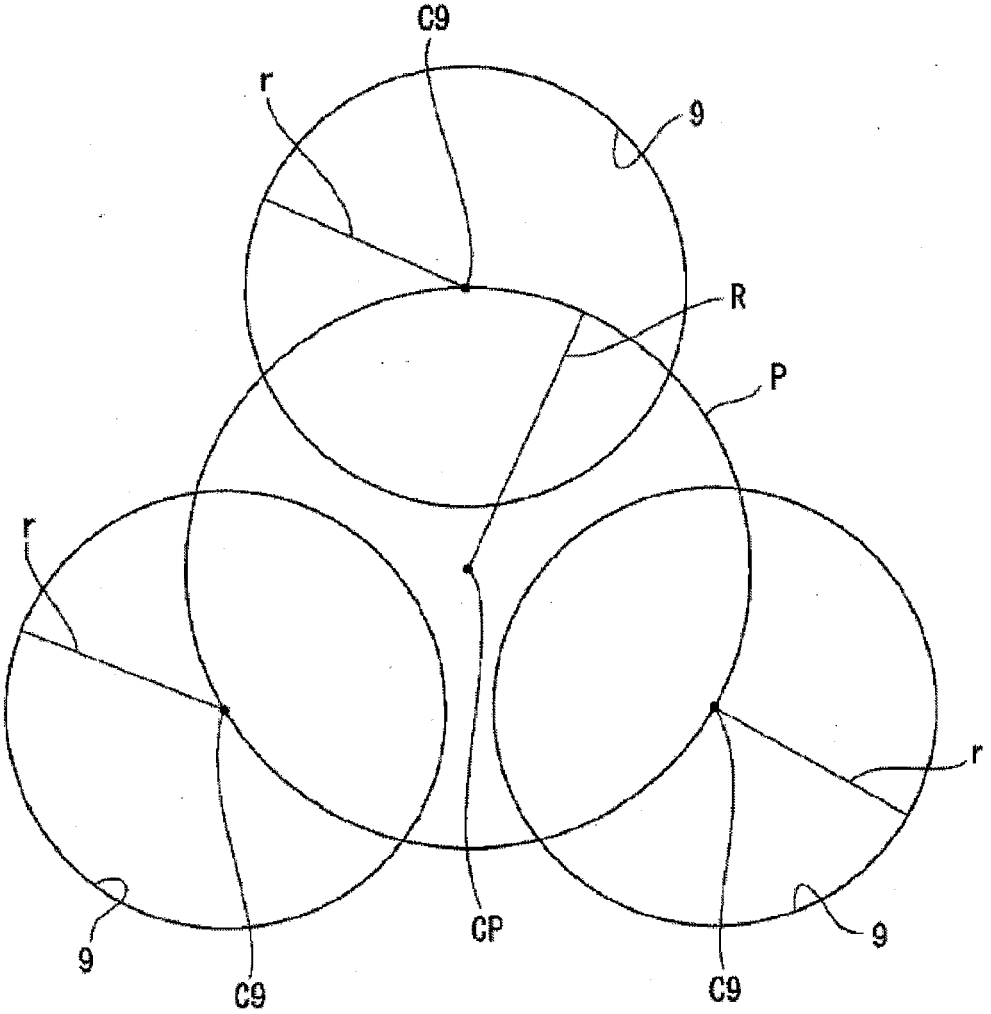


Fig. 3



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EUROPEAN SEARCH REPORT

Application Number
EP 09 16 1077

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (IPC)
A	US 4 996 798 A (MOORE STEVEN C [US]) 5 March 1991 (1991-03-05) * column 2, line 30 - line 39 * -----	1-6	INV. B24B37/04

TECHNICAL FIELDS SEARCHED (IPC)

B24B

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
The Hague	3 September 2009	Eschbach, Dominique

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
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E : earlier patent document, but published on, or after the filing date
D : document cited in the application
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.....
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2

EPO FORM 1503 03.82 (P04C01)

ANNEX TO THE EUROPEAN SEARCH REPORT ON EUROPEAN PATENT APPLICATION NO. EP 09 16 1077

This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report. The members are as contained in the European Patent Office EDP file on
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03-09-2009

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
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EPO FORM P0459

For more details about this annex : see Official Journal of the European Patent Office, No. 12/82

REFERENCES CITED IN THE DESCRIPTION

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