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(54) **LINEAR VOLTAGE REGULATOR**

LINEAR-SPANNUNGSREGLER

RÉGULATEUR DE TENSION LINÉAIRE

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(73) Proprietor: **International Business Machines Corporation**
Armonk, NY 10504 (US)

(72) Inventor: **KIM, Seongwon**
Old Tappan, New Jersey 07675 (US)

(74) Representative: **Ling, Christopher John**
IBM United Kingdom Limited
Intellectual Property Department
Hursley Park
Winchester
Hampshire SO21 2JN (GB)

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EP 2 183 653 B1

Description

FIELD OF THE INVENTION

[0001] This application relates to a linear voltage regulator.

BACKGROUND OF THE INVENTION

[0002] Voltage regulators have been utilized to control voltages applied to devices. A problem with the voltage regulators is that the voltage regulators have not been able to effectively remove both high frequency noise and low frequency noise from a voltage source. Further, the voltage regulators utilize at least two relatively expensive comparator chips which utilize a relatively large amount of power (see e.g. US2007/0188154)

[0003] Accordingly, the inventor herein has recognized a need for an improved voltage regulator that minimizes and/or eliminates the above-mentioned problems.

DISCLOSURE OF THE INVENTION

[0004] A linear voltage regulator in accordance with an exemplary embodiment is provided. The linear voltage regulator includes a first circuit configured to receive the first voltage from a voltage source and to remove frequency components of the first voltage in a first frequency range to obtain an output voltage at a primary output node. The linear voltage regulator further includes a second circuit having first and second inverters electrically coupled to the primary output node of the first circuit. The second circuit is configured to receive the output voltage and to remove frequency components of the output voltage in a second frequency range. The second frequency range is greater than the first frequency range.

[0005] A linear voltage regulator in accordance with another exemplary embodiment is provided. The linear voltage regulator includes a first inverter having a first input terminal and a first output terminal. The first input terminal is electrically coupled to the first output terminal. The first input terminal is further electrically coupled to a capacitor which is further coupled to electrical ground. The first inverter is further electrically coupled to a primary output node such a first voltage on the first output terminal is less than the output voltage at the primary output node. The linear voltage regulator further includes a second inverter having a second input terminal and a second output terminal. The second input terminal is electrically coupled to the first output terminal of the first inverter. The second inverter is further electrically coupled to the primary output node and receiving the first voltage from the first inverter. The linear voltage regulator further includes a p-channel field effect transistor (P-FET transistor) having a gate terminal, a drain terminal and a source terminal. The source terminal is electrically coupled to a voltage source. The drain terminal is coupled to the primary output node. The gate terminal electrically communicates either directly or indirectly with the second output terminal of the second inverter, such that when the output voltage at the primary output node is increased, the first voltage on the first output terminal of the first inverter is less than the output voltage on the primary output node which induces the second inverter to output a high logic voltage on the second output terminal. The P-FET transistor reduces the output voltage on the primary output node in response to the high logic voltage.

BRIEF DESCRIPTION OF THE DRAWINGS

[0006]

Figure 1 is an electrical schematic of an electrical system having a linear voltage regulator in accordance with an exemplary embodiment;

Figure 2 is an electrical schematic of a comparator circuit utilized in the linear voltage regulator of Figure 1;

Figure 3 is an electrical schematic of a plurality of inverters utilized in the linear voltage regulator of Figure 1;

Figure 4 is a schematic of a voltage signal output by a voltage source in the electrical system of Figure 1;

Figure 5 is a schematic of a voltage signal output on a primary output node of the linear voltage regulator of Figure 1;

Figure 6 is a schematic of a voltage signal output on a node in the comparator circuit of Figure 2;

Figure 7 is a schematic of a voltage signal output on a PFET transistor utilized in the linear voltage regulator of Figure 1; and

Figures 8-9 are flowcharts of a method for regulating a voltage using the linear voltage regulator of Figure 1 in accordance with another exemplary embodiment.

DESCRIPTION OF EMBODIMENTS

[0007] Referring to Figure 1, an electrical system 10 having a linear voltage regulator 14 in accordance with an exemplary embodiment is illustrated. The electrical system further includes a voltage source 12 and a load 18. An advantage of the linear voltage regulator 14 is that the regulator is able to output a voltage that has minimal voltage deviation for voltage-sensitive load devices.

[0008] The voltage source 12 is provided to output a voltage that may deviate from a desired voltage level. The voltage source 12 is electrically coupled to the linear voltage regulator 14.

[0009] The linear voltage regulator 14 is provided to receive the voltage from the voltage source 12 and to output a voltage that minimal voltage deviation from a desired voltage level. The linear voltage regulator 14 includes a circuit 20 and a circuit 22.

[0010] The circuit 20 is provided to remove frequency components of the voltage received from voltage source 12 in a first frequency range to obtain an output voltage at the primary voltage node 36 with reduced voltage deviation. In one exemplary embodiment, the circuit 20 is configured to remove frequency components of the voltage received from the voltage source 12 in the frequency range of 0 to 10 Megahertz. Of course, in alternative embodiments of circuit 20, the circuit 20 can remove frequency components in other frequency ranges. The circuit 20 includes a voltage reference device 30, an operational amplifier 32, and a P-FET transistor 34. The operational amplifier 32 has an inverting input terminal "-", a non-inverting input terminal "+", and an output terminal. The P-FET transistor has a gate terminal (G1), a source terminal (S1), and a drain terminal (D1). The voltage reference device 30 is electrically connected to the inverting input terminal "-" of the operational amplifier 32. The voltage reference device 30 is configured to output a desired reference voltage level. The output terminal of the operational amplifier 32 is electrically coupled to the gate terminal (G1) of the P-FET transistor 34. The non-inverting terminal "+" of the operational amplifier 32 is electrically coupled to the drain terminal (D1) of the P-FET transistor 34 and further coupled to the primary output node 36.

[0011] During operation of the circuit 20, when the output voltage of the voltage source 12 decreases, the voltage received by the non-inverting terminal "+" of the operational amplifier 32 has a low logic voltage relative to a high logic voltage on the inverting terminal "-", which induces the operational amplifier 32 to output a low logic voltage. In response to the low logic voltage on the gate terminal (G1) of the P-FET transistor 34, the P-FET transistor 34 increases current flowing from the source terminal (S1) to the drain terminal (D1) which causes the output voltage on the primary output node 36 to increase. Alternately, when the output voltage of the voltage source 12 increases, the voltage received by the non-inverting terminal "+" of the operational amplifier 32 has a high logic voltage relative to a low logic voltage on the inverting terminal "-", which induces the operational amplifier 32 to output a high logic voltage. In response to the high logic voltage on the gate terminal (G1) of the P-FET transistor 34, the P-FET transistor 34 decreases current flowing from the source terminal (S1) to the drain terminal (D1) which causes the output voltage on the primary output node 36 to decrease.

[0012] The circuit 22 is provided to remove frequency components of the voltage received from voltage source 12 in a second frequency range to obtain an output voltage at the primary voltage node 36 with reduced voltage deviation. In one exemplary embodiment, the circuit 22 is configured to remove frequency components of the voltage received from the voltage source 12 in the frequency range of 10 Megahertz to 6 Gigahertz. Of course, in alternative embodiments of circuit 22, the circuit 22 can remove frequency components in other frequency ranges. The circuit 22 includes a comparator circuit 62, 50, inverters 52, 54, 56, 58, 60, and a P-FET transistor 62.

[0013] Referring to Figures 1 and 2, the comparator circuit 50 is provided to detect a voltage deviation on the primary output node 36. The comparator circuit 50 includes inverters 80, 82 and a capacitor 84.

[0014] The inverter 80 includes a P-FET transistor 90, a FET transistor 92, an input terminal 94, and an output terminal 96. The P-FET transistor 90 includes a gate terminal (G3), a source terminal (S3), and a drain terminal (D3). The FET transistor 92 includes a gate terminal (G4), a source terminal (S4), and a drain terminal (D4). The P-FET transistor 90 is electrically coupled to the FET transistor 92. In particular, the gate terminals (G3), (G4) are electrically coupled together at the input terminal 94. The source terminal (S3) is electrically coupled to the primary output node 36. The drain terminal (D3) is electrically coupled to the source terminal (S4) at the output terminal 96. The output terminal 96 is electrically coupled to the input terminal 94. The terminal (D4) is electrically coupled to electrical ground. The capacitor 84 is electrically coupled between the input terminal 94 and electrical ground. During operation, a voltage on the output terminal 96 is less than the output voltage at the primary output node 36. In particular, a voltage on the output terminal 96 is approximately one-half of the voltage at the primary output node 36.

[0015] The inverter 82 includes a P-FET transistor 100, a FET transistor 102, an input terminal 104, and an output terminal 106. The P-FET transistor 100 includes a gate terminal (G5), a source terminal (S5), and a drain terminal (D5). The FET transistor 102 includes a gate terminal (G6), a source terminal (S6), and a drain terminal (D6). The P-FET transistor 100 is electrically coupled to the FET transistor 102. In particular, the gate terminals (G5), (G6) are electrically coupled together at the input terminal 104. The input terminal 104 is electrically coupled to the output terminal 96. The source terminal (S5) is electrically coupled to the primary output node 36. The drain terminal (D5) is electrically coupled to the source terminal (S6) at the output terminal 106. The output terminal 106 is electrically coupled to an input terminal 114. The terminal (D6) is electrically coupled to electrical ground.

[0016] During operation of the comparator circuit 50, when an output voltage at the primary output node 36 is increased, the voltage on the output terminal 96 of the inverter 80 is less than the output voltage on the primary output node 36 which induces the inverter 82 to output a high logic voltage on the output terminal 106. The high logic voltage is utilized to subsequently induce the P-FET transistor 62 to reduce the output voltage on the primary output node 36 in response to the high logic voltage. Alternately, when the output voltage at the primary output node 36 is decreased, the voltage on the output terminal

96 of the inverter 80 is greater than the output voltage on the primary output node 36 which induces the inverter 82 to output a low logic voltage on the output terminal 106. The low logic voltage is subsequently utilized to induce the P-FET transistor 62 to increase the output voltage on the primary output node 36 in response to the low logic voltage.

[0017] Referring to Figures 1 and 3, the chain of inverters 52, 54, 56, 58, 60 are provided to amplify the output voltage from the comparator circuit 50 which is received by the gate terminal (G2) of the P-FET transistor 62.

[0018] The inverter 52 includes a P-FET transistor 110, a FET transistor 112, an input terminal 114, and an output terminal 116. The P-FET transistor 110 includes a gate terminal (G7), a source terminal (S7), and a drain terminal (D7). The FET transistor 112 includes a gate terminal (G8), a source terminal (S8), and a drain terminal (D8). The P-FET transistor 110 is electrically coupled to the FET transistor 112. In particular, the gate terminals (G7), (G8) are electrically coupled together at the input terminal 114. The source terminal (S7) is electrically coupled to the primary output node 36. The drain terminal (D7) is electrically coupled to the source terminal (S8) at the output terminal 116. The output terminal 116 is electrically coupled to an input terminal 124. The terminal (D8) is electrically coupled to electrical ground. During operation, the inverter 52 receives an output voltage at the input terminal 114 from the comparator circuit 50 and outputs an inverted amplified output voltage at the output terminal 116.

[0019] The inverter 54 includes a P-FET transistor 120, a FET transistor 122, an input terminal 124, and an output terminal 126. The P-FET transistor 120 includes a gate terminal (G9), a source terminal (S9), and a drain terminal (D9). The FET transistor 122 includes a gate terminal (G10), a source terminal (S10), and a drain terminal (D10). The P-FET transistor 120 is electrically coupled to the FET transistor 122. In particular, the gate terminals (G9), (G10) are electrically coupled together at the input terminal 124. The source terminal (S9) is electrically coupled to the primary output node 36. The drain terminal (D9) is electrically coupled to the source terminal (S10) at the output terminal 126. The output terminal 126 is electrically coupled to an input terminal 134. The terminal (D10) is electrically coupled to electrical ground. During operation, the inverter 54 receives an output voltage at the input terminal 124 from the inverter 52 and outputs an inverted amplified output voltage at the output terminal 126.

[0020] The inverter 56 includes a P-FET transistor 130, a FET transistor 132, an input terminal 134, and an output terminal 136. The P-FET transistor 130 includes a gate terminal (G11), a source terminal (S11), and a drain terminal (D11). The FET transistor 132 includes a gate terminal (G 12), a source terminal (S12), and a drain terminal (D 12). The P-FET transistor 130 is electrically coupled to the FET transistor 132. In particular, the gate terminals (G11), (G12) are electrically coupled together at the input terminal 134. The source terminal (S11) is electrically coupled to the primary output node 36. The drain terminal (D11) is electrically coupled to the source terminal (S12) at the output terminal 136. The output terminal 136 is electrically coupled to an input terminal 144. The terminal (D12) is electrically coupled to electrical ground. During operation, the inverter 56 receives an output voltage at the input terminal 134 from the inverter 54 and outputs an inverted amplified output voltage at the output terminal 136.

[0021] The inverter 58 includes a P-FET transistor 140, a FET transistor 142, an input terminal 144, and an output terminal 146. The P-FET transistor 140 includes a gate terminal (G 13), a source terminal (S13), and a drain terminal (D13). The FET transistor 142 includes a gate terminal (G14), a source terminal (S14), and a drain terminal (D14). The P-FET transistor 140 is electrically coupled to the FET transistor 142. In particular, the gate terminals (G13), (G14) are electrically coupled together at the input terminal 144. The source terminal (S13) is electrically coupled to the primary output node 36. The drain terminal (D13) is electrically coupled to the source terminal (S14) at the output terminal 146. The output terminal 146 is electrically coupled to an input terminal 154. The terminal (D14) is electrically coupled to electrical ground. During operation, the inverter 58 receives an output voltage at the input terminal 144 from the inverter 56 and outputs an inverted amplified output voltage at the output terminal 146.

[0022] The inverter 60 includes a P-FET transistor 150, a FET transistor 152, an input terminal 154, and an output terminal 156. The P-FET transistor 150 includes a gate terminal (G 15), a source terminal (S15), and a drain terminal (D15). The FET transistor 152 includes a gate terminal (G16), a source terminal (S16), and a drain terminal (D 16). The P-FET transistor 150 is electrically coupled to the FET transistor 152. In particular, the gate terminals (G15), (G16) are electrically coupled together at the input terminal 154. The source terminal (S15) is electrically coupled to the primary output node 36. The drain terminal (D15) is electrically coupled to the source terminal (S16) at the output terminal 156. The output terminal 156 is electrically coupled to a gate terminal (G2) of the P-FET transistor 62. The terminal (D16) is electrically coupled to electrical ground. During operation, the inverter 60 receives an output voltage at the input terminal 154 from the inverter 58 and outputs an inverted amplified output voltage at the output terminal 156.

[0023] It should be noted that in an alternative embodiment, the linear voltage regulator 14 could be constructed by removing inverters 52, 54, 56, 58, 60 where inverter 82 would be directly electrically coupled to the P-FET transistor 62. Further, in other alternative embodiments, the number of inverters in the chain of inverters to amplify the voltage from the comparator circuit 50 can be greater than or less than the number of inverters shown in the chain of inverters of Figure 1.

[0024] Referring to Figure 1, the P-FET transistor 62

is provided to remove voltage deviations at the primary output node 36. In particular, the P-FET transistor 62 is provided to remove frequency components of the output voltage in a second frequency range. The P-FET transistor 62 includes a gate terminal (G2), a source terminal (S2), and a drain terminal (D2). The gate terminal (G2) is electrically coupled to the output terminal 156 of the inverter 60. The source terminal (S2) is electrically coupled to the voltage source 12. The drain terminal (D2) is electrically coupled to the primary node 36. The resistor 18 is electrically between the primary output node 36 and electrical ground. The resistor 18 corresponds to a load receiving the output voltage from the linear voltage regulator 14. During operation, when the P-FET transistor 62 receives a high logic voltage from the inverter 60 at the gate terminal (G2), the P-FET transistor 62 decreases current flowing therethrough to reduce the output voltage on the primary output node 36 in response to the high logic voltage. Alternately, when the P-FET transistor 62 receives a low logic voltage from the inverter 60 at the gate terminal (G2), the P-FET transistor 62 increases current flowing therethrough to increase the output voltage on the primary output node 36 in response to the low logic voltage.

[0025] Referring to Figures 4-7, a brief explanation of exemplary schematics of signals generated by the linear voltage regulator 14 will now be provided. Referring to Figure 4, a voltage curve 170 corresponds to an exemplary output voltage generated by the voltage source 12. As shown, the voltage curve 170 has oscillatory shape over time. Referring to Figure 5, a voltage curve 180 corresponds to an output voltage generated by the linear voltage regulator 14 at the primary output node 36. As shown, the voltage curve 180 is relatively constant over time as desired. Referring to Figure 6, a voltage curve 190 corresponds to an output voltage at the output terminal 96 of the comparator 50. Referring to Figure 7, a voltage curve 200 corresponds to a voltage received at the gate terminal (G2) of the P-FET transistor 62 for controlling operation of the P-FET transistor 62.

[0026] Referring to Figures 8-9, a flowchart of a method for regulating a voltage utilizing the linear voltage regulator 14 will now be described.

[0027] At step 220, the circuit 20 of the linear voltage regulator 14 receives a first voltage from the voltage source 12. The circuit 20 has the primary output node 36.

[0028] At step 222, the circuit 20 removes frequency components of the first voltage in a first frequency range to obtain an output voltage at the primary output node 36.

[0029] At step 224, the circuit 22 of the linear voltage regulator 14 has inverters 80, 82 electrically coupled either directly or indirectly to the primary output node 36 to remove frequency components of the output voltage in a second frequency range. The second frequency range is greater than the first frequency range. The step 224 is implemented utilizing steps 230-240.

[0030] At step 230, the inverter 80 outputs a second voltage on the output terminal 96 that is less than the output voltage on the primary output node 36, when the output voltage at the primary output node 36 is increased.

[0031] At step 232, the inverter 82 outputs a high logic voltage on the output terminal 106 in response to the second voltage being less than the output voltage.

[0032] At step 234, the P-FET transistor 62 reduces the output voltage on the primary output node 36 in response to the high logic voltage.

[0033] At step 236, the inverter 80 outputs the second voltage on the output terminal 96 that is greater than the output voltage on the primary output node 36, when the output voltage at the primary output node 36 is decreased.

[0034] At step 238, the inverter 82 outputs a low logic voltage on the output terminal 106 in response to the second voltage being greater than the output voltage.

[0035] At step 240, the P-FET transistor 62 increases the output voltage on the primary output node 36 in response to the low logic voltage. After step 240, the method returns to step 220.

[0036] The linear voltage regulator provides a substantial advantage over other regulators. In particular, the linear voltage regulator provides a technical effect of removing highfrequency components of a voltage utilizing a plurality of inverters.

[0037] While the invention is described with reference to an exemplary embodiment, it will be understood by those skilled in the art that various changes may be made and equivalent elements may be substituted for elements thereof without departing from the scope of the invention. In addition, many modifications may be made to the teachings of the invention to adapt to a particular situation without departing from the scope thereof. Therefore, it is intended that the invention not be limited the embodiment disclosed for carrying out this invention, but that the invention includes all embodiments falling with the scope of the intended claims. Moreover, the use of the term's first, second, etc. does not denote any order of importance, but rather the term's first, second, etc. are used to distinguish one element from another.

Claims

1. A linear voltage regulator, comprising:

a first circuit (20) configured to receive a first voltage from a voltage source and to remove frequency components of the first voltage in a first frequency range to obtain an output voltage at a primary output node; and

a second circuit (22) having first and second inverters electrically coupled to the primary output node of the first circuit, the second circuit configured to receive the output voltage and to remove frequency components of the output voltage in a second frequency range, the frequencies in the second frequency range being higher

than the frequencies in the first frequency range; the first inverter having a first input terminal and a first output terminal, the first input terminal being electrically coupled to the first output terminal, the first input terminal being further electrically coupled to a capacitor which is further coupled to electrical ground, the first inverter being further electrically coupled to the primary output node such a second voltage on the first output terminal is less than the output voltage at the primary output node; and
the second inverter having a second input terminal and a second output terminal, the second input terminal being electrically coupled to the first output terminal of the first inverter, the second inverter being further electrically coupled to the primary output node; and the second circuit further comprising a P-FET (62) transistor having a gate terminal, a drain terminal and a source terminal, the source terminal being electrically coupled to the voltage source, the drain terminal being electrically coupled to the primary output node, the gate terminal electrically communicating either directly or indirectly with the second output terminal of the second inverter, such that when the output voltage at the primary output node is increased, the second voltage on the first output terminal of the first inverter is less than the output voltage on the primary output node which induces the second inverter to output a high logic voltage on the second output terminal, and the P-FET transistor reduces the output voltage on the primary output node in response to the high logic voltage.

2. The linear voltage regulator of claim 1, wherein when the output voltage at the primary output node is decreased, the second voltage on the first output terminal of the first inverter is greater than the output voltage on the primary output node which induces the second inverter to output a low logic voltage on the second output terminal, and the P-FET transistor increases the output voltage on the primary output node in response to the low logic voltage.

3. The linear voltage regulator of claim 1, further comprising at least third and fourth inverters electrically coupled in series between the second output terminal of the second inverter and the gate terminal of the P-FET transistor.

4. The linear voltage regulator of claim 1, wherein the first frequency range is 0 to 10 Megahertz.

5. The linear voltage regulator of claim 1, wherein the second frequency range is 10 Megahertz to 6 Gigahertz.

6. A method for regulating a voltage using a linear voltage regulator, the linear voltage regulator having a first circuit (20) with a primary output node and a second circuit (22) having first and second inverters electrically coupled to the primary output node, the method comprising:

receiving a first voltage from a voltage source at the first circuit;
removing frequency components of the first voltage in a first frequency range to obtain an output voltage at the primary output node utilizing the first circuit; and
removing frequency components of the output voltage in a second frequency range utilizing the first and second inverters of the second circuit, the second frequency range being greater than the first frequency range;
the second circuit further including a P-FET transistor (62), the first inverter having a first input terminal and a first output terminal, the first input terminal being electrically coupled to the first output terminal, the first input terminal being further electrically coupled to a capacitor which is further coupled to electrical ground, the first inverter being further electrically coupled to the primary output node, the second inverter having a second input terminal and a second output terminal, the second input terminal being electrically coupled to the first output terminal of the first inverter, the second inverter being further electrically coupled to the primary output node, the P-FET transistor having a gate terminal, a drain terminal and a source terminal, the source terminal being electrically coupled to the voltage source, the drain terminal being electrically coupled to the primary output node, the gate terminal electrically communicating either directly or indirectly with the second output terminal of the second inverter, wherein removing frequency components of the output voltage in the second frequency range utilizing the second circuit, comprises:

outputting a second voltage on the first output terminal of the first inverter that is less than the output voltage on the primary output node, when the output voltage at the primary output node is increased;
outputting a high logic voltage from the second inverter on the second output terminal in response to the second voltage being less than the output voltage; and
reducing the output voltage on the primary output node in response to the high logic voltage utilizing the P-FET transistor.

7. The method of claim 6, wherein removing frequency

components of the output voltage in the second frequency range utilizing the second circuit, further comprises:

outputting the second voltage on the first output terminal of the first inverter that is greater than the output voltage on the primary output node, when the output voltage at the primary output node is decreased;
outputting a low logic voltage from the second inverter on the second output terminal in response to the second voltage being greater than the output voltage; and
increasing the output voltage on the primary output node in response to the low logic voltage utilizing the P-FET transistor.

8. The method of claim 6, wherein the first frequency range is 0 to 10 Megahertz.

9. The method of claim 6, wherein the second frequency range is 10 Megahertz to 6 Gigahertz.

Patentansprüche

1. Linearer Spannungsregler, aufweisend:

eine erste Schaltung (20), die so konfiguriert ist, dass sie eine erste Spannung von einer Spannungsquelle empfängt und Frequenzkomponenten der ersten Spannung in einem ersten Frequenzbereich entfernt, um eine Ausgangsspannung an einem primären Ausgangsknoten zu erhalten; und
eine zweite Schaltung (22) mit einem ersten und einem zweiten Inverter, die mit dem primären Ausgangsknoten der ersten Schaltung elektrisch verbunden sind, wobei die zweite Schaltung so konfiguriert ist, dass sie die Ausgangsspannung empfängt und Frequenzkomponenten der Ausgangsspannung in einem zweiten Frequenzbereich entfernt, wobei die Frequenzen im zweiten Frequenzbereich höher als die Frequenzen im ersten Frequenzbereich sind;
wobei der erste Inverter einen ersten Eingangsanschluss und einen ersten Ausgangsanschluss aufweist, wobei der erste Eingangsanschluss mit dem ersten Ausgangsanschluss elektrisch verbunden ist, wobei der erste Eingangsanschluss außerdem mit einem Kondensator elektrisch verbunden ist, der außerdem mit Masse verbunden ist, wobei der erste Inverter außerdem mit dem primären Ausgangsknoten elektrisch verbunden ist, so dass eine zweite Spannung am ersten Ausgangsanschluss niedriger als die Ausgangsspannung am primären Ausgangsknoten ist; und wobei der zweite Inverter einen zweiten Eingangsanschluss und einen zweiten Ausgangsanschluss aufweist, wobei der zweite Eingangsanschluss mit dem ersten Ausgangsanschluss des ersten Inverters elektrisch verbunden ist, wobei der zweite Inverter außerdem mit dem ersten Ausgangsknoten elektrisch verbunden ist; und
wobei die zweite Schaltung außerdem einen p-FET(62) mit einem Gate-Anschluss, einem Drain-Anschluss und einem Source-Anschluss aufweist, wobei der Source-Anschluss mit der Spannungsquelle elektrisch verbunden ist, wobei der Drain-Anschluss mit dem primären Ausgangsknoten elektrisch verbunden ist, wobei der Gate-Anschluss direkt oder indirekt mit dem zweiten Ausgangsanschluss des zweiten Inverters elektrisch in Verbindung steht, so dass, wenn die Ausgangsspannung am primären Ausgangsknoten erhöht wird, die zweite Spannung am ersten Ausgangsanschluss des ersten Inverters geringer als die Ausgangsspannung am primären Ausgangsknoten wird, was den zweiten Inverter veranlasst, eine einem logischem HIGH entsprechende Spannung am zweiten Ausgangsanschluss auszugeben, und der p-FET senkt als Reaktion auf die einem logischem HIGH entsprechende Spannung die Ausgangsspannung am primären Ausgangsknoten.

2. Linearer Spannungsregler nach Anspruch 1, wobei, wenn die Ausgangsspannung am primären Ausgangsknoten abgesenkt wird, die zweite Spannung am ersten Ausgangsanschluss des ersten Inverters größer als die Ausgangsspannung am primären Ausgangsknoten wird, was den zweiten Inverter veranlasst, eine einem logischen LOW entsprechende Spannung am zweiten Ausgangsanschluss auszugeben, und der p-FET erhöht als Reaktion auf die einem logischen LOW entsprechende Spannung die Ausgangsspannung am primären Ausgangsknoten.

3. Linearer Spannungsregler nach Anspruch 1, der außerdem mindestens einen dritten und einen vierten Inverter aufweist, die zwischen dem zweiten Ausgangsanschluss des zweiten Inverters und dem Gate-Anschluss des p-FETs in Reihe geschaltet sind.

4. Linearer Spannungsregler nach Anspruch 1, wobei sich der erste Frequenzbereich von 0 bis 10 Megahertz erstreckt.

5. Linearer Spannungsregler nach Anspruch 1, wobei sich der zweite Frequenzbereich von 10 Megahertz bis 6 Gigahertz erstreckt.

6. Verfahren zum Regeln einer Spannung unter Verwendung eines linearen Spannungsreglers, wobei der lineare Spannungsregler eine erste Schaltung

(20) mit einem ersten primären Ausgangsknoten und eine zweite Schaltung (22) mit einem ersten und einem zweiten Inverter aufweist, die mit dem primären Ausgangsknoten elektrisch verbunden sind, wobei das Verfahren aufweist:

Empfangen einer ersten Spannung von einer Spannungsquelle in der ersten Schaltung;
Entfernen von Frequenzkomponenten der ersten Spannung in einem ersten Frequenzbereich unter Verwendung der ersten Schaltung, um eine Ausgangsspannung am primären Ausgangsknoten zu erhalten; und
Entfernen von Frequenzkomponenten der Ausgangsspannung in einem zweiten Frequenzbereich unter Verwendung des ersten und des zweiten Inverters der zweiten Schaltung, wobei der zweite Frequenzbereich oberhalb des ersten Frequenzbereichs liegt;
wobei die zweite Schaltung außerdem einen p-FET (62) aufweist, wobei der erste Inverter einen ersten Eingangsanschluss und einen ersten Ausgangsanschluss aufweist, wobei der erste Eingangsanschluss mit dem ersten Ausgangsanschluss elektrisch verbunden ist, wobei der erste Eingangsanschluss außerdem mit einem Kondensator elektrisch verbunden ist, der außerdem mit Masse verbunden ist, wobei der erste Inverter außerdem mit dem primären Ausgangsknoten elektrisch verbunden ist, wobei der zweite Inverter einen zweiten Eingangsanschluss und einen zweiten Ausgangsanschluss aufweist, wobei der zweite Eingangsanschluss mit dem ersten Ausgangsanschluss des ersten Inverters elektrisch verbunden ist, wobei der zweite Inverter außerdem mit dem primären Ausgangsknoten elektrisch verbunden ist, wobei der p-FET Transistor einen Gate-Anschluss, einen Drain-Anschluss und einen Source-Anschluss aufweist, wobei der Source-Anschluss mit der Spannungsquelle elektrisch verbunden ist, wobei der Drain-Anschluss mit dem primären Ausgangsknoten elektrisch verbunden ist, wobei der Gate-Anschluss direkt oder
indirekt mit dem zweiten Ausgangsanschluss des zweiten Inverters elektrisch in Verbindung steht, wobei das Entfernen von Frequenzkomponenten der Ausgangsspannung im zweiten Frequenzbereich unter Verwendung der zweiten Schaltung aufweist:
bei Erhöhung der Ausgangsspannung am primären Ausgangsknoten Ausgeben einer zweiten Spannung am ersten Ausgangsanschluss des ersten Inverters, die niedriger als die Ausgangsspannung am primären Ausgangsknoten ist;
Ausgeben einer einem logischen HIGH entsprechenden Spannung am zweiten Ausgangsanschluss durch den zweiten Inverter als Reaktion darauf, dass die zweite Spannung niedriger als die Ausgangsspannung ist; und
Absenken der Ausgangsspannung am primären Ausgangsknoten als Reaktion auf die einem logischen HIGH entsprechende Spannung unter Verwendung des p-FETs.

7. Verfahren nach Anspruch 6, wobei das Entfernen von Frequenzkomponenten der Ausgangsspannung im zweiten Frequenzbereich unter Verwendung der zweiten Schaltung außerdem aufweist:

Ausgeben der zweiten Spannung am ersten Ausgangsanschluss des ersten Inverters, die höher als die Ausgangsspannung am primären Ausgangsanschluss ist, wenn die Ausgangsspannung am primären Ausgangsanschluss abgesenkt wird;
Ausgeben einer einem logischen LOW entsprechenden Spannung durch den zweiten Inverter am zweiten Ausgangsanschluss als Reaktion darauf, dass die zweite Spannung höher als die Ausgangsspannung ist; und
Erhöhen der Ausgangsspannung am primären Ausgangsknoten als Reaktion auf die einem logischen LOW entsprechende Spannung unter Verwendung des p-FETs.

8. Verfahren nach Anspruch 6, wobei sich der erste Frequenzbereich von 0 bis 10 Megahertz erstreckt.

9. Verfahren nach Anspruch 6, wobei sich der zweite Frequenzbereich von 10 Megahertz bis 6 Gigahertz erstreckt.

Revendications

1. Régulateur de tension linéaire, comprenant :

un premier circuit (20) configuré pour recevoir une première tension à partir d'une source de tension et pour supprimer des composantes de fréquence de la première tension dans une première plage de fréquences pour obtenir une tension de sortie au niveau d'un noeud de sortie primaire ; et
un second circuit (22) ayant un premier et un second inverseur connectés électriquement au noeud de sortie primaire du premier circuit, le second circuit étant configuré pour recevoir la tension de sortie et pour supprimer des composantes de fréquence de la tension de sortie dans une seconde plage de fréquences, les fréquences de la seconde plage de fréquences étant plus élevées que les fréquences de la première plage de fréquences ;

le premier inverseur ayant une première borne d'entrée et une première borne de sortie, la première borne d'entrée étant connectée électriquement à la première borne de sortie, la première borne d'entrée étant en outre connectée électriquement à un condensateur qui est en outre connecté à une mise électrique à la masse, le premier inverseur étant en outre connecté électriquement au noeud de sortie primaire de sorte qu'une seconde tension sur la première borne de sortie est inférieure à la tension de sortie au niveau du noeud de sortie primaire ; et

le second inverseur ayant une seconde borne d'entrée et une seconde borne de sortie, la seconde borne d'entrée étant connectée électriquement à la première borne de sortie du premier inverseur, le second inverseur étant en outre connecté électriquement au noeud de sortie primaire ; et

le second circuit comprenant en outre un transistor P-FET (62) ayant une borne de grille, une borne de drain et une borne de source, la borne de source étant connectée électriquement à la source de tension, la borne de drain étant connectée électriquement au noeud de sortie primaire, la borne de grille communiquant électriquement directement ou indirectement avec la seconde borne de sortie du second inverseur, de telle sorte que lorsque la tension de sortie au niveau du noeud de sortie primaire est augmentée, la seconde tension sur la première borne de sortie du premier inverseur est inférieure à la tension de sortie sur le noeud de sortie primaire, ce qui amène le second inverseur à délivrer en sortie une tension de niveau logique haut sur la seconde borne de sortie, et le transistor P-FET réduit la tension de sortie sur le noeud de sortie primaire en réponse à la tension de niveau logique haut.

2. Régulateur de tension linéaire selon la revendication 1, dans lequel, lorsque la tension de sortie au niveau du noeud de sortie primaire est diminuée, la seconde tension sur la première borne de sortie du premier inverseur est supérieure à la tension de sortie sur le noeud de sortie primaire, ce qui amène le second inverseur à délivrer en sortie une tension de niveau logique bas sur la seconde borne de sortie, et le transistor P-FET augmente la tension de sortie sur le noeud de sortie primaire en réponse à la tension de niveau logique bas.

3. Régulateur de tension linéaire selon la revendication 1, comprenant en outre au moins un troisième et un quatrième inverseur connectés électriquement en série entre la seconde borne de sortie du second inverseur et la borne de grille du transistor P-FET.

4. Régulateur de tension linéaire selon la revendication 1, dans lequel la première plage de fréquences est de 0 à 10 mégahertz.

5. Régulateur de tension linéaire selon la revendication 1, dans lequel la seconde plage de fréquences est de 10 mégahertz à 6 gigahertz.

6. Procédé de régulation d'une tension en utilisant d'un régulateur de tension linéaire, le régulateur de tension linéaire comportant un premier circuit (20) avec un noeud de sortie primaire, et un second circuit (22) comportant un premier et un second inverseur connectés électriquement au noeud de sortie primaire, le procédé comprenant :

la réception d'une première tension à partir d'une source de tension au niveau du premier circuit ;

la suppression des composantes de fréquence de la première tension dans une première plage de fréquences pour obtenir une tension de sortie au niveau du noeud de sortie primaire en utilisant le premier circuit ; et

la suppression des composantes de fréquence de la tension de sortie dans une seconde plage de fréquences en utilisant les premier et second inverseurs du second circuit, la seconde plage de fréquences étant supérieure à la première plage de fréquences ;

le second circuit incluant en outre un transistor P-FET (62), le premier inverseur ayant une première borne d'entrée et une première borne de sortie, la première borne d'entrée étant connectée électriquement à la première borne de sortie, la première borne d'entrée étant en outre connectée électriquement à un condensateur qui est en outre connecté à une mise électrique à la masse, le premier inverseur étant en outre connecté électriquement au noeud de sortie primaire, le second inverseur ayant une seconde borne d'entrée et une seconde borne de sortie, la seconde borne d'entrée étant connectée électriquement à la première borne de sortie du premier inverseur, le second inverseur étant en outre connecté électriquement au noeud de sortie primaire, le transistor P-FET ayant une borne de grille, une borne de drain et une borne de source, la borne de source étant connectée électriquement à la source de tension, la borne de drain étant connectée électriquement au noeud de sortie primaire, la borne de grille communiquant électriquement directement ou indirectement avec la seconde borne de sortie du second inverseur, dans lequel la suppression de composantes de fréquence de la tension de sortie dans la seconde plage de fréquences en utilisant le second circuit comprend : la livraison

en sortie d'une seconde tension sur la première borne de sortie du premier inverseur qui est inférieure à la tension de sortie sur le noeud de sortie primaire, lorsque la tension de sortie au niveau du noeud de sortie primaire est augmentée ;
la livraison en sortie d'une tension de niveau logique haut à partir du second inverseur sur la seconde borne de sortie en réponse au fait que la seconde tension soit inférieure à la tension de sortie ; et
la réduction de la tension de sortie sur le noeud de sortie primaire en réponse à la tension de niveau logique haut en utilisant le transistor P-FET.

7. Procédé selon la revendication 6, dans lequel la suppression de composantes de fréquence de la tension de sortie dans la seconde plage de fréquences en utilisant le second circuit comprend en outre :

la livraison en sortie de la seconde tension sur la première borne de sortie du premier inverseur qui est supérieure à la tension de sortie sur le noeud de sortie primaire, lorsque la tension de sortie au niveau du noeud de sortie primaire est diminuée ;
la livraison en sortie d'une tension de niveau logique bas à partir du second inverseur sur la seconde borne de sortie en réponse au fait que la seconde tension soit supérieure à la tension de sortie ; et l'augmentation de la tension de sortie sur le noeud de sortie primaire en réponse à la tension de niveau logique bas en utilisant le transistor P-FET.

8. Procédé selon la revendication 6, dans lequel la première plage de fréquences est de 0 à 10 mégahertz.

9. Procédé selon la revendication 6, dans lequel la seconde plage de fréquences est de 10 mégahertz à 6 gigahertz.

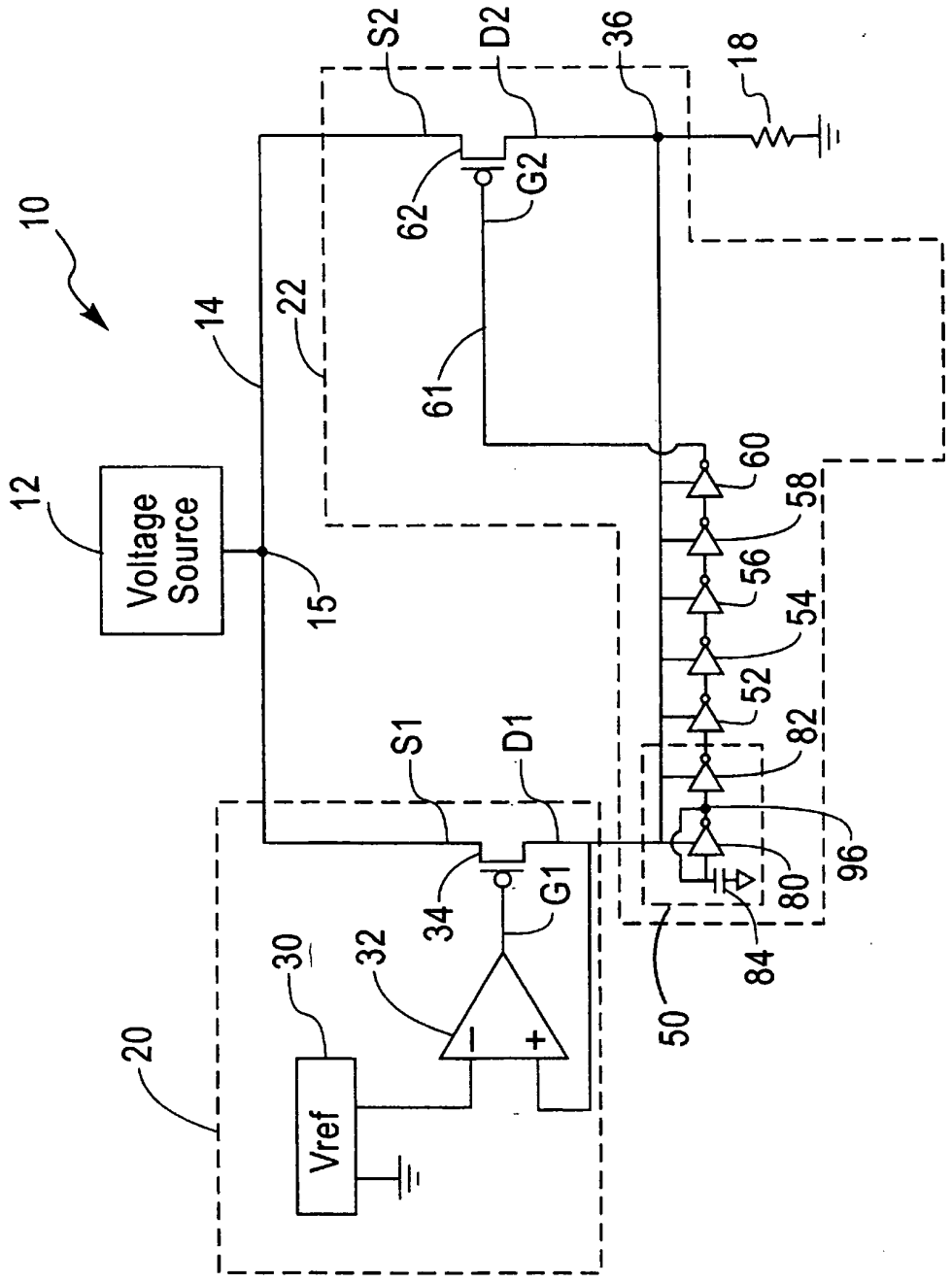
10
12
Voltage Source
14
15
18
20
22
30
32
34
36
50
52
54
56
58
60
61
62
80
82
84
96
S1
D1
G1
S2
D2
G2
Vref

FIG. 1

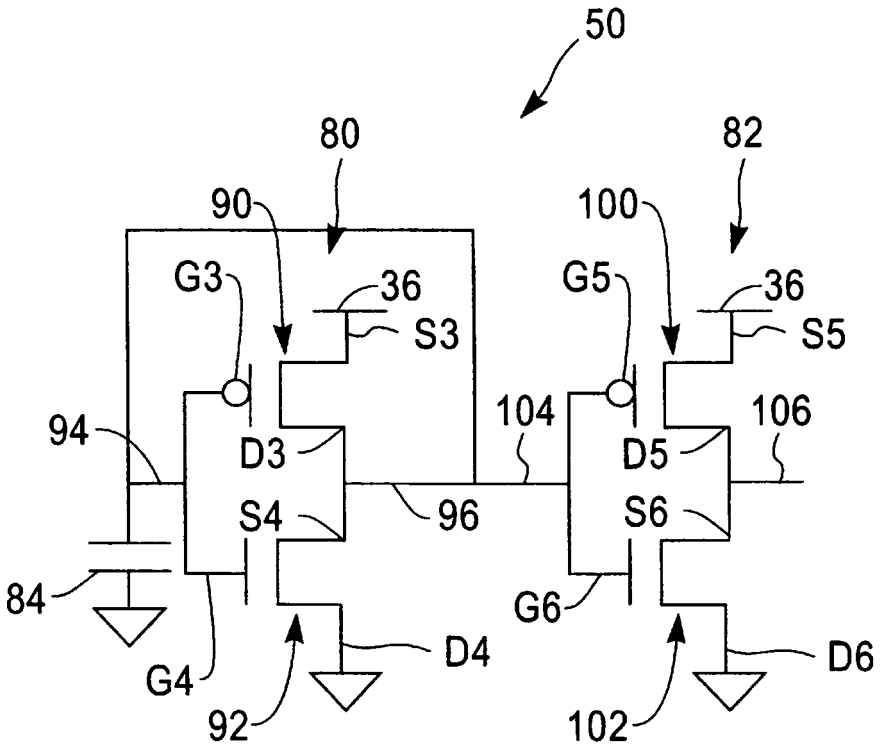
50
80
82
90
100
G3
36
S3
G5
36
S5
94
D3
104
D5
106
S4
96
S6
84
G6
G4
D4
D6
92
102

FIG. 2

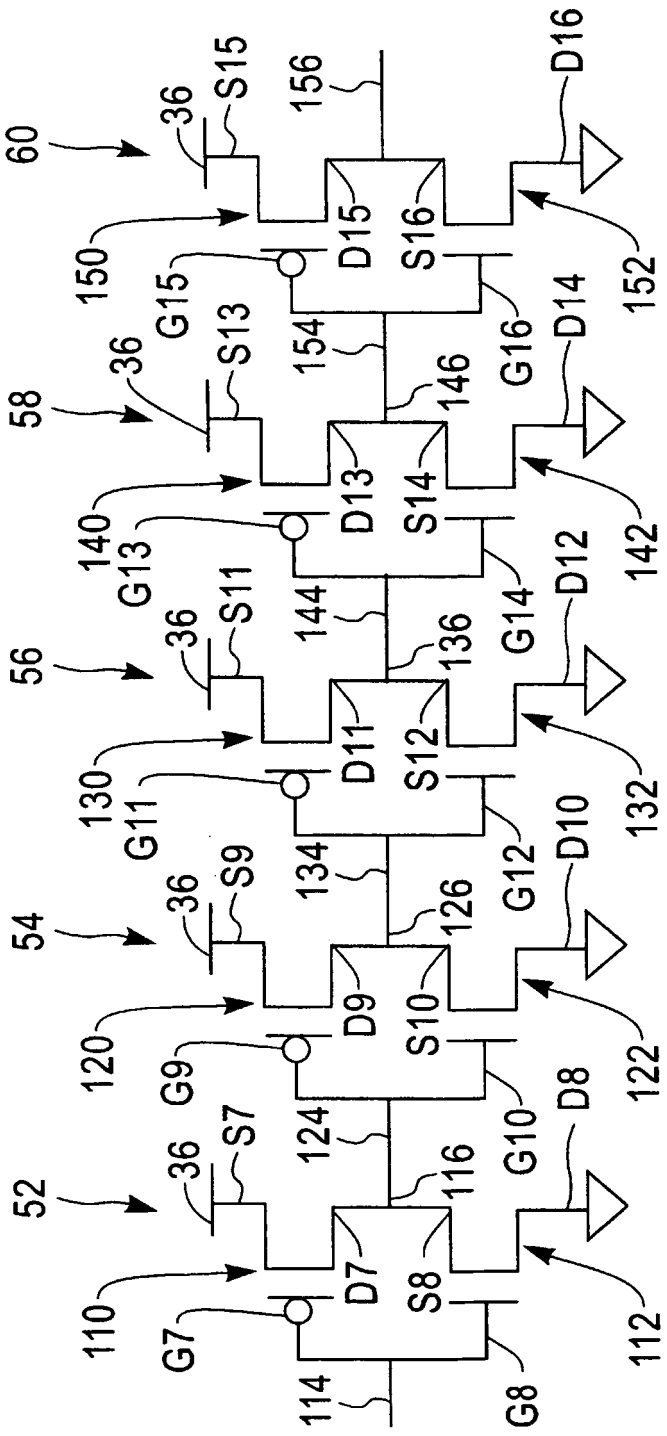
60
58
56
54
52
36
S15
S13
S11
S9
S7
D16
D14
D12
D10
D8
156
154
146
144
136
134
126
124
116
114
150
152
140
142
130
132
120
122
110
112
G15
G16
G13
G14
G11
G12
G9
G10
G7
G8
D15
S16
D13
S14
D11
S12
D9
S10
D7
S8

FIG. 3

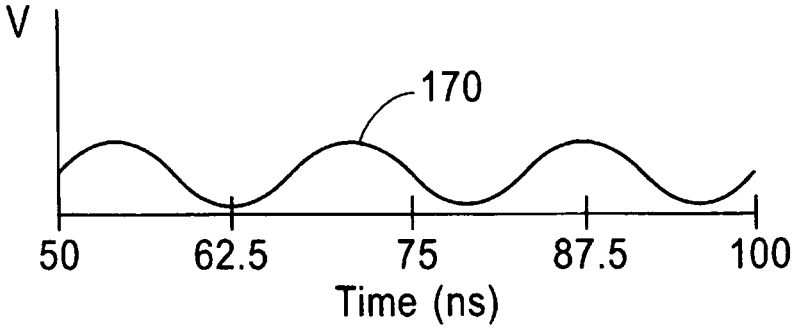

FIG. 4

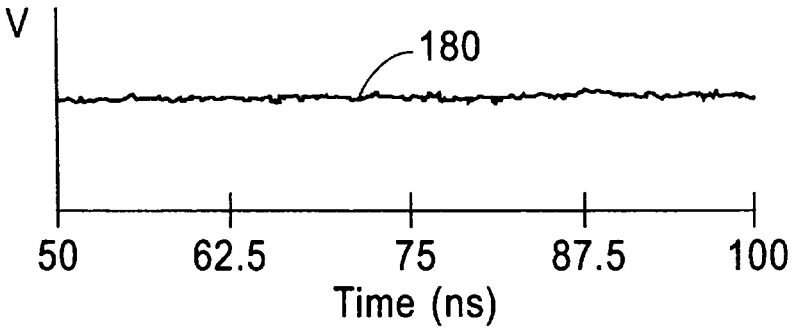

FIG. 5

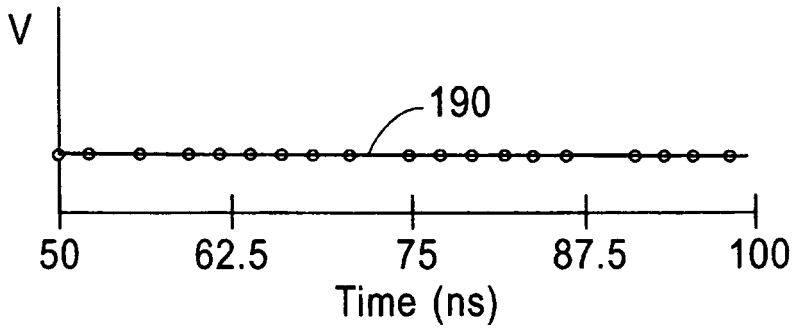

FIG. 6

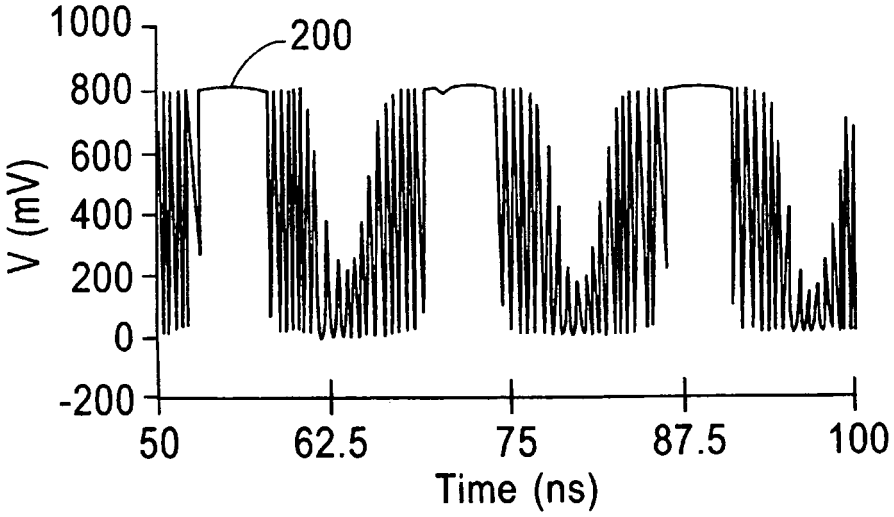

FIG. 7

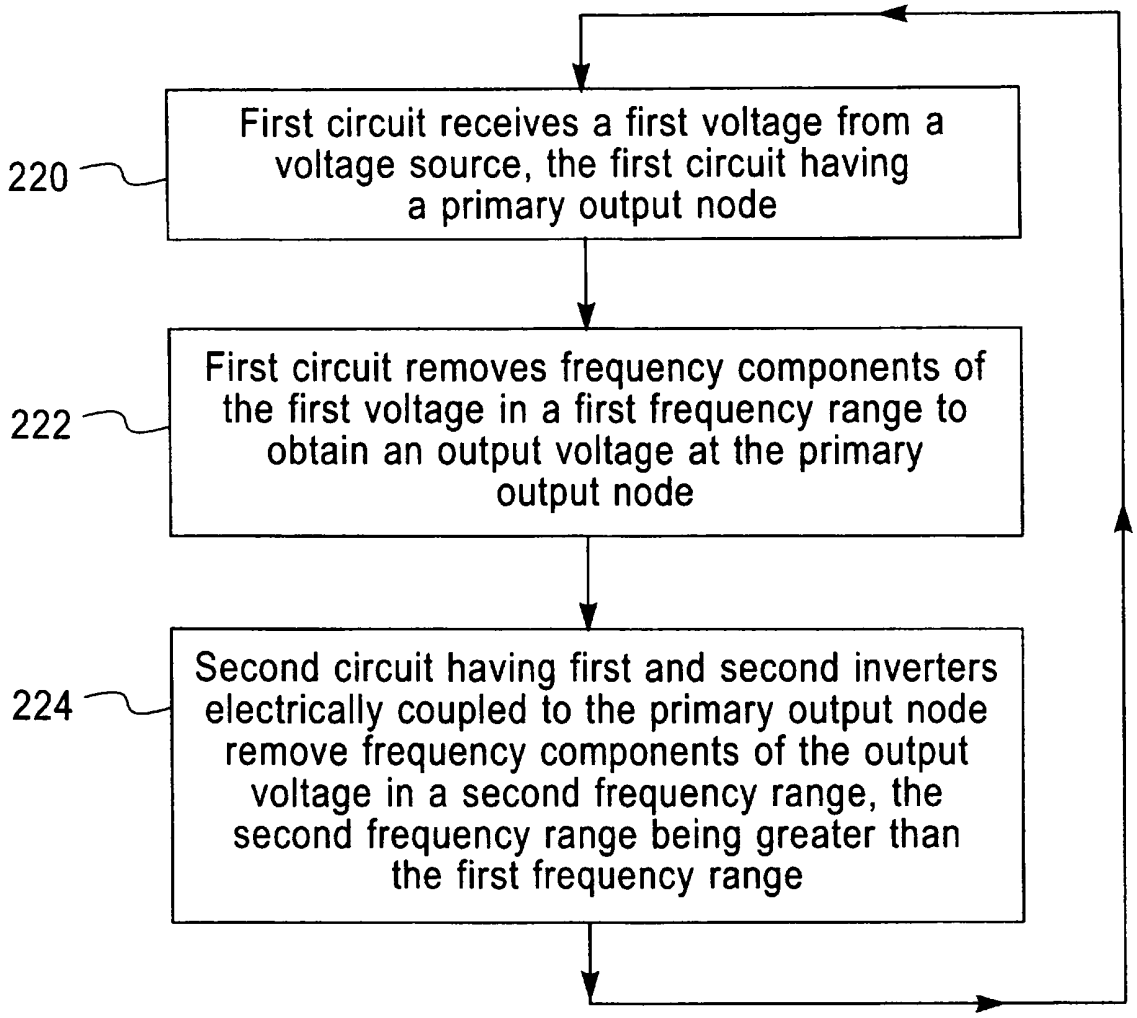
220
First circuit receives a first voltage from a voltage source, the first circuit having a primary output node
222
First circuit removes frequency components of the first voltage in a first frequency range to obtain an output voltage at the primary output node
224
Second circuit having first and second inverters electrically coupled to the primary output node remove frequency components of the output voltage in a second frequency range, the second frequency range being greater than the first frequency range

FIG. 8

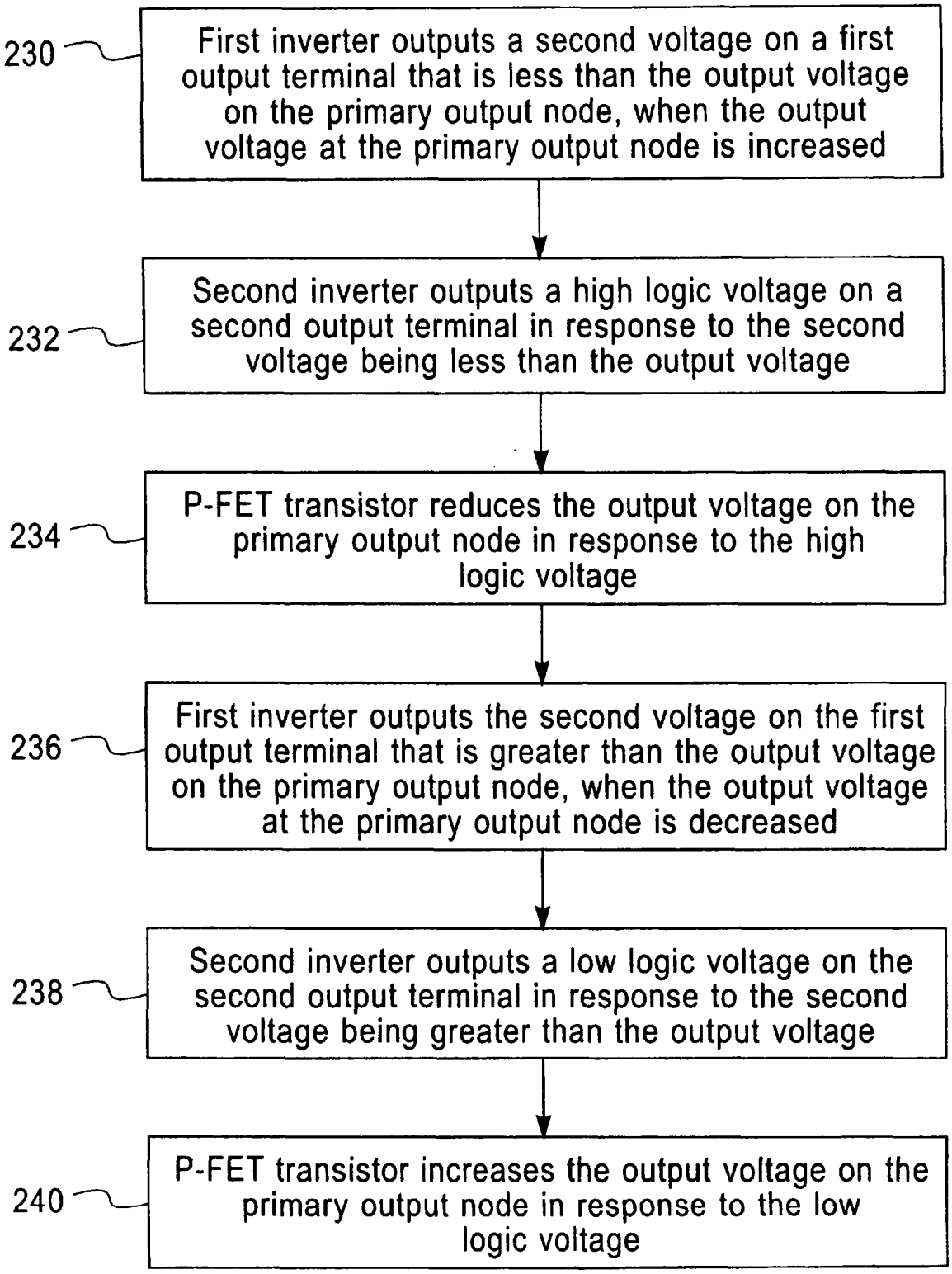
230
First inverter outputs a second voltage on a first output terminal that is less than the output voltage on the primary output node, when the output voltage at the primary output node is increased
232
Second inverter outputs a high logic voltage on a second output terminal in response to the second voltage being less than the output voltage
234
P-FET transistor reduces the output voltage on the primary output node in response to the high logic voltage
236
First inverter outputs the second voltage on the first output terminal that is greater than the output voltage on the primary output node, when the output voltage at the primary output node is decreased
238
Second inverter outputs a low logic voltage on the second output terminal in response to the second voltage being greater than the output voltage
240
P-FET transistor increases the output voltage on the primary output node in response to the low logic voltage

FIG. 9

REFERENCES CITED IN THE DESCRIPTION

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Patent documents cited in the description

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