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(54) **SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE**

INTEGRIERTES HALBLEITERSCHALTUNGSBAUELEMENT

DISPOSITIF DE CIRCUIT INTEGRE SEMI-CONDUCTEUR

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Description

TECHNICAL FIELD

[0001] The present invention relates to a semiconductor integrated circuit device, and more particularly to a semiconductor integrated circuit apparatus having a configuration capable of facilitating a packaging design operation thereof.

BACKGROUND ART

[0002] Conventionally, in a typical flow of a packaging design operation of a semiconductor integrated circuit, due to limited development resources, to effectively perform the packaging design operation of the semiconductor integrated circuit device as much as possible, a fundamental logic circuit block is designed first and so-called a flip development is performed on the logic circuit block.

[0003] FIG. 1 is a top view illustrating an example of semiconductor integrated circuit.

[0004] As illustrated in FIG. 1, the semiconductor integrated circuit device includes blocks 1 and 2 as logic circuit blocks, and each block includes six cache memories. Further, in this case of FIG. 1, it is assumed that those six cache memories have similar packaging design with each other, thereby facilitating the packaging design.

[0005] Herein, the flip development refers to an operation of copying packaging design so that laterally symmetric packaging design can be formed as exemplarily illustrated in FIG. 1. In the case of FIG. 1, the packaging design of the block 1 having six cache memories is copied to form the packaging design of the block 2 so that the packaging design of the blocks 1 and 2 are bilaterally symmetric with each other. By repeating the flip development, the whole floor plan is provided.

[0006] FIG. 2 illustrates an exemplary relationship between bumps formed in an upper layer of the semiconductor integrated circuit device having the configuration of FIG. 1 and the cache memories included in the semiconductor integrated circuit device. Further, FIG. 3 obliquely illustrates an example of an arrangement of the bumps and a structure of power source patterns in such a semiconductor integrated circuit device.

[0007] This configuration illustrated in FIG. 3 corresponds to, for example, one of the six cache memories in FIG. 2.

[0008] The bump refers to an electrode to supply power source to the semiconductor integrated circuit device from an external power source and may also be called a power source terminal.

[0009] In FIG. 2, a relationship is described between one of the six cache memories in the block 1 and the positions of the bumps formed on an upper layer. In FIG. 2, symbols VSS and VDD denote the positions of VSS bumps and VDD bumps, respectively. The VSS bump and the VDD bump refer to a power source (i.e., positive) terminal and a ground (i.e., negative) terminal, respectively. Further, as illustrated in FIG. 2, a distance corresponding to a position interval of the VSS bump and the VDD bump adjacent to each other refers to a bump pitch.

[0010] Further, as illustrated in FIGS. 2 and 3, the VDD bumps and the VCC bumps, which are different in type from each other, are alternately arranged one after another so that the same type of the bumps (e.g., the VDD bumps or the VCC bumps) are not adjacent to each other. This is because the positive terminal and the negative terminal are required to be formed in a mutually corresponding manner to supply a power source.

[0011] FIG. 3 illustrates the positions of the VSS bumps B11 through B14 and the VDD bumps B21 through B25 formed on an upper layer of the block and the positions of VSS power source patterns P11 through P15 and VDD power source patterns P21 through P25 formed on a lower layer.

[0012] In the corresponding figures, the VSS bumps and the VDD bumps are depicted as circles on the uppermost layer of the block; and the VSS power source patterns and the VDD power source patterns are depicted as elongated belt-like patterns extending in the vertical and lateral directions in the lowermost layer of the block.

[0013] The VSS bumps and the VDD bumps are electrically connected to the VSS power source patterns and the VDD power source patterns, respectively, through vias or the like. By having this configuration, an external power source is supplied to the VSS power source patterns and the VDD power source patterns through the VSS bumps and the VDD bumps, the VSS power source patterns and the VDD power source patterns being formed on the lowermost layer of the block and the VSS bumps and the VDD bumps being formed on the upper most layer of the block.

[0014] As schematically illustrated in FIG. 3, plural VSS power source patterns and plural VDD power source patterns of the semiconductor integrated circuit device are formed (disposed) at regular intervals corresponding to the VSS bumps and the VDD bumps on the uppermost layer.

[0015] On the other hand, in a design process of the cache memories and the like to be formed on a layer lower than that on which the VSS power source patterns and the VDD power source patterns are formed, it is generally intended to reduce the size of each cache memory as much as possible to reduce the chip area of the semiconductor integrated circuit device.

[0016] This design method may be effective in the viewpoint of reducing the area of each cache memory.

[0017] However, when this design method is simply employed, as exemplarily illustrated in FIG. 2, the size of each cache memory may not match with the bump pitch of the VSS bumps and the VDD bumps on the uppermost layer.

[0018] More specifically, as exemplarily illustrated in the middle left-hand cache memory of block 1 in FIG. 2, the lengths in the vertical and lateral directions of the cache memory are longer than three times the bump pitch

and shorter than four times the bump pitch. Furthermore, as illustrated in FIG. 2, four VSS bumps (corresponding to the rectangles in which "VSS" is indicated) and five VDD bumps (corresponding to the rectangles in which "VDD" is indicated) belong to the cache memory.

[0019] FIG. 4 is a top view illustrating the cache memories C1 and C2 included in the semiconductor integrated circuit device. Further, in the configuration of FIG. 4, the power source patterns are disposed at regular intervals.

[0020] Next, the relationships between the power source patterns in cache memories C1 and C2 and the power source patterns illustrated in FIG. 3 are described.

[0021] In FIG. 3, for the purposes of facilitating the understanding of the relationship between the bumps on the upper layer and the power source patterns, a case is described where two power source patterns are provided for each of the bumps. More specifically, in the case of FIG. 3, the VSS bump B14 corresponds to two VSS power source patterns P11 and P12; and VDD bump B24 corresponds to two VDD power source patterns P21 and P22.

[0022] On the other hand, generally, more than two power source patterns are corresponded to a single bump. Similar to the case of FIG. 3, in the example illustrated in FIG. 4, two power source patterns are corresponded (connected) to a single bump B. Further, in the example of FIG. 4, each of the VSS power source patterns and the VDD power source patterns is depicted as an elongated belt-like pattern extending in the upper and lower (vertical) direction in the figure. Further, in FIG. 4, which is similar to FIG. 3, the half-toned bumps B represent the VSS bump and the bumps B without half-toned pattern represent the VDD bumps.

[0023] Further, in FIG. 4, pins A, B, C, and D represent input/output terminals of the logic circuit block formed on a layer lower than that on which the power source patterns are formed. To electrically connect the pins A, B, C, and D to the outside of the semiconductor integrated circuit device, as described in FIG. 4, wiring patterns P151, P152, P153, and P154 extending in the vertical direction in FIG. 4 are provided so as to be connected to the pins A, B, C, and D, respectively.

[0024] In this case, when a terminal inside the cache memory is required to be connected to the outside of the cache memory using a wiring, the wiring may be required to be formed so as not to be in contact with any of the VSS power source patterns P111 and P112 and the VDD power source patterns P121 and P122 and the like.

[0025] Further, in a case where the flip development is performed on the block of the logic circuit to effectively perform the packaging design operation, it may be required to consider that any of the VSS power source patterns and the VDD power source patterns on the upper layer does not short-circuit with any of the wirings connecting between the terminals inside the cache memories and the outside of the cache memories. To that end, it may be desirable that the wirings are disposed in a manner such that the relative positions of the wirings with respect to the VSS power source patterns and the VDD power source patterns on the upper layer are constant (common) in each cache memory, the wirings connecting between the terminals inside the cache memories and the outside of the cache memories.

[0026] However, for example, in the case where the lengths in the vertical and lateral directions of the cache memory are longer than three times the bump pitch and shorter than four times the bump pitch as illustrated in FIG. 2, relative positions of the VSS bumps and the VDD bumps on the upper layer with respect to the respective cache memories on the lower layer may vary depending on the cache memories. In this case, as illustrated in FIG. 4, the relative positions of the VSS power source patterns and the VDD power source patterns on the upper layer with respect to the cache memory C1 may differ from that with respect to the cache memory C2.

[0027] More specifically, in the example of FIG. 4, in the cache memory C1, there are VSS power source pattern P111 and VDD power source pattern P121 on the left-hand side of the pins A and B. On the other hand, in the cache memory C2, the VSS power source pattern P111, the VDD power source pattern P121, and the pins A and B are also provided similar to the cache memory C1. However, the VSS power source pattern P111 and the VDD power source pattern P121 in the cache memory C2 are more shifted to the left-hand side from the pins A and B when compared with the case of cache memory C1.

[0028] Further, as described above, the plural VSS power source patterns and the plural VDD power source patterns are formed at regular intervals. Because of this feature, in the cache memory C2, the VSS power source pattern P111 and the VDD power source pattern P121 on the right-hand side of the pins A and B are also more shifted to the left-hand side than in the case of the cache memory C1. In this state, if the same wiring pattern as that formed in the cache memory C1 is formed (disposed) in the cache memory C2 and vice verse, a problem may occur.

[0029] More specifically, as illustrated in FIG. 4, in the cache memory C1, the wiring patterns P151 and P152 are bent in L shape near the bottom end of the cache memory C1, so that the patterns are shifted to the right-hand side. However, if the wiring patterns P151 and P152 bent to the right-hand side in the cache memory C1 are applied to the wiring patterns P161 and P162 in the same manner in the cache memory C2, as may be apparent from FIG. 4, the wiring pattern P162 from pin B may be in contact with (i.e., may short-circuit with) the adjacent VSS power source pattern P112. Therefore, in this state, to avoid the contact, as illustrated in FIG. 4 and unlike the case of the cache memory C1, the wiring patterns P161 and P162 are bent in L shape near the bottom end of the cache memory C2, so that the patterns are shifted to the left-hand side.

[0030] Therefore, in such a case described above, it may become necessary to perform different packaging

design with respect to each cache memory, which may degrade the efficiency of the total packaging design operation.

[0031] Patent Document 1: Japanese Patent Application Publication No.: 7-22510

[0032] Patent Document 2: Japanese Patent Application Publication No.: 11-250700

[0033] US-A1-2006/0267706 discloses a system and method for configuring conductors within an integrated circuit to reduce impedance variation caused by connection bumps.

DISCLOSURE OF INVENTION

PROBLEMS TO BE SOLVED BY THE INVENTION

[0034] The present invention is made in light of the above problems, and an object of the pesent invention is to provide a semiconductor integrated circuit device having a configuration capable of facilitating a packaging design operation without degrading the packaging efficiency.

MEANS FOR SOLVING THE PROBLEMS

[0035] The present invention is defined by the independent claim, to which reference should now be made. Specific embodiments are defined in the dependent claims.

ADVANTAGEOUS EFFECT OF THE INVENTION

[0036] According to an embodiment of the present invention, the relative positions of the bumps on the upper layer with respect to each of the cache memories may become constant while a problem of reducing the packaging efficiency of the semiconductor integrated circuit device is resolved. Therefore, it may become possible to repeatedly use packaging design data of one cache memory to be applied to the other cache memories, thereby enabling to improve the efficiency of the packaging design operation.

BRIEF DESCRIPTION OF DRAWINGS

[0037]

FIG. 1 is a top view illustrating an example of packaging design of a semiconductor integrated circuit device;

FIG. 2 is a drawing illustrating a problem which may occur in a conventional semiconductor integrated circuit device;

FIG. 3 is an oblique perspective view illustrating an example of packaging design of a semiconductor integrated circuit device;

FIG. 4 is another drawing illustrating a problem which may occur in a conventional semiconductor integrated circuit device;

FIG. 5 illustrates a schematic comparison of a configuration of a conventional semiconductor integrated circuit device (FIG. 5(a)) and an exemplary configuration of a semiconductor integrated circuit device according to an embodiment of the present invention (FIG. 5(b));

FIG. 6 illustrates exemplary circuit diagrams which may be included in a clock generator of a cache memory in a semiconductor integrated circuit device according to an embodiment of the present invention;

FIG. 7 illustrates another schematic comparison of a configuration of a conventional semiconductor integrated circuit device (FIG. 7(a)) and an exemplary configuration of a semiconductor integrated circuit device according to an embodiment of the present invention (FIG. 7(b));

FIG. 8 is a top view illustrating an exemplary configuration of a semiconductor integrated circuit device according to an embodiment of the present invention; and

FIG. 9 is another top view illustrating an exemplary configuration of a semiconductor integrated circuit device according to an embodiment of the present invention.

EXPLANATION OF REFERENCES

[0038]

11, 13, 21, 23, 31, 33: MEMORY CELL ARRAY
12, 22, 32: CONTROL CIRCUIT
14, 16, 24, 26, 34, 36: I/O CIRCUIT
15, 25, 35: CLOCK GENERATOR
37: STANDARD CELL ARRAY
C1, C2, C11, C21, C31, C41, C42: CACHE MEMORY
B, B11-B15, B21-B24: BUMP
P11-P15, P21-P25: POWER SOURCE PATTERN
P111, P112, P121, P122: POWER SOURCE PATTERN
P151, P152, P161, P162: WIRING PATTERN

BEST MODE FOR CARRYING OUT THE INVENTION

[0039] In the above description, a case is described with reference to FIG. 2 where the lengths in the vertical and lateral directions of the cache memory are longer than three times the bump pitch and shorter than four times the bump pitch, which may cause a problem of degradation of the efficiency of the total packaging design.

[0040] On the other hand, according to an embodiment of the present invention, a packaging design of the cache memories is performed in a manner such that the lengths in the vertical and lateral directions of the cache memory are equal to an even multiple of (e.g., four times) the

bump pitch.

[0041] By performing the packaging design operation in this way, the relative positions of the VSS bumps and the VDD bumps on the upper layer with respect to the cache memories may not differ from each other and may become similar to each other. Therefore, the problem described above may be resolved. More specifically, by performing the packaging design operation in this way, it may become unnecessary to perform packaging design operation on each cache memory; that is, the packaging design data of one cache memory may also be applied to the other cache memories without changing the packaging design data (i.e., without necessity of performing additional packaging design operation to modify the packaging design data for other cache memories).

[0042] However, if the lengths in the vertical and lateral directions of the cache memory are equal to an odd multiple of the bump pitch, the following problem may occur.

[0043] As described above, in the semiconductor integrated circuit device, there are required two types of bumps, which are the bump for the power source side (i.e., the VDD bump) and the bump for the ground side (I.e., the VSS bump). This may be obvious because both positive and negative electrodes (terminals) are required to supply power source to the semiconductor integrated circuit device.

[0044] Next, a case is described in more detail where the lengths in the vertical and lateral directions of the cache memory are equal to an odd multiple of (in this case, as an example, three times) the bump pitch. In this case, as described above, four VSS bumps and five VDD bumps may belong to some of the cache memories. As a result, the number of the VSS bumps is not equal to the number of the VDD bumps. However, as described above, the VDD bump and the VCC bump are to be used as a pair; therefore, it may be required that the number of the VSS bumps is to be equal to the number of the VDD bumps in each of the cache memories.

[0045] On the other hand, according to an embodiment of the present invention, as described above, the lengths in the vertical and lateral directions of the cache memory are equal to an even multiple of the bump pitch. For example, by performing the packaging design operation in a manner such that the lengths in the vertical and lateral directions of the cache memory are equal to four times the bump pitch, the number of VSS bumps may be equal to the number of the VDD bumps in each of the cache memories.

[0046] Further, in this case where the lengths in the vertical and lateral directions of the cache memory are equal to an even multiple of the bump pitch, it is not always necessary that the same even number of times such as four times are applied to both the vertical direction and the lateral directions of the cache memory. In other words, different even number of times, for example, four times and six times, may be separately applied to the vertical direction and the lateral directions, respectively, of the cache memories. This is because, even in such a case, the number of VSS bumps may be equal to the number of the VDD bumps in each of the cache memories.

[0047] In the following, an embodiment of the present inventions is further described with reference to the accompanying drawings. Further, the embodiment of the present invention is described by illustrating the cache memory as an example.

[0048] According to an embodiment of the present invention, in a packaging design operation of a semiconductor integrated circuit device, by enlarging an area of the cache memory, the lengths in the vertical and lateral directions of the cache memory may be adjusted to be equal to an even multiple (i.e., 2n, herein a symbol "n" denotes an integer greater than zero) of the bump pitch. Further, a typical logic circuit such as a logic circuit having a repeated pattern, a test circuit and the like may be included (integrated) in the cache memories.

[0049] According to this embodiment of the present invention, by integrating a typical logic circuit such as a logic circuit having a repeated pattern, a test circuit and the like in the cache memories of the semiconductor integrated circuit, the lengths in the vertical and lateral directions of the cache memory may be adjusted to be equal to 2n of the bump pitch. As a result, it may become possible to remove a wasteful dead space which may be created in a block of a basic circuit generated in a high-level design operation.

[0050] As a result, after the flip development is performed on the block of the basic circuit in the high-level design operation, it may become unnecessary to separately design the relative positions of the wirings with respect to the power source patterns on the upper layer, the wirings being connecting between the terminals inside the cache memories and the outside of the cache memories; and further, it may become possible to repeatedly use packaging design data of one cache memory to be applied to the other cache memories, which may remarkably improve the efficiency of the packaging design operation.

[0051] Further, by integrating a standard cell area in the cache memory, it may become possible to reduce the necessity of creating a new site outside the cache memory, thereby enabling to control the gaps between the cache memories. As a result, it may become possible to improve the packaging density of the entire chip of the semiconductor integrated circuit device.

[0052] Further, by adjusting the lengths (size) in the vertical and lateral directions of the cache memory to be equal to 2n of the bump pitch, the cache memories having the adjusted size may have an extra space. Then, by using the extra space, each area of the blocks of the basic circuits in the cache memory may be enlarged. As a result, the packaging design operation based on the study of DFM (Design for Manufacturing) may be performed, thereby enabling to extend the distances between the positions of transistors and the distances between the signal wirings to reduce the capacitance be-

tween the signal wirings. Therefore, it may become possible to provide a cache memory having more tolerance against noise and increase the yield rate of the semiconductor integrated circuit device.

[0053] FIG. 5 schematically illustrates a comparison between a configuration of a conventional semiconductor integrated circuit device (FIG. 5(a)) and an exemplary configuration of a semiconductor integrated circuit device according to an embodiment of the present invention (FIG. 5(b)).

[0054] Namely, FIG. 5(a) illustrates a conventional cache memory C11 where no embodiments of the present invention are applied. As illustrated in FIG. 5(a), the cache memory C11 includes blocks of basic circuits as main circuits including memory cell arrays 11 and 13, a clock generator 15, input/output circuits 14 and 16 serving as an interface to the outside of the cache memory C11, and a control circuit 12 having functions such as an address decoder.

[0055] Accordingly, FIG. 5(a) illustrates an exemplary circuit configuration of the cache memory C11, the circuit configuration being formed by performing packaging design operation in which an emphasis is mainly placed on packaging efficiency to minimize the packaging area).

[0056] In this case, as illustrated in FIG. 5(a), the lengths (size) in the vertical and lateral directions of the cache memory may not be equal to 2n of the bump pitch. Because of this feature, it may become necessary to separately perform packaging design operation with respect to each of the cache memories, thereby degrading the efficiency of the packaging design operation.

[0057] On the other hand, FIG. 5(b) illustrates an exemplary circuit configuration of the cache memory C21 in a semiconductor integrated circuit device according to an embodiment of the present invention.

[0058] As illustrated in FIG. 5(b), the packaging design operation of the cache memory C21 is performed in a manner such that the lengths (size) in the vertical and lateral directions of the cache memory are equal to 2n of the bump pitch. As a result, it may become possible to improve the efficiency of the packaging design operation.

[0059] As illustrated in FIG. 5(b), the lengths (size) in the vertical and lateral directions of the cache memory are adjusted to be equal to 2n of the bump pitch by enlarging the areas of the blocks of the basic circuits in the cache memory C11 illustrated in FIG. 5(a).

[0060] As illustrated in FIG. 5(b), similar to the cache memory C11 of FIG. 5(a), the cache memory C21 includes blocks of basic circuits as main circuits including memory cell arrays 21 and 23, a clock generator 25, input/output circuits 24 and 26 serving as an interface to the outside of the cache memory C21, and a control circuit 22 such as an address decoder. This configuration of the blocks of the basic circuits are similar to that of the cache memory C11 of FIG. 5(a). However, the sizes of the areas of the blocks of the basic circuits of the cache memory C21 in FIG. 5(b) are larger than the respective areas of the blocks of the basic circuits of the cache memory C11 in FIG. 5(a).

[0061] One of the methods of enlarging the areas of the blocks of the basic circuits is to extend the distances between the transistors and the distances between the signal wirings. In a general packaging design operation, the transistors, signal wirings and the like may be disposed in a manner such that the size of the cache memories can be minimized based on the minimum rule of MDR (Mask Design Rule). However, in this embodiment of the present invention, as described above, the packaging design operation is performed in a manner such that the lengths (size) in the vertical and lateral directions of the cache memory are adjusted to be equal to 2n of the bump pitch by enlarging the block areas of the basic circuits in the cache memories. By performing the packaging design operation in this way, the cache memories may have an extra space. Then, by using the extra space, it may become possible to extend the distances between the positions of transistors and the distances between the signal wirings.

[0062] As a result, it may become possible to reduce the capacitance between the signal wirings in the cache memories, thereby enabling to produce cache memories having more tolerance against noise. Namely, the packaging design operation based on the study of DFM (Design for Manufacturing) may be performed, thereby enabling to increase the yield rate of the semiconductor integrated circuit device.

[0063] Another exemplary method of enlarging the areas of the blocks of the basic circuits may be to add a timing adjusting circuit 51B, a dummy transistor circuit 51E for chip update, a test circuit 51C as illustrated in FIGS. 6B through 6D or the like to the clock generator 15.

[0064] FIG. 6(a) illustrates a clock generator 25 including duty (or clock signal phase) adjustment circuits 51A and 51D. The duty adjustment circuits 51A and 51D receive a main clock signal CLK from outside of the cache memory and distribute the received clock signal CLK to the other blocks of the basic circuits in the cache memory. To that end, as illustrated in FIG. 6(a), the duty adjustment circuits 51A and 51D provide a function to adequately adjust the clock signal phase or duty by using the functions of inverter circuits INV connected in series and a NAND circuit NAND.

[0065] Recently, with miniaturization of the packaging structure of semiconductor integrated circuit devices, variation of manufacturing of the transistors may become a serious problem. Especially, in the cache memories of the semiconductor integrated circuit devices, there may be cases where it is difficult to adequately adjust the timing within the cache memory. Therefore, in the worst case, it may be supposed that the cache memory does not operate normally due to the variation of manufacturing of the transistors.

[0066] In contrast, by using the extra space obtained by enlarging the areas of the blocks of the basic circuits in the cache memory, the timing adjusting circuit 51B may be added to the clock generator 15 to adequately

adjust the timing of the clock signal to the cache memory. By adding the timing adjusting circuit 51B in this way, it may become possible to perform fine timing adjustment in the cache memory, thereby enabling to produce a cache memory having higher tolerance against the variation of manufacturing.

[0067] FIG. 6(b) illustrates an exemplary circuit configuration of the timing adjusting circuit 51B.

[0068] As illustrated in FIG. 6(b), the timing adjusting circuit 51B is made of a combination of inverter circuits INV and pass transistors PAS. By the switching control of the pass transistors PAS, the number of series of inverters constituting the timing adjusting circuit 51B can be determined. By doing this, a delay amount of the signal to be output from the timing adjusting circuit 51B may be determined.

[0069] Otherwise, by using the extra space obtained by enlarging the areas of the blocks of the basic circuits in the cache memory, the dummy transistor circuit 51E may be added to the clock generator 15 to update the chip of the semiconductor integrated circuit device. By adding the dummy transistor circuit 51E in this way, when the chip of the semiconductor integrated circuit device is faulty due to a fault in a cache memory, it may become possible to update the chip of the semiconductor integrated circuit device by changing wiring patterns between transistors and the like (a.k.a. metal update) without changing the positions of the transistors and the like (a.k.a. bulk update); thereby enabling to remarkably reduce the cost to update the chip.

[0070] FIG. 6(c) illustrates an exemplary circuit configuration of the dummy transistor circuit 51E.

[0071] As illustrated in FIG. 6(c), the dummy transistor circuit 51E includes plural inverters connected in series with each other. By changing the wiring patterns between transistors and the like (performing the metal update), the dummy transistor circuit 51E may be added to the duty (or clock signal phase) adjustment circuit 51D. By adding the dummy transistor circuit 51E in this way, it may become possible to change the waveform of the clock signal generated by the duty (or clock signal phase) adjustment circuit 51D. As a result, by updating the chip in this way, it may become possible to update a faulty chip by removing the cause of the trouble.

[0072] Otherwise, by using the extra space obtained by enlarging the areas of the blocks of the basic circuits in the cache memory, the test circuit 51C may be added to the clock generator 15. By adding the test circuit 51C in this way, it may become possible to conduct a test of the cache memory by using the added test circuit 51C.

[0073] FIG. 6(d) illustrates an exemplary circuit configuration of the test circuit 51C.

[0074] As illustrated in FIG. 6(d), the test circuit 51C is made of a combination of the inverter circuits INV and the pass transistors PAS. By the switching control of the pass transistors PAS based on an externally-supplied test signal TEST, the number of series of inverters constituting the test circuit 51C can be determined. By doing this, a delay amount of the signal to be output from the test circuit 51C may be determined. By using this feature, it may become possible to test the operations of the circuits in response to various delay amounts.

[0075] Further, in the case where the areas of the blocks of the basic circuits in the cache memories are enlarged so that the lengths (size) in the vertical and lateral directions of the cache memory are adjusted to be equal to 2n of the bump pitch, if the difference in the lengths (size) in the vertical and/or lateral directions of the cache memory between before the enlargement and after the enlargement exceeds a predetermined value (e.g., approximately 100 μm), the lengths of the wirings between the blocks of the basic circuits become longer; and as a result, a delay amount during the operations of the cache memory may be increased.

[0076] In such a case, instead of simply enlarging the areas of the blocks of the basic circuits in the cache memory so that the lengths (size) in the vertical and lateral directions of the cache memory are adjusted to be equal to 2n of the bump pitch, the following method may be employed.

[0077] As illustrated in FIGS. 7(a) and 7(b), in addition to enlarging the areas of the blocks of the basic circuits in the cache memory in the method described above, a standard cell like a repeater which is not expressed (configured) using complicated logic circuits may be integrated (included) in the cache memory.

[0078] As illustrated in FIG. 7(b), similar to the cache memory C11 of FIG. 7(a), the cache memory C31 includes blocks of basic circuits as main circuits including memory cell arrays 31 and 33, a clock generator 35, input/output circuits 34 and 36, and a control circuit 32 having functions such as an address decoder. This configuration of the blocks of the basic circuits is similar to that of the cache memory C11 of FIG. 7(a). However, as illustrated in FIG. 7(b), the sizes of the areas of the blocks of the basic circuits of the cache memory C31 in FIG. 7(b) are larger than those of the cache memory C11 in FIG. 7(a) by a predetermined amount.

[0079] In addition to that, in the case of FIG. 7(b), a standard cell area 37 is provided in which a standard cell is added in the cache memory C31. As a result, as illustrated in FIG. 7(b), due to the added standard cell area 37, the area of the cache memory C31 may further be enlarged, so that the lengths (size) in the vertical and lateral directions of the cache memory are adjusted to be equal to 2n of the bump pitch.

[0080] By employing the method illustrated in FIG. 7(b, it may become possible to adjust the lengths (size) in the vertical and lateral directions of the cache memory to be equal to 2n of the bump pitch without inadequately extending the lengths of the wirings between the blocks of the basic circuits in the cache memory.

[0081] Further, by employing the method illustrated in FIG. 7(b) to integrate the repeater-like standard cell area in the cache memory, it may become possible to maximally remove the necessity to separately provide a site

such as the standard cell area outside the cache memory after the flip development is performed on the blocks of the basic circuits in the high-level design operation. As a result, as illustrated in FIG. 8, it may become possible to arrange the cache memories closer together, thereby enabling to improve the packaging density of the entire chip of the semiconductor integrated circuit device.

[0082] As described above, by adjusting the lengths (size) in the vertical and lateral directions of the cache memory to be equal to 2n of the bump pitch by enlarging the areas of the blocks of the basic circuits in the cache memory or by integrating the standard cell in the cache memory, it may become possible to remove the necessity of separately considering the difference in relative positions of the wiring patterns P151 and P152 connecting between the terminals inside the cache memories and the outside of the cache memories with respect to the power source patterns P111, P121, P112, and P122 on the upper layer with respect to each cache memory. As a result, it may become possible to repeatedly use packaging design data of one cache memory to be applied to the other cache memories; which may remarkably improve the efficiency of the packaging design operation.

[0083] In the case of FIG. 9, the lengths (size) in the vertical and lateral directions of the cache memories C41 and C42 are adjusted to be equal to 2n of the bump pitch, the bumps on the upper layer being disposed in the same manner for all the cache memories. Further, in FIG. 9, same as the case in FIG. 4, the half-toned bumps B represent the VSS bumps and the bumps B without half-toned pattern represent the VDD bumps.

[0084] In the case where the lengths in the vertical and lateral directions of the cache memory are equal to an odd multiple of (in this case, as an example, three times) the bump pitch, the number of bumps belonging to each cache memory is nine ($3\times3=9$). In this case, in some cache memories, there are five VDD bumps and four VSS bumps, and in other cache memories adjacent to the above cache memories, there are four VDD bumps and five VSS bumps. Therefore, the arrangement of the bumps in the cache memories may vary and may not be constant in the same semiconductor integrated circuit device.

[0085] On the other hand, according to an embodiment of the present invention, as described above, the lengths in the vertical and lateral directions of the cache memory are equal to an even multiple of the bump pitch. For example, by performing the packaging design operation in a manner such that the lengths in the vertical and lateral directions of the cache memory are equal to four times the bump pitch, the number of the bumps belonging to each of the cache memories is sixteen ($4\times4=16$)), and the number of the VDD bumps is eight (8) and the number of the VSS bumps is also eight (8). Further, the arrangement of those bumps becomes constant in all the cache memories. Therefore, for example, in the case of FIG. 9, the relative positions of the bumps with respect to the cache memory C41 and the relative positions of the bumps with respect to the cache memory C42 may become the same. As a result, the arrangement of the power source patterns, that are disposed lower than the bumps and higher than the layer where the logic circuits constituting the cache memories are formed and that are connected to the bumps B, may become constant between cache memories C41 and C42 as illustrated in FIG. 9.

[0086] As a result, the relative positions of the pins A, B, C, and D with respect the power source patterns P111, P121, P112, P122 and the like formed on an upper layer may become constant between cache memories C41 and C42. Therefore, in the packaging design operation of the cache memories C41 and C42, packaging design data of one cache memory may be applied to the other cache memory without performing the packaging design operation with respect to both of the cache memories.

[0087] Therefore, it may become possible to repeatedly use packaging design data of one cache memory to be applied to the other cache memories, thereby enabling to improve the efficiency of the packaging design operation.

[0088] According to an embodiment of the present invention, it may become possible to effectively reduce the total development man-hours of the semiconductor integrated circuit devices and costs; and it may become possible to design and manufacture products having higher performances at a higher yield rate in a shorter time period.

[0089] In FIGS. 1, 2, 4, 5, 7, 8, 9, for the explanatory purposes, the gaps between the cache memories may be explicitly expressed. However, the actual gaps between adjacent cache memories, between the cache memory and the adjacent standard cell area and the like are negligibly small compared with the lengths (size) in the vertical and lateral directions of the cache memories. Because of this feature, the above description "the lengths in the vertical and lateral directions of the cache memory are adjusted to be equal to an even multiple of the bump pitch" may be regarded as equivalent to the description "when a substrate of a semiconductor integrated circuit device is divided and the areas of the cache memories are allocated, the lengths in the vertical and lateral directions of the areas to be allocated to the cache memories are adjusted to be equal to an even multiple of the bump pitch". Then, in such a configuration, the relative positions of the bumps on an upper layer with respect to each of the cache memories may become constant.

[0090] In the above embodiments, as an example, a case is described where the lengths in the vertical and lateral directions of the cache memory are adjusted to be equal to an even multiple (e.g., four times) of the bump pitch. However, the present invention is not limited to this configuration. For example, the present invention may include a configuration in which at least one of the length in the vertical direction and the length in the lateral direction of the cache memory is adjusted to be equal to an even multiple of the bump pitch.

Claims

1. A semiconductor integrated circuit device comprising:

   plural units (C21; C31) each having plural logic circuits (21 to 26; 31 to 37); and
   plural bumps (B) configured to supply a power source from outside to the semiconductor integrated circuit device,
   characterised in that
   the plural units (C21; C31) each having plural logic circuits (21 to 26; 31 to 37) have a common packaging design with each other;
   the bumps (B) are arranged in a grid array over the units (C21; C31); and
   at least one of lengths and widths of the units (C21; C31) each having plural logic circuits (21 to 26; 31 to 37) are substantially equal to an even multiple of the bump pitch.

2. The semiconductor integrated circuit device according to claim 1, wherein
   each of the plural units (C21; C31) each having plural logic circuits (21 to 26; 31 to 37) includes respective power source patterns connected to the bumps (B), and
   an even number of the bumps (B) belong to each of the plural units (C21; C31) each having plural logic circuits (21 to 26; 31 to 37).

3. The semiconductor integrated circuit device according to claim 1, wherein
   the plural units (C21; C31) each having plural logic circuits (21 to 26; 31 to 37) are cache memories.

4. The semiconductor integrated circuit device according to claim 3, wherein
   the cache memory includes at least one of a logic circuit having a repeated pattern, a test circuit, and a standard cell.

Patentansprüche

1. Integrierte Halbleitcrschaltungsvorrichtung, umfasscnd:

   mehrere Einheiten (C21; C31), die jeweils mehrere Logikschaltungen (21 bis 26; 31 bis 37) haben; und
   mehrere Bumps (B), die konfiguriert sind, um der integrierten Halbleiterschaltungsvorrichtung eine Energiequelle von außen zuzuführen,
   dadurch gekennzeichnet, das
   die mehreren Einheiten (C21; C31) , die jeweils mehrere Logikschaltungen (21 bis 26; 31 bis 37) haben, miteinander eine gemeinsame Eakkungskonstruktion haben;
   die Bumps (B) über den Einheiten (C21; C31) in einem Gitter-Array angeordnet sind; und
   wenigstens eines von Längen und Breiten der Einheiten (C21; C31), die jeweils mehrere Logikschaltungen (21 bis 26; 31 bis 37) haben, im Wesentlichen einem geradzahligen Vielfachen der Bump-Teilung gleich ist.

2. Integrierte Halbleiterschaltungsvorrichtung nach Anspruch 1, bei der
   jede von den mehreren Einheiten (C21; C31), die jeweils mehrere Logikschaltungen (21 bis 26; 31 bis 37) haben, jeweilige Enerrgiequellenmuster enthält, die mit den Bumps (B) verbunden sind, und
   eine gerade Anzahl der Bumps (B) zu jeder der mehreren Einheiten (C21; C31) gehört, die jeweils mehrere Logikschaltungen (21 bis 26; 31 bis 37) haben.

3. Integrierte Halblelterschaltungsvorrichtung nach Anspruch 1, bei der
   die mehreren Einheiten (C21; C31), die jeweils mehrere Logikschaltungen (21 bis 26; 31 bis 37) haben, Cache-Speicher sind.

4. Integrierte Halbleiterschaltungsvorrichtung nach Anspruch 3, bei der
   der Cache-Speicher wenigstens eine von einer Logikschaltung mit einem wiederholten Muster, einer Testschaltung und einer Standardzelle enthält.

Revendications

1. Dispositif de circuit intégré à semi-conducteurs comprenant :

   une pluralité d'unités (C21 ; C31) comportant chacune une pluralité de circuits logiques (21 à 26 ; 31 à 37) ; et
   une pluralité de bosses (B) configurées pour appliquer une source de puissance de l'extérieur au dispositif de circuit intégré à semi-conducteurs,
   caractérisé en ce que
   la pluralité d'unités (C21 ; C31) comportant chacune une pluralité de circuits logiques (21 à 26 ; 31 à 37) ont une conception de boîtier commune les unes aux autres ;
   les bosses (B) sont agencées en un réseau en forme de grille sur les unités (C21 ; C31) ; et
   au moins l'une des longueurs et des largeurs des unités (C21 ; C31) comportant chacune une pluralité de circuits logiques (21 à 26 ; 31 à 37) est sensiblement égale à un multiple pair du pas des bosses.

2. Dispositif de circuit intégré à semi-conducteurs selon

la revendication 1, dans lequel
chacune de la pluralité d'unités (C21 ; C31) comportant chacune une pluralité de circuits logiques (21 à 26 ; 31 à 37) comprend des motifs de source de puissance respectifs connectés aux bosses (B), et
un nombre pair des bosses (B) appartiennent à chacune de la pluralité d'unités (C21 ; C31) comportant chacune une pluralité de circuits logiques (21 à 26 ; 31 à 37).

3. Dispositif de circuit intégré à semi-conducteurs selon la revendication 1, dans lequel
la pluralité d'unités (C21 ; C31) comportant chacune une pluralité de circuits logiques (21 à 26 ; 31 à 37) sont des mémoires caches.

4. Dispositif de circuit intégré à semi-conducteurs selon la revendication 3, dans lequel
la mémoire cache comprend au moins l'un d'un circuit logique présentant un motif répété, d'un circuit de test et d'une cellule standard.

FIG.1

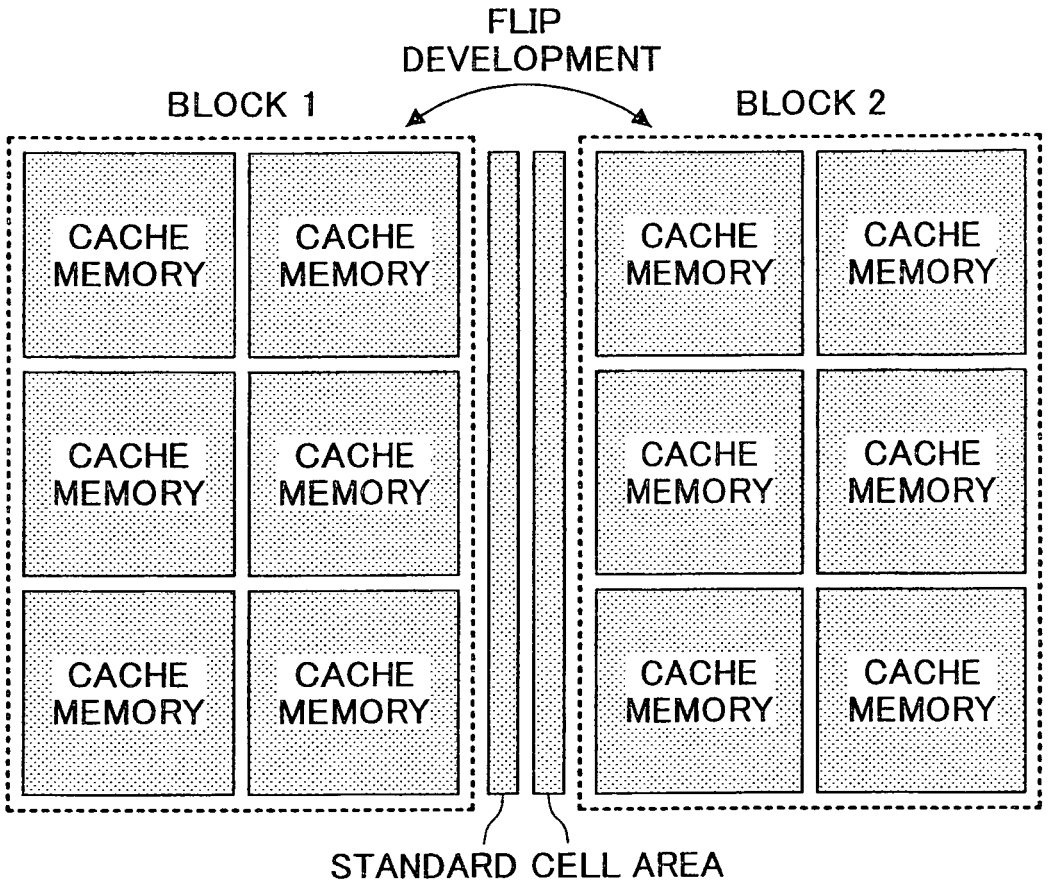

FLIP
DEVELOPMENT
BLOCK 1
BLOCK 2
CACHE MEMORY
CACHE MEMORY
CACHE MEMORY
CACHE MEMORY
CACHE MEMORY
CACHE MEMORY
CACHE MEMORY
CACHE MEMORY
CACHE MEMORY
CACHE MEMORY
CACHE MEMORY
CACHE MEMORY
STANDARD CELL AREA

FIG.2

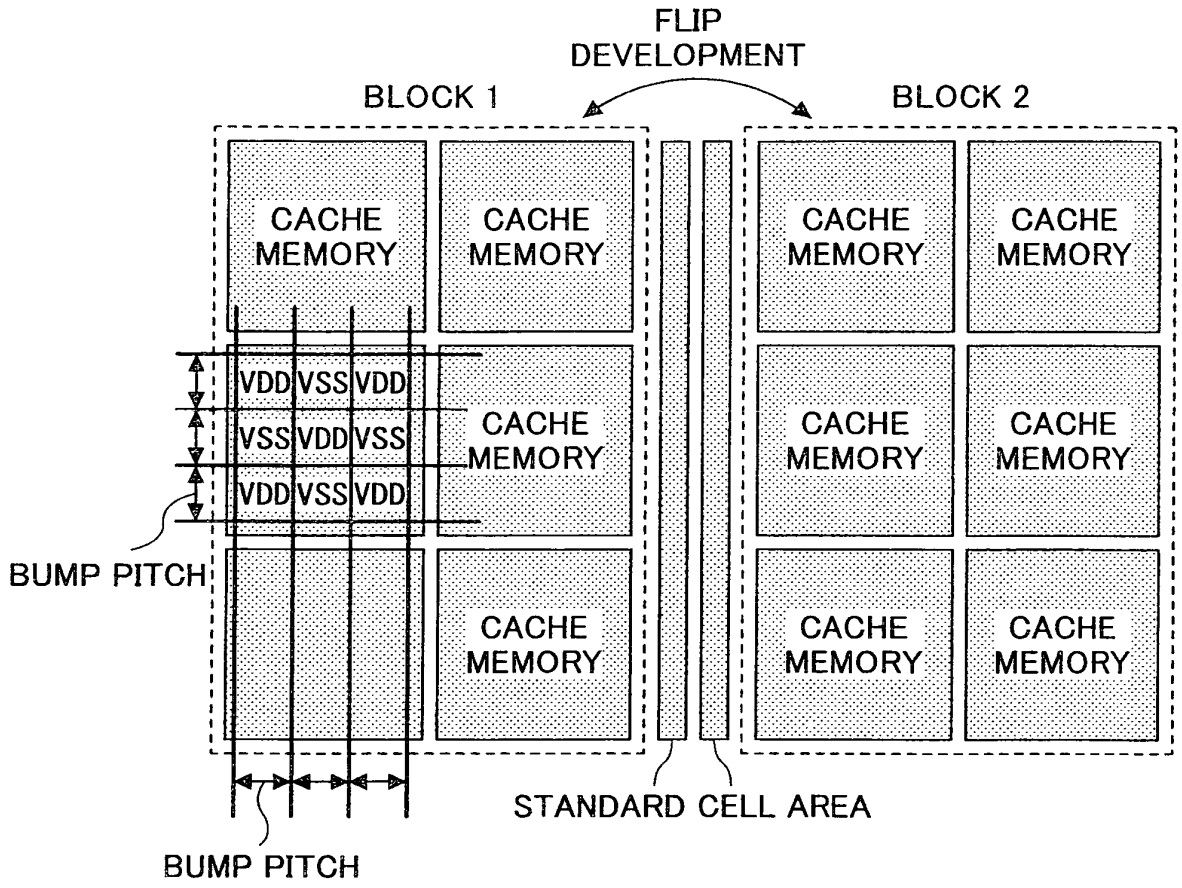

FLIP
DEVELOPMENT
BLOCK 1
BLOCK 2
CACHE MEMORY
CACHE MEMORY
CACHE MEMORY
CACHE MEMORY
VDD VSS VDD
VSS VDD VSS
VDD VSS VDD
CACHE MEMORY
CACHE MEMORY
CACHE MEMORY
BUMP PITCH
CACHE MEMORY
CACHE MEMORY
CACHE MEMORY
STANDARD CELL AREA
BUMP PITCH

FIG.3

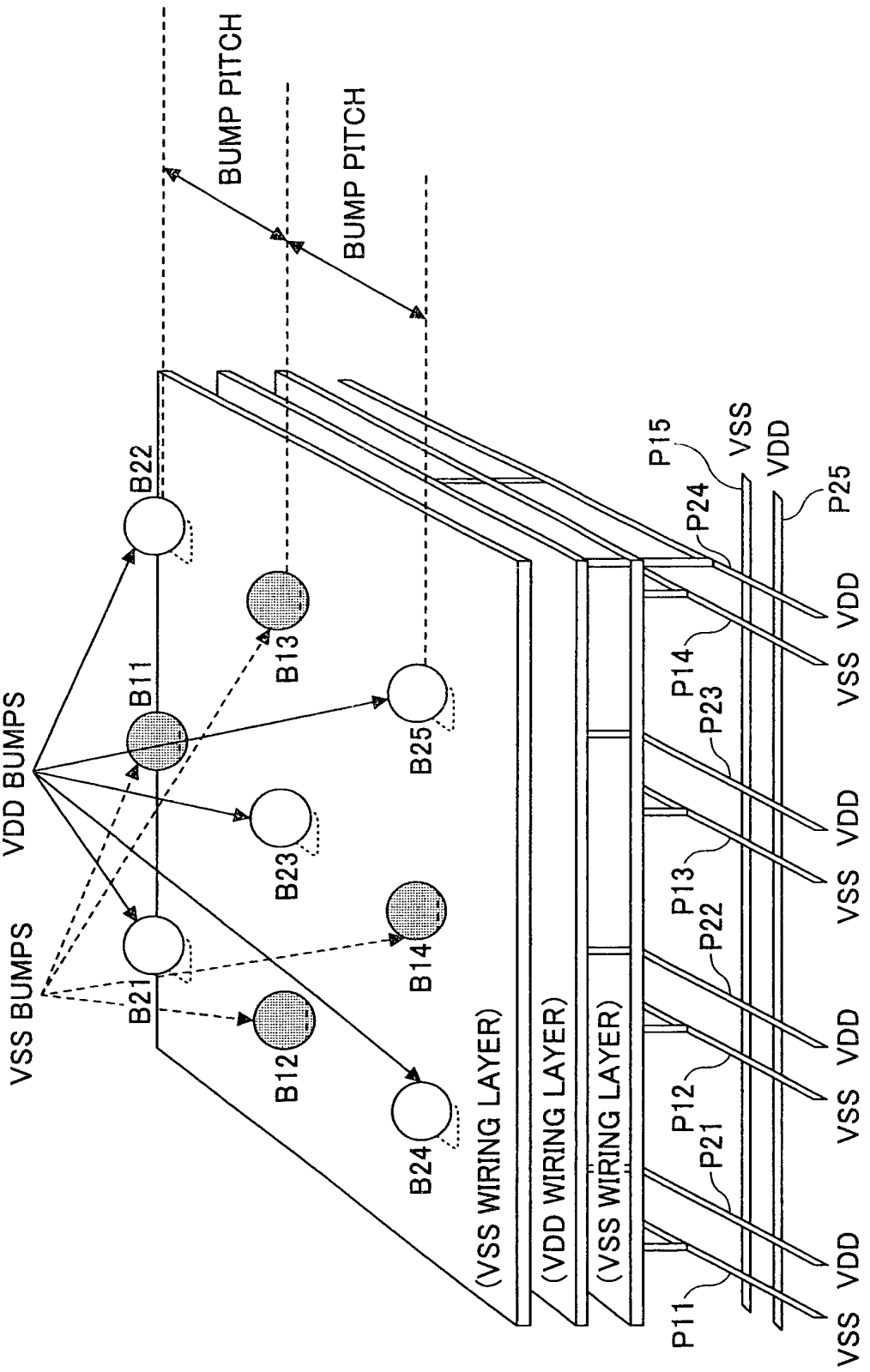

BUMP PITCH
BUMP PITCH
VDD BUMPS
VSS BUMPS
B22
B11
B13
B25
B23
B21
B14
B12
B24
(VSS WIRING LAYER)
(VDD WIRING LAYER)
(VSS WIRING LAYER)
P15
P24
P14
P23
P13
P22
P12
P21
P11
VSS
VDD
P25
VSS VDD
VSS VDD
VSS VDD
VSS VDD

FIG.4

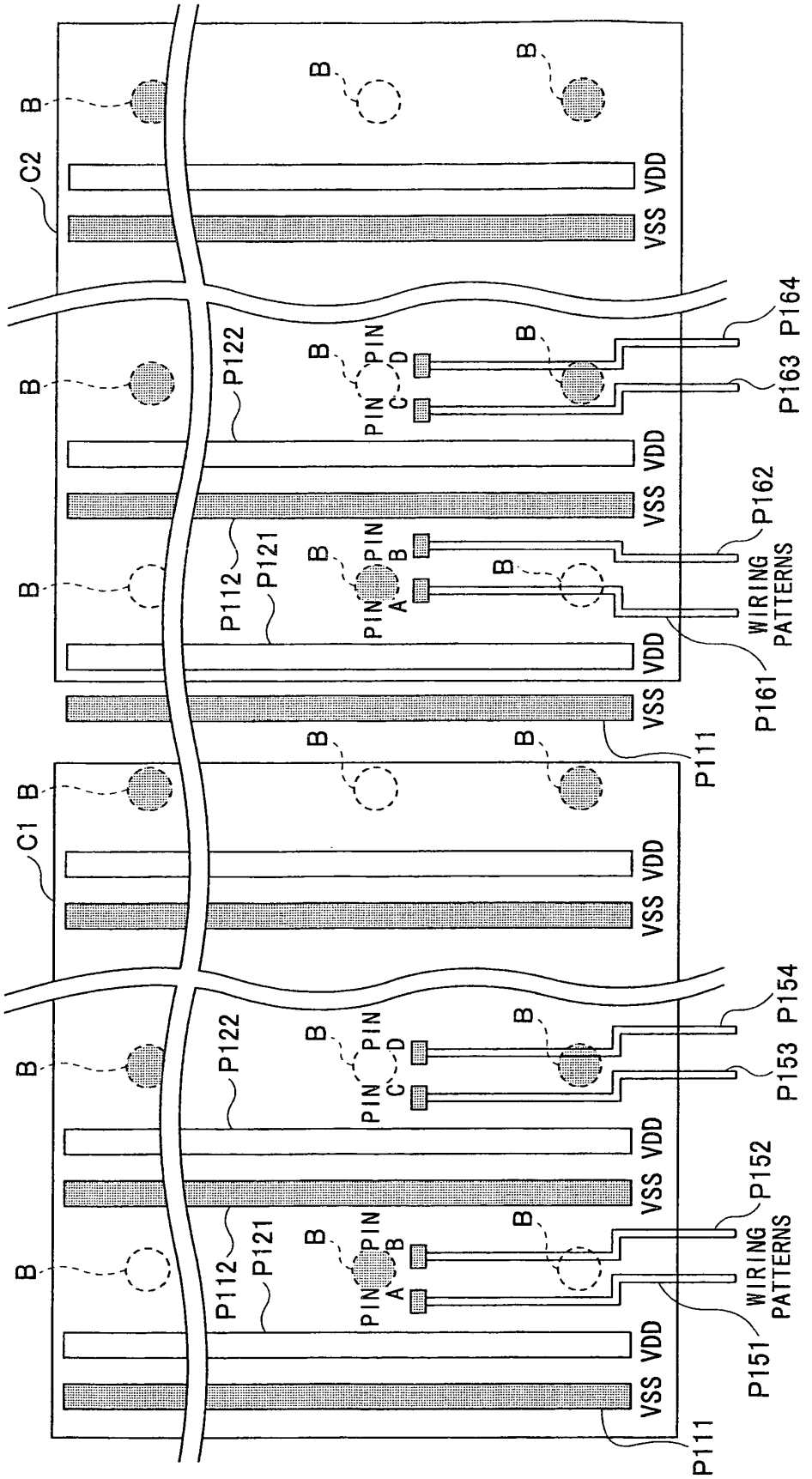

B
C2
VSS VDD
P122
PIN
C
D
P164
P163
P112
P121
A
P162
WIRING PATTERNS
P161
P111
C1
P154
P153
P152
P151

FIG.5

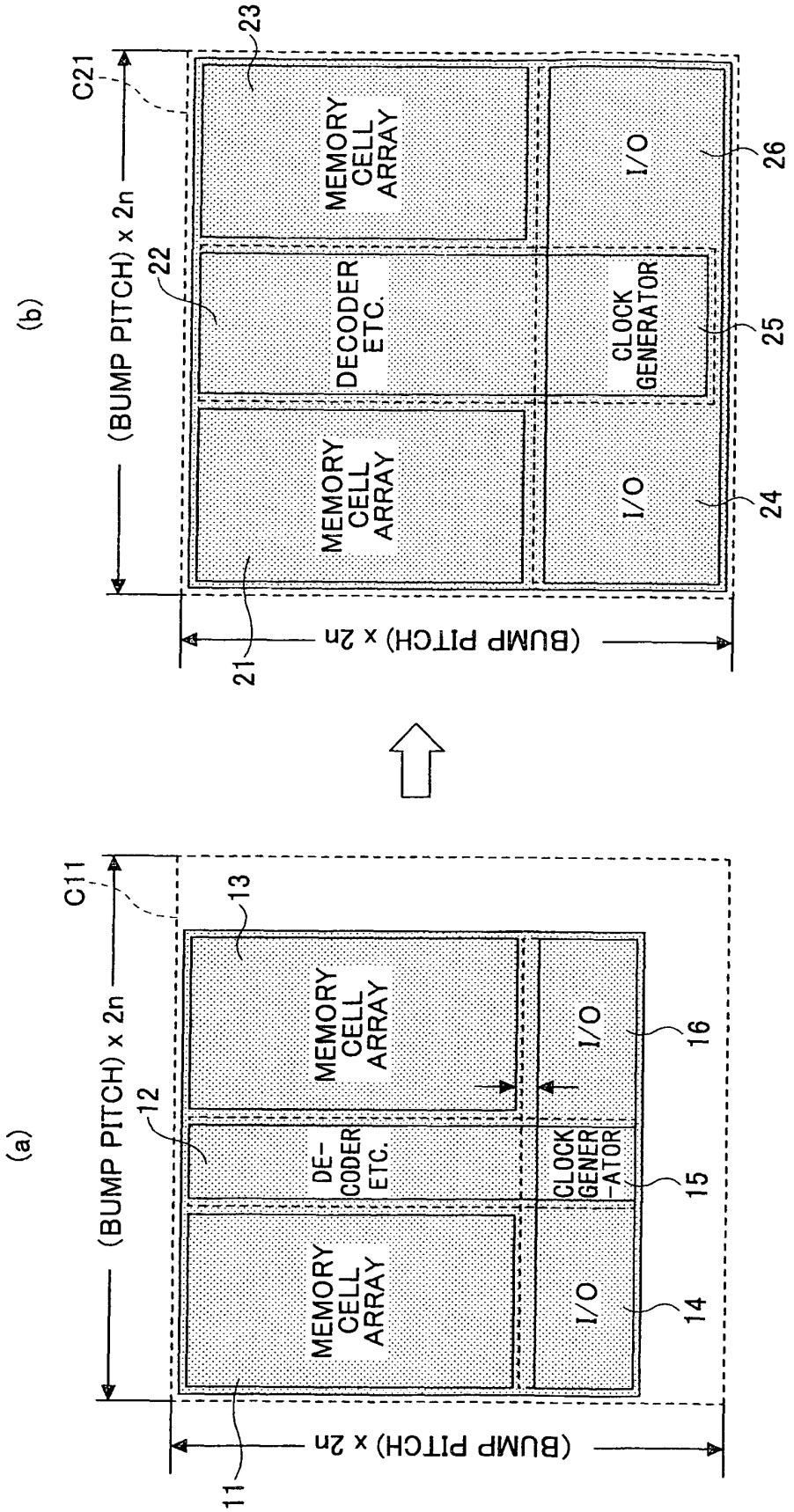

(a)
C11
(BUMP PITCH) x 2n
12
13
MEMORY CELL ARRAY
DE-CODER ETC.
CLOCK GENER-ATOR
I/O
16
15
14
11
(BUMP PITCH) x 2n
(b)
C21
(BUMP PITCH) x 2n
22
23
MEMORY CELL ARRAY
DECODER ETC.
CLOCK GENERATOR
I/O
26
25
24
21
(BUMP PITCH) x 2n

FIG.6

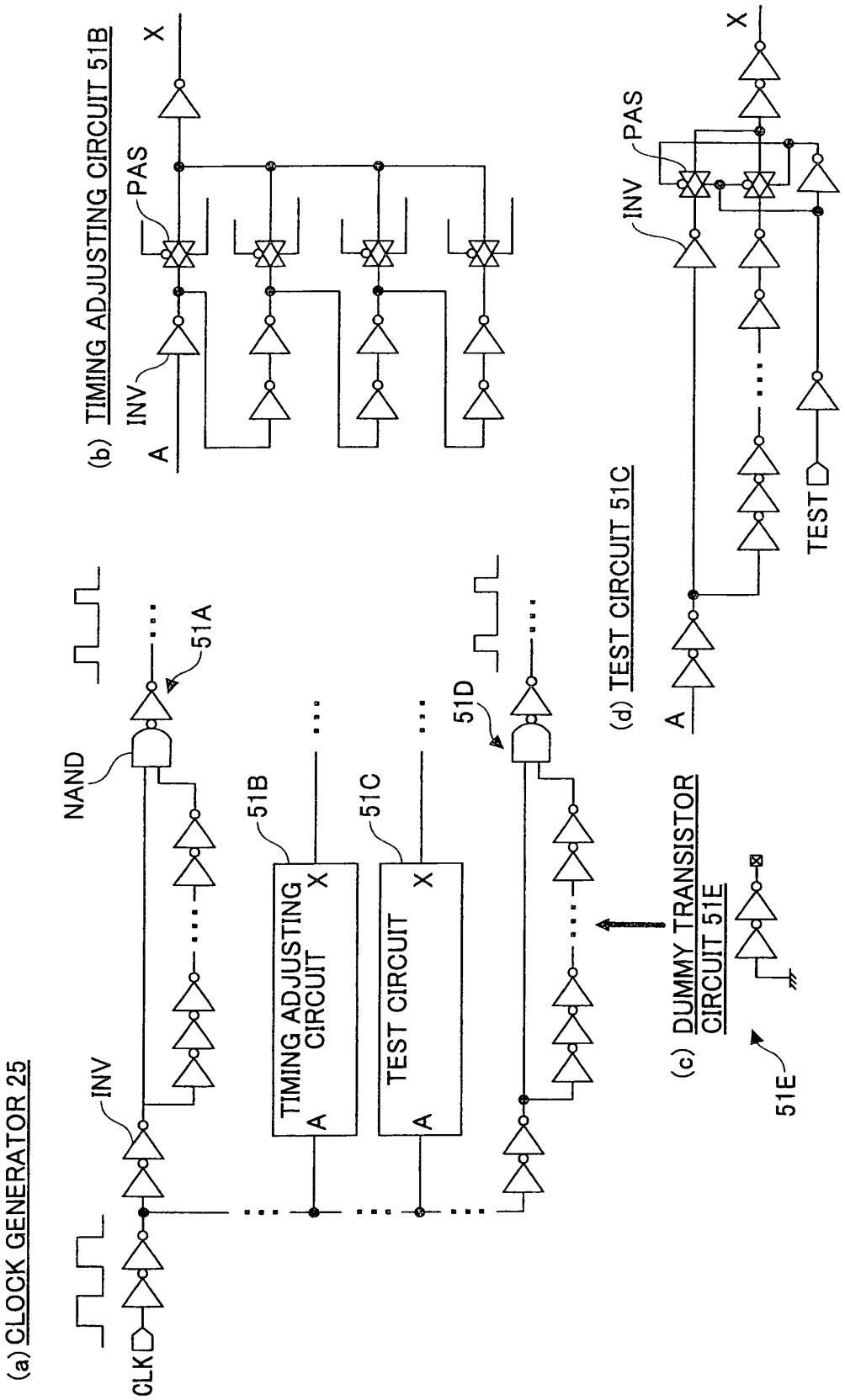

(a) CLOCK GENERATOR 25
CLK
INV
NAND
51A
51B
TIMING ADJUSTING CIRCUIT
A
X
51C
TEST CIRCUIT
A
X
51D
(b) TIMING ADJUSTING CIRCUIT 51B
INV
PAS
A
X
(c) DUMMY TRANSISTOR CIRCUIT 51E
51E
(d) TEST CIRCUIT 51C
INV
PAS
A
X
TEST

FIG.7

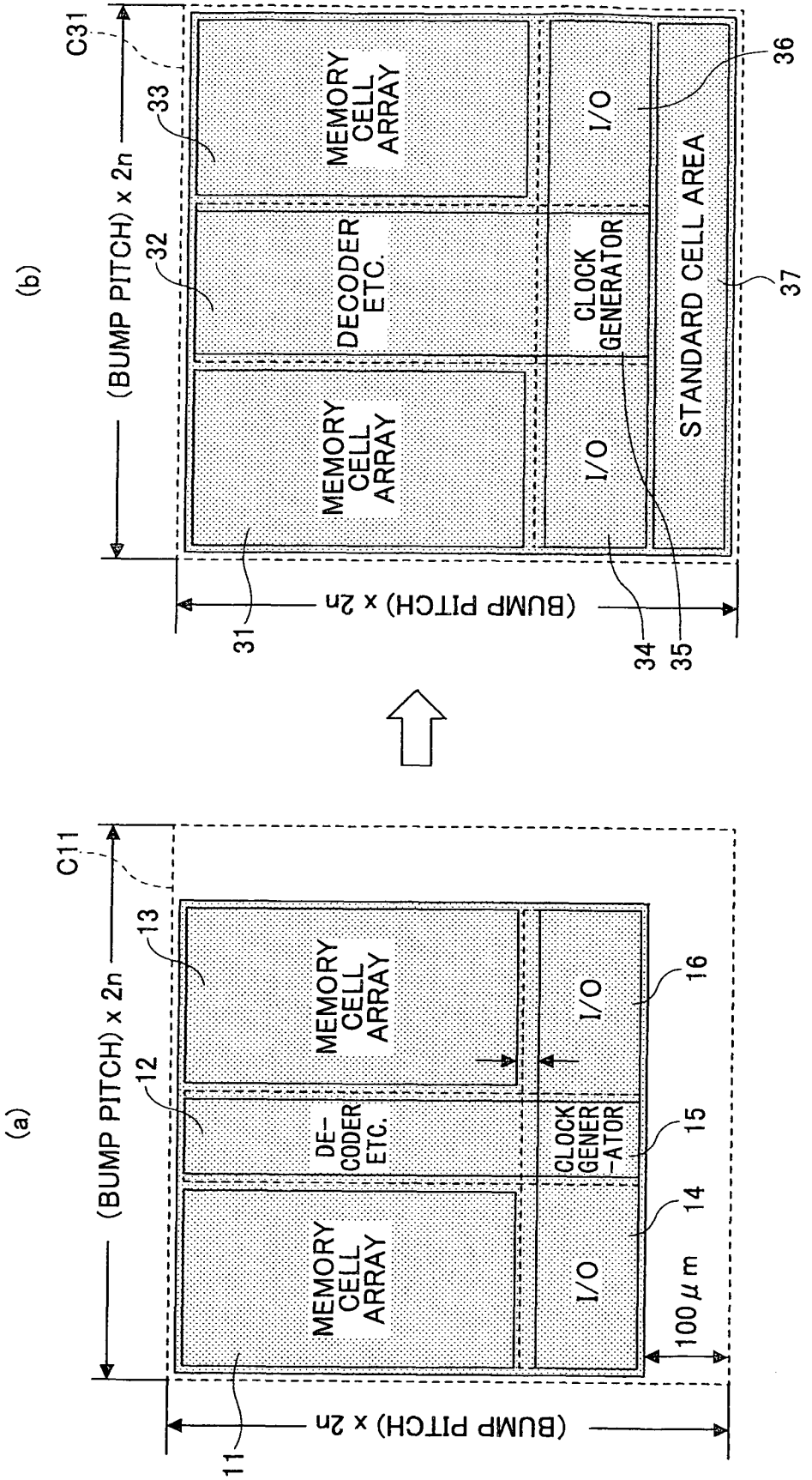

(a)
C11
(BUMP PITCH) x 2n
13
12
MEMORY CELL ARRAY
DE-CODER ETC.
I/O
CLOCK GENER-ATOR
16
15
14
100 μm
11
(BUMP PITCH) x 2n
(b)
C31
(BUMP PITCH) x 2n
33
32
MEMORY CELL ARRAY
DECODER ETC.
I/O
CLOCK GENERATOR
STANDARD CELL AREA
36
37
31
(BUMP PITCH) x 2n
34
35

FIG.8

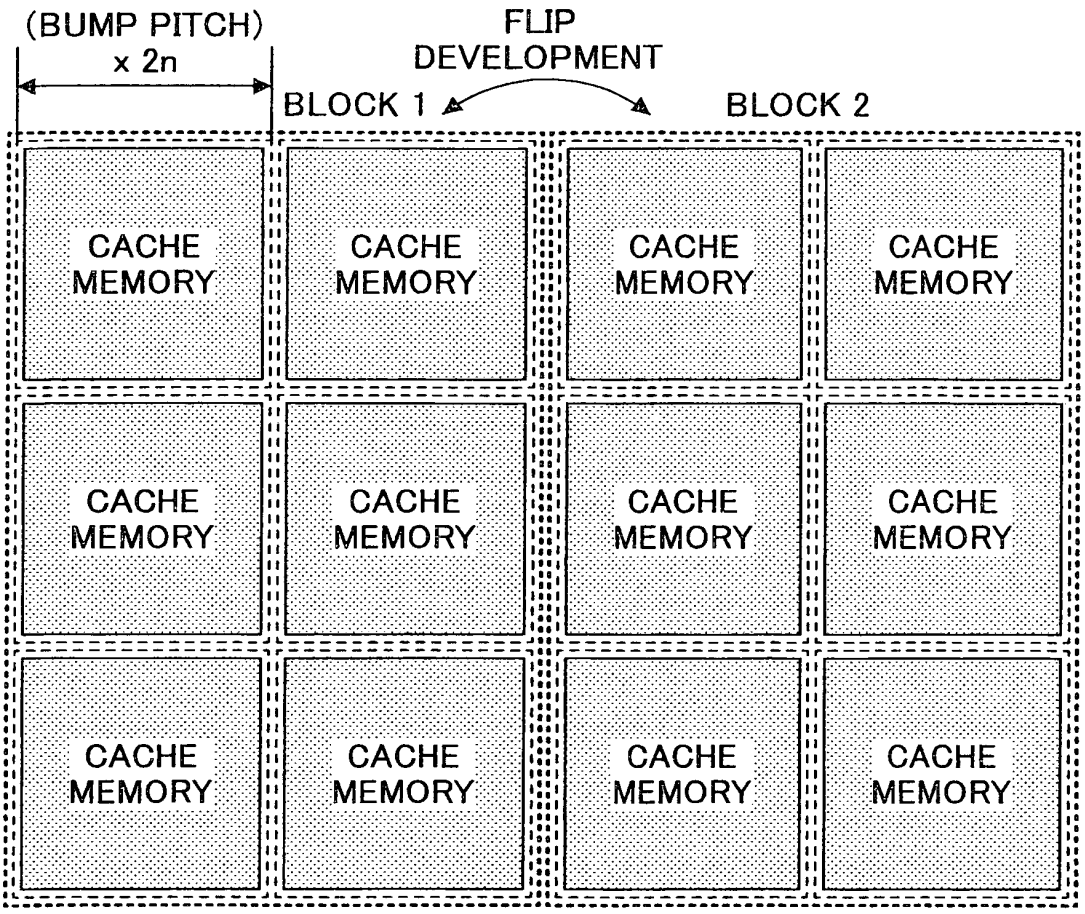
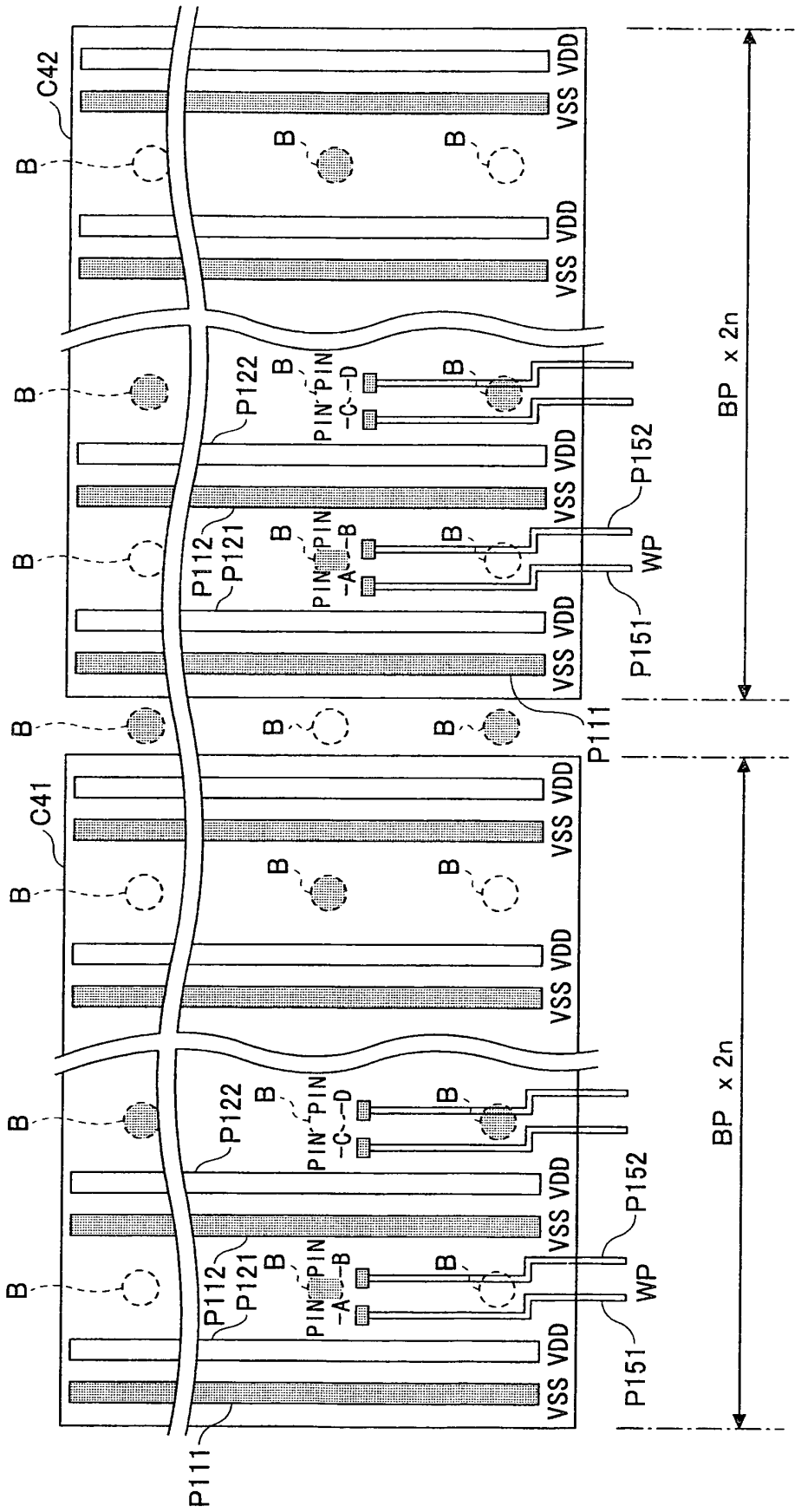

(BUMP PITCH)
x 2n
FLIP
DEVELOPMENT
BLOCK 1
BLOCK 2
CACHE MEMORY
CACHE MEMORY
CACHE MEMORY
CACHE MEMORY
CACHE MEMORY
CACHE MEMORY
CACHE MEMORY
CACHE MEMORY
CACHE MEMORY
CACHE MEMORY
CACHE MEMORY
CACHE MEMORY

FIG.9


C42
C41
B
VSS VDD
P122
P121
P112
P111
P152
P151
WP
PIN -A
PIN -B
PIN -C
PIN -D
BP x 2n

REFERENCES CITED IN THE DESCRIPTION

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Patent documents cited in the description

- JP 7022510 A **[0031]**
- JP 11250700 A **[0032]**
- US 20060267706 A1 **[0033]**